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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild <a href="general-regarding-numbers-n

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FDBL0200N100

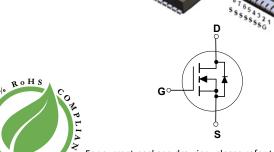
N-Channel PowerTrench[®] MOSFET 100 V, 300 A, 2.0 m Ω

Features

- Typical $R_{DS(on)}$ = 1.5 m Ω at V_{GS} = 10V, I_D = 80 A
- Typical $Q_{q(tot)}$ = 95 nC at V_{GS} = 10V, I_D = 80 A
- UIS Capability
- RoHS Compliant

Applications

- Industrial Motor Drive
- Industrial Power Supply
- Industrial Automation
- Battery Operated tools
- Battery Protection
- Solar Inverters
- UPS and Energy Inverters
- Energy Storage
- Load Switch



For current package drawing, please refer to the Fairchild website at http://www.fairchildsemi.com/dwg/PS/PSOF08A.pdf.

MOSFET Maximum Ratings T_J = 25°C unless otherwise noted.

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-to-Source Voltage		100	V
V_{GS}	Gate-to-Source Voltage		±20	V
ı	Drain Current - Continuous (V _{GS} =10) (Note 1)	T _C = 25°C	300	Α
ID	Pulsed Drain Current	T _C = 25°C	See Figure 4	
E _{AS}	Single Pulse Avalanche Energy	(Note 2)	352	mJ
D	Power Dissipation		429	W
P_{D}	Derate Above 25°C		2.9	W/°C
T_J, T_{STG}	Operating and Storage Temperature		-55 to + 175	°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Note 3)	0.35	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 3a)	43	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 3b)	62.5	°C/W

Notes:

- 1: Current is limited by silicon.
- 2: Starting $T_J = 25^{\circ}C$, L = 0.1mH, $I_{AS} = 84$ A, $V_{DD} = 100$ V during inductor charging and $V_{DD} = 0$ V during time in avalanche.
- 3: R_{0,JA} is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{0,JC} is guaranteed by design, while R_{0,JA} is determined by the board design.
 - a) 43 °C/W when mounted on a 1 in² pad of 2 oz copper
 - b) 62.5 °C/W when mounted on a minimum pad of 2 oz copper

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDBL0200N100	FDBL0200N100	MO-299A	13"	24mm	2000 units

Units

Max.

Electrical Characteristics $T_J = 25$ °C unless otherwise noted.

Parameter

Off Characteristics							
B_{VDSS}	Drain-to-Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	100	-	-	V	
ı	Drain-to-Source Leakage Current	$V_{DS} = 100V, T_J = 25^{\circ}C$	-	-	5	μΑ	
IDSS		$V_{GS} = 0V$ $T_J = 175^{\circ}C \text{ (Note 4)}$	-	-	2	mA	
less	Gate-to-Source Leakage Current	$V_{CS} = +20V$	_	_	+100	nA	

Test Conditions

Min.

Тур.

On Characteristics

Symbol

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$		2.0	3.1	4.5	V
R _{DS(on)}	Drain to Source On Resistance	I _D = 80A,	$T_{J} = 25^{\circ}C$	-	1.5	2.0	$m\Omega$
		V _{GS} = 10V	$T_J = 175^{\circ}C \text{ (Note 4)}$	-	3.3	4.3	mΩ

Dynamic Characteristics

C _{iss}	Input Capacitance	V _{DS} = 50V, V _{GS} = 0V, f = 1MHz		-	6970	9760	pF
C _{oss}	Output Capacitance			-	3950	5530	pF
C _{rss}	Reverse Transfer Capacitance			-	29	41	pF
R_g	Gate Resistance	f = 1MHz	f = 1MHz		0.45	1	Ω
Q _{g(ToT)}	Total Gate Charge at 10V	V _{GS} = 0 to 10V	V _{DD} = 80V	-	95	133	nC
$Q_{g(th)}$	Threshold Gate Charge	$V_{GS} = 0 \text{ to } 2V$	100 001	-	13	-	nC
Q _{gs}	Gate-to-Source Gate Charge		_		31	-	nC
Q_{gd}	Gate-to-Drain "Miller" Charge			-	20	-	nC

Switching Characteristics

t _{on}	Turn-On Time		-	-	73	ns
t _{d(on)}	Turn-On Delay		-	31	50	ns
t _r	Rise Time	V _{DD} = 50V, I _D = 80A,	-	25	40	ns
t _{d(off)}	Turn-Off Delay	$V_{GS} = 10V, R_{GEN} = 6\Omega$	-	36	58	ns
t _f	Fall Time		-	9	18	ns
t _{off}	Turn-Off Time		-	-	59	ns

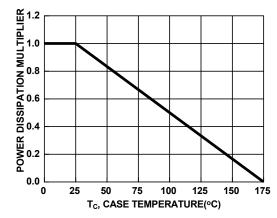
Drain-Source Diode Characteristics

V _{SD}	Source-to-Drain Diode Voltage	I _{SD} =80A, V _{GS} = 0V	-	-	1.25	V
		I_{SD} = 40A, V_{GS} = 0V	-	-	1.2	V
t _{rr}	Reverse-Recovery Time	$I_F = 80A$, $dI_{SD}/dt = 100A/\mu s$,	-	115	184	ns
Q _{rr}	Reverse-Recovery Charge	V_{DD} =80V	-	172	273	nC

Note:

4: The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production.

Typical Characteristics



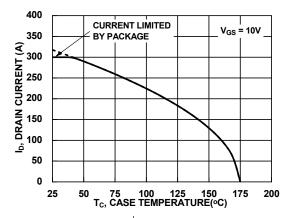


Figure 1. Normalized Power Dissipation vs. Case Temperature

Figure 2. Maximum Continuous Drain Current vs.

Case Temperature

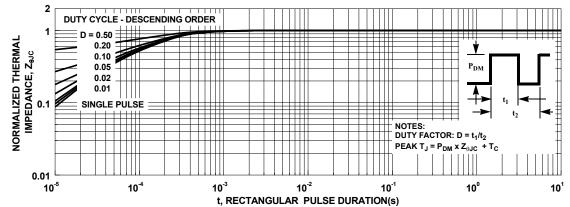


Figure 3. Normalized Maximum Transient Thermal Impedance

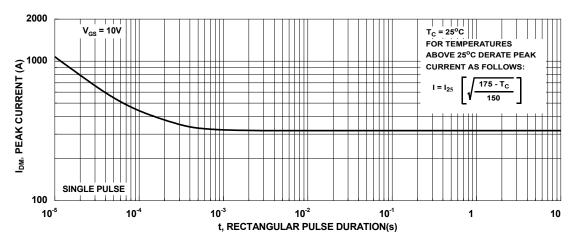


Figure 4. Peak Current Capability

Typical Characteristics

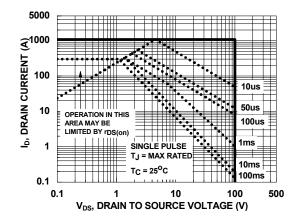
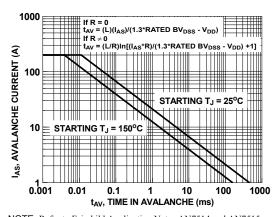
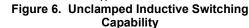


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515



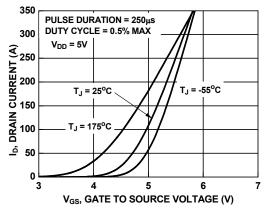


Figure 7. Transfer Characteristics

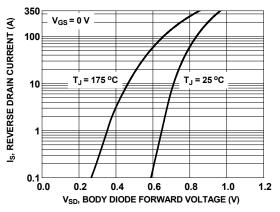


Figure 8. Forward Diode Characteristics

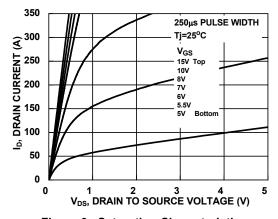


Figure 9. Saturation Characteristics

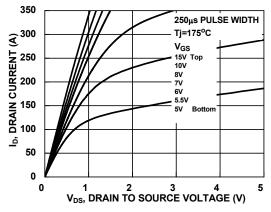


Figure 10. Saturation Characteristics

Typical Characteristics

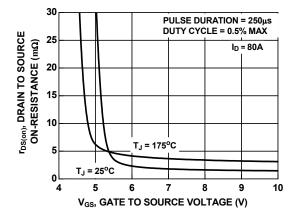


Figure 11. R_{DSON} vs. Gate Voltage

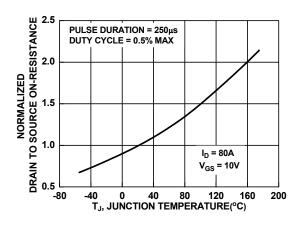


Figure 12. Normalized R_{DSON} vs. Junction Temperature

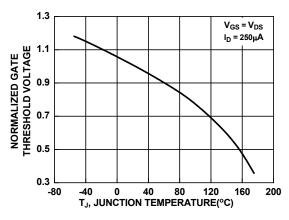


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

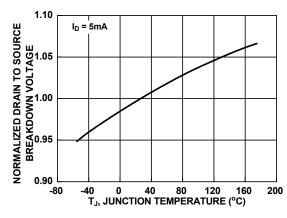


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

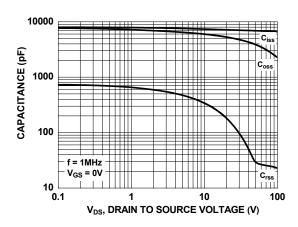


Figure 15. Capacitance vs. Drain to Source Voltage

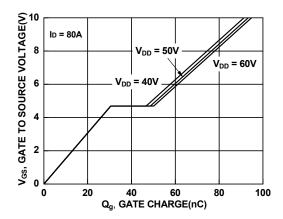
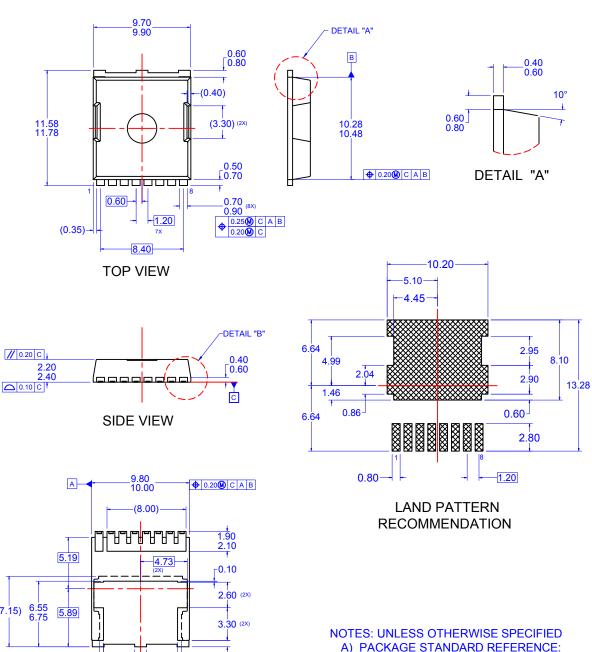
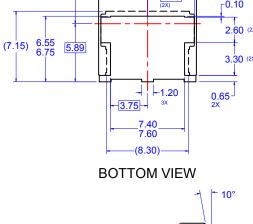


Figure 16. Gate Charge vs. Gate to Source Voltage



- A) PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE A, DATED NOVEMBER 2009.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- E) DRAWING FILE NAME: MKT-PSOF08AREV3



DETAIL "B"

- (0.35)

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