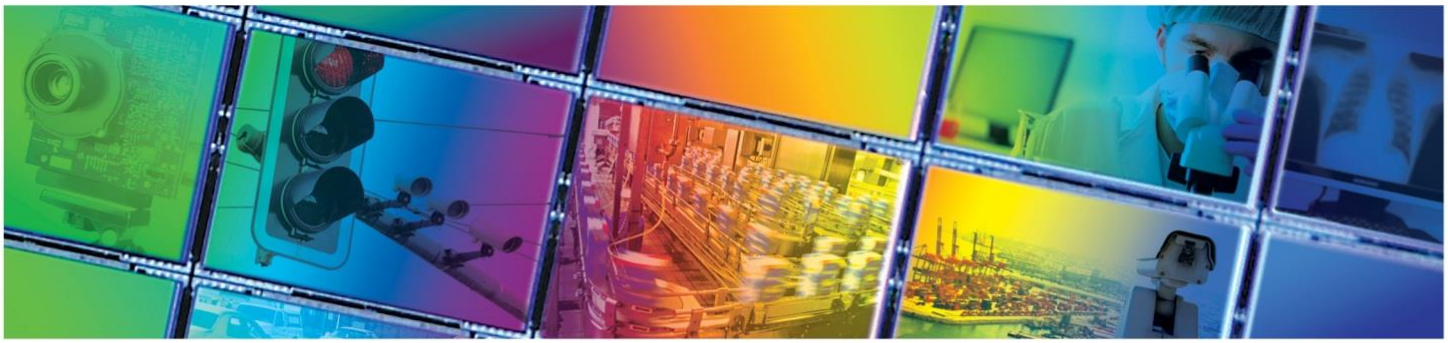
ON Semiconductor®

KLI-8023 IMAGE SENSOR

LINEAR CCD IMAGE SENSOR



JUNE 12, 2014

DEVICE PERFORMANCE SPECIFICATION

REVISION 1.1 PS-0052

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KLI-8023 Image Sensor

DESCRIPTION

The KLI-8023 Image Sensor is a multispectral, linear solid state image sensor for color scanning applications where ultra-high resolution is required.

The imager consists of three parallel linear photodiode arrays, each with 8000 active photosites for the output of red, green, and blue (R, G, B) signals. This device offers high sensitivity, high data rates, low noise and negligible lag. Individual electronic exposure control for each color allows the KLI-8023 sensor to be used under a variety of illumination conditions. The imager can be operated in an Extended Dynamic Range mode for the most demanding applications.

FEATURES

- 12 line spacing between color channels
- Single shift register per channel
- High offband spectral rejection
- Dark reference pixels provided
- Antireflective glass
- Wide dynamic range, low noise
- Dual dynamic range mode operation
- No image lag
- Electronic exposure control
- High charge transfer efficiency
- Two-phase register clocking
- 74 ACT logic compatible clocks
- 6 MHz maximum data rate

APPLICATIONS

- Digitization
- Medical Imaging
- Photography

Parameter	Typical Value
Architecture	3 Channel, RGB Trilinear CCD
Pixel Count	8002 x 3
Pixel Size	9 µm (H) x 9 µm (V)
Pixel Pitch	9 µm
Inter-Array Spacing	108 µm (12 lines effective)
Imager Size	72.0 mm (H) x 0.225 mm (V)
Saturation Signal	185 k electrons (Normal DR mode) 400 k electrons (Extended DR mode)
Dynamic Range (2 MHz Data Rate)	84 dB (Normal DR mode) 90 dB (Extended DR mode)
Responsivity (wavelength= 460, 540, 650 nm)	14, 17, 26 V/µJ/cm^2
Output Sensitivity	14.4 µV/electron
Dark Current	0.002 pA/pixel
Dark Current Doubling Rate	8 °C
Charge Transfer Efficiency	0.999998/Transfer
Photoresponse Non-uniformity	3% Peak-Peak
Lag (First Field)	0.025%
Maximum Data Rate	6 MHz/Channel
Package	CERDIP (Sidebrazed, CuW)
Cover Glass	AR coated, 2 sides

Parameters above are specified at T = 25 °C (junction temperature) and 1 MHz clock rates unless otherwise noted.

Ordering Information

Catalog Number	Product Name	Description	Marking Code
4H0614	KLI- 8023-AAA-ED-AA	Monochrome, No Microlens, CERDIP Package (leadframe), Clear Cover Glass with AR coating (both sides), Standard Grade	KLI-8023-AAA (Serial Number)
4H0617	KLI- 8023-AAA-ED-AE	Monochrome, No Microlens, CERDIP Package (leadframe), Clear Cover Glass with AR coating (both sides), Engineering Sample	
4H0615	KLI- 8023-DAA-ED-AA	Color (RGB), No Microlens, CERDIP Package (leadframe), Clear Cover Glass with AR coating (both sides), Standard Grade	KLI-8023-DAA (Serial Number
4H0618	KLI- 8023-DAA-ED-AE	Color (RGB), No Microlens, CERDIP Package (leadframe), Clear Cover Glass with AR coating (both sides), Engineering Sample	
4H0093	KEK-4H0093-KLI-8023-12-5	Evaluation Board (Complete Kit)	N/A

See Application Note *Product Naming Convention* for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.truesenseimaging.com.

Please address all inquiries and purchase orders to:

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Device Description

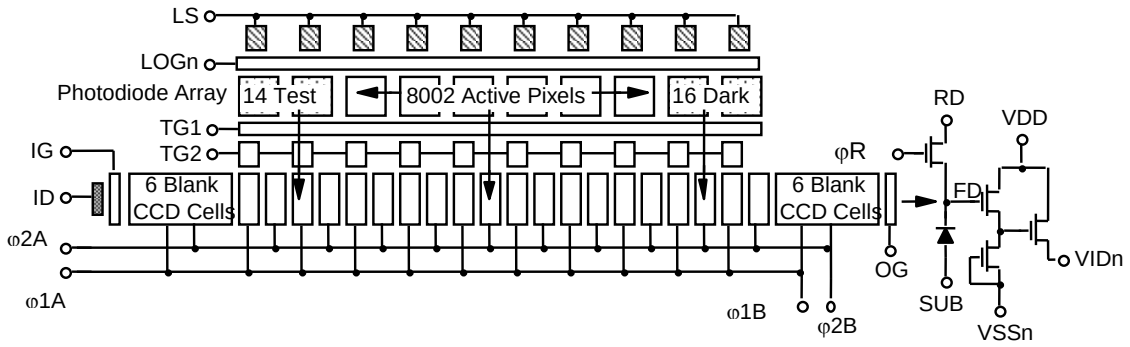


Figure 1: Single Channel Schematic

Dark Reference Pixels

Dark reference pixels are groups of photosensitive pixels covered by a metal light shield. These pixels are used as a black level reference for the image sensor output. Since the incident light is blocked from entering these pixels, the signal contained in these pixels is due only to dark current. It is assumed that each photosensitive pixel (active and dark reference) will have approximately the same dark signal; thus, subtracting the average dark reference signal from each active pixel signal will remove the background dark signal level. Dark reference pixels are typically located at one or both ends of the arrays, as shown earlier in this document for a linear image sensor in the single channel schematic.

Dynamic Range

Dynamic Range (DR) is the ratio of the maximum output signal, or saturation level, of an image sensor to the dark noise level of the imager. The dark noise level, or noise floor of an imager is typically expressed as the root mean square (rms) variation in dark signal voltage. The dark signal includes components from dark current within the photosite and CCD regions, reset transistor and output amplifier noise, and input clocking noise. An input referred noise signal in the charge domain can be calculated by dividing the dark noise voltage by the imager charge-to-voltage conversion factor. The dynamic range is typically expressed in units of decibels as: DR = 20 X LOG (Nsat/Noise).

High Dynamic Range Mode (DR)

Two modes of device operation can be realized, the ‘normal mode’ and ‘high dynamic range mode’. In ‘the normal mode’ of operation, clocking of the output structure reset gate (PHIR, pin 12) remains similar to all other clocks at 6.25 Vp-p. The usable saturation exposure in this mode is approximately 180,000 electrons, yielding a saturation voltage of 2.5 volts. In the ‘high dynamic range’ mode, the reset gate clocking is increased to 12 Vp-p and the reset drain bias (RD, pin 29) is increased to the upper amplifier supply voltage (VDD, pin 26). The usable saturation exposure in this mode increases to 400,000 electrons with a saturation voltage in excess of 5 volts.

Image Acquisition

During the integration period, an image is obtained by gathering electrons generated by photons incident upon the photodiodes. The charge collected in the photodiode array is a linear function of the local exposure. The charge is stored in the photodiode itself and is isolated from the CCD shift registers during the integration period by the transfer gates TG1 and TG2, which are held at barrier potentials. At the end of the integration period, the CCD register clocking is stopped with the φ1 and φ2 gates being held in a 'high' and 'low' state respectively. Next, the TG gates are

turned 'on' causing the charge to drain from the photodiode into the TG1 storage region. As TG1 is turned back 'off' charge is transferred through TG2 and into the φ1 storage region. The TG2 gate is then turned 'off', isolating the shift registers from the accumulation region once again. Complementary clocking of the φ1 and φ2 phases now resumes for readout of the current line of data while the next line of data is integrated.

CHARGE TRANSPORT

Readout of the signal charge is accomplished by two-phase, complementary clocking of the φ1 and φ2 gates. The register architecture has been designed for high speed clocking with minimal transport and output signal degradation, while still maintaining low (6.25 Vp-p min) clock swings for reduced power dissipation, lower clock noise and simpler driver design. The data in all registers is clocked simultaneously toward the output structures. The signal is then transferred to the output structures in a parallel format at the falling edge of the φ2 clocks. Re-settable floating diffusions are used for the charge-to-voltage conversion while source followers provide buffering to external connections. The potential change on the floating diffusion is dependent on the amount of signal charge and is given by $\Delta VFD = \Delta Q/C_{FD}$, where ΔVFD is the change in potential of the floating diffusion, ΔQ is the amount of charge deposited on the floating diffusion, and C_{FD} is the floating diffusion capacitance. Prior to each pixel output, the floating diffusion is returned to the RD level by the reset clock, φR.

Charge Transfer Efficiency

Charge Transfer Efficiency (CTE) is a measure of how efficiently electronic charge can be transported by a Charge Coupled Device (CCD). This parameter is especially important in linear imager technology due to the fact that CCDs are often required to transport charge packets over long distances at very high speeds. The result of poor CTE is to reduce the overall MTF of the line image in a nonlinear fashion: the portion of the line image at the far end of the CCD will be degraded more than the image at the output end of the CCD, since it will undergo more CCD transfers. There are many possible mechanisms that can negatively influence the CTE. Amongst these mechanisms are included excessive CCD clocking frequency, insufficient drive potential on the CCD clocking gates, and incorrect voltage bias on the output gate (OG signal). The effect of these mechanisms is that some charge is "left behind" during a CCD transfer clocking cycle. Depending on the limiting mechanism, the lost charge could be added to the immediate trailing cell or to a cell further back in time; thus, causing a horizontal smearing of the line image.

The charge lost from a CCD cell, after being transferred out of the CCD, is measured with respect to the original charge level and is termed the charge transfer inefficiency (CTI). CTI is defined as

$$CTI = \left(\frac{Total\ Charge\ Lost}{Initial\ Charge}\right) X \left(\frac{1}{Number\ of\ Transfers}\right)$$

The efficiency of the CCD transfer (CTE) is then defined as simply

$$CTE = 1 - CTI$$

Note that the total transfer efficiency for the entire line (TTE) is equal to (CTE)N, where N is the total number of transfers which is equal to the number of phases per cell, times the number of cells (n).

$$TTE = (CTE)\ X\ (2)\ X\ (8022)$$

Dark Signal Evaluation

The dark signal evaluation measures the thermally generated electronic current (i.e. background noise signal) at a specific operating temperature. Dark current is measured will all incident radiation removed (i.e. imager is in the dark). The current measured by the picoammeter is the dark current of the photodiode array plus the dark current of the CCD array. Multiplying the dark current by the total integration time yields the quantity of dark charge. And dividing the

dark current by the number of photodiodes yields the dark current per photodiode (I_{Dark}). Dark voltage increases linearly with integration time, the worst-case value occurs at the slowest clocking frequency. Additionally, dark current doubles for approximately every 8 °C increase in temperature.

Fixed Pattern Noise

If the output of an image sensor under no illumination is viewed at high gain, a distinct non-uniform pattern or fixed pattern noise can be seen. This fixed pattern can be removed from the video by subtracting the dark value of each pixel from the pixel values read out in all subsequent frames. Dark fixed pattern noise is usually caused by variations in dark current across an imager, but can also be caused by input clocking signals abruptly starting or stopping, or by having the CCD clocks not being close compliments of each other. Mismatched CCD clocks can result in high instantaneous substrate currents, which when combined with the fact that the silicon substrate has some non-zero resistance, can result in the substrate potential bouncing. The pattern noise can also be seen when the imager is under uniform illumination. An imager that exhibits a fixed pattern noise under uniform illumination and shows no pattern in the dark is said to have light pattern noise or photosensitivity pattern noise. In addition to the reasons mentioned above, light pattern noise can be caused by the imager entering saturation, the nonuniform clipping effect of the antiblooming circuit, and by non-uniform photosensitive pixel areas often caused by debris covering portions of some pixels.

Exposure Control

Exposure control is implemented by selectively clocking the LOG gates during portions of the scanning line time. By applying a large enough positive bias to the LOG gate, the channel potential is increased to a level beyond the 'pinning level' of the photodiode. (The 'pinning' level is the maximum channel potential that the photodiode can achieve and is fixed by the doping levels of the structure.) With TG1 in an 'off' state and LOG strongly biased, all of the photocurrent will be drawn off to the LS drain. Referring to the timing diagrams in Figure 13 and Figure 14, one notes that the exposure can be controlled by pulsing the LOG gate to a 'high' level while TG1 is turning 'off' and then returning the LOG gate to a 'low' bias level sometime during the line scan. The effective exposure (t_{exp}) is the net time between the falling edge of the LOG gate and the falling edge of the TG1 gate (end of the line). Separate LOG connections for each channel are provided, enabling on-chip light source and image spectral color balancing. As a cautionary note, the switching transients of the LOG gates during line readout may inject an artifact at the sensor output. Rising edge artifacts can be avoided by switching LOG during the photodiode-to-CCD transfer period, preferably during the TG1 falling edge. Depending on clocking speeds, the falling edge of the LOG should be synchronous with the φ1/φ2 shift register readout clocks. For very fast applications, the falling edge of the LOG gate may be limited by on-chip RC delays across the array. In this case artifacts may extend across one or more pixels. Correlated double sampling (CDS) processing of the output waveform can remove the first order magnitude of such artifacts. In high dynamic range applications, it may be advisable to limit the LOG fall times to minimize the current transients in the device substrate and limit the magnitude of the artifact to an acceptable level.

Lag

Lag, or decay lag is a measure of the amount of photogenerated charge left behind during a photodiode-to-CCD transfer cycle. Ideally, no charge is left behind during such transfers and lag is equal to zero; that is, 100% of the collected photogenerated charge is transferred to the adjacent CCD. The use of "pinned" photodiode technology enables the linear imagers to achieve near perfect lag performance. Improper Transfer Gate (TG) clocking levels can introduce a lag type response. Thus, care must be taken to ensure that the clocking levels are not limiting the lag performance.

Imager Responsivity

Responsivity is a measure of the imager output when exposed to a given optical energy density. It is measured on monochrome and color (if applicable) versions of an imager over the entire wavelength range of operation. Imagers having multiple photodiode arrays with differing color filters and/or photodiode dimensions have responsivity measured on each array. Responsivity is reported in units of

$$\frac{V}{\mu J/cm^2}$$

Linearity

The non-linearity of an image sensor is typically defined as the percent deviation from the ideal linear response, which is defined by the line passing through V_{sat} and V_{dark}. The percent linearity is then 100 minus the non-linearity. The output linearity of a solid-state image sensor is determined from the linearity of the photon collection process, the electron exposure structure nonlinearities (if any exists), the efficiency of charge transportation from the photosite to the output amplifier, and the output amplifier linearity. The absorption of photons within the silicon substrate can be considered an ideal linear function of incident illumination level when averaged over a given period of time. The existence of an electronic exposure control circuit adjacent to the photosensitive sites can introduce a non-linearity into the overall response by allowing small quantities of charge to remain isolated in unwanted potential wells. Whether or not any potential wells exist depends on the design and manufacturing of the particular image sensor. The existence of such potential wells in the exposure circuitry, also called exposure control defects, will degrade the linearity only at small signal levels and may be different from one photosite to the next. An image sensor with excessive exposure control defects would be rejected during quality assurance testing. The loss of charge during the transportation of charge packets from the photosite to the CCD, which is termed lag, tends to affect the linearity only at very small signal levels. "Pinned" photodiodes, or buried photodiodes, have extremely small lag (< 0.5%), and can be considered to be lag free. The CCD charge transfer inefficiency (CTI) will reduce the amplitude of the charge packet as it is transported towards the output amplifier, with the greatest effect realized at very small signal levels. Modern CCD's have CTE in excess of 0.999999 per CCD transfer; thus, the overall effect on linearity is generally not a concern. If biased properly, the output amplifier will yield a nonlinearity of typically less than 2%. Non linearity at signal levels beyond the saturation level is expected and can often vary significantly from pixel to pixel.

Linearity Evaluation

Ideally, the output video amplitude should vary linearly with incident light intensity over the entire input range of irradiance. There are many possible phenomena that can cause non-linearity in the response curve; inadequate CTE and improper biasing or clocking to name a few.

Electronic exposure control could be used to vary the photodiode integration time; however, since electronic exposure control can introduce non-linearity, it is not recommended as a method of limiting the input signal. The output signal versus relative irradiance is graphed and a least squares, linear regression fit to the data is performed. The best fit data curve should pass through zero volts and remain linear ($R^2 > 0.99$) up to the Vsat level.

Modulation Transfer Function (MTF)

MTF is the magnitude of the spatial frequency response of a solid-state imager. The three main components of imager MTF are termed the aperture MTF, diffusion MTF, and charge transfer efficiency MTF. The aperture MTF results from the discrete sampling nature of solid-state imagers, with smaller pixel pitches yielding a better high frequency MTF response. The diffusion of photogenerated charge degrades the imager response and is responsible for the second component. The third component is due to inefficient charge transfer in the shift register. The maximum spatial

frequency an imager can detect without aliasing occurring is defined as the Nyquist frequency and is equal to the inverse of two times the pixel pitch. MTF is typically reported at the Nyquist frequency, 1/2 Nyquist, and 1/4 Nyquist. The aperture MTF limits the maximum response at Nyquist to 0.637. (Note that the maximum MTF response is 1.0). The diffusion component will further degrade this value, especially at longer optical wavelengths.

Noise

Noise is defined as any unwanted signal added to the imager output. Temporal noise sources present in a typical imager include the dark current, photon shot noise, reset transistor noise, CCD clocking noise, and the output amplifier noise. Dark current is dependent on the imager operating temperature and can be reduced by cooling the imager. The reset transistor noise can be removed using correlated double sampling signal processing. The photon shot noise cannot be eliminated; however, by acquiring and averaging several frames it, and all temporal noise sources, can be reduced. Another source of noise is the variation in dark current from pixel to pixel leads to a dark noise pattern across an imager. The effects of this dark pattern noise can also be minimized by averaging several frames and then using the pixel-referenced, dark frame data as the zero reference level for each pixel.

Noise Evaluation

The noise evaluation measures the noise levels associated with operating the imager at the specified clocking speeds and temperatures. The test is performed with imager temperature held stable and all incident light removed. The noise contributions of the evaluation circuitry also need to be removed from the calculation. Once this is done, the total imager noise will be approximately equal to the sum of squares of each of the CCD clocking noise, output amplifier noise, and the dark current noise.

Photodiode Quantum Efficiency

For a given area, absolute quantum efficiency is defined as the ratio of the number of photogenerated electrons captured during an integration period to the number of impinging photons during that period. Higher values indicate a more efficient photon conversion process and hence are more desirable.

Absolute photodiode quantum efficiency is calculated from the charge-to-voltage, imager responsivity, and measured active photodiode area. It is calculated over the entire wavelength range of operation and graphed on a curve as percent Quantum Efficiency versus Wavelength.

Once the charge-to-voltage, responsivity, and active photodiode dimensions have all been measured, the absolute quantum efficiency can be calculated as:

$$\text{Quantum Efficiency}(\lambda) = \text{Responsivity}(\lambda) \div \text{Charge to Voltage} \div \text{Active Photodiode Area} \times \text{Energy per Photon}(\lambda),$$

where

$$\text{Energy per Photon}\ (\lambda) = \frac{h \cdot c}{\lambda},$$

and

$$h \cdot c = 1.98647E\ -25\ [J - m]$$

Care should be taken to ensure that all quantities are represented in similar units before any calculations are performed. Using the above formulas, the absolute quantum efficiency can be expressed as:

$$QE(\lambda) = 100\%\ \times R(\lambda) \div \frac{dV}{dN_e} \div \text{Area}_{\text{Diode}} \times \frac{hc}{\lambda}$$

Photoresponse Non-Uniformity (PRNU)

The PRNU measurement is taken in a flat field of collimated white light. The intensity of the light is set to a value approximately 10% to 20% below the saturated signal level. One region (or “window”) of pixels is observed for uniformity at a given time, and the average response is calculated for each non-overlapping windowed section. In the case of medium or low frequency PRNU measurements, a medium filter of 3-7 pixels is applied to this region to eliminate the effects of single point defects. The maximum and minimum pixel is determined for each windowed section. Again, for each section, the following formula is applied:

$$\text{PRNU} = 100\%\ \times \left(\frac{\text{Maximum\_Pixel\_Value}\ - \text{Minimum\_Pixel\_Value}}{\text{Mean\_Pixel\_Value}}\right)$$

Each section is then compared against the specification to identify the region with the largest percent deviation from the average response for the imager.

Resolution

The resolution of a solid-state image sensor is the spatial resolving power of that sensor. The spatial resolution of a sensor is descried in the spatial frequency domain by the modulation transfer function (MTF). The discrete sampling nature of solid-state image sensors gives rise to a sampling frequency that will determine the upper limit of the sensor's frequency response. Resolution is frequently described in terms of the number of dots or photosites per inch (DPI) in the imager or object planes. For example, a linear image sensor with a single array of 1000 photosites of pitch 10 µm would have a resolution of 2540 DPI (1000 / (1000 x .01 mm x 1"/25.4 mm)). If the sensor were used in an

optical system to image an 8" wide document, then the resolution in the document plane would be 125 DPI (1000 pixels / 8"). This example is slightly misleading in that it does not consider the frequency response of the sensor or the optics. In reality, the sensor will have an MTF of between 0.2 and 0.7 at the Nyquist spatial frequency and the optics are likely to have an MTF of 0.6 to 0.9 at the Nyquist frequency. It is important to note that even though a sensor may have a high enough sampling frequency for a particular application, the overall frequency response of the sensor and optics may not be sufficient for that application!

Saturation Voltage

The saturated signal level is the output voltage corresponding to the maximum charge packet the imager can handle. Adding charge above the saturated level results in the excess charge "spilling" over into neighboring photosites or CCD structures. Either the photodiode capacity or the CCD capacity, with the latter being the most typical case, can limit the charge capacity. The saturated signal level is measured by monitoring the dark-to-light transition between the first-out dark reference pixels and the first active pixels while the irradiance is slowly increased. Note that improper settings on either the output gate (OG) or the reset gate (ΦR) can have a clipping effect on the output waveform.

Smear

Smear, also referred to as Photodiode-to-CCD Crosstalk, occurs when photogenerated charge diffuses to an adjacent CCD (such as a transfer register) and is collected, as opposed to being collected in the photodiode where the photon absorption occurred. The result of smear is to increase the background signal within the dark reference pixels and CCD buffer pixels. This increased background signal reduces the achievable dynamic range; hence, a high smear value is undesirable. The further the photodiode array and the CCD are apart, the less the smear. Contributors to increased smear are a short photodiode-to-CCD separation and improper transfer gate clocking levels or timing. Smear is also highly dependent on incident photon wavelength. In the application, an IR cut-off filter (~710 nm) is recommended.

PHYSICAL DESCRIPTION

Pin Description and Device Orientation

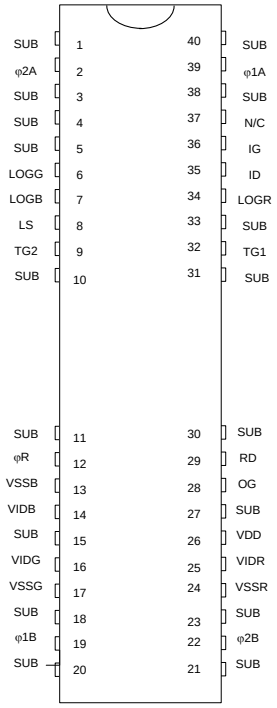


Figure 2: KLI-8023 Pinout

Pin	Name	Description
1	SUB	Substrate/Ground
2	φ2n	Phase 2 CCD Clock (n = A or B)
3	SUB	Substrate/Ground
4	SUB	Substrate/Ground
5	SUB	Substrate/Ground
6	LOGn	Exposure Control for Channel (n = R, G, B)
7	LOGn	Exposure Control for Channel (n = R, G, B)
8	LS	Light Shield / Exposure Drain
9	TG2	Transfer Gate 2 Clock
10	SUB	Substrate/Ground
11	SUB	Substrate/Ground
12	φR	Reset Clock
13	VSSn	Ground Reference (n = R, G, B)
14	VIDn	Blue Output Video (n = R, G, B)
15	SUB	Substrate/Ground
16	VIDn	Blue Output Video (n = R, G, B)
17	VSSn	Ground Reference (n = R, G, B)
18	SUB	Substrate/Ground
19	φ1n	Phase 1 CCD Clock (n = A or b)
20	SUB	Substrate/Ground

Pin	Name	Description
40	SUB	Substrate/Ground
39	φ1n	Phase 1 CCD Clock (n = A or B)
38	SUB	Substrate/Ground
37	SUB	Substrate/Ground
36	IG	Test Input - Input Gate
35	ID	Test Input - Input Diode
34	LOGn	Exposure Control for Channel (n = R, G, B)
33	SUB	Substrate/Ground
32	TG1	Transfer Gate 1
31	SUB	Substrate/Ground
30	SUB	Substrate/Ground
29	RD	Reset Drain
28	OG	Output Gate
27	SUB	Substrate/Ground
26	VDD	Amplifier Supply
25	VIDn	Blue Output Video (n = R, G, B)
24	VSSn	Ground Reference (n = R, G, B)
23	SUB	Substrate/Ground
22	φ2n	Phase 2 CCD Clock (n = A or B)
21	SUB	Substrate/Ground

Imaging Performance

Typical Operational Conditions

Specifications given under nominally specified operating conditions for the given mode of operation at 25 °C, f_{CLK} = 1 MHz, AR coverglass, color filters, and an active load as shown in Figure 3 unless otherwise specified. See notes on next page for further descriptions.

Specifications – High Dynamic Range Mode

VRD = 15 V, φR (High) = 12 V

Description	Symbol	Min.	Nom.	Max.	Units	Notes	Verification Plan
Saturation Output Voltage	Vsat	5.2	5.5		Vp-p	1, 9	die[17]
Output Sensitivity	$\Delta V_o/\Delta N_e$		14		μV/e$^-$		design[18]
Saturation Signal Charge	Ne,sat		400k		electrons		design[18]
Responsivity (@ 450nm) (@ 550nm) (@ 650nm)	R		 14 19 28		V/μJ/cm^2	2, 9, 10 ± 10 % ± 10 % ± 10 %	design[18]
Dynamic Range	DR		87		dB	3	design[18]
Dark Signal Non-Uniformity	DSNU		0.006	0.02	V		design[18]
DC Gain, amplifier	A_{DC}	0.725	0.775	0.825			design[18]
Dark Current	I_{dark}		0.003	0.005	pA/pixel		design[18]
Charge Transfer Efficiency	CTE, η	0.999995				5	die[17]
Lag	L		0.003	0.06	%		design[18]
DC Output Offset	$V_{o,dc}$	8	11	13	Volts	9	design[18]
Photoresponse Uniformity, Low Frequency	PRNU, Low		4	7	% p-p	6	die[17]
Photoresponse Uniformity, Medium Frequency	PRNU, Medium		4	7	% p-p	7	die[17]
Photoresponse Uniformity, High Frequency	PRNU, High		4	7	% p-p	8	die[17]
Darkfield Defect, brightpoint	Dark Def			0	Allowed	12	die[17]
Brightfield Defect, dark or bright	Bfld Def			0	Allowed	13	die[17]
Exposure Control Defects	Exp Def			32	Allowed	11, 14, 15, 16	die[17]

SPECIFICATIONS – NORMAL MODE

VRD= 11 V, φR(High) = 6.5 V

Description	Symbol	Min.	Nom.	Max	Units	Notes	Verification Plan
Saturation Output Voltage	Vsat	2.3	2.6		Vp-p	1, 9	design[18]
Saturation Signal Charge	Nsat		200K		electrons		design[18]
Dynamic Range	DR	78	82		dB	3	design[18]
DC Output Offset	V_{odc}	5.5	7.75	10	Volts	9	design[18]

Notes:

1. Defined as the maximum output level achievable before linearity or PRNU performance is degraded beyond specification
2. With color filter. Values specified at filter peaks. 50% bandwidth = ±30 nm. Color filter arrays become transparent after 710 nm. It is recommended that a suitable IR cut filter be used to maintain spectral balance and optimal MTF. See Figure 4.
3. As measured at 2 MHz data rate. This device utilizes 2-phase clocking for cancellation of driver displacement currents. Symmetry between φ1 and φ2 phases must be maintained to minimize clock noise.
4. Dark current doubles approximately every +8 °C.
5. Measured per transfer. For the total line: (.999995) * 16044 = 0.9229.
6. Low frequency response is measured across the entire array with a 1000 pixel-moving window and a 5 pixel median filter evaluated under a flat field illumination.
7. Medium frequency response is measured across the entire array with a 50 pixel-moving window and a 5 pixel median filter evaluated under a flat field illumination.
8. High frequency response non-uniformity represents individual pixel defects evaluated under a flat field illumination. An individual pixel value may deviate above or below the average response for the entire array. Zero individual defects allowed per this specification.
9. Increasing the current load (nominally 4 mA) to improve signal bandwidth will decrease these parameters.
10. If resistive loads are used to set current, the amplifier gain will be reduced, thereby reducing the output sensitivity and net responsivity. (e.g. with 2.2K Ohm loads to ground, the sensitivity drops to 12.5 microvolts per electron).
11. Defective pixels will be separated by at least one non-defective pixel within and across channels.
12. Pixels whose response is greater than the average response by the specified threshold, (16 mV). See Figure 3.
13. Pixels whose response is greater or less than the average response by the specified threshold, (±10%). See Figure 3.
14. Pixels whose response deviates from the average pixel response by the specified threshold, (4 mV), when operating in exposure control mode. See Figure 3. If dark pattern correction is used with exposure control, the dark pattern acquisition should be completed with exposure control actuated. Dark current tends to suppress the magnitude of these defects as observed in typical applications, hence line rate changes may affect perceived defect magnitude. Note: Zero defects allowed for those pixels whose response deviates from the average pixel response by a 20 mV threshold.
15. Defect coordinates are available upon request.
16. The quantity and type of defects acceptable for a specific application will be negotiated with each customer.
17. A parameter that is measured on every sensor during production testing.
18. A parameter that is quantified during the design verification activity.

Typical Performance Curves

DEFECTIVE PIXEL CLASSIFICATION

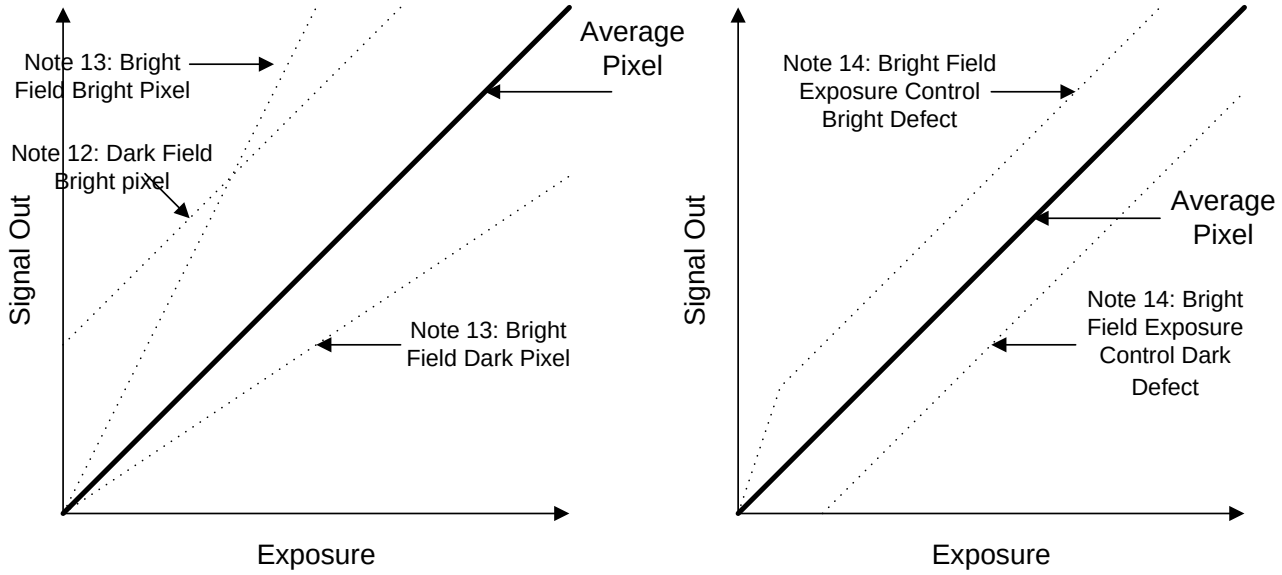


Figure 3: Illustration of Defect Classifications

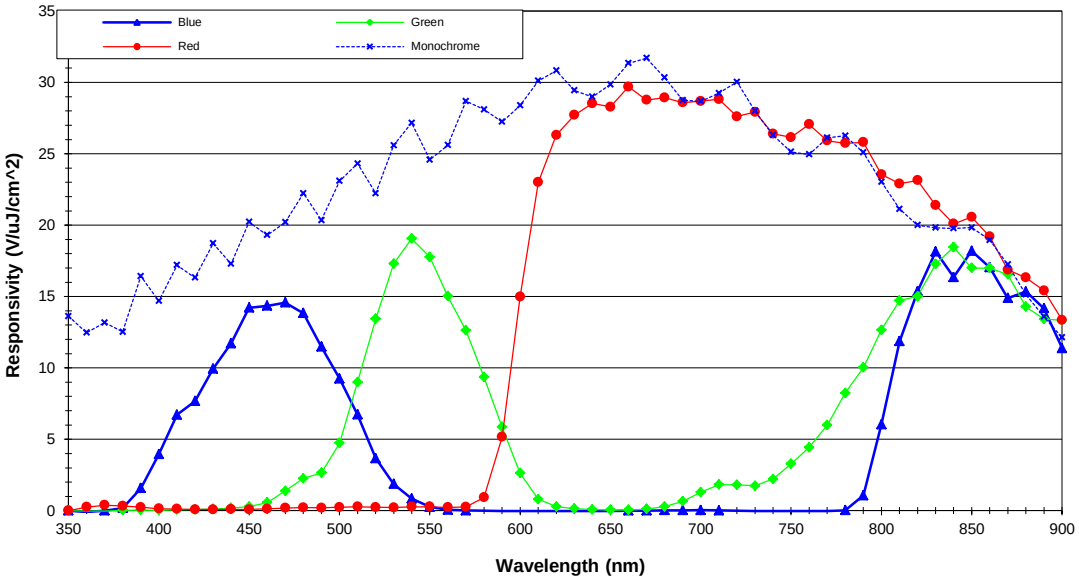


Figure 4: KLI-8023 Typical Responsivity

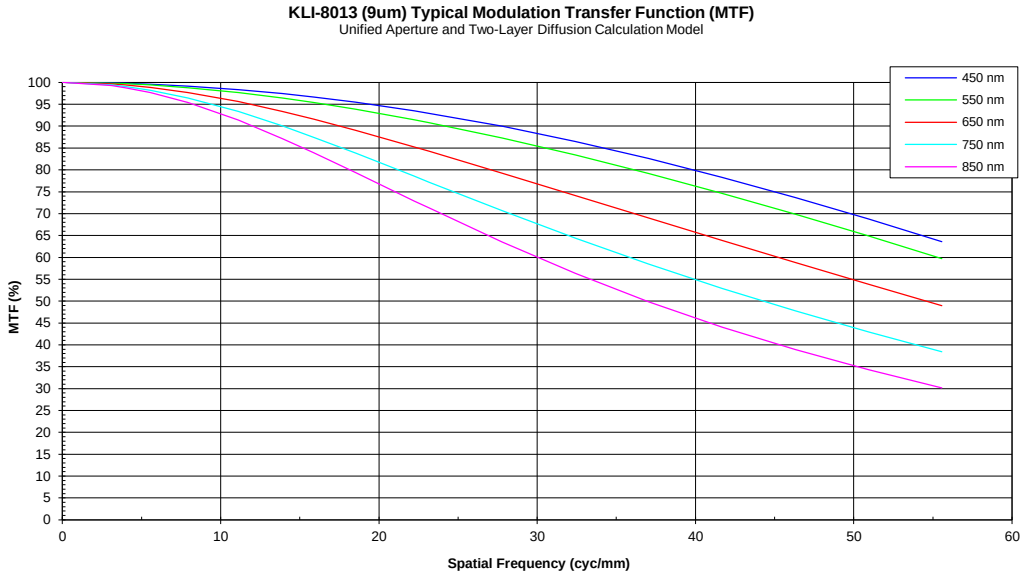


Figure 5: KLI-8023 Typical Modulation Transfer Function

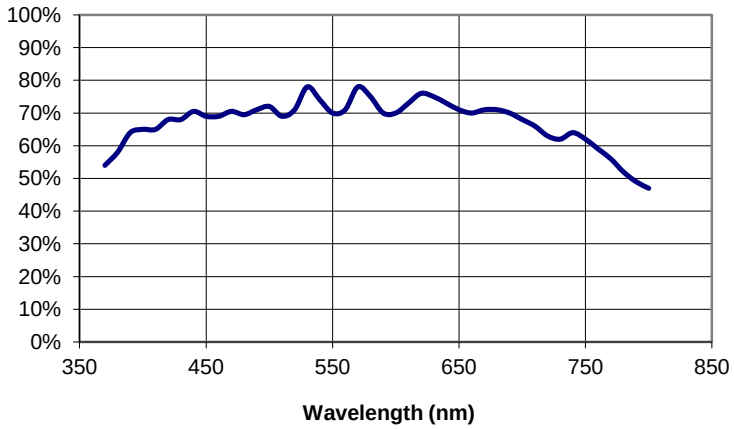


Figure 6: KLI-8023 (monochrome) Typical Quantum Efficiency (%)

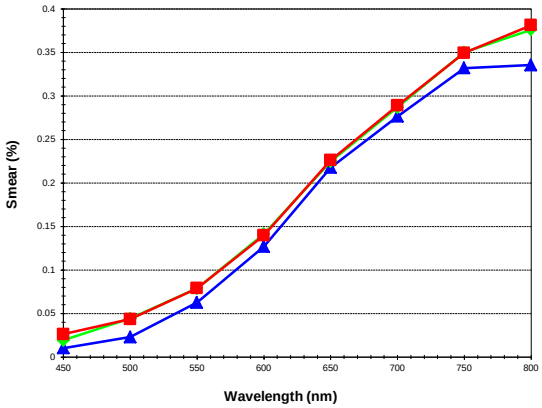


Figure 7: KLI-8023 Smear - LDR Operation / 1 MHz / 35 °C

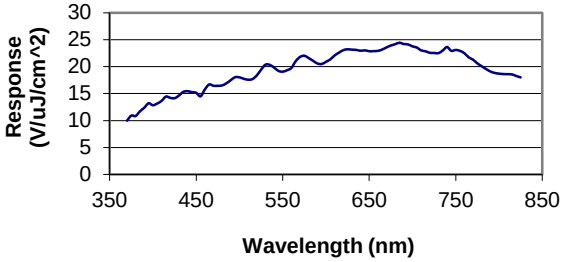


Figure 8: Monochrome KLI-8023 Spectral Response

ΦR_{HIGH}=12V

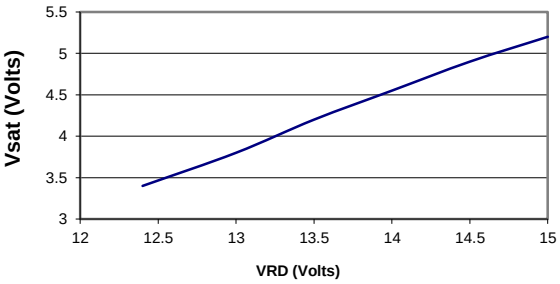


Figure 9: KLI-8023 Typical Saturation Voltage vs. VRD

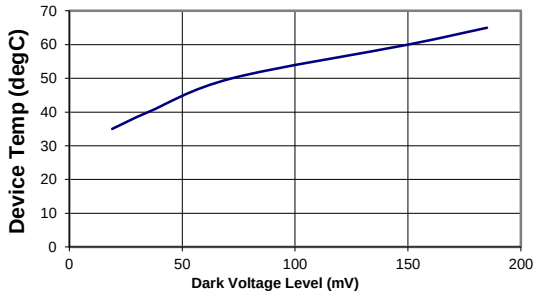


Figure 10: KLI-8023 Typical Dark Pixel Voltage Level vs. Temperature

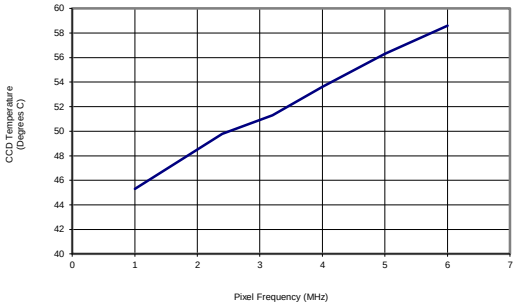


Figure 11: KLI-8023 Typical CCD Temperature vs. Operating Frequency

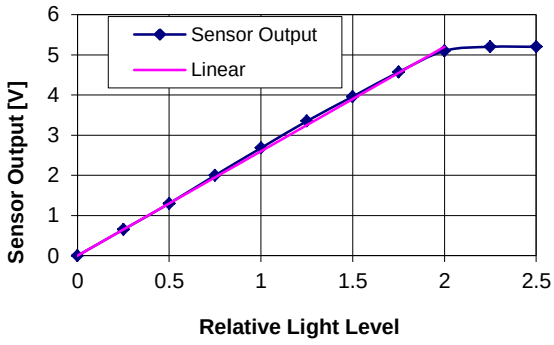


Figure 12: KLI-8023 Typical Device Response Linearity

KLI-8023 Reference Design

The KLI-8023 Reference Design provides a baseline reference for the design of a KLI-8023 image sensor into your electronic imaging application. The circuit below uses inexpensive off-the-shelf components to provide voltage-translated clock signals and DC bias supplies required to support the KLI-8023.

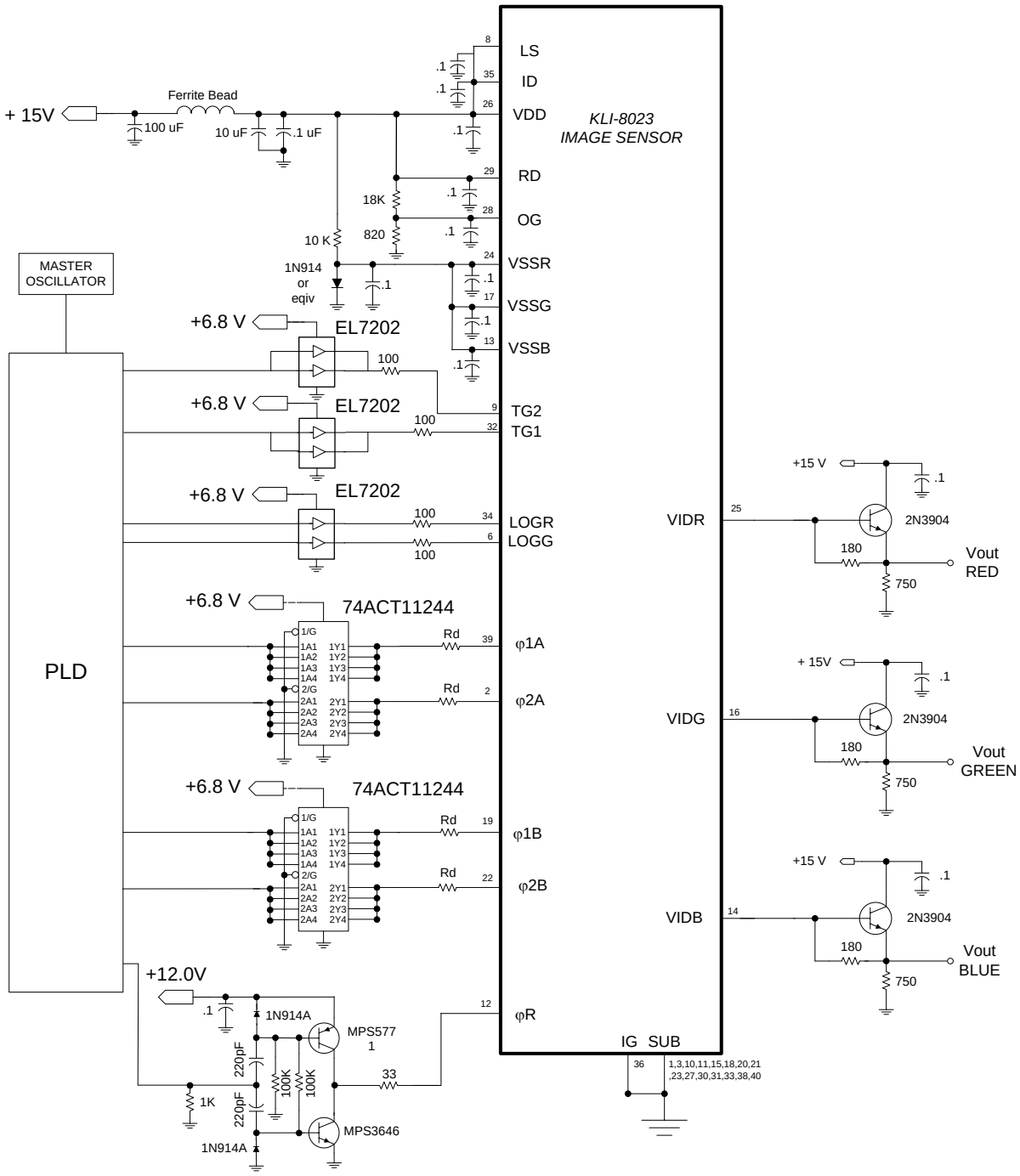


Figure 13: Reference Design

Reference Design Circuit Overview

PROGRAMMABLE LOGIC

See the timing waveform requirements earlier in this document before programming a logic device.

CLOCK DRIVERS

There are three types of clock drivers (voltage translating buffers) used in this reference design. The most important performance consideration is the ability of the clock driver to drive the capacitive loads presented by the various gates of the CCD.

Reset Driver

The RESET, (φR), gate presents a small capacitive load of 100 pF, and requires fast rise and fall times. The complimentary bipolar switching transistor circuit shown in Figure 13 provides a low cost solution. The circuit alternately drives the PNP and NPN transistors into saturation, which switches the output between VCC and ground. A 33 - ohm series-damping resistor is used to suppress ringing.

Exposure Control and Transfer Gates

The exposure control gates; LOGR and LOGG, and the transfer gates; TG1 and TG2 each present a moderate capacitive load of 500 pF. The Elantec 7202 Dual-Channel Power MOSFET driver delivers a peak output current of 2 amperes: more than enough to meet the rise and fall requirements of the LOG and TG gates. Series damping resistors are used to prevent ringing in the LOGR and LOGG gates. The transfer gates are connected together and driven by a single EL7202.

CCD Shift Register Driver

The CCD clock phases (φ1A, φ2A, φ1B and φ2B) present a significant load of 3100 pF per phase. Two 74ACT11244 octal buffers provide an efficient solution. Each clock phase is driven by four gates connected in parallel to increase output drive current. The 6.5-volt swing required by the shift register is obtained by setting VCC to 6.8 volts. Series damping resistors Rd are used to suppress ringing of the clock signals. Values for Rd should be varied to eliminate ringing and achieve 50% crossover between each pair of shift register clocks.

BIAS SUPPLIES

VDD, RD and OG

VDD and VRD are supplied directly from the 15 V input power supply and OG is supplied by a voltage divider. The input power should be sufficiently filtered to prevent noise from coupling into the output stage of the KLI-8013 through the VDD node. Current spikes in the VRD and VDD nodes, due to switching of the on-chip reset FET, are suppressed by the addition of a 0.1 µF decoupling capacitor to ground at each node. The decoupling capacitors should be located as close as possible to the pins of the CCD and should have a solid connection to ground. OG is also decoupled to suppress voltage spikes the output gate of the device. The OG node draws negligible current.

OG, VSSR, VSSG, VSSB

A forward-biased diode provides an inexpensive and reliable voltage source for all three VSS nodes. The switching action of the reset FET of the output stage can cause voltage spikes to occur on the VSS nodes. A decoupling capacitor located as close as practical to each VSS pin, and connected to a solid system ground, will minimize voltage spiking. In high dynamic range systems, crosstalk between VSS channels might present a noise problem. A separate supply for each of the three VSS nodes will minimize channel crosstalk if it proves to be a problem.

Output Buffers

An emitter follower circuit buffers each output channel. The emitter follower provides a high impedance load to the on-chip source follower output stage, and provides low output impedance for driving the downstream analog signal processing circuits. A 180-ohm resistor connected between the base and emitter of the emitter follower uses the forward biased base to emitter voltage drop to provide a constant current load for the on-chip output stage.

Defect Definitions

Operationing Conditions

Test conditions: T = 25 °C, f_{CLK} = 1 MHz, t_{int} = 8.054 msec

Specifications

Field	Defect Type	Threshold	Units	Notes	Number
Dark	Bright	16.0	mV	1, 2	0
Bright	Bright/Dark	10	%	1, 3	0
Bright	Exposure Control	4.0	mV	1, 4, 5	≤32

Notes:

1. Defective pixels will be separated by at least one non-defective pixel within and across channels.
2. Pixels whose response is greater than the average response by the specified threshold. See Figure 14 below.
3. Pixels whose response is greater or less than the average response by the specified threshold. See Figure 14 below.
4. Pixels whose response deviates from the average pixel response by the specified threshold when operating in exposure control mode. See Figure 14 below.
5. Defect coordinates are available upon request.

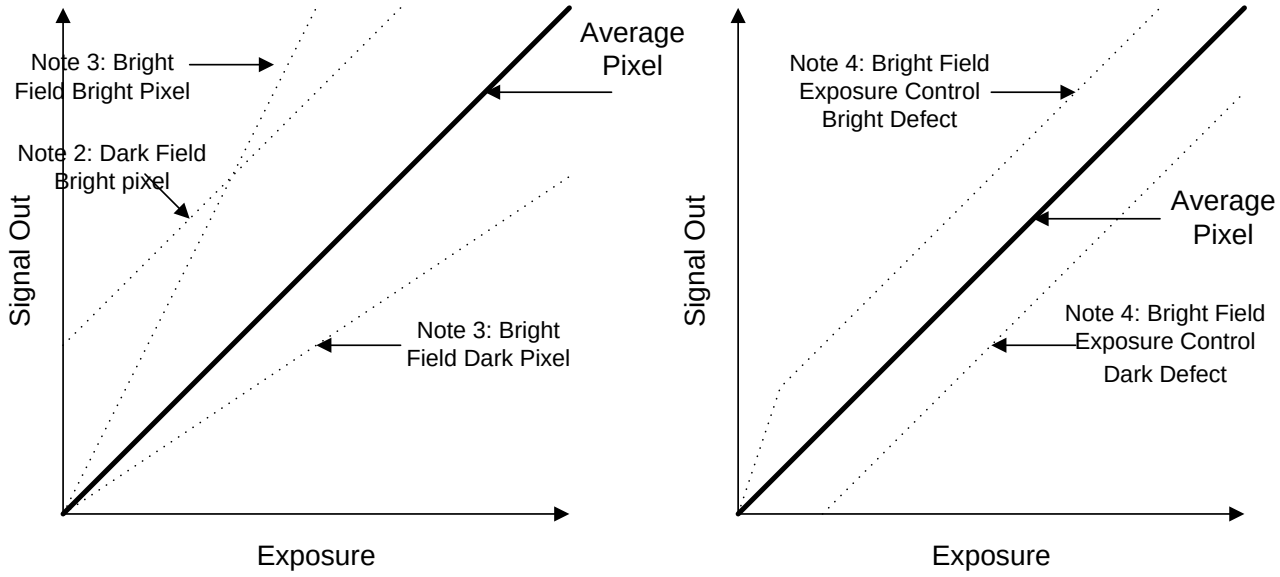


Figure 14: Illustration of Defect Classifications

Operation

ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Minimum	Maximum	Units	Notes
Gate Pin Voltages	V_{GATE}	-0.5	+16	V	1, 2
Pin to Pin Voltage	$V_{PIN-PIN}$		16	V	1, 3
Diode Pin Voltages	V_{DIODE}	-0.5	+16	V	1,4
Output Bias Current	I_{DD}		-10	mA	5
Output Load Capacitance	$C_{VID,LOAD}$		15	pF	
CCD Clocking Frequency	f_C		20	MHz	6

Notes:

1. Referenced to substrate voltage.
2. Includes pins: φ1n (n = A or B), φ2n (n = A or B), TG1, TG2, φR, OG, IG, and LOGn (n = R, G, B).
3. Voltage difference (either polarity) between any two pins.
4. Includes pins: VIDn, VSSn, RD, VDD, LS and ID (n = R, G, B).
5. Care must be taken not to short output pins to ground during operation as this may cause permanent damage to the output structures.
6. Charge transfer efficiency will degrade at frequencies higher than the maximum clocking frequency. VIDn load resistor values may need to be decreased as well.
7. Noise performance will degrade with increasing temperatures.
8. Long-term storage at the maximum temperature will accelerate color filter degradation.
9. Exceeding the upper limit on output load capacitance will greatly reduce the output frequency response. Thus, direct probing of the output pins with conventional oscilloscope probes is not recommended.
10. The absolute maximum ratings for the entire table indicate the limits of this device beyond which damage may occur. The Operating ratings indicate the conditions where the design should operate the device. Operating at or near these ratings do not guarantee specific performance limits. Guaranteed specifications and test conditions are contained in the Imaging Performance section.

Device Input ESD Protection Circuit (schematic)

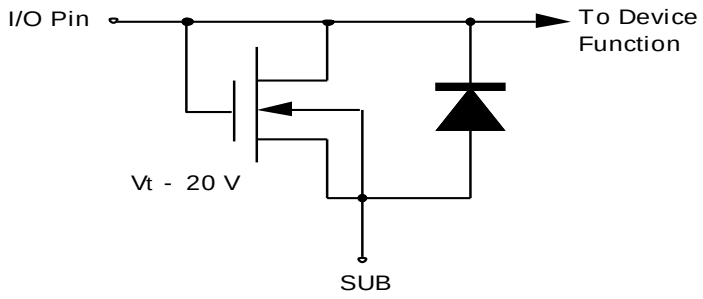


Figure 15: ESD Circuit

CAUTION:

To allow for maximum performance, this device was designed with limited input protection; thus, it is sensitive to electrostatic induced damage. These devices should be installed in accordance with strict ESD handling procedures!

DC Bias Operating Conditions

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
Substrate	V_{SUB}	-	0	-	V	
Output Buffer Return	V_{VSS}	0.5	0.65	0.75	V	
Reset Drain Bias (Normal Mode)	V_{RD}	10.5	11	11.5	V	
Reset Drain Bias (High DR Mode)	V_{RD}	14.5	V_{VDD}	15.5	V	
Output Buffer Supply	V_{VDD}	14.5	15	15.5	V	
Output Bias Current/Channel	I_{IDD}	-8	-4	-2	mA	1
Output Gate Bias	V_{OG}	0.5	0.65	0.75	V	
Light Shield/Drain Bias	V_{LS}	12	15	15.5	V	
Test Pin – Input Gate	V_{IG}	-	0	-	V	
Test Pin – Input Diode	V_{ID}	12	15	15.5	V	

Notes:

1. A current sink must be supplied for each output. Load capacitance should be minimized so as not to limit bandwidth. Rx serves as the load bias for the on-chip amplifiers. Values of Rx and RL should be chose to optimize performance for a given operating frequency, but Rx should not be less than 75 Ohms. Figure 16 below shows one such solution.

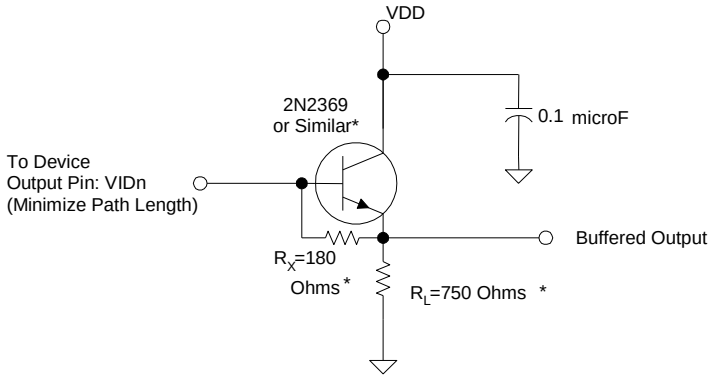


Figure 16: Typical Output Bias/Buffer Circuit

AC Operating Conditions

AC Electrical Characteristics – AC Timing Requirements

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
CCD Element Duration	1e (= $1/f_{CLK}$)	167	1000	-	ns	1e count
H1A/B, H2A/B Rise Time	trise	20	100	-	ns	
Line Integration Period	1L (=tint)	1.343	8054	-	ms	8054e counts
PD-CCD Transfer Period	T_{pd}	2666	16000	-	ns	16e counts
Transfer Gate 1 Clear	T_{tg1}	167	1000	-	ns	1e count
Transfer Gate 2 Clear	T_{tg2}	167	1000	-	ns	1e count
Charge Drain Duration	T_{dr}	1000	-	-	ns	3
Reset Pulse Duration	T_{rst}	20	-	-	ns	1
Clamp to H2 Delay	T_{cd}	6	-	-	ns	2
Sample to Reset Edge Delay	T_{sd}	6	-	-	ns	2

Note:

1. Minimum values given are for 6 MHz CCD operation.
2. Recommended delays for Correlated Double Sampling (CDS) for output.
3. Minimum value required to ensure proper operation, allowing for on-chip propagation delay.

AC Electrical Characteristics – Clock Level Conditions for Operation

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
CCD Readout Clocks High (n = A or B)	V_{H1nH}, V_{H2nH}	6.25	6.5	7.0	V	
CCD Readout Clocks Low (n = A or B)	V_{H1nL}, V_{H2nL}	-0.1	0.0	0.1	V	1
Transfer Clocks High (n = 1 or 2)	V_{TGnH}	6.25	6.5	7.0	V	
Transfer Clocks Low (n = 1 or 2)	V_{TGnL}	-0.1	0.0	0.1	V	1
Reset Clock High (Normal Mode)	$V_{\phi RH}$	6.25	6.5	7.0	V	
Reset Clock High (High DR Mode)	$V_{\phi RH}$	11.5	12.0	12.5	V	
Reset Clock Low	$V_{\phi RL}$	-0.1	0.0	0.1	V	1
Exposure Clocks High (n = R, G, B)	V_{LOGnH}	6.25	6.5	7.0	V	2
Exposure Clocks Low (n = R, G, B)	V_{LOGnL}	-0.1	0.0	0.1	V	1, 2

Notes:
1. Care should be taken to insure that low rail overshoot does not exceed –0.5 VDC. Exceeding this value may result in non-photogenerated charge being injected into the video signal.
2. Connect pin to ground potential for applications where exposure control is not required.

Clock Line Capacitance

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
Phase 1 Clock Capacitance	$C_{\phi 1}$	-	4180	-	pF	1
Phase 2 Clock Capacitance	$C_{\phi 2}$	-	2000	-	pF	1
Transfer Gate 1 Capacitance	C_{TG1}	-	925	-	pF	
Transfer Gate 2 Capacitance	C_{TG2}	-	475	-	pF	
Exposure Gate Capacitance	C_{LOG}	-	190	-	pF	
Reset Gate Capacitance	$C_{\phi R}$	-	11	-	pF	

Notes:
1. This is the total load capacitance per CCD phase. Since the CCDs are driven from both ends of the sensor, the effective load capacitance per drive pin is approximately half the value listed.

Timing

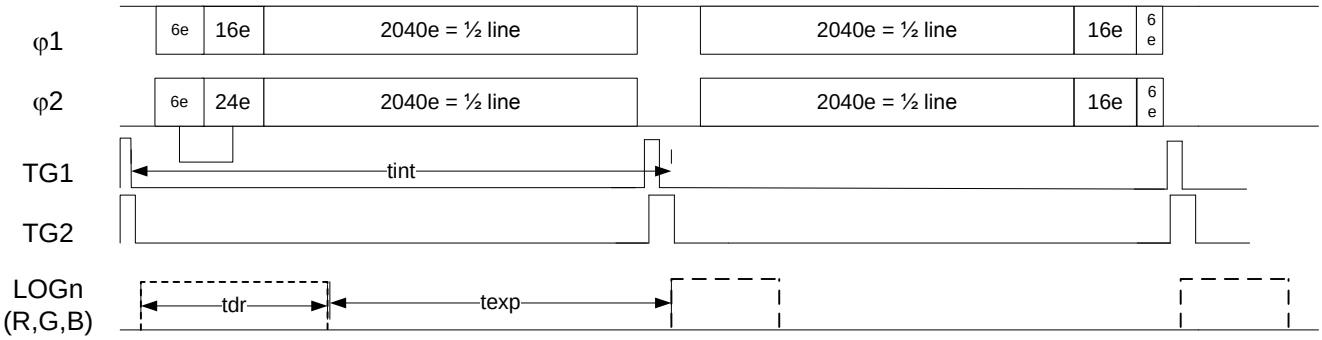


Figure 17: Line Timing

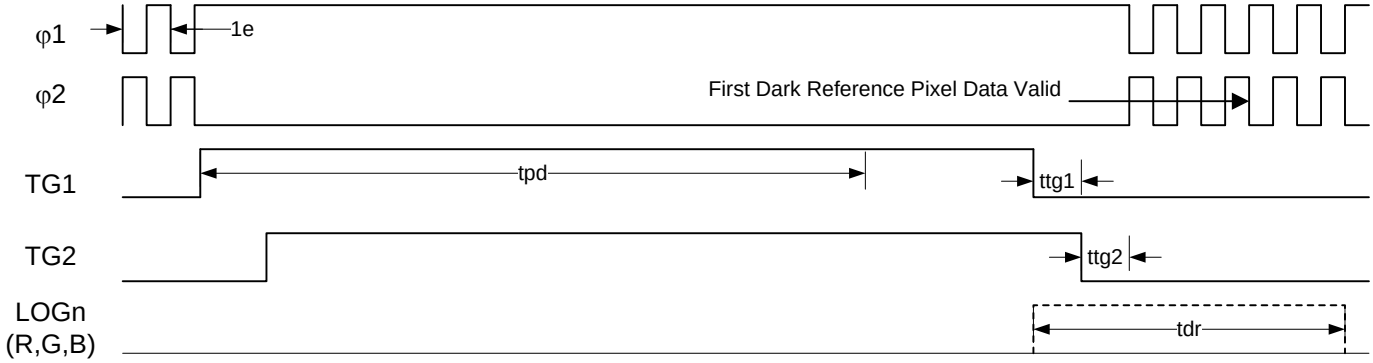
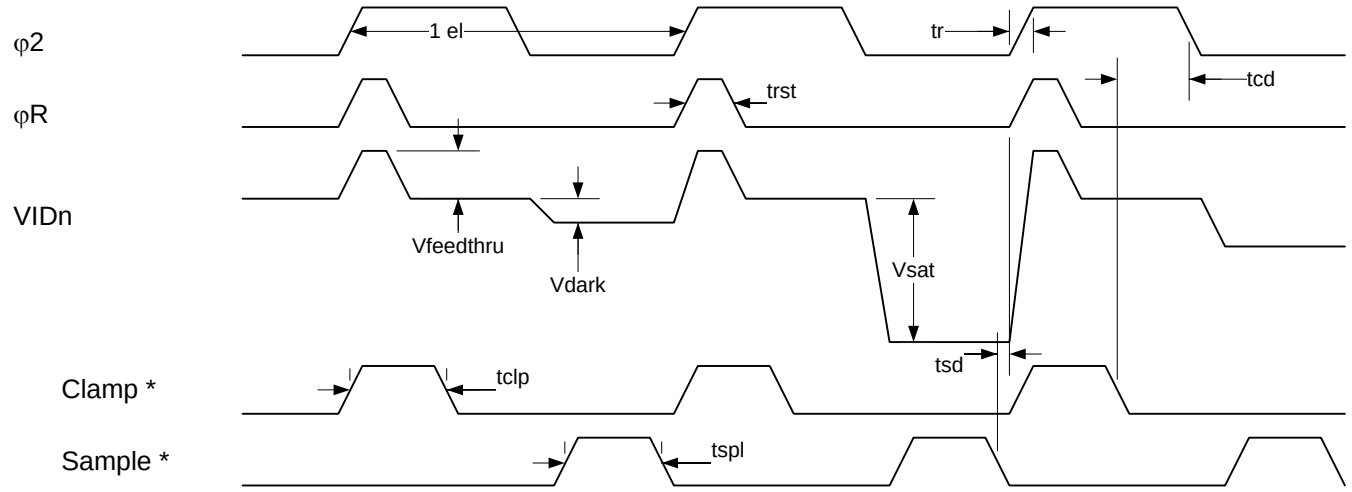


Figure 18: Photodiode-to-CCD Transfer



* Required for Optional Off-Chip, Analog, Correlated Double Sampling (CDS) Signal Processing

Figure 19: Output Timing

Storage and Handling

Storage Conditions

Description	Symbol	Minimum	Maximum	Units	Notes
Operating Temperature	T_{op}	0	70	°C	1
Storage Temperature	T_{st}	-25	+80	°C	2

Notes:
1. Noise performance will degrade with increasing temperatures.
2. Long term storage at these temperatures will accelerate color filter degradation.

ESD

1. This device contains limited protection against Electrostatic Discharge (ESD). ESD events may cause irreparable damage to a CCD image sensor either immediately or well after the ESD event occurred. Failure to protect the sensor from electrostatic discharge may affect device performance and reliability.
2. Devices should be handled in accordance with strict ESD procedures for Class 0 (<250 V per JESD22 Human Body Model test), or Class A (<200 V JESD22 Machine Model test) devices. Devices are shipped in static-safe containers and should only be handled at static-safe workstations.
3. See Application Note *Image Sensor Handling Best Practices* for proper handling and grounding procedures. This application note also contains workplace recommendations to minimize electrostatic discharge.
4. Store devices in containers made of electro-conductive materials.

Cover Glass Care and Cleanliness

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided.
3. Improper cleaning of the cover glass may damage these devices. Refer to Application Note *Image Sensor Handling Best Practices*.

Environmental Exposure

1. Extremely bright light can potentially harm CCD image sensors. Do not expose to strong sunlight for long periods of time, as the color filters and/or microlenses may become discolored. In addition, long time exposures to a static high contrast scene should be avoided. Localized changes in response may occur from color filter/microlens aging. For Interline devices, refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible lighting Conditions*.
2. Exposure to temperatures exceeding maximum specified levels should be avoided for storage and operation, as device performance and reliability may be affected.
3. Avoid sudden temperature changes.
4. Exposure to excessive humidity may affect device characteristics and may alter device performance and reliability, and therefore should be avoided.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases, as deterioration of lead solderability may occur. It is advised that the solderability of the device leads be assessed after an extended period of storage, over one year.

Soldering Recommendations

1. The soldering iron tip temperature is not to exceed 370 °C. Higher temperatures may alter device performance and reliability.
2. Flow soldering method is not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. Recommended method is by partial heating using a grounded 30 W soldering iron. Heat each pin for less than 2 seconds duration.

Mechanical Information

COMPLETED ASSEMBLY

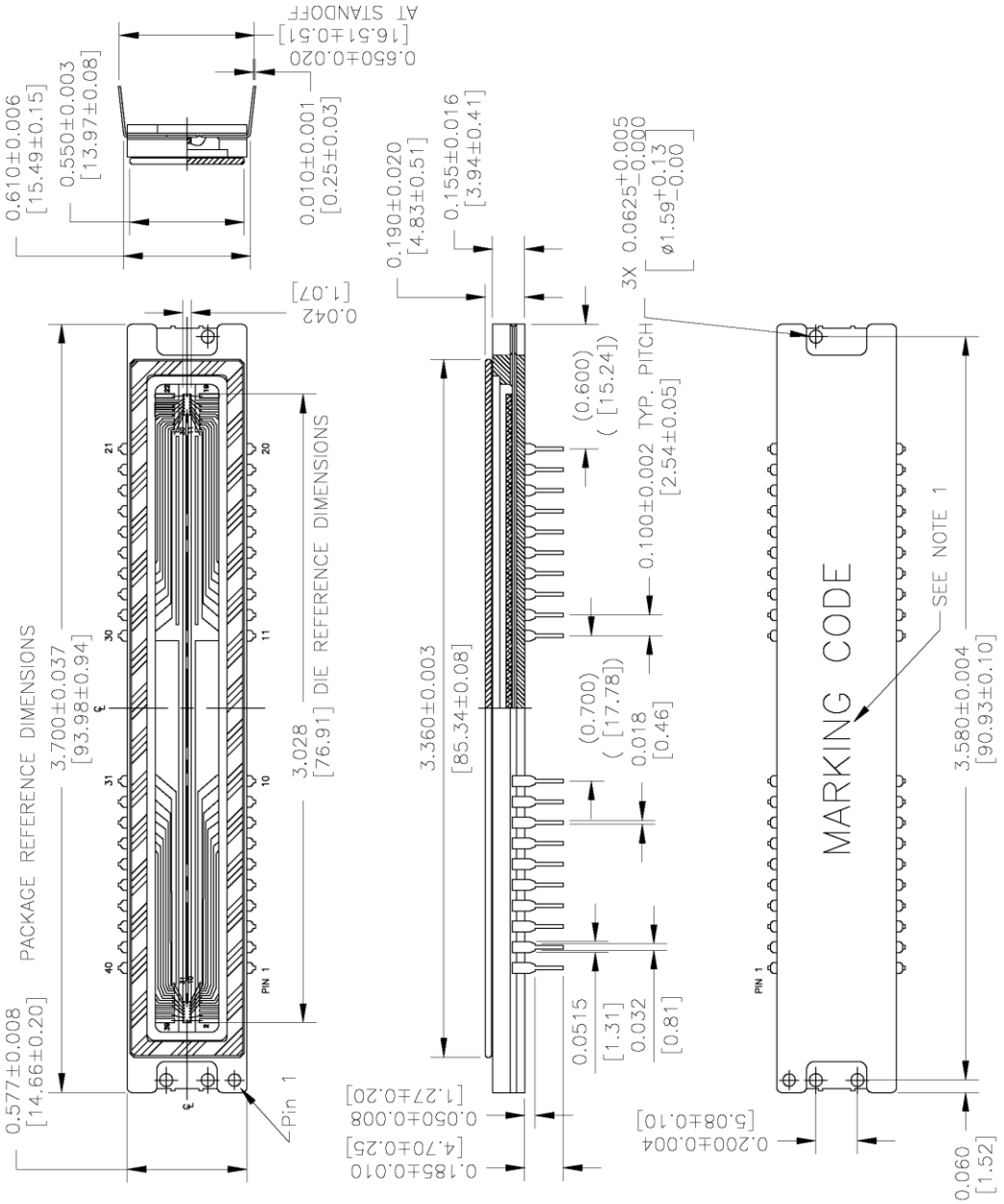


Figure 20: Completed Assembly Drawing (1 of 2)

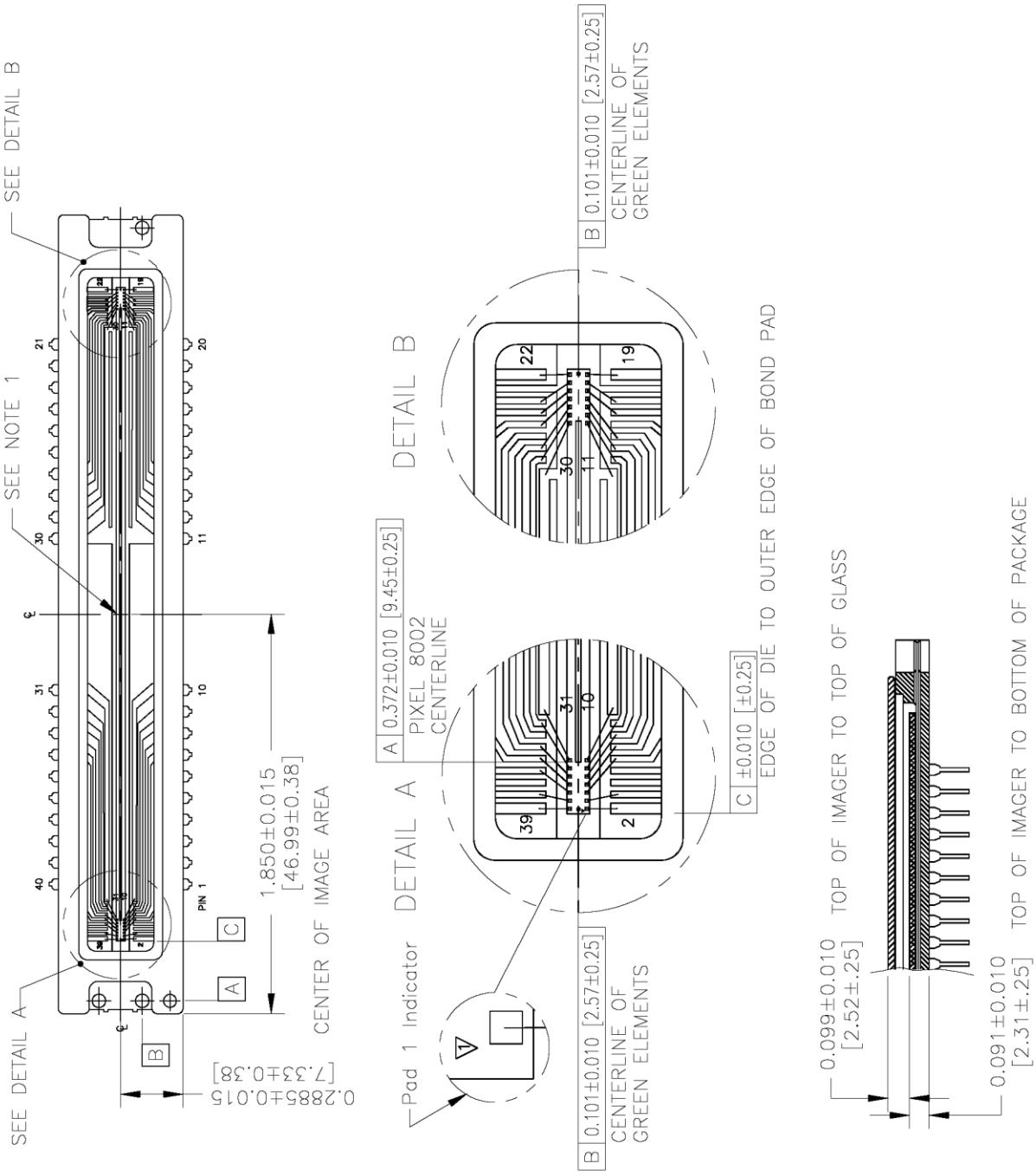


Figure 21: Completed Assembly Drawing (2 of 2)

COVER GLASS

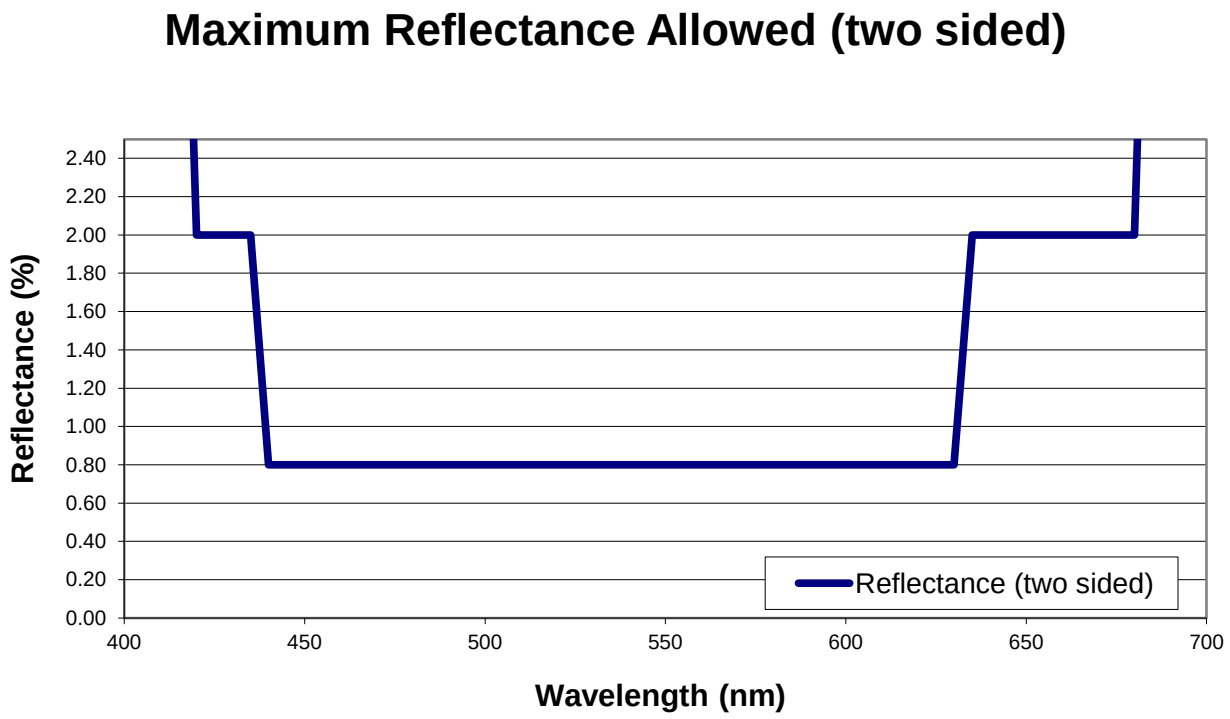


Figure 22: Two-Sided Multilayer Anti-Reflective Cover Glass Specification (MAR)

Quality Assurance and Reliability

Quality and Reliability

All image sensors conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and visual inspection and electrical testing at key points of the manufacturing process, using industry standard methods. Information concerning the quality assurance and reliability testing procedures and results are available from ON Semiconductor upon request. For further information refer to Application Note *Quality and Reliability*.

Replacement

All devices are warranted against failure in accordance with the *Terms of Sale*. Devices that fail due to mechanical and electrical damage caused by the customer will not be replaced.

Liability of the Supplier

A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer. Product liability is limited to the cost of the defective item, as defined in the *Terms of Sale*.

Liability of the Customer

Damage from mishandling (scratches or breakage), electrostatic discharge (ESD), or other electrical misuse of the device beyond the stated operating or storage limits, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

Test Data Retention

Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

Mechanical

The device assembly drawing is provided as a reference.

ON Semiconductor reserves the right to change any information contained herein without notice. All information furnished by ON Semiconductor is believed to be accurate.

Life Support Applications Policy

ON Semiconductor image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of ON Semiconductor.

Revision Changes

MTD/PS-0219

Revision Number	Description of Changes
1.0	• Initial Issue of Document
2.0	• Removed reference to notes 11 and 16 for Darkfield and Brightfield defects in table on page 3. These do not apply since no defects allowed.
3.0	• Updated document format.
4.0	• Corrected Completed Assembly Drawings

PS-0052

Revision Number	Description of Changes
1.0	• Initial release with new document number, updated branding and document template • Updated *Storage and Handling* and *Quality Assurance and Reliability* sections
1.1	• Updated branding

PUBLICATION ORDERING INFORMATION

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