

# ESD7361, SZESD7361

## ESD Protection Diodes

### Low Capacitance ESD Protection Diode for High Speed Data Line

The ESD7361 Series ESD protection diodes are designed to protect high speed data lines from ESD. Ultra-low capacitance make this device an ideal solution for protecting voltage sensitive high speed data lines.

#### Features

- Low Capacitance (0.55 pF Max, I/O to GND)
- Protection for the Following IEC Standards:
  - ♦ IEC61000-4-2 (ESD): Level 4 ±15 kV Contact
  - ♦ IEC61000-4-4 (EFT): 40 A -5/50 ns
  - ♦ IEC61000-4-5 (Lightning): 1 A (8/20 μs)
- ISO 10605 (ESD) 330 pF/2 kΩ ±15 kV Contact
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

#### Typical Applications

- Wireless Charger
- Near Field Communications

#### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T <sub>J</sub>	-55 to +125	°C
Storage Temperature Range	T <sub>stg</sub>	-55 to +150	°C
Lead Solder Temperature – Maximum (10 Seconds)	T <sub>L</sub>	260	°C
IEC 61000-4-2 Contact (ESD)	ESD	±15	kV
IEC 61000-4-2 Air (ESD)	ESD	±15	kV
ISO 10605 330 pF/2 kΩ Contact (ESD)	ESD	±15	kV

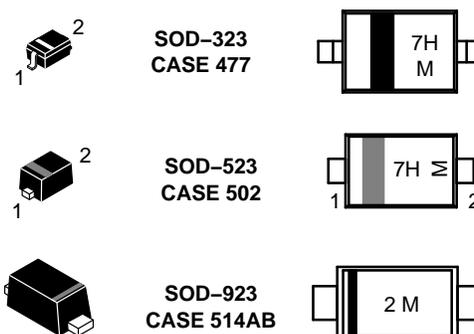
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



ON Semiconductor®

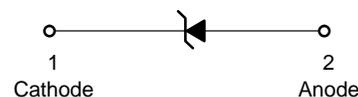
[www.onsemi.com](http://www.onsemi.com)

#### MARKING DIAGRAMS



X, XX = Specific Device Code  
M = Date Code

#### PIN CONFIGURATION AND SCHEMATIC



#### ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

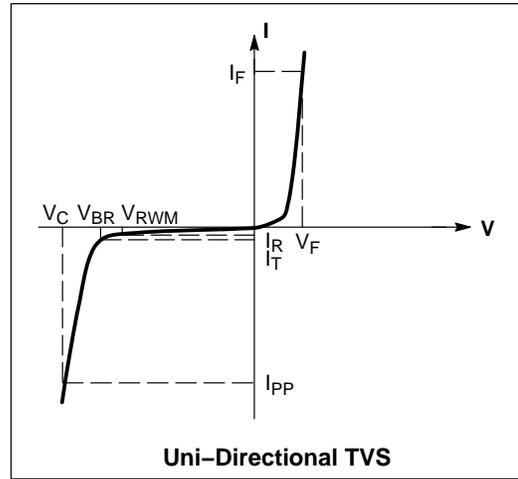
# ESD7361, SZESD7361

## ELECTRICAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter
$I_{PP}$	Maximum Reverse Peak Pulse Current
$V_C$	Clamping Voltage @ $I_{PP}$
$V_{RWM}$	Working Peak Reverse Voltage
$I_R$	Maximum Reverse Leakage Current @ $V_{RWM}$
$V_{BR}$	Breakdown Voltage @ $I_T$
$I_T$	Test Current

\*See Application Note AND8308/D for detailed explanations of datasheet parameters.



## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	$V_{RWM}$			5	16	V
Breakdown Voltage	$V_{BR}$	$I_T = 1 \text{ mA}$ ; pin 1 to pin 2	16.5			V
Reverse Leakage Current	$I_R$	$V_{RWM} = 5.0 \text{ V}$		<1	1000	nA
Clamping Voltage (Note 2)	$V_C$	$I_{PP} = 8 \text{ A}$		31		V
Clamping Voltage (Note 2)	$V_C$	$I_{PP} = 16 \text{ A}$		34		V
Junction Capacitance	$C_J$	$V_R = 0 \text{ V}$ , $f = 1 \text{ MHz}$ $V_R = 0 \text{ V}$ , $f < 1 \text{ GHz}$			0.55 0.55	pF
Dynamic Resistance	$R_{DYN}$	TLP Pulse		0.735		$\Omega$
Insertion Loss		$f = 1 \text{ MHz}$ $f = 5 \text{ GHz}$		0.01 2		dB

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- For test procedure see Figures 9 and 10 and application note AND8307/D.
- ANSI/ESD STM5.5.1 – Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.  
TLP conditions:  $Z_0 = 50 \Omega$ ,  $t_p = 100 \text{ ns}$ ,  $t_r = 4 \text{ ns}$ , averaging window;  $t_1 = 30 \text{ ns}$  to  $t_2 = 60 \text{ ns}$ .

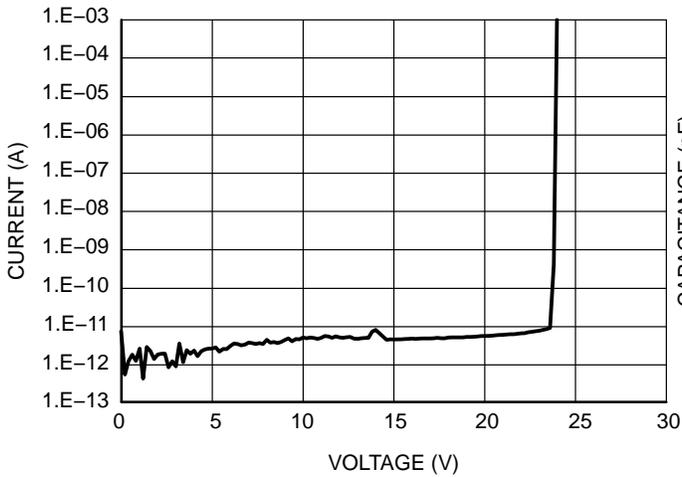


Figure 1. Typical IV Characteristics

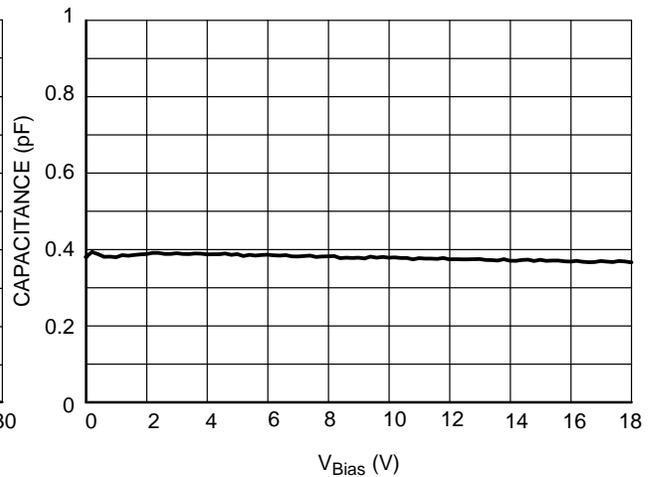
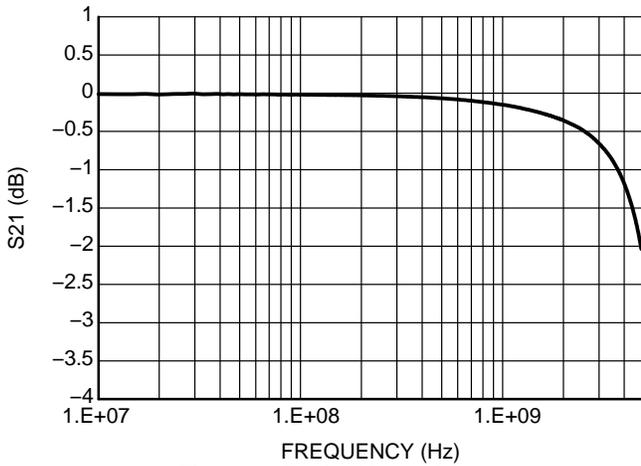
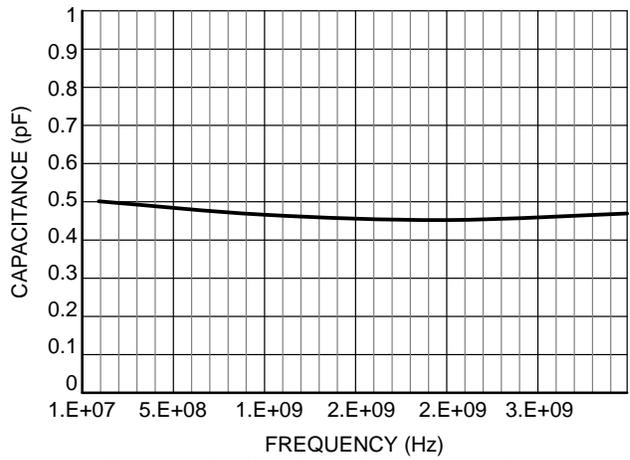


Figure 2. Typical CV Characteristics

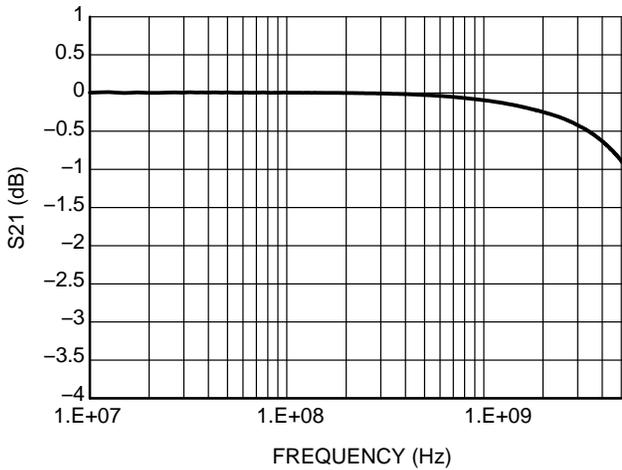
# ESD7361, SZESD7361



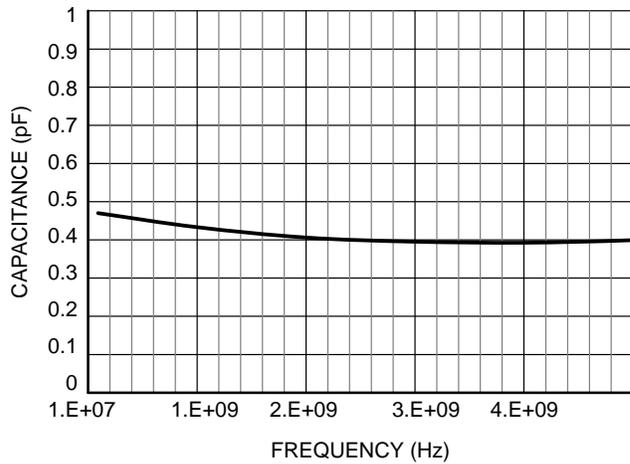
**Figure 3. Typical Insertion Loss  
ESD7361HT1G (SOD323)**



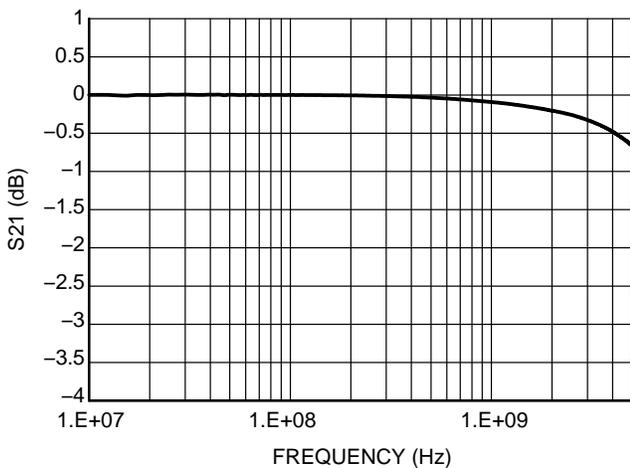
**Figure 4. Typical Capacitance Over Frequency  
ESD7361HT1G (SOD323)**



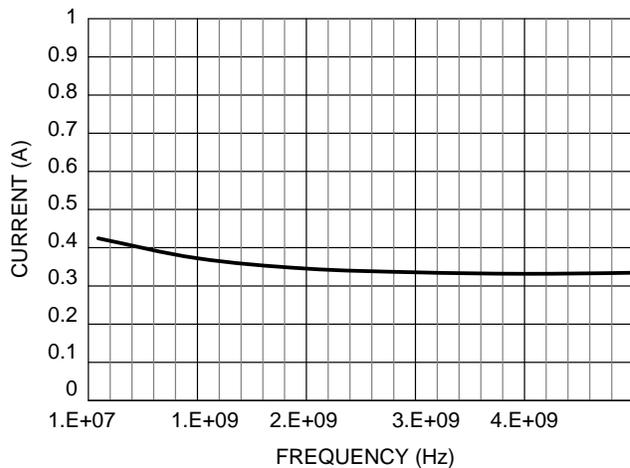
**Figure 5. Typical Insertion Loss  
ESD7361XV2T1G (SOD523)**



**Figure 6. Typical Capacitance Over Frequency  
ESD7361XV2T1G (SOD523)**



**Figure 7. Typical Insertion Loss  
ESD7361P2T5G (SOD923)**



**Figure 8. Typical Capacitance Over Frequency  
ESD7361P2T5G (SOD923)**

# ESD7361, SZESD7361

## IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

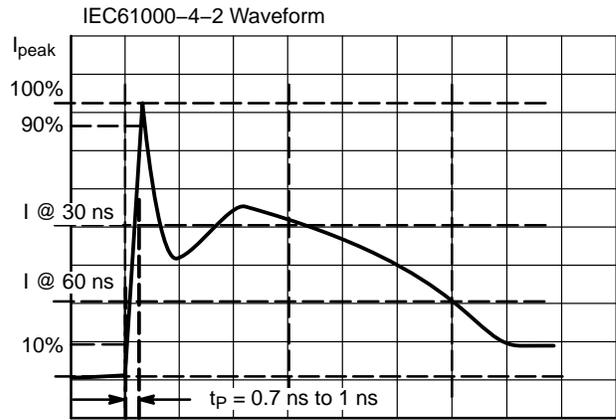


Figure 9. IEC61000-4-2 Spec

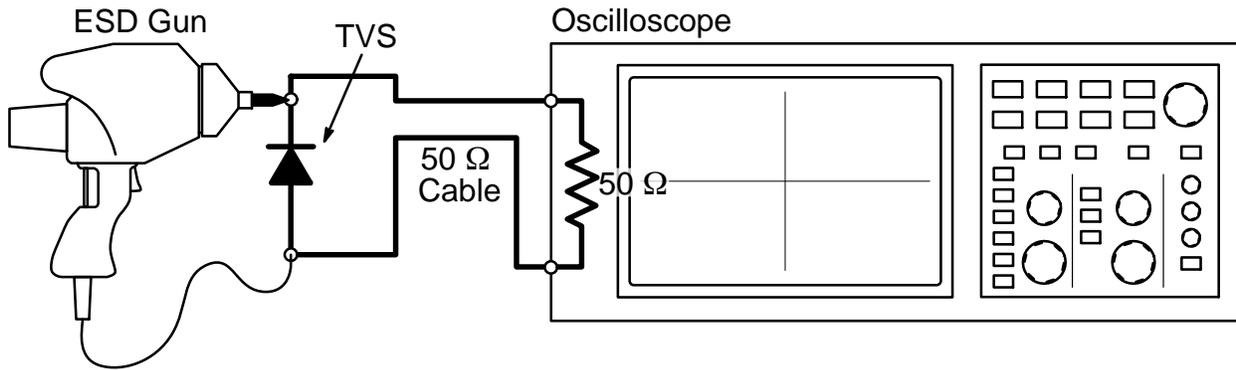


Figure 10. Diagram of ESD Clamping Voltage Test Setup

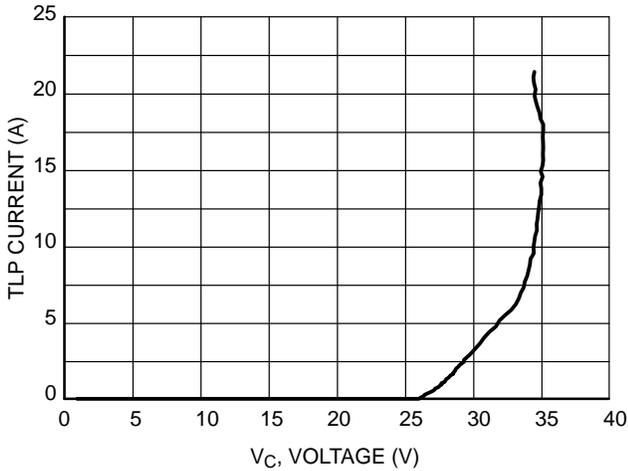
The following is taken from Application Note AND8308/D – Interpretation of Datasheet Parameters for ESD Devices.

### ESD Voltage Clamping

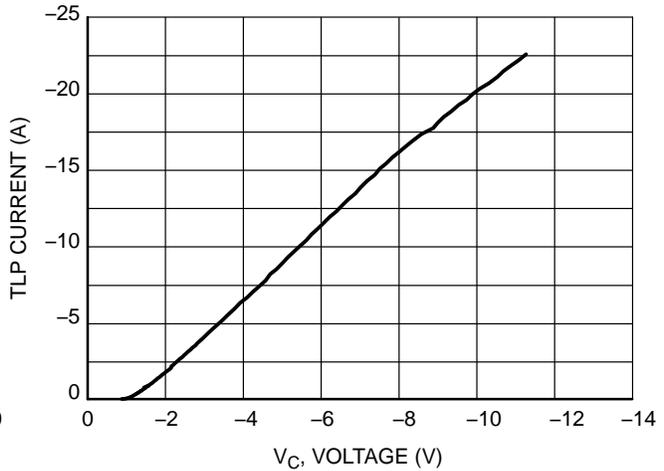
For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger

systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

## ESD7361, SZESD7361



**Figure 11. Positive TLP I-V Curve**

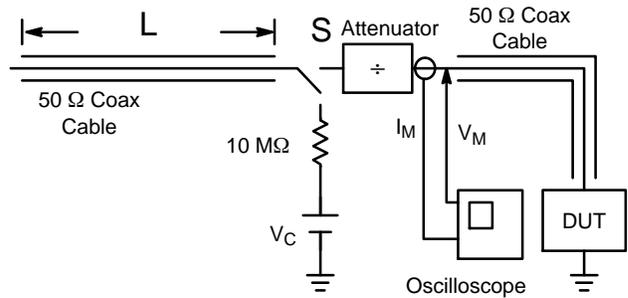


**Figure 12. Negative TLP I-V Curve**

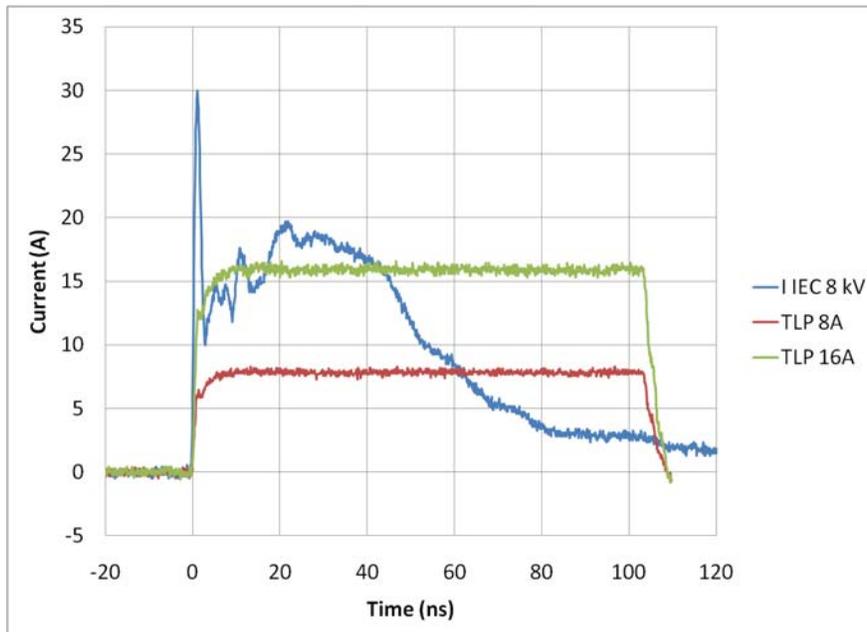
NOTE: TLP parameter:  $Z_0 = 50 \Omega$ ,  $t_p = 100 \text{ ns}$ ,  $t_r = 300 \text{ ps}$ , averaging window:  $t_1 = 30 \text{ ns}$  to  $t_2 = 60 \text{ ns}$ .  $V_{IEC}$  is the equivalent voltage stress level calculated at the secondary peak of the IEC 61000-4-2 waveform at  $t = 30 \text{ ns}$  with  $2 \text{ A/kV}$ . See TLP description below for more information.

### Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I-V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 13. TLP I-V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 14 where an 8 kV IEC 61000-4-2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I-V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.



**Figure 13. Simplified Schematic of a Typical TLP System**



**Figure 14. Comparison Between 8 kV IEC 61000-4-2 and 8 A and 16 A TLP Waveforms**

# ESD7361, SZESD7361

## ORDERING INFORMATION

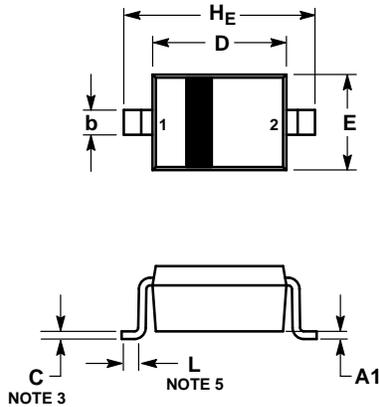
Device	Package	Shipping†
ESD7361HT1G	SOD-323 (Pb-Free)	3000 / Tape & Reel
ESD7361XV2T1G	SOD-523 (Pb-Free)	3000 / Tape & Reel
ESD7361P2T5G	SOD-923 (Pb-Free)	8000 / Tape & Reel
SZESD7361HT1G	SOD-323 (Pb-Free)	3000 / Tape & Reel
SZESD7361XV2T1G	SOD-523 (Pb-Free)	3000 / Tape & Reel
SZESD7361P2T5G	SOD-923 (Pb-Free)	8000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# ESD7361, SZESD7361

## PACKAGE DIMENSIONS

SOD-323  
CASE 477-02  
ISSUE H

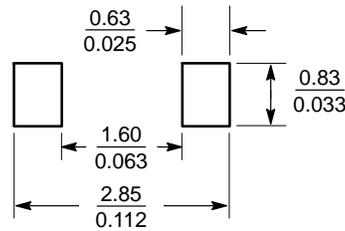


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. LEAD THICKNESS SPECIFIED PER L/F DRAWING WITH SOLDER PLATING.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
5. DIMENSION L IS MEASURED FROM END OF RADIUS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.031	0.035	0.040
A1	0.00	0.05	0.10	0.000	0.002	0.004
A3	0.15 REF			0.006 REF		
b	0.25	0.32	0.4	0.010	0.012	0.016
C	0.089	0.12	0.177	0.003	0.005	0.007
D	1.60	1.70	1.80	0.062	0.066	0.070
E	1.15	1.25	1.35	0.045	0.049	0.053
L	0.08			0.003		
HE	2.30	2.50	2.70	0.090	0.098	0.105

### SOLDERING FOOTPRINT\*

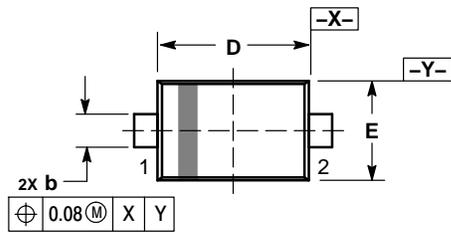


\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

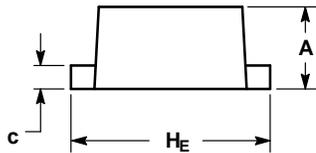
# ESD7361, SZESD7361

## PACKAGE DIMENSIONS

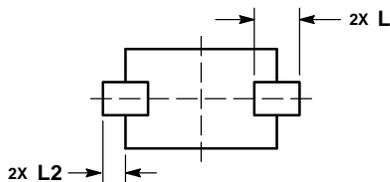
**SOD-523**  
CASE 502  
ISSUE E



**TOP VIEW**



**SIDE VIEW**



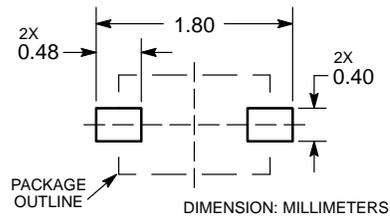
**BOTTOM VIEW**

**NOTES:**

6. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
7. CONTROLLING DIMENSION: MILLIMETERS.
8. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
9. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.50	0.60	0.70
b	0.25	0.30	0.35
c	0.07	0.14	0.20
D	1.10	1.20	1.30
E	0.70	0.80	0.90
H E	1.50	1.60	1.70
L	0.30 REF		
L2	0.15	0.20	0.25

**RECOMMENDED  
SOLDERING FOOTPRINT\***

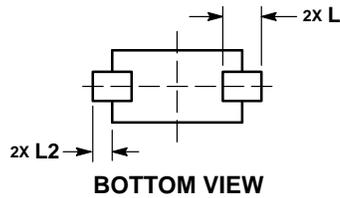
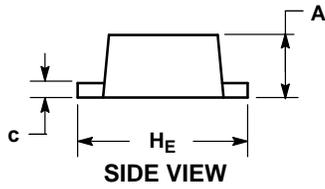
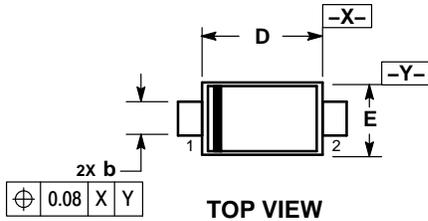


\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# ESD7361, SZESD7361

## PACKAGE DIMENSIONS

**SOD-923**  
CASE 514AB  
ISSUE C

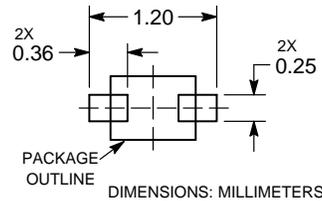


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.34	0.37	0.40	0.013	0.015	0.016
b	0.15	0.20	0.25	0.006	0.008	0.010
c	0.07	0.12	0.17	0.003	0.005	0.007
D	0.75	0.80	0.85	0.030	0.031	0.033
E	0.55	0.60	0.65	0.022	0.024	0.026
HE	0.95	1.00	1.05	0.037	0.039	0.041
L	0.19 REF			0.007 REF		
L2	0.05	0.10	0.15	0.002	0.004	0.006

**SOLDERING FOOTPRINT\***



See Application Note AND8455/D for more mounting details

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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