XR10910

16:1 Sensor Interface AFE

General Description

The XR10910 is a unique sensor interface integrated circuit with an on-board 16:1 multiplexer, offset correction DAC, instrumentation amplifier and voltage reference. The XR10910 is designed to integrate multiple bridge sensors with a microcontroller (MCU) or field-programmable gate array (FPGA).

The integrated offset correction DAC provides digital calibration of the variable and in many cases substantial offset voltage generated by the bridge sensors. The DAC is controlled by an I2C compatible 2 wire serial interface. The serial interface also provides the user with easy controls to the XR10910's many functions such as input and gain selection.

An integrated LDO provides a regulated voltage to power the input bridge sensors and is selectable, between 3V and 2.65V, via the serial interface for lower voltage compatibility. The LDO current can be sensed and a proportional voltage present at the output of the IC for monitoring the LDO current.

The XR10910 offers 8 fixed gain settings (from 2V/V to 760V/V), each with an error of only ±0.5%, that are selectable via the I2C interface. It also offers less than 1mV maximum input offset voltage, 100pA maximum input bias current, and 100pA maximum input offset current.

The XR10910 is designed to operate from 2.7V to 5V supplies and is specified over the industrial temperature range of -40°C to +85°C. It is offered in a space saving 6mm x 6mm QFN-40 package. It consumes less than 556µA maximum supply current and offers a sleep mode for added power savings.

The low power, low input bias current and integrated features make the XR10910 well suited for both industrial and consumer applications using bridge sensors.

FEATURES

- Integrated features for interfacing multiple bridge sensors with an MCU or FPGA:
  - 16:1 differential mux with I²C interface
  - Instrumentation amplifier
  - LDO
  - Offset correction DAC with I²C interface (±560mV offset correction range - RTI)
- Eight selectable voltage gains from 2V/V to 760V/V with only ±0.5% gain error
- 1mV maximum input offset voltage
- 100pA maximum input bias current
- 556µA maximum supply current
- 2.7V to 5V analog supply voltage range
- 1.8V to 5V digital supply voltage range
- -40˚C to +85˚C temperature range
- 6mm x 6mm QFN-40 package

APPLICATIONS

- Bridge sensor interface
- Pressure & temperature sensors
- Strain gauge amplifier
- Industrial process controls
- Weigh scales

Ordering Information - back page

Typical Application

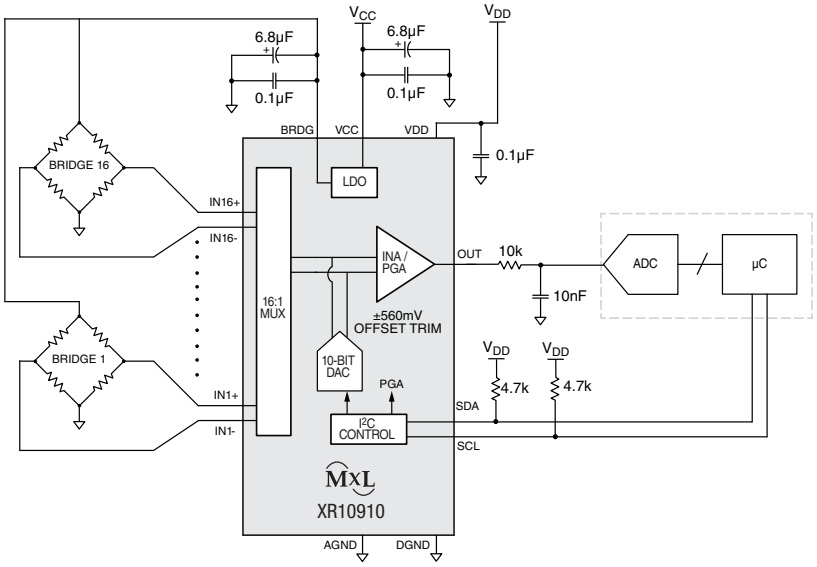


Figure 1. Typical Application

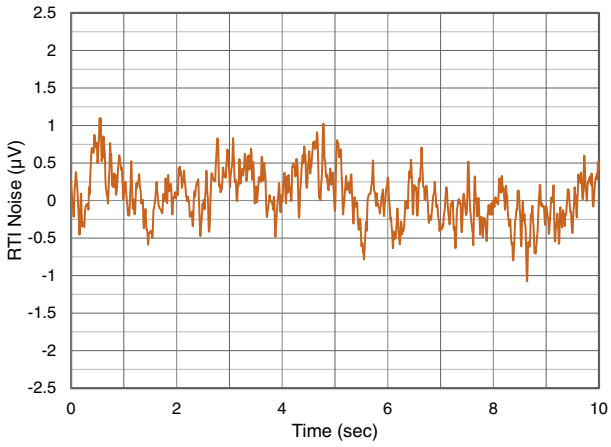


Figure 2. 0.1Hz to 10Hz RTI Voltage Noise

Absolute Maximum Ratings

Stresses beyond the limits listed below may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Analog Supply Voltage (V_{CC}) ..... 0V to 5.5V
Digital Supply Voltage (V_{DD}) ..... 0V to 5.5V
Digital Input/Output (V_{DDIO}) ..... 0V to 5.5V
V_{IN} ..... 0 to V_{CC}
Differential Input Voltage (current limit of 10mA) ..... V_{CC}
ESD Rating (HBM - Human Body Model) 4kV

Operating Conditions

Analog Supply Voltage Range ..... 2.7V to 5.25V
Digital Supply Voltage Range ..... 1.7V to 5.25V
Operating Temperature Range ..... -40°C to 85°C
Junction Temperature ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10s) ..... 260°C

Package thermal resistance θ_{JA} ..... 32°C/W

NOTE:

1. JEDEC standard, multi-layer test boards, still air.

Electrical Characteristics

T_A = 25°C, V_{CC} = 3.3V, V_{DD} = 1.8V, R_L = 10kΩ to 1.5V; G = 760; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DC Performance						
V_{IO}	Input offset voltage	Input referred	-1	±0.02	1	mV
d_{VIO}	Input offset voltage average drift			3		µV/°C
I_B	Input bias current		-100	15	100	pA
I_{OS}	Input offset current		-100	1	100	pA
PSRR	Power supply rejection ratio	V_{CC} = 2.7V to 5V	60	91		dB
Gain	Gain = 2	Nominal; refer to Gain Register Table (pg. 10)		2.0		V/V
	Gain = 20			20.0		V/V
	Gain = 40			40.0		V/V
	Gain = 80			80.0		V/V
	Gain = 150			150.0		V/V
	Gain = 300			299.9		V/V
	Gain = 600			599.6		V/V
	Gain = 760			759.4		V/V
G_E	Gain error		-0.5		0.5	%
	Gain error vs temperature			±10		ppm/°C
I_{SVCC}	V_{CC} supply current	No load to output; no load to LDO		435	530	µA
I_{SVCCD}	Disable V_{CC} supply current	No load to output; no load to LDO		48	59	µA
I_{SVDD}	V_{DD} supply current	No load to output; no load to LDO; I^2C running		22	26	µA
I_{STOTAL}	Total supply current	No load to output; no load to LDO		457	556	µA
$I_{SDTOTAL}$	Total disable supply current	No load to output; no load to LDO; LDO DIS		45		µA
		No load to output; no load to LDO; LDO EN		70	85	µA
Input Characteristics						
	Input impedance			10^{13} || 11.2		Ω || pF
CMIR	Common mode input range		0.5	0.23 to 3.06	2.5	V
CMRR	Common mode rejection ratio	Input referred. V_{CM} = 0.5 to 2.0V	75	88		dB
Output Characteristics						
V_{OUT}	Output voltage swing	R_L = 10kΩ to 1.5V	0.1	0.04 to 3.29	3.1	V
V_{OO}	Output offset	Offset DAC 0 00 0000 0000; G = 2	1.4	1.5	1.6	V
Offset DAC						
	Offset DAC range	RTI (referred to input)	±560			mV
	Offset monotonicity		8	10		Bits
LDO						
	Output voltage	1.5k load, LDO bit LOW	-6%	3	+6%	V
		1.5k load, LDO bit HIGH	-6%	2.65	+6%	V
	Dropout voltage	V_{CC} = 2.8V, LDO = 2.65V, I_{LOAD} = 10mA			150	mV
	Output current		10	25		mA
	Power supply rejection ratio	Output referred, V_{CC} = 3V to 5V, LDO = 2.65V	45	63		dB
		Output referred, V_{CC} = 3.3V to5V, LDO = 3V	45	63		dB
	Output current sense transimpedance slope	Output voltage relative to 1.5V / LDO current, G = 2	0.08	0.1	0.12	V/mA
	Output current sense range clip	G = 2		18.8		mA

Electrical Characteristics (Continued)

T_A = 25°C, V_{CC} = 3.3V, V_{DD} = 1.8V, R_L = 10kΩ to 1.5V; G = 760; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Dynamic Performance						
BW	-3dB bandwidth	G = 760		66		kHz
		G = 2		1300		kHz
SR	Slew rate	V_{OUT} = 1V_{pp}; Gain = 2		1		V/µs
e_{ni}	Input voltage noise - RTI	f = 10Hz		75		nV/√Hz
		f = 100Hz		46		nV/√Hz
		f = 1kHz		35		nV/√Hz
i_n	Input current noise	f = 10Hz		0.6		fA/√Hz
e_{npp}	Peak-to-peak noise	f = 0.1 to 10Hz		2		µV_{pp}
XTALK	Crosstalk	Channel-to-channel, f = 1kHz		90		dB
T_S	Set-up time, 1% settling	Analog ready after serial register finished write		3.5		µs
T_{WAKE}	Wake up time, 1% settling	Wake from ACK of SLEEP_OUT command		9.6		µs

Digital Characteristics (CMOS)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Logic Input HIGH		0.7 x V_{DD}		V_{DD}	V
V_{IL}	Logic Input LOW		0		0.3 x V_{DD}	V
I_{IH}	Input Leakage HIGH	$V_I = V_S$			10	µA
I_{IL}	Input Leakage LOW	V_I = 0	-10			µA
CLK_F	Clock Rate				0.4	MHz

I²C Bus Timing

T_A = -40 to +85°C, V_{DD} = 1.8 - 5V; unless otherwise noted.

Symbol	Parameter	Standard Mode I²C-BUS		Fast Mode I²C-BUS		Units
		Min	Max	Min	Max	
f_{SCL}	Operating frequency	0	100	0	400	kHz
T_{BUF}	Bus free time between STOP and START	4.7		1.3		µs
$T_{HD;STA}$	START condition hold time	4.0		0.6		µs
$T_{SU;STA}$	START condition setup time	4.7		0.6		µs
$T_{HD;DAT}$	Data hold time	0		0		µs
$T_{VD;ACK}$	Data valid acknowledge		0.6		0.6	µs
$T_{VD;DAT}$	SCL LOW to data out valid		0.6		0.6	ns
$T_{SU;DAT}$	Data setup time	250		150		ns
T_{LOW}	Clock LOW period	4.7		1.3		µs
T_{HIGH}	Clock HIGH period	4.0		0.6		µs
T_F	Clock/data fall time		300		300	ns
T_R	Clock/data rise time		1000		300	ns
T_{SP}	Pulse width of spikes tolerance	0.5		0.5		µs

Electrical Characteristics (Continued)

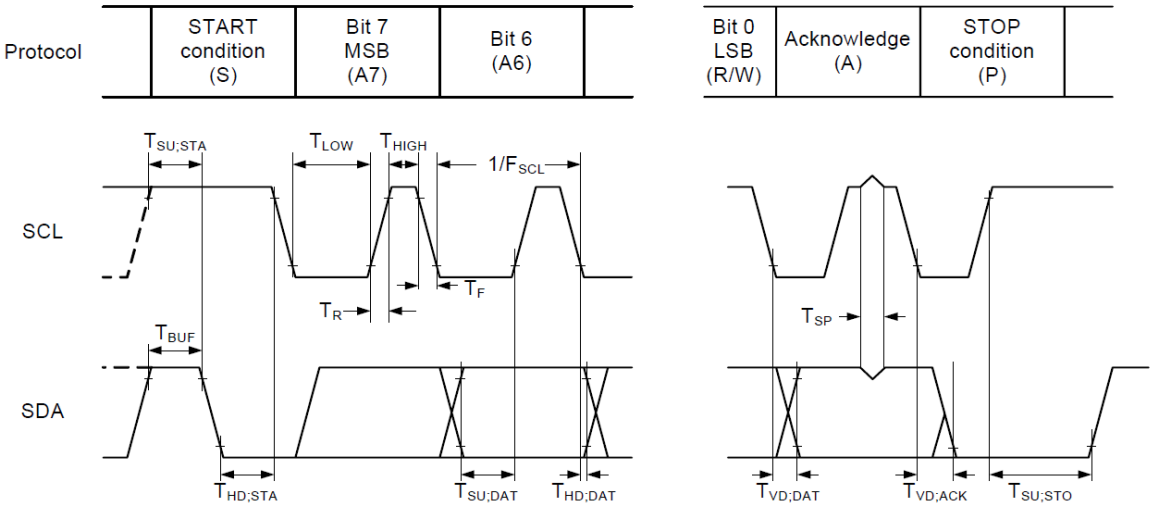


Figure 3: I²C Bus Timing Diagram

Register Information

Table 1. Register List

Reg No. Hex	Reg No. Dec	Name	Function	R/W/C	Byte of Parameter	Parameter	Default Code	Power-up Condition	Remark
0x00	0	NOP	No operation	C	0		N/A		Does not execute a function. NOP is used to test successful I²C communication
Reset									
0x01	1	SW_RESET	Software reset	C	0		N/A		Resets all registers to default values
Read ID									
0x02	2	DEVICE_ID	Read Device ID	R	2	[15:0]: report “0910” in BCD	0x0910		Instructs the XR10910 to report its device ID “0910” in binary form (0000 1001 0001 0000)
0x03	3	VERSION_ID	Read HW & SW version numbers	R	2	[15:12]: reserved [11:8]: Hardware version # [7:0]: Software version #	N/A		Initial H/W version number is ‘0’; Initial S/W version number is ‘01’.
Sleep in/out									
0x04	4	SLEEP_OUT _ REG	Normal operating mode, system active	C	0		N/A	Active	Puts the XR10190 into active mode. (wake up)
0x05	5	SLEEP_IN_ REG	Sleep Mode	C	0		N/A	Active	Puts the analog portion of the XR10910 into sleep mode. During sleep mode, the only I²C command that can be received/processed is the SLEEP_OUT command (0x04). All other register addresses will be ignored.
Basic Config									
0x06	6	Gain	Gain select	R/W	1	[2:0]: Gain select	0x00	Gain = 2	Eight gain settings are selectable (from 2V/V to 760V/V), refer to the Gain Register Table for more information.
0x07	7	LDO	LDO Settings	R/W	1	[0]:LDO 3V, 2.65V [1]:LDO disable	0x00	LDO = 3V	Bit 0 controls the LDO voltage (0: 3V; 1: 2.65V). Bit 1 (Sleep Mode only). Bit 1 controls whether the LDO shuts down or stays on during Sleep Mode. (0: Enable; 1: Disable). When the XR10910 is active, the LDO is always on.
0x08	8	LDO Current Sense Select	LDO Current Sense	C	0		N/A	Off	When on, the LDO current is sensed and a proportional voltage is present at the output of the XR10910. Current Sense Mode remains active until an input select command is received by the XR10910.

Reg No.		Name	Function	R/W/C	Byte of Parameter	Parameter	Default Code	Power-up Condition	Remark
Hex	Dec								
Channel Switch (Input Mux Select)									
0x10	16	Select_ Input_1	Select Channel 1	C	0		N/A	Channel 1 is selected	Select +IN1, -IN1; Channel 1
0x11	17	Select_ Input_2	Select Channel 2	C	0				Select +IN2, -IN2; Channel 2
0x12	18	Select_ Input_3	Select Channel 3	C	0				Select +IN3, -IN3; Channel 3
0x13	19	Select_ Input_4	Select Channel 4	C	0				Select +IN4, -IN4; Channel 4
0x14	20	Select_ Input_5	Select Channel 5	C	0				Select +IN5, -IN5; Channel 5
0x15	21	Select_ Input_6	Select Channel 6	C	0				Select +IN6, -IN6; Channel 6
0x16	22	Select_ Input_7	Select Channel 7	C	0				Select +IN7, -IN7; Channel 7
0x17	23	Select_ Input_8	Select Channel 8	C	0				Select +IN8, -IN8; Channel 8
0x18	24	Select_ Input_9	Select Channel 9	C	0				Select +IN9, -IN9; Channel 9
0x19	25	Select_ Input_10	Select Channel 10	C	0				Select +IN10, -IN10; Channel 10
0x1A	26	Select_ Input_11	Select Channel 11	C	0				Select +IN11, -IN11; Channel 11
0x1B	27	Select_ Input_12	Select Channel 12	C	0				Select +IN12, -IN12; Channel 12
0x1C	28	Select_ Input_13	Select Channel 13	C	0				Select +IN13, -IN13; Channel 13
0x1D	29	Select_ Input_14	Select Channel 14	C	0				Select +IN14, -IN14; Channel 14
0x1E	30	Select_ Input_15	Select Channel 15	C	0				Select +IN15, -IN15; Channel 15
0x1F	31	Select_ Input_16	Select Channel 16	C	0				Select +IN16, -IN16; Channel 16

Reg No.		Name	Function	R/W/C	Byte of Parameter	Parameter	Default Code	Power-up Condition	Remark
Hex	Dec								
Offset DAC Config									
0x20	32	DAC1	Configures DAC offset applied to Channel 1	R/W	2	[10]: DAC Sign [9:0]: DAC Range	0x00	0mV offset	Bit 10 controls the sign of the DAC offset voltage. Bits 9 thru 0 control the value of the DAC offset voltage. [10]: DAC Sign 0 = positive; 1 = negative
0x21	33	DAC2	Configures DAC offset applied to Channel 2	R/W	2				
0x22	34	DAC3	Configures DAC offset applied to Channel 3	R/W	2				
0x23	35	DAC4	Configures DAC offset applied to Channel 4	R/W	2				
0x24	36	DAC5	Configures DAC offset applied to Channel 5	R/W	2				
0x25	37	DAC6	Configures DAC offset applied to Channel 6	R/W	2				
0x26	38	DAC7	Configures DAC offset applied to Channel 7	R/W	2				
0x27	39	DAC8	Configures DAC offset applied to Channel 8	R/W	2				
0x28	40	DAC9	Configures DAC offset applied to Channel 9	R/W	2				
0x29	41	DAC10	Configures DAC offset applied to Channel 10	R/W	2				
0x2A	42	DAC11	Configures DAC offset applied to Channel 11	R/W	2				
0x2B	43	DAC12	Configures DAC offset applied to Channel 12	R/W	2				
0x2C	44	DAC13	Configures DAC offset applied to Channel 13	R/W	2				
0x2D	45	DAC14	Configures DAC offset applied to Channel 14	R/W	2				
0x2E	46	DAC15	Configures DAC offset applied to Channel 15	R/W	2				
0x2F	47	DAC16	Configures DAC offset applied to Channel 16	R/W	2				

NOTE:

Register Numbers not listed above have no function.

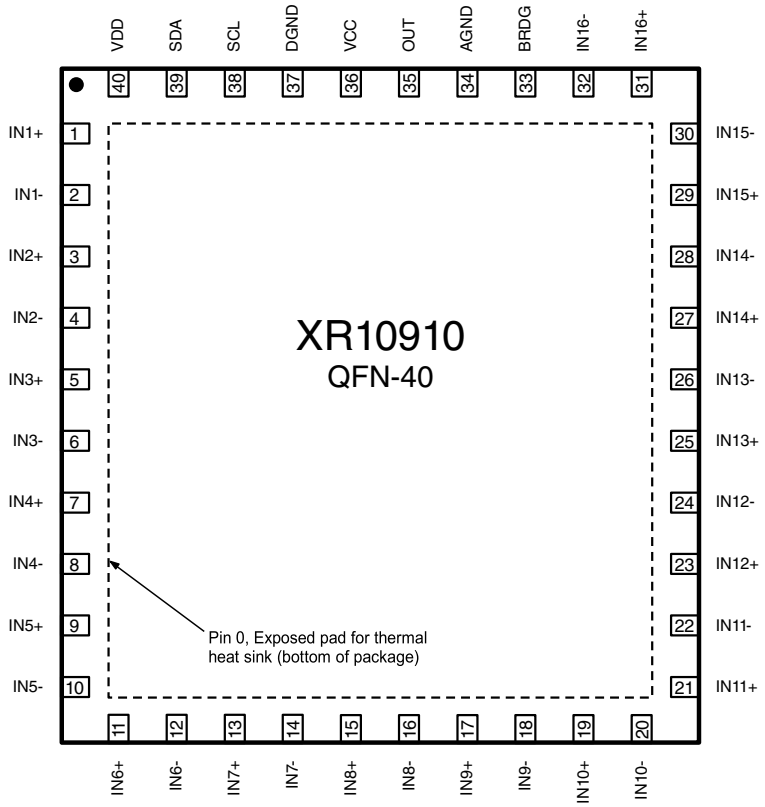
Table 2. DAC Registers

Hex	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Offset % of FS Input	Voltage RTI
0x3FF	0	1	1	1	1	1	1	1	1	1	1	50	+560mV
0x000	0	0	0	0	0	0	0	0	0	0	0	0	0
0x7FF	1	1	1	1	1	1	1	1	1	1	1	-50	-560mV
0x400	1	0	0	0	0	0	0	0	0	0	0	0	0
	DAC Sign	10-bit DAC Range											

Table 3: Gain Registers

Hex	D2	D1	D0	Gain
0x00	0	0	0	2
0x01	0	0	1	20
0x02	0	1	0	40
0x03	0	1	1	80
0x04	1	0	0	150
0x05	1	0	1	300
0x06	1	1	0	600
0x07	1	1	1	760

Pin Configuration



NOTE:

MaxLinear recommends grounding the exposed pad.

Pin Functions

Pin No.	Pin Name	Description
1	IN1+	Positive Input 1
2	IN1-	Negative Input 1
3	IN2+	Positive Input 2
4	IN2-	Negative Input 2
5	IN3+	Positive Input 3
6	IN3-	Negative Input 3
7	IN4+	Positive Input 4
8	IN4-	Negative Input 4
9	IN5+	Positive Input 5
10	IN5-	Negative Input 5
11	IN6+	Positive Input 6
12	IN6-	Negative Input 6
13	IN7+	Positive Input 7
14	IN7-	Negative Input 7
15	IN8+	Positive Input 8
16	IN8-	Negative Input 8
17	IN9+	Positive Input 9
18	IN9-	Negative Input 9
19	IN10+	Positive Input 10
20	IN10-	Negative Input 10

Pin No.	Pin Name	Description
21	IN11+	Positive Input 11
22	IN11-	Negative Input 11
23	IN12+	Positive Input 12
24	IN12-	Negative Input 12
25	IN13+	Positive Input 13
26	IN13-	Negative Input 13
27	IN14+	Positive Input 14
28	IN14-	Negative Input 14
29	IN15+	Positive Input 15
30	IN15-	Negative Input 15
31	IN16+	Positive Input 16
32	IN16-	Negative Input 16
33	BRDG	BRDG Power Connection (LDO output)
34	AGND	Analog Ground
35	OUT	Output
36	VCC	Analog Supply
37	DGND	Digital Ground
38	SCL	Serial Clock Input
39	SDA	Serial Data Input/Output
40	VDD	Digital Supply

Typical Performance Characteristics

T_A = 25°C, V_{CC} = 3.3V, V_{DD} = 1.8V, R_L = 10kΩ to 1.5V; G = 760; unless otherwise noted.

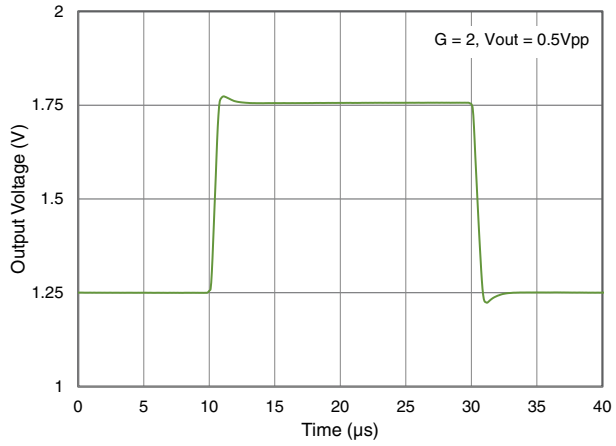


Figure 4. Small Signal Pulse Response at G = 2

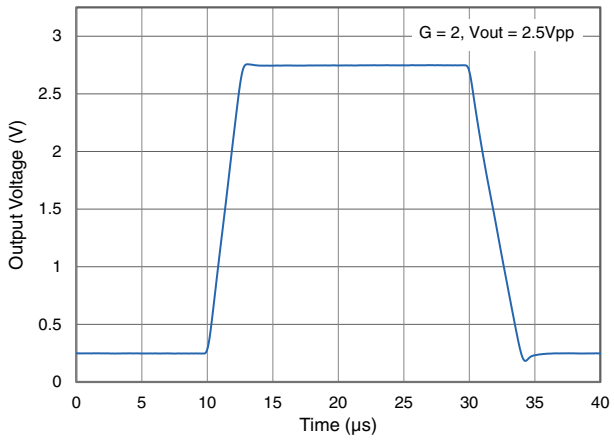


Figure 5. Large Signal Pulse Response at G = 2

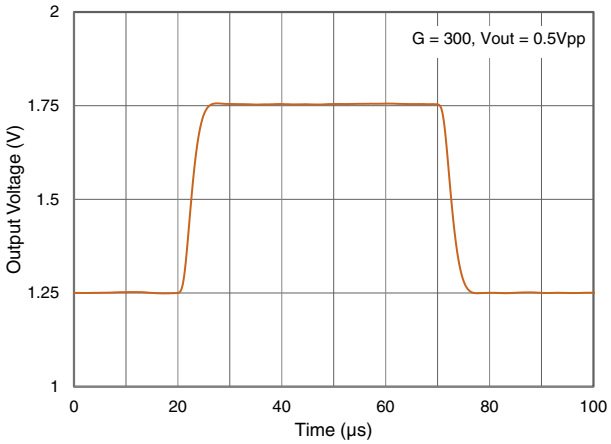


Figure 6. Small Signal Pulse Response at G = 300

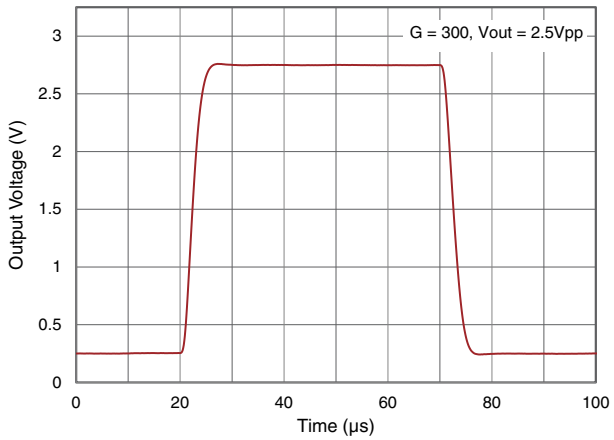


Figure 7. Large Signal Pulse Response at G = 300

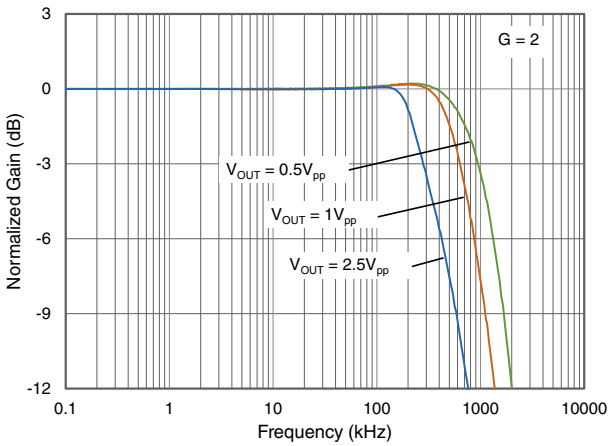


Figure 8. Frequency Response at G = 2

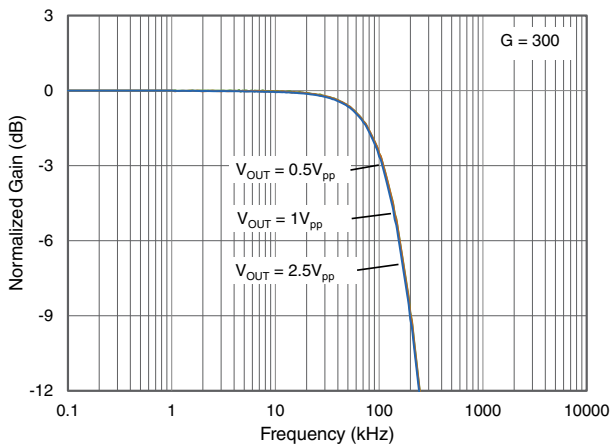


Figure 9. Frequency Response at G = 300

Typical Performance Characteristics

T_A = 25°C, V_{CC} = 3.3V, V_{DD} = 1.8V, R_L = 10kΩ to 1.5V; G = 760; unless otherwise noted.

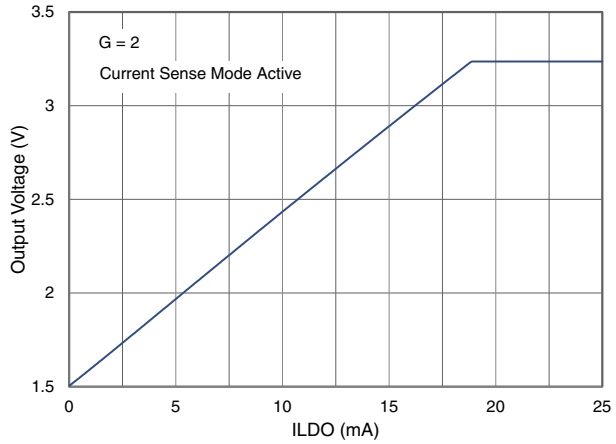


Figure 10. LDO Current vs. Output Voltage

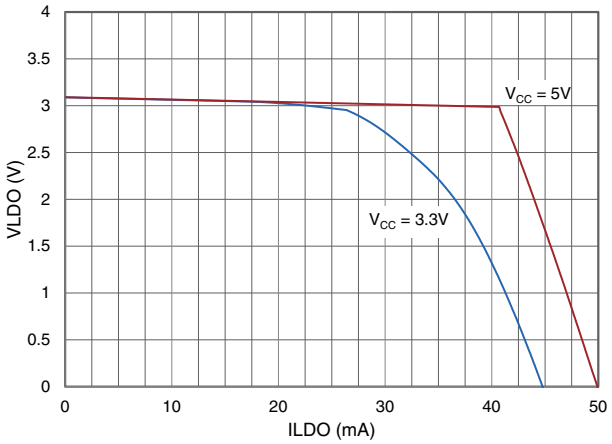


Figure 11. LDO Output Current

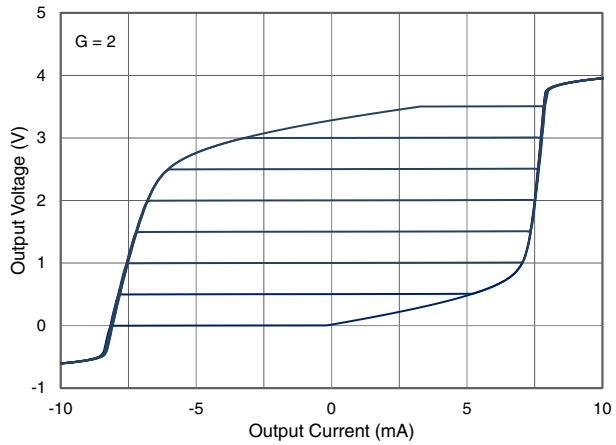


Figure 12. Output Offset Voltage vs. Output Current

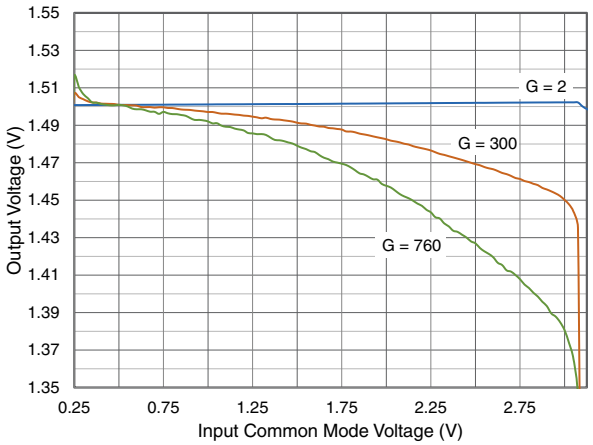


Figure 13. Output Offset vs. Input Common Mode Voltage

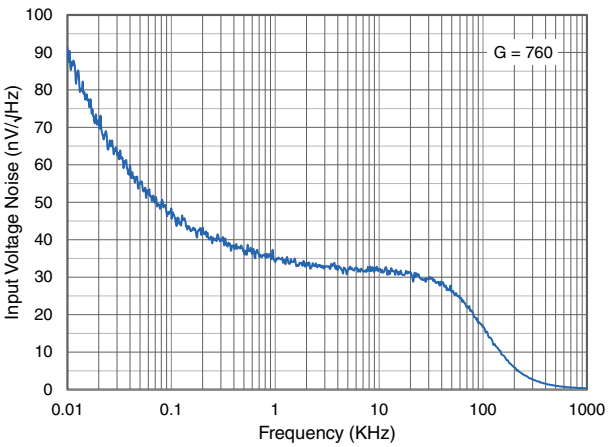


Figure 14. Input Voltage Noise vs. Frequency

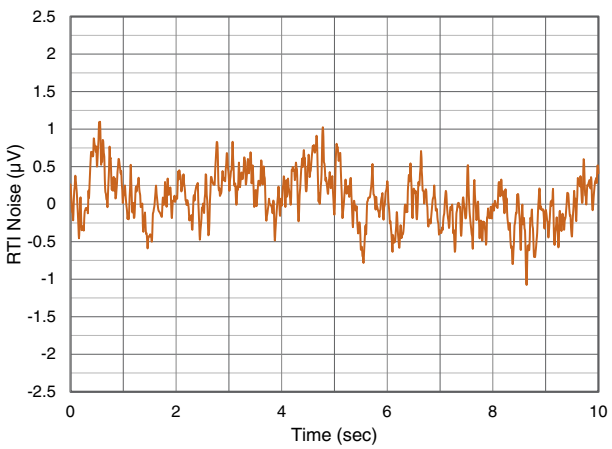


Figure 15. 0.1Hz to 10Hz RTI Voltage Noise

Typical Performance Characteristics

T_A = 25°C, V_{CC} = 3.3V, V_{DD} = 1.8V, R_L = 10kΩ to 1.5V; G = 760; unless otherwise noted.

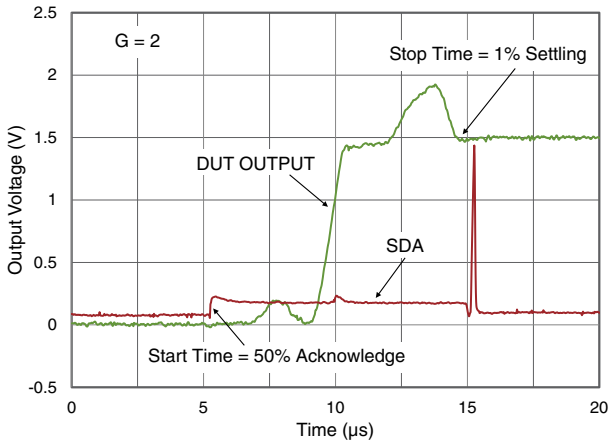


Figure 16. Sleep to Wake Time (DUT Output)

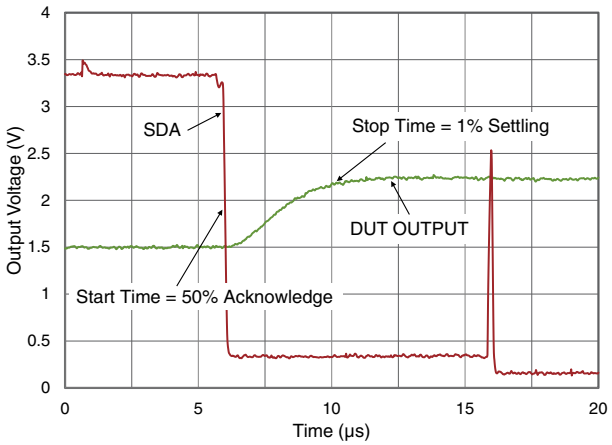


Figure 17. Set-up Time - from G = 2 to G = 300 (DUT Output)

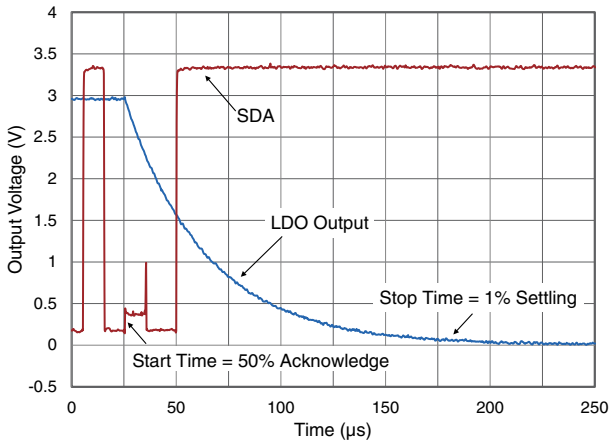


Figure 18. LDO Enable to Disable Time

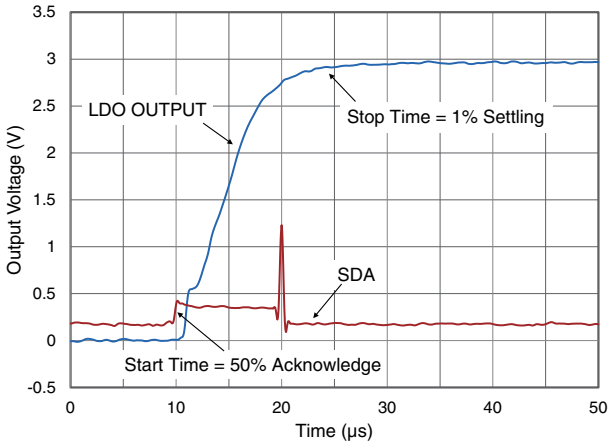


Figure 19. LDO Disable to Enable Time

Functional Block Diagram

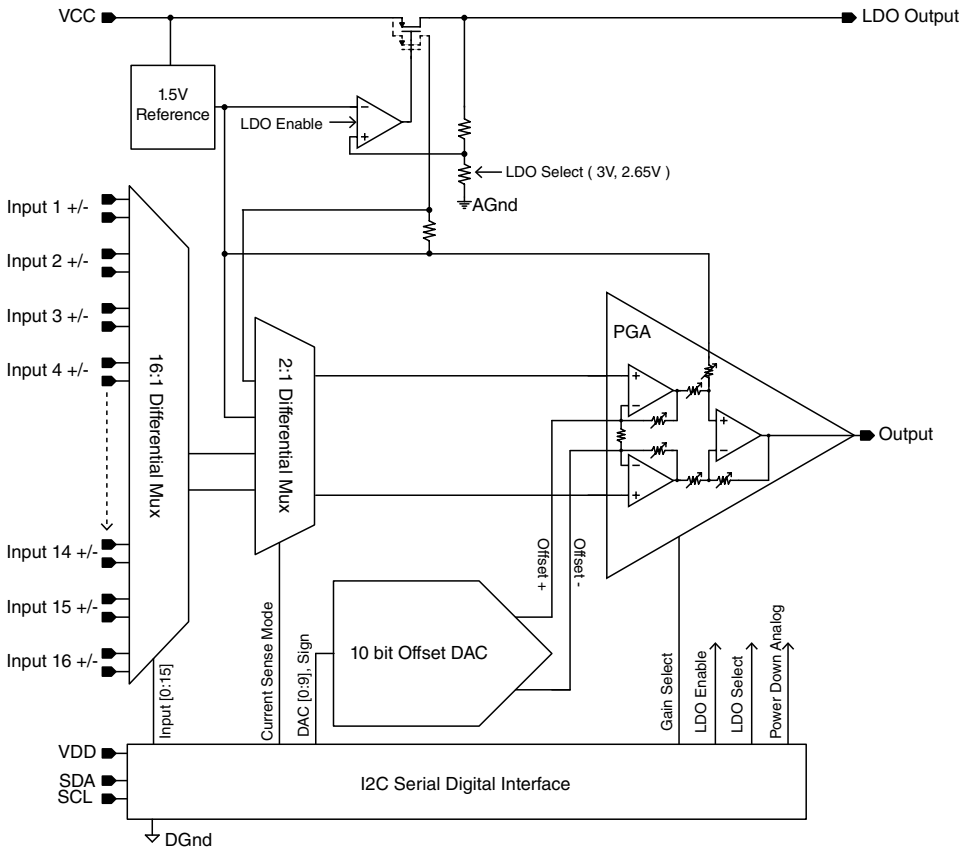


Figure 20: Functional Block Diagram

Application Information

The XR10910 sensor interface includes a 16:1 differential multiplexor (mux), a programmable gain instrumentation amplifier, a 10-bit offset correction DAC and an LDO. An I^2C interface controls the many functions and features of the XR10910. The XR10910 is designed to integrate multiple bridge sensors with an ADC/MCU or FPGA.

Each bridge sensor connected to the XR10910 has its own inherent offset that if not calibrated out can decrease sensitivity and overall performance of the sensor system. The on-board DAC introduces an offset into the instrumentation amplifier to calibrate the offset voltage generated by the sensors. An independent offset can be set for each of the 16 channels. Only the offset voltage of the active channel is applied to the PGA.

The programmable gain instrumentation amplifier offers 8 selectable gains from 2V/V to 760V/V to amplify the signal such that it falls within the input range of the ADC.

An integrated LDO provides a regulated voltage to power the input bridge sensors and is selectable, between 3V and 2.65V. The LDO can be set to turn off when the XR10910 is in Sleep Mode to save power.

The XR10910 also provides the ability to monitor the LDO current. When the XR10910 is in Current Sense Mode, an internal 2:1 mux allows a voltage proportional to the LDO current to be present at the output. Once all channels have been calibrated, the LDO current can be used to indirectly monitor any voltage or resistive changes seen by the inputs.

The XR10910 also includes an internal 1.5V reference that is used by the internal LDO circuitry and used to set the reference voltage for the programmable gain instrumentation amplifier.

During sleep mode, the analog components of the XR10910 are powered down for added power savings.

The XR10910 offers many functions, each controlled by the I^2C compatible serial interface:

- Input Selection
- Gain Selection
- Offset Correction
- LDO Enable / Select
- Current Sense Mode
- Sleep Mode (Analog Power Down)

Application Information (Continued)

Power Up

After initial system power up, the I²C master must provide one SCL clock pulse prior to the first I²C access (first start condition). The first access to the XR10910 must be a RESET command.

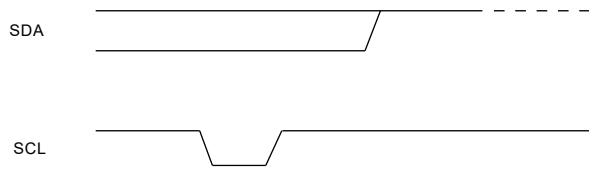


Figure 21: I²C Power Up

I²C Bus Interface

The I²C-bus interface consists of two lines: serial data (SDA) and serial clock (SCL). The XR10910 works as a slave and supports both standard mode transfer rates (100 kbps) and fast mode transfer rates (400 kbps) as defined in the I²C-Bus specification. The I²C-bus interface follows all standard I²C protocols. Some information is provided below, for additional information, refer to the I²C-bus specifications.

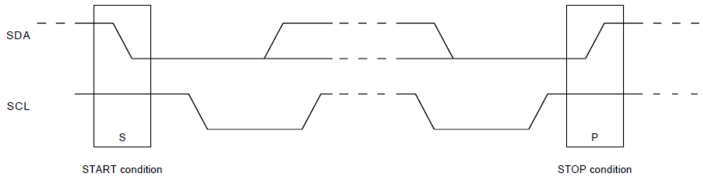


Figure 22: I²C Start and Stop Conditions

The basic I²C access cycle for the XR10910 consists of:

- A start condition
- A slave address cycle
- Zero, one, or two data cycles - depending on the XR10910 register accessed
- A stop condition

Start Condition

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 22.

Slave Address Cycle

After the start condition, the first byte sent by the master is the 7-bit address and the read/write direction bit R/W on the SDA line. If the address matches the XR10910's internal fixed address, the XR10910 will respond with an acknowledge by pulling the SDA line low for one clock cycle while SCL is high.

Data Cycle

After the master detects this acknowledge, the next byte transmitted by the master is the sub-address. This 8-bit sub-address contains the address of the register to access. The XR10910 Register List is shown in Table 1. Depending on the register accessed, there will be up to two additional data bytes transmitted by the master. Refer to the "Byte of Parameter" column in the Register Table. The XR10910 will respond to each write with an acknowledge.

Stop Condition

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high, as shown in Figure 22.

Figures 23 and 24 illustrate a write and a read cycle. For complete details, see the I²C-bus specifications.

NOTES:
White Block = host to XR10910, Red Block = XR10910 to host

Figure 23: Master Writes to Slave (XR10910)

NOTES:
White Block = host to XR10910, Red Block = XR10910 to host

Figure 24: Master Reads from Slave (XR10910)

I²C Bus Addressing

The XR10910 uses a 7-bit address space. For the standard XR10910, the default address is 0x67 (110 0111).

Table 4: XR10910 I²C Address Map

I²C Address	Orderable Part Number
0x67	XR10910IL40TR-F

A read or write transaction is determined by bit-0 of the slave address, (shown as an "**x**" in Table 4 above). If bit-0 is '0', then it is a write transaction. If bit-0 is '1', then it is a read transaction.

An I2C sub-address is sent by the I2C master following the slave address. The sub-address contains the XR10910 register address being accessed. Table 1 illustrates the available XR10910 register addresses.

After the last read or write transaction, the I2C-bus master will set the SCL signal back to its idle state (HIGH).

Application Information (Continued)

Inputs and Input Selection

The XR10910 includes 16 differential inputs and a 16:1 differential mux that is controlled by an I²C compatible 2 wire serial interface. The XR10910 is designed to accept 16 differential inputs.

- If fewer than 16 differential inputs are required, tie the unused inputs to GND.
- If single ended inputs are required, tie the unused inputs to 1.5V.

The input common mode range of the XR10910 is typically 0.6V to 2.4V when running from a 3.3V supply. The XR10910 offers a very wide gain range. In most cases, the output voltage swing will be the limiting factor.

When the XR10910 is powered-up, the default input selected is Channel 1.

Inputs are selected via I²C using one of 16 register addresses 0x10 thru 0x1F. Refer to the Register List in Table 1.

Example: The example below illustrates how to select Channel 5.

Step 1	0
Master sends start condition	S

Step 2	7	6	5	4	3	2	1	0
Master sends XR10910 address with write bit	1	1	0	0	1	1	1	0
	7-bit XR10910 Address = 0x67							W

Step 3	9
XR10910 sends acknowledge	A

Step 4	7	6	5	4	3	2	1	0
Master sends address of register to access	0	0	0	1	0	1	0	0
	Select_Input 5 register address = 0x14							

Step 5	9
XR10910 sends acknowledge	A

Step 6	0
Master sends stop condition	P

White Block = host to XR10910, Red Block = XR10910 to host

Grey Block = Notes

Gain Selection

The XR10910 offers 8 selectable fixed gains ranging from 2V/V to 760V/V. When the XR10910 is powered-up, the default gain is 2V/V.

The gain is selected via I²C using the register address 0x06 followed by another byte of data to select the gain. Refer to the Register List in Table 1 and the Gain Register list in Table 3.

Example: The example below illustrates how to select a gain of 150V/V.

To start communication with the XR10910, repeat steps 1-3 as shown in the Inputs and Input Selection section on page 16.

Step 4	7	6	5	4	3	2	1	0
Master sends address of register to access	0	0	0	0	0	1	1	0
	Gain Select register address = 0x06							

Step 5	9
XR10910 sends acknowledge	A

Since the Gain Select register was accessed, the XR10910 is expecting another byte of data from the master to complete the command. Refer to the “Byte of Parameter” column in the Register List (Table 1). D0 thru D2 are used to select the gain. Refer to the Gain Register list in Table 3, 150V/V is D2 = 1, D1 = 0, and D0 = 0. This translates to a hex code of 0x04, since a full byte of data (8-bits) will be sent.

Step 6	7	6	5	4	3	2	1	0
Master sends gain register data to select G=150	0	0	0	0	0	1	0	0
	Gain of 150V/V = 0x04							

Step 7	9
XR10910 sends acknowledge	A

Step 8	0
Master sends stop condition	P

White Block = host to XR10910, Red Block = XR10910 to host

Grey Block = Notes

Application Information (Continued)

Offset Correction

The XR10910 has a 10-bit offset correction DAC that can be used to provide digital calibration on each of the 16 inputs. Only the offset voltage of the active channel is applied to the PGA.

The DAC offset of each channel is controlled by the I^2C compatible interface. At any time, the master can read or write to any of the DAC offset registers. The DAC offset for each channel is set via I^2C using the register addresses 0x20 thru 0x2F followed by another two bytes of data to set the polarity and value of the offset voltage. Refer to the Register List in Table 1.

A ±560mV offset correction range is available. The full range of the DAC offset is only available at a gain of 2. At higher gains, the output voltage range of the XR10910 will be exceeded if the full range of the DAC offset is used. The internal 10-bit DAC allows 1,024 different offset voltage settings between 0mV and 560mV. The polarity of the offset correction is set with an additional bit. The unit offset is determined by the following:

$$\text{Unit offset} = \frac{\text{Total Offset}}{\text{DAC output levels}} = \frac{560\text{mV}}{1024} = 547\mu\text{V}$$

From Table 3:

- 0x00 (hex) or 0 00 0000 0000 (binary) applies a 0mV offset
- 0x3FF (hex) or 0 11 1111 1111 (binary) applies a +560mV offset
- 0x7FF (hex) or 1 11 1111 1111 (binary) applies a -560mV offset

Each DAC output level provides an additional 547µV of offset. To determine what DAC output level corresponds to a specific desired offset, use the following equation:

$$x = \frac{\text{Desired Offset}}{\text{Unit Offset}}$$

See example below for additional information.

Example: The example below illustrates how to set the DAC offset for channel 4 to a value of 75mV.

To start communication with the XR10910, repeat steps 1-3 as shown in the Inputs and Input Selection section on page 16.

Step 4	7	6	5	4	3	2	1	0
Master sends address of register to access	0	0	1	0	0	1	1	0
	DAC4 register address = 0x25							

Step 5	9
XR10910 sends acknowledge	A

Since a DAC Offset register was accessed, the XR10910 is expecting another two bytes of data from the master to complete the command. Refer to the “Byte of Parameter” column in the Register List (Table 1). D0 thru D9 are used to set the offset voltage and D10 is used to set the sign of the offset voltage, 0 = positive and 1 = negative. Refer to the DAC Offset register list in Table 2.

To determine what DAC output level corresponds to 75mV, use the following equation:

$$\text{DAC Output Level} = \frac{\text{Desired Offset}}{\text{Unit Offset}} = \frac{75\text{mV}}{547\mu\text{V}} = 137$$

A decimal value of 137 corresponds to 75mV. Therefore:

- 0x89 (hex) or 0 00 1000 1001 (binary) applies a +75mV offset
- 0x489 (hex) or 1 00 1000 1001 (binary) applies a -75mV offset

Step 6	15	14	13	12	11	10	9	8
Master sends 1st byte of DAC offset register data to select an offset of +75mV	0	0	0	0	0	0	0	0
						Sign	2 MSBs of 10-bit DAC output level that corresponds to 137 (0x89)	

Step 7	9
XR10910 sends acknowledge	A

Step 8	7	6	5	4	3	2	1	0
Master sends 2nd byte of DAC offset register data to select an offset of +75mV	1	0	0	0	1	0	0	1
	8 LSBs of 10-bit DAC output level that corresponds to 137 (0x89)							

Step 9	9
XR10910 sends acknowledge	A

Step 10	0
Master sends stop condition	P

White Block = host to XR10910, Red Block = XR10910 to host
Grey Block = Notes

Application Information (Continued)

LDO Enable / Select (Power to External Bridge Sensors)

The XR10910 includes an on-board LDO that provides a regulated voltage that can be used to power external input bridge sensors. Two voltage options are available, 3V and 2.65V. The LDO voltage is selected via the I²C compatible two-wire serial interface.

When the XR10910 is powered-up, the default LDO voltage is 3V.

When the XR10910 is active (not in sleep mode), the LDO is always on. If the LDO voltage is not used, the LDO output can be left floating. The LDO can either stay on or shut down while the XR10910 is in Sleep Mode.

- Set LDO to shut down while XR10910 is in Sleep Mode to save power
- Set LDO to stay on while XR10910 is in Sleep Mode to improve wake-up time

The LDO voltage and disable setting are selected via I²C using the register address 0x07 followed by another byte of data to select the voltage and disable setting. Refer to the Register List in Table 1 and the example below for more information.

Example: The example below illustrates how to select an LDO voltage of 2.65V and keep the LDO enabled during Sleep Mode.

To start communication with the XR10910, repeat steps 1-3 as shown in the Inputs and Input Selection section on page 11.

Step 4	7	6	5	4	3	2	1	0
Master sends address of register to access	0	0	0	0	0	1	1	1
	LDO Settings register address = 0x07							

Step 5	9
XR10910 sends acknowledge	A

Since the LDO Settings register was accessed, the XR10910 is expecting another byte of data from the master to complete the command. Refer to the “Byte of Parameter” column in the Register List (Table 1). D0 and D1 are used to select the LDO voltage and enable/disable the LDO during Sleep Mode. Bit 0 (D0) controls the LDO voltage (0: 3V; 1: 2.65V). Bit 1 (D1) is only applicable in Sleep Mode. Bit 1 controls whether the LDO shuts down or stays on during sleep mode (0: Enable; 1: Disable). When the XR0910 is active, the LDO is always on.

Step 6	7	6	5	4	3	2	1	0
Master sends code to select LDO voltage of 2.65V and Enable LDO during Sleep Mode	0	0	0	0	0	0	0	0
							0 = Enable	1 = 2.65V

Step 7	9
XR10910 sends acknowledge	A

Step 8	0
Master sends stop condition	P

White Block = host to XR10910, Red Block = XR10910 to host

Grey Block = Notes

Current Sense Mode (Monitoring the LDO Current)

Current Sense Mode is activated via I²C using the register address 0x08. When activated, the LDO current is sensed and a proportional voltage is present at the output of the XR10910 (ILDO = VOUT/RL). Current Sense Mode stays active until the XR10910 receives any input select command (0x10 thru 0x1F).

Current sense mode can be used to monitor the change over time of the bridge impedance.

Sleep Mode (Analog Power Down)

Sleep Mode is activated via I²C using the register address 0x05. When activated, the XR10910 will enter Sleep Mode. During Sleep Mode, the analog portion of the XR10910 is disabled. All register settings are retained during Sleep Mode.

During Sleep Mode, the nominal supply current will drop below 70µA (with LDO on) and below 45µA (with LDO off).

During Sleep Mode, the master can read the value in any register that saves a value during sleep mode. The only I²C commands that can be received or processed is the SLEEP_OUT (wake up) command (0x04) or the LDO on/off and voltage command (0x07). All other register addresses will be ignored.

Register address 0x04 is used to return to normal operation (exit Sleep Mode).

By default, the XR10910 is active.

Application Information (Continued)

Typical Application – 16:1 Bridge Sensor Interface

The XR10910 was designed to interface multiple bridge sensors with a microcontroller or FPGA as illustrated in Figure 25.

The bridge output signal is differential (Vo+ and Vo-). Ideally, the unloaded bridge output is zero (Vo+ and Vo- are identical). However, in-exact resistive values result in a difference between Vo+ and Vo-. This bridge offset voltage can be substantial and vary between sensors. The XR10910 provides the ability to calibrate the bridge offset on each of the 16 bridge sensors using the on-board DAC.

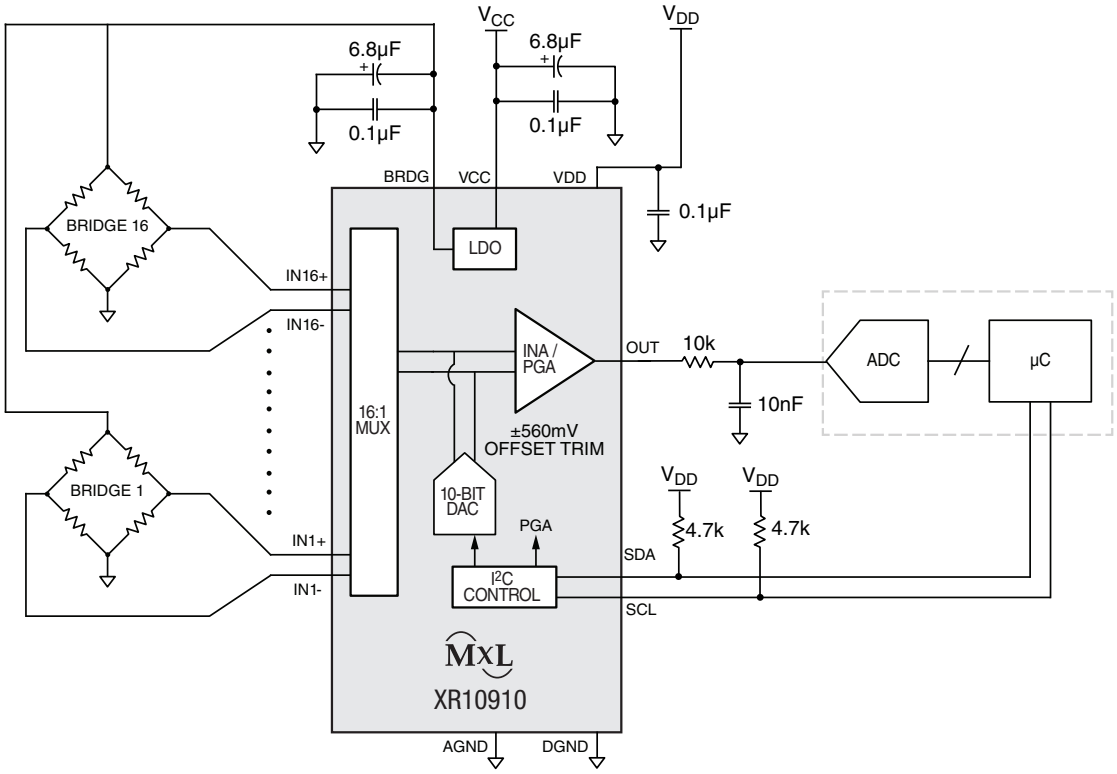


Figure 25: 16:1 Bridge Sensor Interface

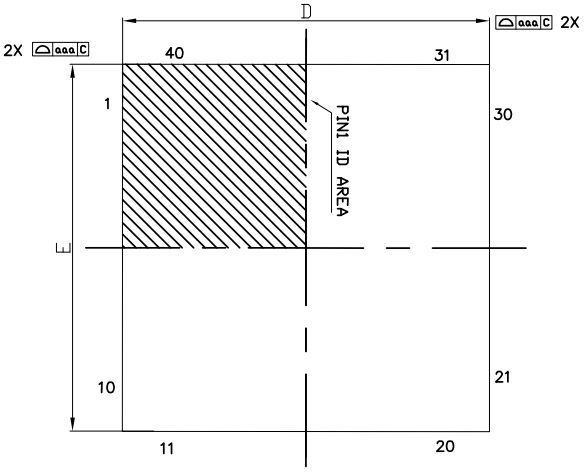
Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. Follow the steps below as a basis for high frequency layout:

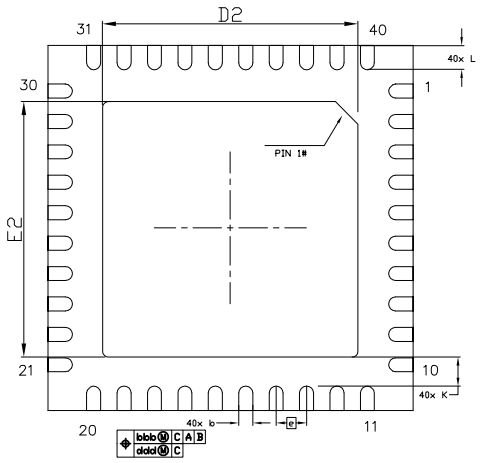
- Include 6.8µF and 0.1µF ceramic capacitors for power supply decoupling
- Place the 6.8µF capacitor within 0.75 inches of the power pin
- Place the 0.1µF capacitor within 0.1 inches of the power pin
- Connection to the exposed pad is not required. Exposed pad can be connected to ground (GND).
- Minimize all trace lengths to reduce series inductances

Mechanical Dimensions

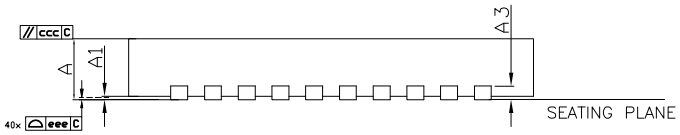
QFN-40 Package



TOP VIEW



BOTTOM VIEW



SIDE VIEW

DIMENSION TABLE				
SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	
A3	---	0.20Ref	---	
b	0.20	0.25	0.30	
D		6.00 BSC		
E		6.00 BSC		
e		0.50 BSC		
D2	4.50	4.65	4.80	
E2	4.50	4.65	4.80	
L	0.35	0.40	0.45	
K	0.20	–	–	
aaa		0.15		
bbb		0.10		
ccc		0.10		
ddd		0.05		
eee		0.08		
N		40		

TERMINAL DETAILS

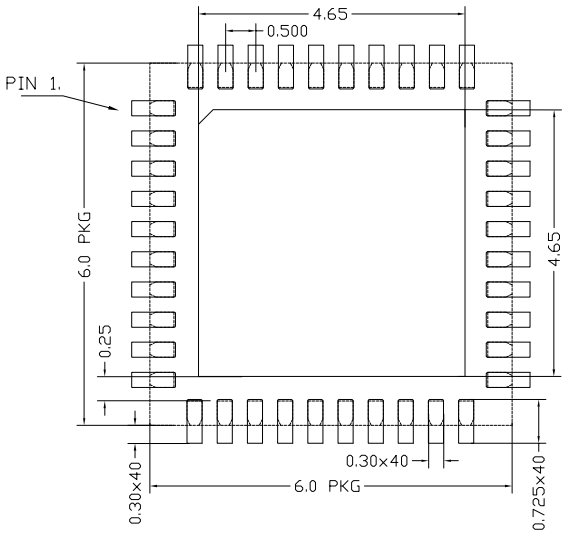
- ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.
- DIMENSIONS AND TOLERANCE PER JEDEC MO-220.

Drawing No.: POD-00000041

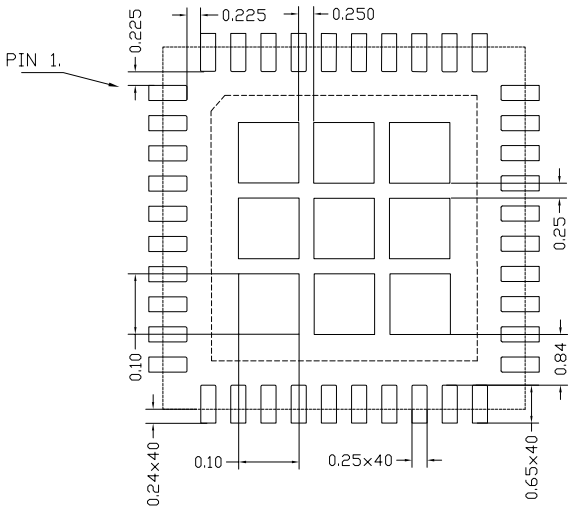
Revision: B.2

Recommended Land Pattern and Stencil

QFN-40 Package



TYPICAL RECOMMENDED LAND PATTERN



TYPICAL RECOMMENDED STENCIL

Drawing No.: POD-00000041

Revision: B.2

Ordering Information[1]

Part Number	Operating Temperature Range	Lead-Free	Package	Packaging Method
XR10910IL40-F	-40°C to +85°C	Yes[2]	QFN-40	Tray
XR10910IL40TR-F				Tape & Reel
XR10910IL40EVB	Evaluation Board			

NOTES:
1. Refer to www.exar.com/XR10910 for most up-to-date Ordering Information.
2. Visit www.exar.com for additional information on Environmental Rating.

Revision History

Part	Part	Part
1A	May 2015	Initial Release
1B	July 2015	Added Typical Performance Characteristics section.
1C	May 2016	Updated to latest format and added figure numbers. Updated Figures 1 and 25. Added Figure 2. Updated page number reference in Gain section of Electrical Characteristics table. Updated Figure 24. Added clarity to I^2C Bus Addressing section. Updated Table 4. Updated Step 2 in Inputs and Input Selection section.
1D	March 2018	Updated to MaxLinear logo. Updated format and Ordering information table. Added I^2C Power Up section.

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