

1. General description

Planar passivated high commutation three quadrant triac in a SOT404 plastic package. This "series E" triac balances the requirements of commutation performance and gate sensitivity. The "sensitive gate" "series E" is intended for interfacing with low power drivers including microcontrollers.

2. Features and benefits

- 3Q technology for improved noise immunity
- Direct interfacing with low power drivers and microcontrollers
- Good immunity to false turn-on by dV/dt
- High commutation capability with sensitive gate
- High voltage capability
- Planar passivated for voltage ruggedness and reliability
- Surface mountable package
- Triggering in three quadrants only

3. Applications

- Electronic thermostats (heating and cooling)
- High power motor controls e.g. washing machines and vacuum cleaners

4. Quick reference data

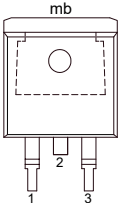
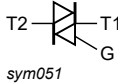
Table 1. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|--------------------------------------|--|-----|-----|-----|------|
| V_{DRM} | repetitive peak off-state voltage | | - | - | 600 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 101\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3 | - | - | 16 | A |
| I_{TSM} | non-repetitive peak on-state current | full sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5 | - | - | 140 | A |
| | | full sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 16.7\text{ ms}$ | - | - | 150 | A |
| T_j | junction temperature | | - | - | 125 | °C |
| Static characteristics | | | | | | |
| I_{GT} | gate trigger current | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ °C}$; Fig. 7 | - | - | 10 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ °C}$; Fig. 7 | - | - | 10 | mA |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|---------------------------------------|--|-----|-----|-----|------------------|
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7 | - | - | 10 | mA |
| I_H | holding current | $V_D = 12\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9 | - | - | 15 | mA |
| V_T | on-state voltage | $I_T = 18\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 10 | - | 1.3 | 1.5 | V |
| Dynamic characteristics | | | | | | |
| dV_D/dt | rate of rise of off-state voltage | $V_{DM} = 402\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit | 50 | - | - | V/ μs |
| dI_{com}/dt | rate of change of commutating current | $V_D = 400\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; $I_{T(RMS)} = 16\text{ A}$; $dV_{com}/dt = 20\text{ V}/\mu\text{s}$; (snubberless condition); gate open circuit | 3 | - | - | A/ms |
| | | $V_D = 400\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; $I_{T(RMS)} = 16\text{ A}$; $dV_{com}/dt = 10\text{ V}/\mu\text{s}$; gate open circuit | 6 | - | - | A/ms |
| | | $V_D = 400\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; $I_{T(RMS)} = 16\text{ A}$; $dV_{com}/dt = 1\text{ V}/\mu\text{s}$; gate open circuit | 10 | - | - | A/ms |

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|--------------------------------|--|---|
| 1 | T1 | main terminal 1 |  <p>D2PAK (SOT404)</p> |  <p>sym051</p> |
| 2 | T2 | main terminal 2 | | |
| 3 | G | gate | | |
| mb | T2 | mounting base; main terminal 2 | | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|--------------|---------|--|---------|
| | Name | Description | Version |
| BTA316B-600E | D2PAK | plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) | SOT404 |

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------------|--------------------------------------|--|-----|-----|------------------|
| V_{DRM} | repetitive peak off-state voltage | | - | 600 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 101\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3 | - | 16 | A |
| I_{TSM} | non-repetitive peak on-state current | full sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5 | - | 140 | A |
| | | full sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 16.7\text{ ms}$ | - | 150 | A |
| I^2t | I^2t for fusing | $t_p = 10\text{ ms}$; SIN | - | 98 | A ² s |
| di_T/dt | rate of rise of on-state current | $I_G = 20\text{ mA}$ | - | 100 | A/ μ s |
| I_{GM} | peak gate current | | - | 2 | A |
| P_{GM} | peak gate power | | - | 5 | W |
| $P_{G(AV)}$ | average gate power | over any 20 ms period | - | 0.5 | W |
| T_{stg} | storage temperature | | -40 | 150 | °C |
| T_j | junction temperature | | - | 125 | °C |



Fig. 1. RMS on-state current as a function of surge duration; maximum values



Fig. 2. RMS on-state current as a function of mounting base temperature; maximum values

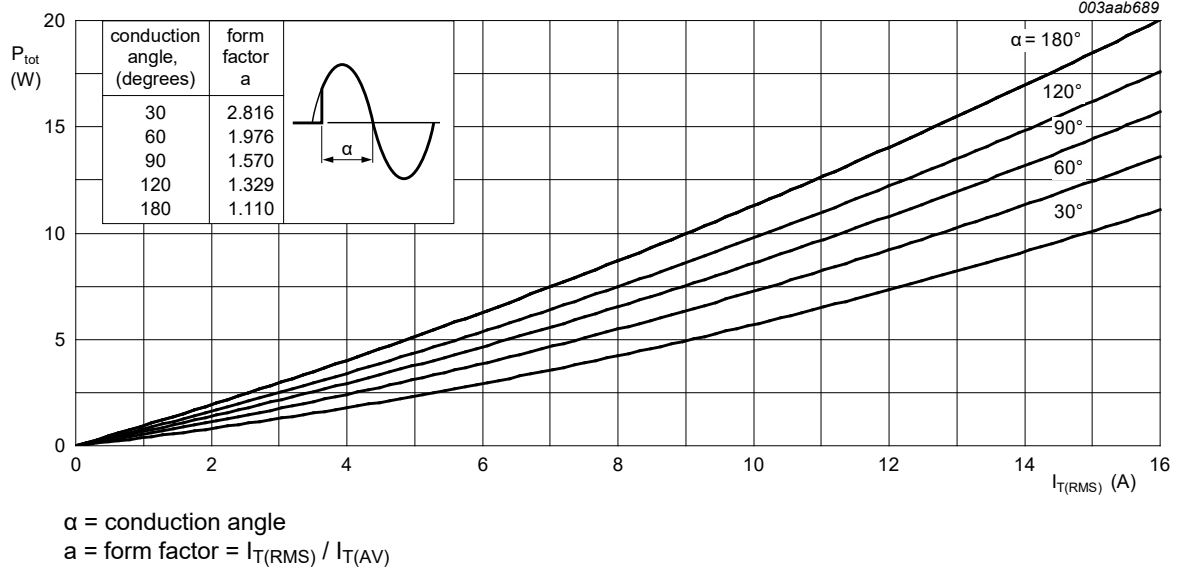


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

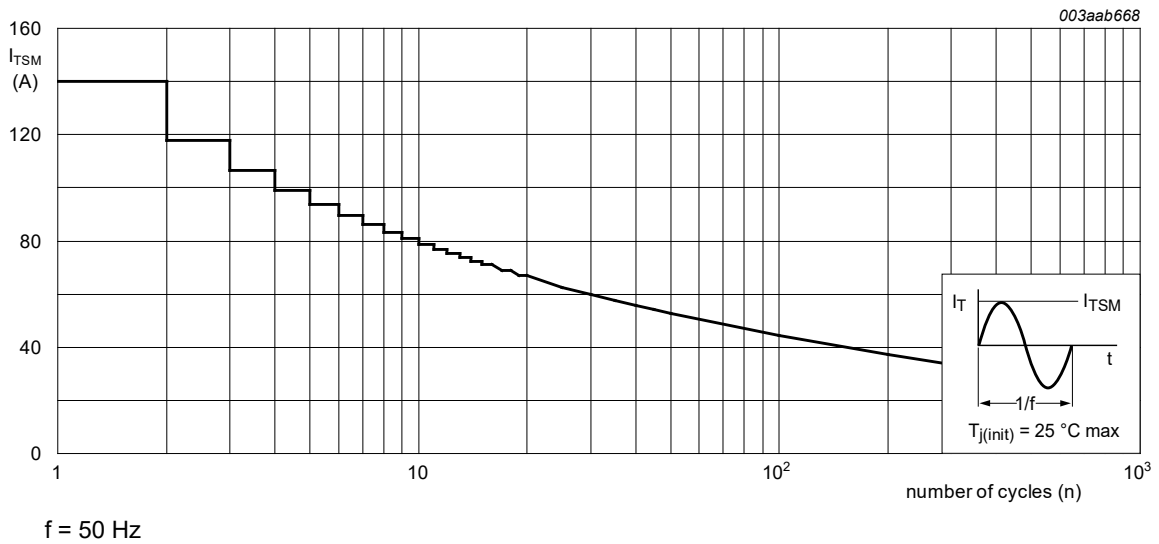


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



8. Thermal characteristics

Table 5. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------|--|--|-----|-----|-----|------|
| R _{th(j-mb)} | thermal resistance from junction to mounting base | full cycle; Fig. 6 | - | - | 1.2 | K/W |
| | | half cycle; Fig. 6 | - | - | 1.7 | K/W |
| R _{th(j-a)} | thermal resistance from junction to ambient free air | printed circuit board mounted; minimum footprint | - | 55 | - | K/W |



9. Characteristics

Table 6. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|---------------------------------------|--|------|-----|-----|------|
| Static characteristics | | | | | | |
| I _{GT} | gate trigger current | V _D = 12 V; I _T = 0.1 A; T2+ G+; T _j = 25 °C; Fig. 7 | - | - | 10 | mA |
| | | V _D = 12 V; I _T = 0.1 A; T2+ G-; T _j = 25 °C; Fig. 7 | - | - | 10 | mA |
| | | V _D = 12 V; I _T = 0.1 A; T2- G-; T _j = 25 °C; Fig. 7 | - | - | 10 | mA |
| I _L | latching current | V _D = 12 V; I _G = 0.1 A; T2+ G+; T _j = 25 °C; Fig. 8 | - | - | 25 | mA |
| | | V _D = 12 V; I _G = 0.1 A; T2+ G-; T _j = 25 °C; Fig. 8 | - | - | 30 | mA |
| | | V _D = 12 V; I _G = 0.1 A; T2- G-; T _j = 25 °C; Fig. 8 | - | - | 25 | mA |
| I _H | holding current | V _D = 12 V; T _j = 25 °C; Fig. 9 | - | - | 15 | mA |
| V _T | on-state voltage | I _T = 18 A; T _j = 25 °C; Fig. 10 | - | 1.3 | 1.5 | V |
| V _{GT} | gate trigger voltage | V _D = 12 V; I _T = 0.1 A; T _j = 25 °C; Fig. 11 | - | 0.8 | 1 | V |
| | | V _D = 400 V; I _T = 0.1 A; T _j = 125 °C; Fig. 11 | 0.25 | 0.4 | - | V |
| I _D | off-state current | V _D = 600 V; T _j = 125 °C | - | 0.1 | 0.5 | mA |
| Dynamic characteristics | | | | | | |
| dV _D /dt | rate of rise of off-state voltage | V _{DM} = 402 V; T _j = 125 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit | 50 | - | - | V/μs |
| dI _{com} /dt | rate of change of commutating current | V _D = 400 V; T _j = 125 °C; I _{T(RMS)} = 16 A; dV _{com} /dt = 20 V/μs; (snubberless condition); gate open circuit | 3 | - | - | A/ms |
| | | V _D = 400 V; T _j = 125 °C; I _{T(RMS)} = 16 A; dV _{com} /dt = 10 V/μs; gate open circuit | 6 | - | - | A/ms |
| | | V _D = 400 V; T _j = 125 °C; I _{T(RMS)} = 16 A; dV _{com} /dt = 1 V/μs; gate open circuit | 10 | - | - | A/ms |



Fig. 7. Normalized gate trigger current as a function of junction temperature



Fig. 8. Normalized latching current as a function of junction temperature

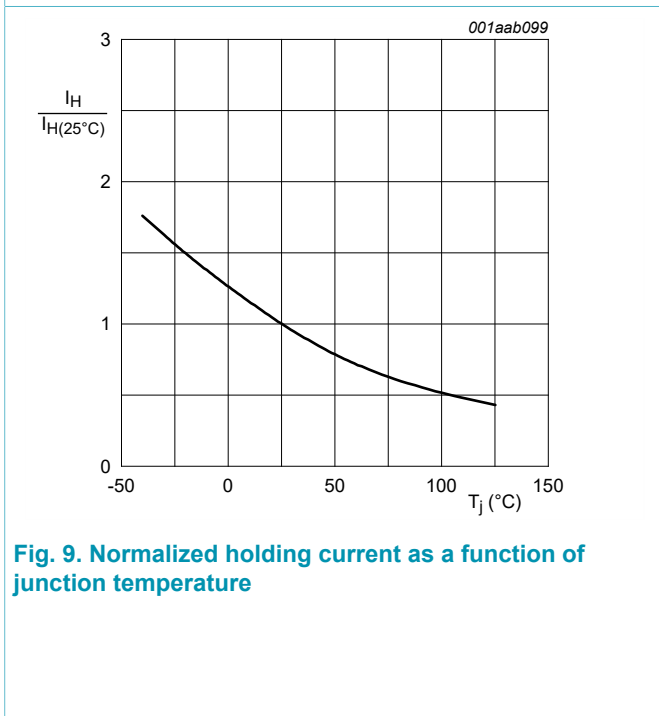


Fig. 9. Normalized holding current as a function of junction temperature

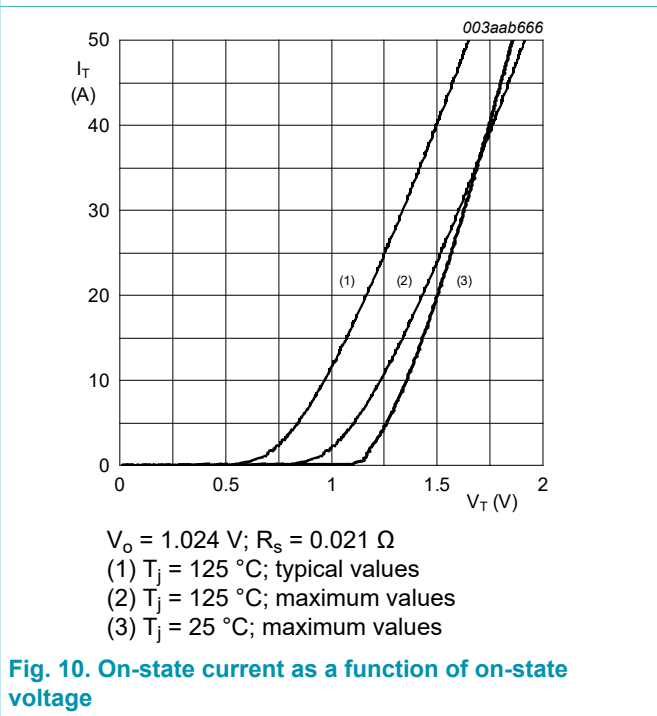


Fig. 10. On-state current as a function of on-state voltage



Fig. 11. Normalized gate trigger voltage as a function of junction temperature

10. Package outline



Fig. 12. Package outline D2PAK (SOT404)

11. Legal information

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|--------------------------------|--------------------|---|
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