

74LVC16240A

16-bit buffer/line driver with 5V tolerant inputs/outputs;
inverting; 3-state

Rev. 5 — 25 April 2019

Product data sheet

1. General description

The 74LVC16240A is a 16-bit inverting buffer/line driver with 3-state outputs. The device can be used as four 4-bit buffers, two 8-bit buffers or one 16-bit buffer. The device features four output enables ($1\bar{OE}$, $2\bar{OE}$, $3\bar{OE}$ and $4\bar{OE}$), each controlling four of the 3-state outputs. A HIGH on $n\bar{OE}$ causes the outputs to assume a high-impedance OFF-state.

Inputs can be driven from either 3.3 V or 5 V devices. When disabled, up to 5.5 V can be applied to the outputs. These features allow the use of these devices in mixed 3.3 V and 5 V applications.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. Features and benefits

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- MULTIBYTE flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Complies with JEDEC standard:
 - JESD8-7A (1.65 V to 1.95 V)
 - JESD8-5A (2.3 V to 2.7 V)
 - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115B exceeds 200 V
 - CDM JESD22-C101E exceeds 1000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C.

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC16240ADGG	-40 °C to +125 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1

4. Functional diagram

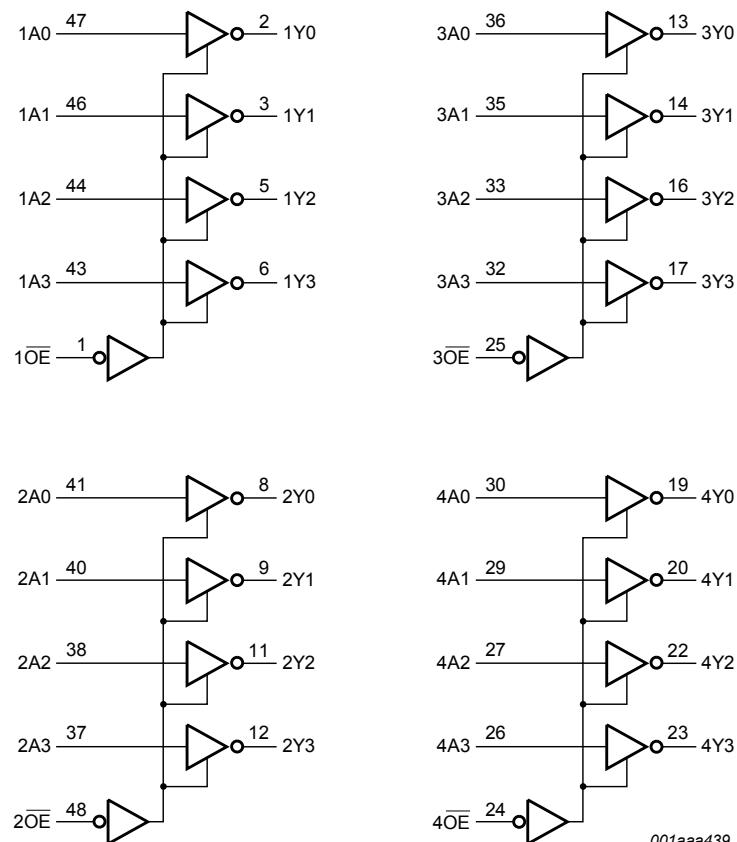


Fig. 1. Logic symbol

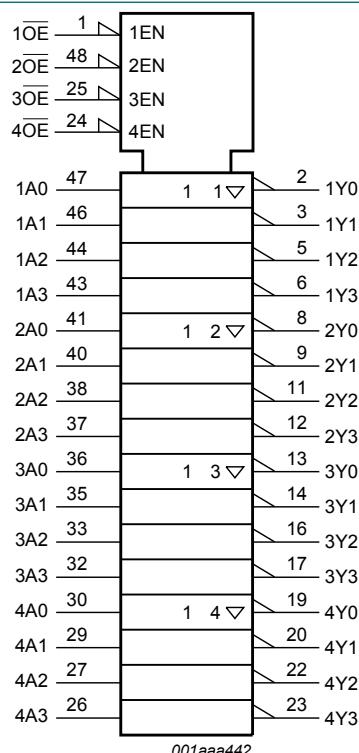


Fig. 2. IEC logic symbol

5. Pinning information

5.1. Pinning

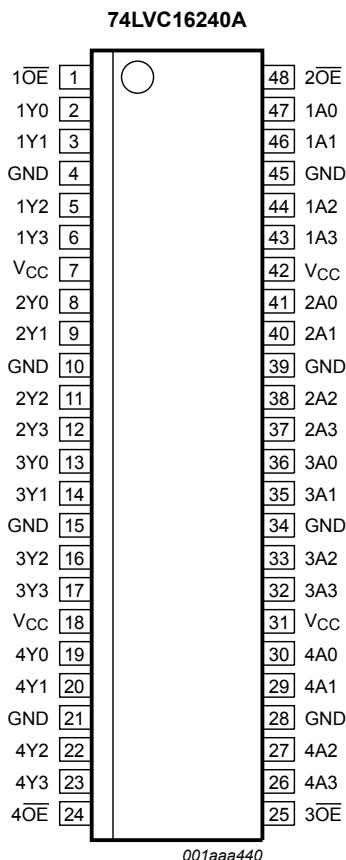


Fig. 3. Pin configuration SOT362-1 (TSSOP48)

5.2. Pin description

Table 2. Pin description

Name	Pin	Description
1 \overline{OE} , 2 \overline{OE} , 3 \overline{OE} , 4 \overline{OE}	1, 48, 25, 24	output enable input (active LOW)
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V _{CC}	7, 18, 31, 42	supply voltage
1Y ₀ , 1Y ₁ , 1Y ₂ , 1Y ₃	2, 3, 5, 6	data output
2Y ₀ , 2Y ₁ , 2Y ₂ , 2Y ₃	8, 9, 11, 12	data output
3Y ₀ , 3Y ₁ , 3Y ₂ , 3Y ₃	13, 14, 16, 17	data output
4Y ₀ , 4Y ₁ , 4Y ₂ , 4Y ₃	19, 20, 22, 23	data output
1A ₀ , 1A ₁ , 1A ₂ , 1A ₃	47, 46, 44, 43	data input
2A ₀ , 2A ₁ , 2A ₂ , 2A ₃	41, 40, 38, 37	data input
3A ₀ , 3A ₁ , 3A ₂ , 3A ₃	36, 35, 33, 32	data input
4A ₀ , 4A ₁ , 4A ₂ , 4A ₃	30, 29, 27, 26	data input

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state

Input	Output		
nOE	nAn	nYn	
L	L	H	
L	H	L	
H	X	Z	

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
V _I	input voltage		[1]	-0.5	+6.5
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0 V	-	±50	mA
		output HIGH or LOW state	[2]	-0.5	V _{CC} + 0.5
V _O	output voltage	output 3-state	[2]	-0.5	+6.5
		V _O = 0 V to V _{CC}	-	±50	mA
I _O	output current		-	100	mA
I _{CC}	supply current		-100	-	mA
I _{GND}	ground current		-65	+150	°C
T _{stg}	storage temperature				
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	[3]	-	500
					mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] Above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V _I	input voltage		0	-	5.5	V
V _O	output voltage	output HIGH or LOW state	0	-	V _{CC}	V
		output 3-state	0	-	5.5	V
T _{amb}	ambient temperature	in free air	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.65 V to 2.7 V	-	-	20	ns/V
		V _{CC} = 2.7 V to 3.6 V	-	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	1.08	-	-	1.08	-	V
		V _{CC} = 1.65 V to 1.95 V	0.65V _{CC}	-	-	0.65V _{CC}	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	0.12	-	0.12	V
		V _{CC} = 1.65 V to 1.95 V	-	-	0.35V _{CC}	-	0.35V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = -100 µA; V _{CC} = 1.65 V to 3.6 V	V _{CC} - 0.2	-	-	V _{CC} - 0.3	-	V
		I _O = -4 mA; V _{CC} = 1.65 V	1.2	-	-	1.05	-	V
		I _O = -8 mA; V _{CC} = 2.3 V	1.8	-	-	1.65	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	2.2	-	-	2.05	-	V
		I _O = -18 mA; V _{CC} = 3.0 V	2.4	-	-	2.25	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	2.2	-	-	2.0	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 100 µA; V _{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	-	0.65	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.6	-	0.8	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	-	0.8	V
I _I	input leakage current	V _{CC} = 3.6 V; V _I = 5.5 V or GND	-	±0.1	±5	-	±20	µA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _{CC} = 3.6 V; V _O = 5.5 V or GND	-	0.1	±5	-	±20	µA
I _{OFF}	power-off leakage current	V _{CC} = 0 V; V _I or V _O = 5.5 V	-	0.1	±10	-	±20	µA
I _{CC}	supply current	V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A	-	0.1	20	-	80	µA
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 2.7 V to 3.6 V; V _I = V _{CC} - 0.6 V; I _O = 0 A	-	5	500	-	5000	µA
C _I	input capacitance	V _{CC} = 0 V to 3.6 V; V _I = GND to V _{CC}	-	5.0	-	-	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see [Fig. 6](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t_{pd}	propagation delay	nAn to nYn; see Fig. 4 [2]						
		$V_{CC} = 1.2 \text{ V}$	-	12.0	-	-	-	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	1.0	5.1	11.0	1.0	11.7	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0.5	2.7	5.5	0.5	6.1	ns
		$V_{CC} = 2.7 \text{ V}$	1.0	2.7	5.2	1.0	6.5	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.0	2.3	4.2	1.0	5.5	ns
t_{en}	enable time	n $\bar{O}E$ to nYn; see Fig. 5 [2]						
		$V_{CC} = 1.2 \text{ V}$	-	18.0	-	-	-	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	1.5	6.6	12.8	1.5	13.5	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.0	3.8	6.8	1.0	7.5	ns
		$V_{CC} = 2.7 \text{ V}$	1.5	3.5	5.8	1.5	7.5	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.0	3.0	5.0	1.0	6.5	ns
t_{dis}	disable time	n $\bar{O}E$ to nYn; see Fig. 5 [2]						
		$V_{CC} = 1.2 \text{ V}$	-	11.0	-	-	-	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	2.9	4.7	9.2	2.9	9.7	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.0	2.6	5.0	1.0	5.6	ns
		$V_{CC} = 2.7 \text{ V}$	1.5	3.5	5.1	1.5	6.5	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.5	3.2	4.9	1.5	6.5	ns
$t_{sk(o)}$	output skew time	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$ [3]	-	-	1.0	-	1.5	ns
C_{PD}	power dissipation capacitance	per input; $V_I = \text{GND to } V_{CC}$ [4]						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	-	4.8	-	-	-	pF
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	-	8.3	-	-	-	pF
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	-	11.4	-	-	-	pF

[1] Typical values are measured at $T_{amb} = 25 \text{ }^{\circ}\text{C}$ and $V_{CC} = 1.2 \text{ V}, 1.8 \text{ V}, 2.5 \text{ V}, 2.7 \text{ V}$, and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

t_{en} is the same as t_{PZL} and t_{PZH} .

t_{dis} is the same as t_{PLZ} and t_{PHZ} .

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; f_o = output frequency in MHz

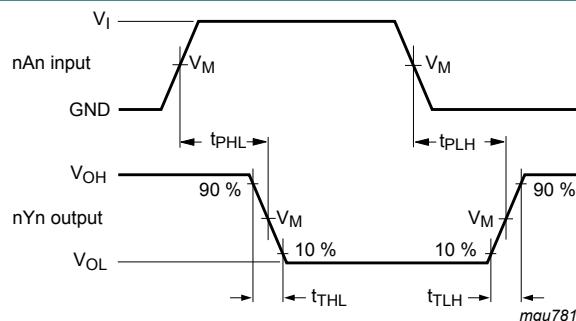
C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs

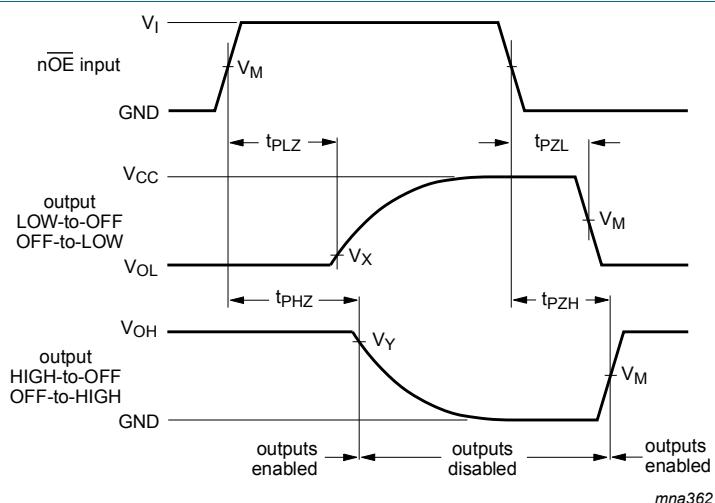
10.1. Waveforms and test circuit



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 4. The input nAn to output nYn propagation delays



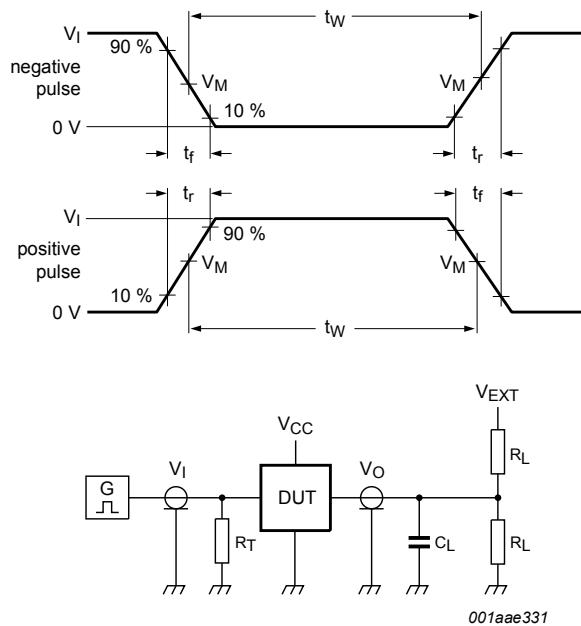
Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 5. 3-state enable and disable times

Table 8. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
1.2 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.1 \text{ V}$	$V_{OH} - 0.1 \text{ V}$
1.65 V to 1.95 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.1 \text{ V}$	$V_{OH} - 0.1 \text{ V}$
2.3 V to 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.1 \text{ V}$	$V_{OH} - 0.1 \text{ V}$
2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
3.0 V to 3.6 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$



Test data is given in [Table 9](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_0 of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig. 6. Test circuit for measuring switching times

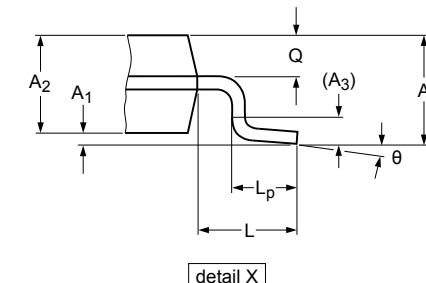
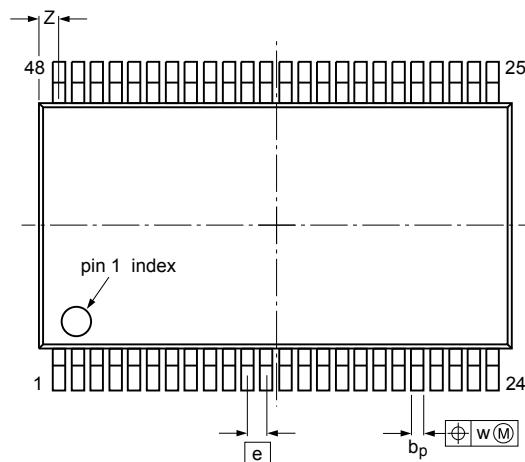
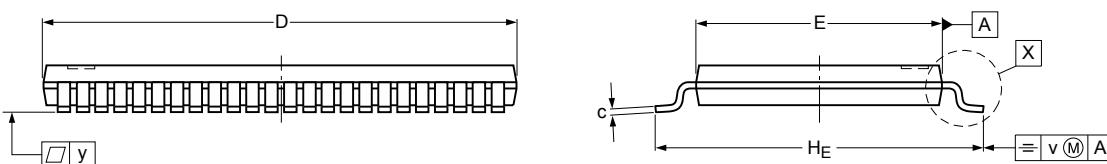
Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.2 V	V_{CC}	≤ 2 ns	30 pF	1 k Ω	open	$2 \times V_{CC}$	GND
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 k Ω	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND

11. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1



0 2.5 5 mm
scale

Dimensions (mm are the original dimensions)

Unit	A	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z	θ
mm	max	0.15	1.05		0.28	0.2	12.6	6.2		8.3		0.8	0.50			0.8	8°	
mm	nom	1.2		0.25					0.5		1		0.25	0.08	0.1		0.4	0°
mm	min	0.05	0.85		0.17	0.1	12.4	6.0		7.9		0.4	0.35					

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot362-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				03-02-19 13-08-05

Fig. 7. Package outline SOT362-1 (TSSOP48)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC16240A v.5	20190425	Product data sheet	-	74LVC16240A v.4
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type number 74LVC16240ADL (SOT370-1) removed. Package outline drawing SOT362-1 (TSSOP48) updated. Typo corrected in Section 5.2. 			
74LVC16240A v.4	20111103	Product data sheet	-	74LVC16240A v.3
Modifications:	<ul style="list-style-type: none"> The format of this document has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Table 4, Table 5, Table 6, Table 7, and Table 9: values added for lower voltage ranges. 			
74LVC16240A v.3	20040305	Product specification	-	74LVC16240A v.2
74LVC16240A v.2	19970729	Product specification	-	74LVC16240A v.1
74LVC16240A v.1	19951226	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Contents

1. General description.....	1
2. Features and benefits.....	1
3. Ordering information.....	1
4. Functional diagram.....	2
5. Pinning information.....	3
5.1. Pinning.....	3
5.2. Pin description.....	3
6. Functional description.....	4
7. Limiting values.....	4
8. Recommended operating conditions.....	4
9. Static characteristics.....	5
10. Dynamic characteristics.....	6
10.1. Waveforms and test circuit.....	7
11. Package outline.....	9
12. Abbreviations.....	10
13. Revision history.....	10
14. Legal information.....	11

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Date of release: 25 April 2019

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