features

- **Multi-Rate Operation from 155 Mbps Up to 3.3 Gbps**
- **106-mW Power Consumption**
- **Input Offset Cancellation**
- **High Input Dynamic Range**
- **Output Disable**
- **Output Polarity Select**
- **CML Data Outputs**
- **Receive Signals Strength Indicator (RSSI)**
- **Loss of Signal Detection**
- **Single 3.3-V Supply**
- **Surface Mount Small Footprint 3 mm × 3 mm 16-Pin QFN Package**

applications

- **SONET/SDH Transmission Systems at OC3, OC12, OC24, OC48**
- **1.0625-Gbps and 2.125-Gbps Fibre Channel Receivers**
- **Gigabit Ethernet Receivers**

description

The ONET3301PA is a versatile high-speed limiting amplifier for multiple fiber optic applications with data rates up to 3.3 Gbps.

This device provides a gain of about 50 dB, which ensures a fully differential output swing for input signals as low as 3 mV_{p-p}.

The high input signal dynamic range ensures low jitter output signals even when overdriven with input signal swings as high as 1200 mV_{p-p}.

The ONET3301PA comprises a loss of signals detection, as well as a received signal strength indicator.

The ONET3301PA is available in a small footprint 3 mm × 3 mm 16-pin QFN package and requires a single 3.3-V supply.

This power efficient limiting amplifier dissipates less than 106 mW typical. It is characterized for operation from –40°C to 85°C.

available options

T_A	PACKAGED DEVICE	FEATURES
−40°C to 85°C	ONET3301PARGT	16-pin 3 mm x 3 mm QFN, tube
−40°C to 85°C	ONET3301PARGTR	16-pin 3 mm x 3 mm QFN, tape and reel



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2004, Texas Instruments Incorporated

block diagram

A simplified block diagram of the ONET3301PA is shown in Figure 1.

This compact, low power 3.3-Gbps limiting amplifier consists of a high-speed data path with offset cancellation block, a loss of signal and RSSI detection block, and a bandgap voltage reference and bias current generation block.

The limiting amplifier requires a single 3.3-V supply voltage. All circuit parts are described in detail below.

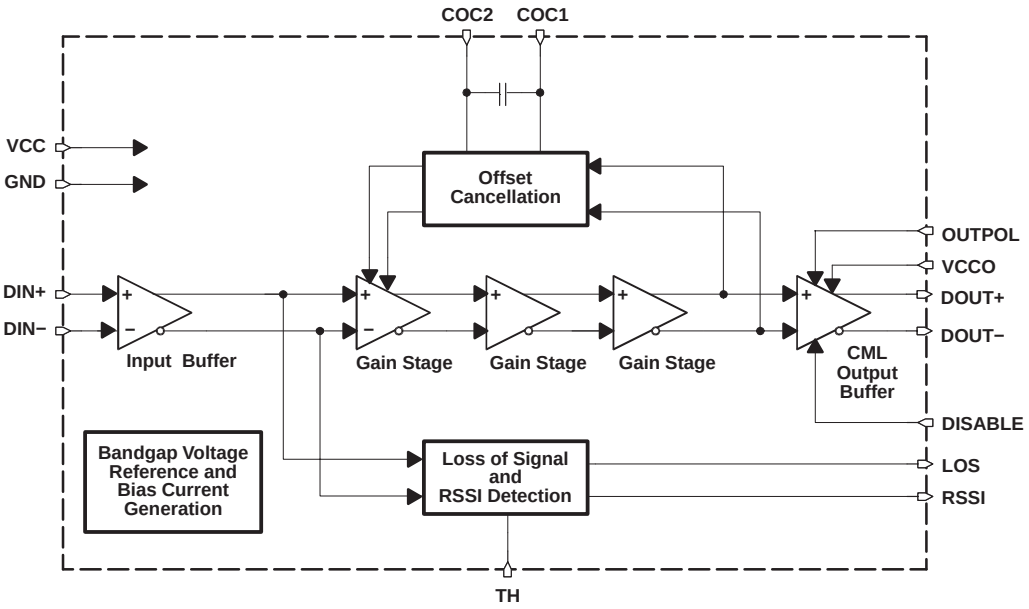


Figure 1. Block Diagram

high-speed data path

The high-speed data signal is applied to the data path by means of the input signal pins DIN+/DIN–. The data path consists of the input stage with $2 \times 50\text{-}\Omega$ on-chip line termination to VCC, three gain stages, which provide the required typical gain of about 50 dB and a CML output stage. The amplified data output signal is available at the output pins DOUT+/DOUT–, which provide $2 \times 50\text{-}\Omega$ back-termination to VCCO. The output stage also includes a data polarity switching function, which is controlled by the OUTPOL input and a disable function, controlled by the signal applied to the DISABLE input pin.

An offset cancellation compensates inevitable internal offset voltages and thus ensures proper operation even for small input data signals.

The low frequency cutoff is as low as 45 kHz with the built-in filter capacitor.

For applications, which require even lower cutoff frequencies, an additional external filter capacitor may be connected to the COC1/COC2 pins.

loss of signal and RSSI detection

The output signal of the input buffer is monitored by the loss of signal and RSSI detection circuitry. In this block a signal is generated, which is linear proportional to the input amplitude over a wide input voltage range. This signal is available at the RSSI output pin.

Furthermore, this circuit block compares the input signal to a threshold, which can be programmed by means of an external resistor connected to the TH pin. If the input signal falls below the specified threshold, a loss of signal is indicated at the LOS pin.

bandgap voltage and bias generation

The ONET3301PA limiting amplifier is supplied by a single 3.3-V ±10% supply voltage connected to the VCC and VCCO pins. This voltage is referred to ground (GND).

An on-chip bandgap voltage circuitry generates a supply voltage independent reference from which all other internally required voltages and bias currents are derived.

package

For the ONET3301PA, a small footprint 3 mm × 3 mm 16-pin QFN package is used with a lead pitch of 0,5 mm. The pin out is shown in Figure 2.

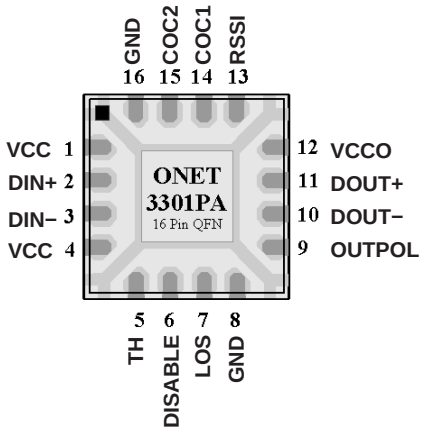


Figure 2. Pinout of ONET3301PA in a 3 mm × 3 mm 16-Pin QFN Package

terminal functions

The following table shows a pin description for the ONET3301PA in a 3 mm x 3 mm 16-pin QFN package.

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
VCC	1, 4	Supply	3.3-V ±10% supply voltage
DIN+	2	Analog in	Noninverted data input. On-chip 50-Ω terminated to VCC
DIN–	3	Analog in	Inverted data input. On-chip 50-Ω terminated to VCC
TH	5	Analog in	LOS threshold adjustment with resistor to GND.
DISABLE	6	CMOS in	Disables CML output stage when set to high level.
LOS	7	CMOS out	High level indicates that the input signal amplitude is below the programmed threshold level.
GND	8, 16, EP	Supply	Circuit ground. Exposed die pad (EP) must be grounded.
OUTPOL	9	CMOS in	Output data signal polarity select (internally pulled up): Setting to high level or leaving pin open selects normal polarity. Low level selects inverted polarity.
DOUT–	10	CML out	Inverted data output. On-chip 50-Ω back-terminated to VCCO
DOUT+	11	CML out	Noninverted data output. On-chip 50-Ω back-terminated to VCCO
VCCO	12	Supply	3.3-V ±10% supply voltage for output stage
RSSI	13	Analog out	Analog output voltage proportional to the input data amplitude. Indicates the strength of the received signal (RSSI).
COC1	14	Analog	Offset cancellation filter capacitor terminal 1. Connect an additional filter capacitor between this pin and COC2 (pin 15). To disable the offset cancellation loop connect COC1 and COC2 (pins 14 and 15).
COC2	15	Analog	Offset cancellation filter capacitor terminal 2. Connect an additional filter capacitor between this pin and COC1 (pin 14). To disable the offset cancellation loop connect COC1 and COC2 (pins 14 and 15).

absolute maximum ratings

over operating free-air temperature range unless otherwise noted†

		VALUE	UNIT
V_{CC}, V_{CCO}	Supply voltage, See Note 1	–0.3 to 4	V
V_{DIN+}, $V_{DIN–}$	Voltage at DIN+, DIN–, See Note 1	0.5 to 4	V
V_{TH}, $V_{DISABLE}$, V_{LOS}, V_{OUTPOL}, V_{DOUT+}, $V_{DOUT–}$, V_{RSSI}, V_{COC1}, V_{COC2}	Voltage at TH, DISABLE, LOS, OUTPOL, DOUT+, DOUT–, RSSI, COC1, and COC2, See Note 1	–0.3 to 4	V
V_{COC_DIFF}	Differential voltage between COC1 and COC2	±1	V
V_{DIN_DIFF}	Differential voltage between DIN+ and DIN–	±2.5	V
I_{LOS}	Current into LOS	–1 to 9	mA
I_{DIN+}, $I_{DIN–}$, I_{DOUT+}, $I_{DOUT–}$	Continuous current at inputs and outputs	–25 to 25	mA
ESD	ESD rating at all pins except VCCO	3	kV (HBM)
	ESD rating at VCCO	1.1	
$T_{J(max)}$	Maximum junction temperature	125	°C
T_{stg}	Storage temperature range	−65 to 85	°C
T_A	Characterized free-air operating temperature range	−40 to 85	°C
T_L	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260	°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

	MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}, V_{CCO}	3	3.3	3.6	V
Operating free-air temperature, T_A	−40		85	°C

dc electrical characteristics

over recommended operating conditions (unless otherwise noted), typical operating condition is at V_{CC} = 3.3 V and T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC},V_{CCO}	Supply voltage		3	3.3	3.6	V
I_{CC}	Supply current	DISABLE = low (excludes CML output current)		32	40	mA
V_{OD}	Differential data output voltage swing	DISABLE = high		0.25	10	mV_{p-p}
		DISABLE = low	600	780	1200	mV_{p-p}
r_{IN}, r_{OUT}	Data input/output resistance	Single ended		50		Ω
	RSSI output voltage	Input = 2 mV_{p-p}, R_{RSSI} ≥ 10 kΩ		100		mV
		Input = 80 mV_{p-p}, R_{RSSI} ≥ 10 kΩ		2800		
	RSSI linearity	20−dB input signal, V_{IN} ≤ 80 mVpp		±3%	±8%	
$V_{(IN_MIN)}$	Data input sensitivity	BER < 10^{-10}		3	5	mV_{p-p}
$V_{(IN_MAX)}$	Data input overload		1200			mV_{p-p}
	CMOS input high voltage		2.1			V
	CMOS input low voltage				0.6	V
	LOS high voltage	I_{SINK} = –30 µA	2.4			V
	LOS low voltage	I_{SOURCE} = 1 mA			0.4	V
	LOS hysteresis	2^{23}–1 PRBS (at 2.5 Gbps and 155 Mbps)	2.5	4.5		dB
V_{TH}	LOS assert threshold range	2^{23}–1 PRBS (at 2.5 Gbps and 155 Mbps)		5−40		mV_{p-p}

ac electrical characteristics

over recommended operating conditions (unless otherwise noted), typical operating condition is at V_{CC} = 3.3 V and T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Low frequency −3-dB bandwidth	C_{OC} = open		45	70	kHz
		C_{OC} = 2.2 nF		0.8		
	Data rate		3.3			Gb/s
v_{NI}	Input referred noise			180		$µV_{RMS}$
DJ	Deterministic jitter, See Note 2	K28.5 pattern at 3.3 Gbps		8.5	25	ps_{p-p}
		2^{23}–1 PRBS equivalent pattern at 2.7 Gbps		9.3	30	
		K28.5 pattern at 2.1 Gbps		7.8	25	
		2^{23}–1 PRBS equivalent pattern at 155 Mbps		25	50	
RJ	Random jitter	Input = 5 mVpp		6.5		ps_{RMS}
		Input = 10 mVpp		3		
t_r	Output rise time	20% to 80%		60	85	ps
t_f	Output fall time	20% to 80%		60	85	ps
PSNR	Power supply noise rejection	f < 2 MHz	26			dB
t_{DIS}	Disable response time			20		ns
t_{LOS}	LOS assert/deassert time		2		100	µs

NOTE 2: Deterministic jitter does not include pulse-width distortion due to residual small output offset voltage.

APPLICATION INFORMATION

Figure 3 shows the ONET3301PA connected with an ac-coupled interface to the data signal source as well as to the output load.

Besides the ac-coupling capacitors, C_1 through C_4 in the input and output data signal lines, the only required external component is the LOS threshold setting resistor R_{TH}. In addition, an optional external filter capacitor (C_{OC}) may be used if a low cutoff frequency is desired.

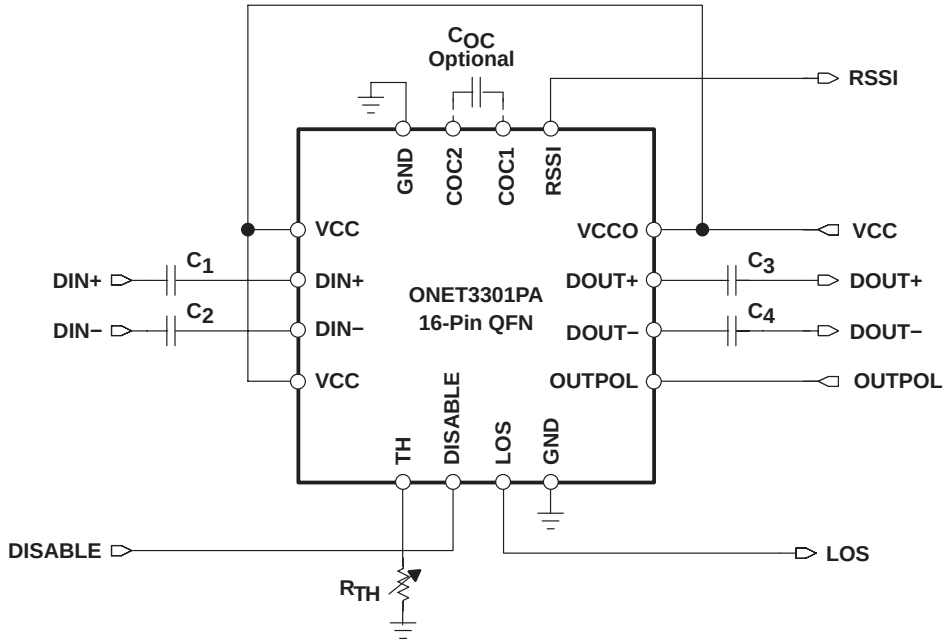


Figure 3. Basic Application Circuit With AC-Coupled I/Os

DIFFERENTIAL OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

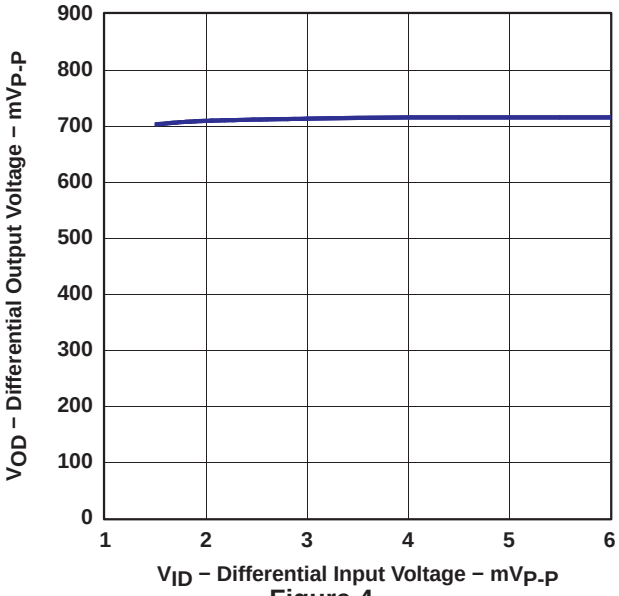


Figure 4

RANDOM JITTER vs DIFFERENTIAL INPUT VOLTAGE

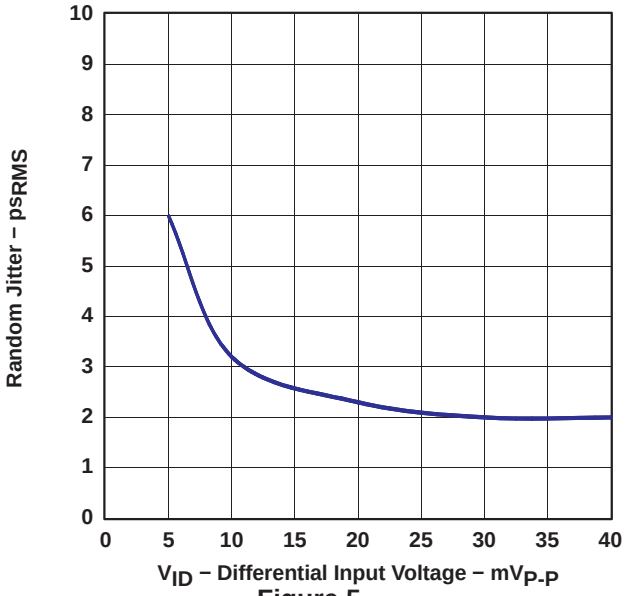


Figure 5

BIT ERROR RATIO vs DIFFERENTIAL INPUT VOLTAGE

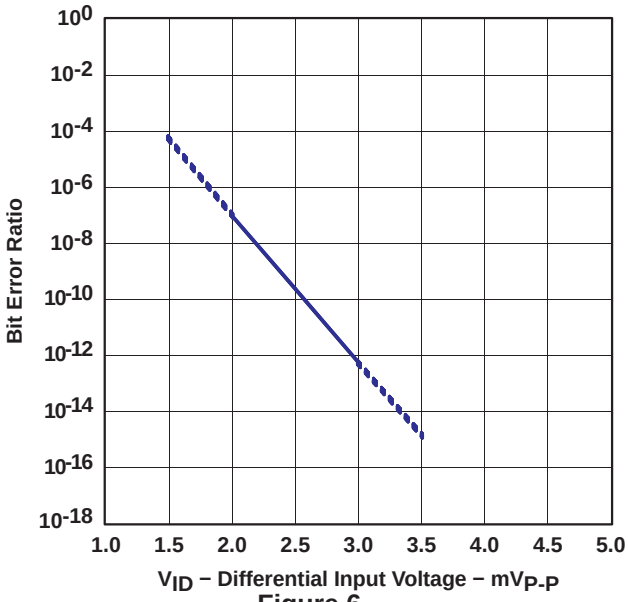


Figure 6

SMALL SIGNAL GAIN vs FREQUENCY

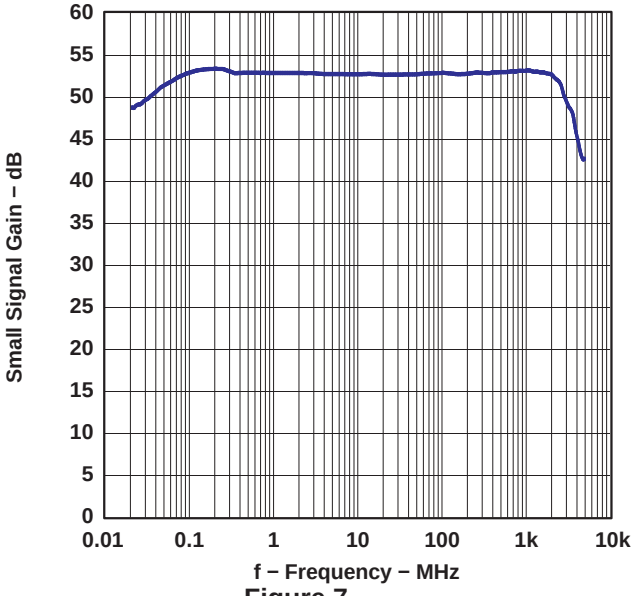


Figure 7

OUTPUT EYE-DIAGRAM AT 3.3 GBPS AND MINIMUM INPUT VOLTAGE (1200 mV_{p-p})

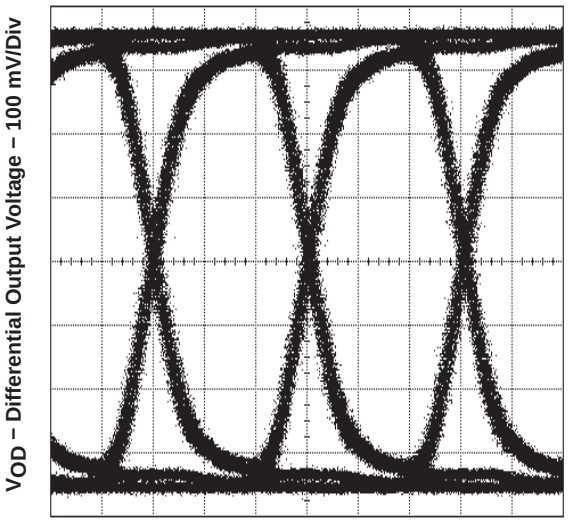


Figure 8

OUTPUT EYE-DIAGRAM AT 3.3 GBPS AND MAXIMUM INPUT VOLTAGE (1200 mV_{p-p})

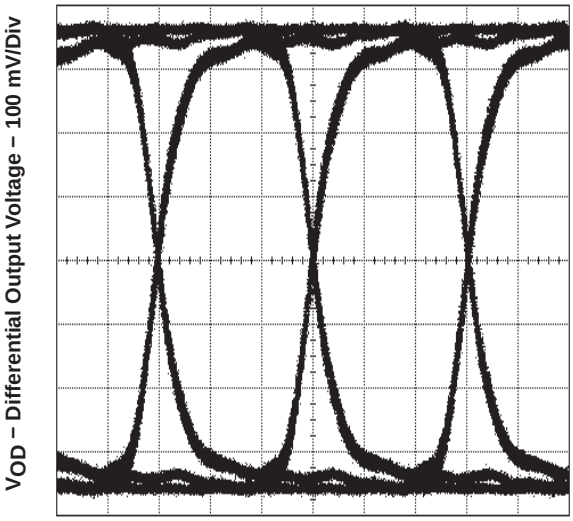


Figure 9

OUTPUT EYE-DIAGRAM AT 3.3 GBPS AND 85°C MINIMUM INPUT VOLTAGE (5 mV_{p-p})

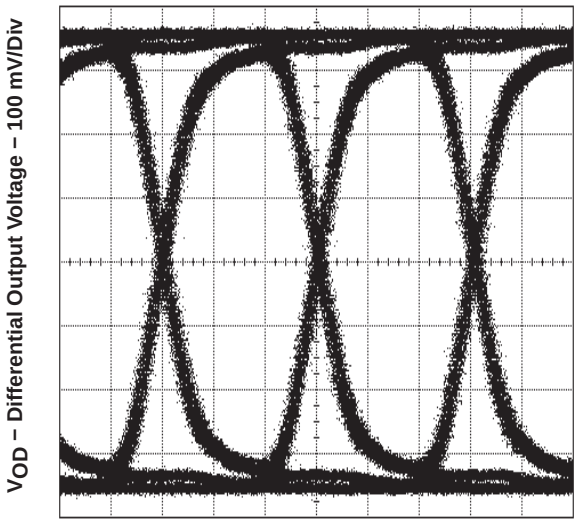


Figure 10

OUTPUT EYE-DIAGRAM AT 2.5 GBPS AND MINIMUM INPUT VOLTAGE (5 mV_{p-p})

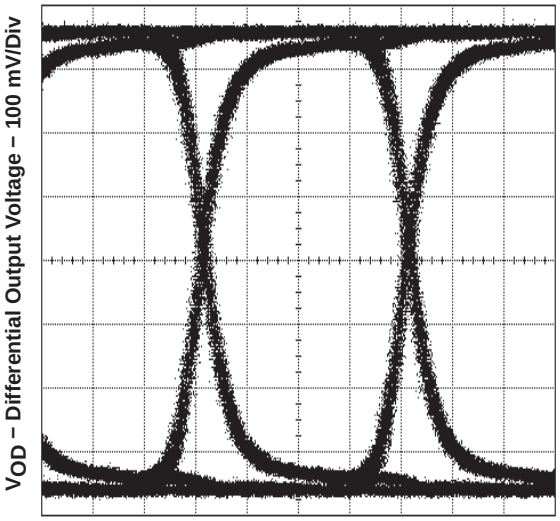


Figure 11

OUTPUT EYE-DIAGRAM AT 2.5 GBPS AND MAXIMUM INPUT VOLTAGE (1200 mV_{p-p})

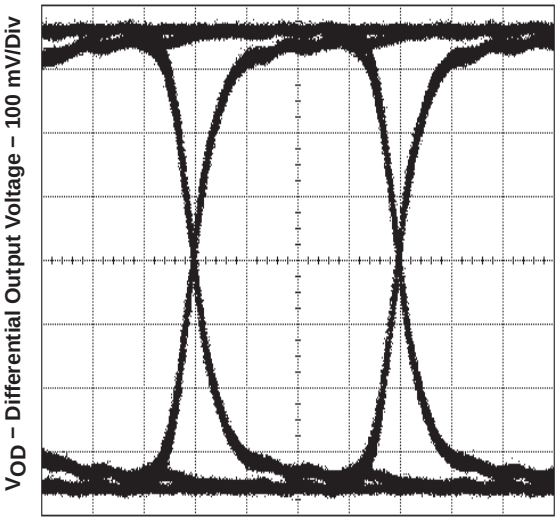


Figure 12

LOS ASSERT/DEASSERT VOLTAGE vs EXTERNAL RESISTANCE R_{TH}

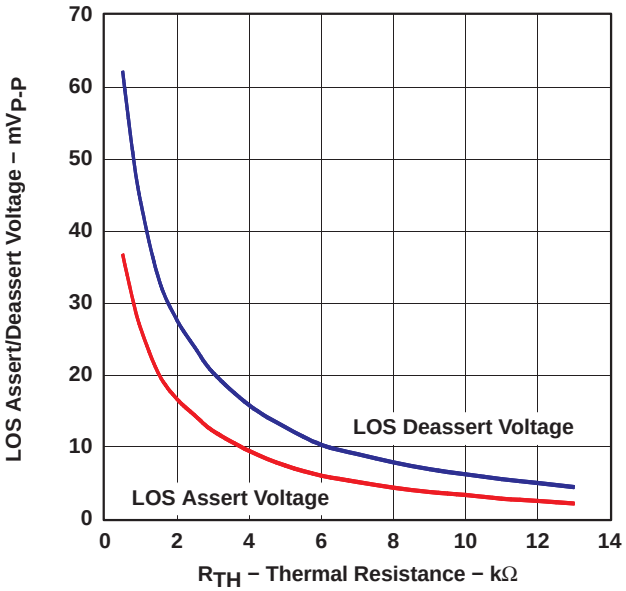


Figure 13

DIFFERENTIAL INPUT RETURN GAIN vs FREQUENCY

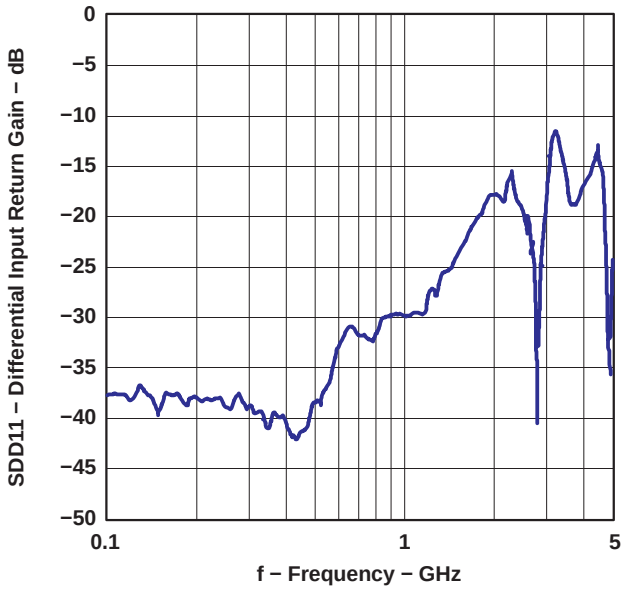


Figure 14

DIFFERENTIAL OUTPUT RETURN GAIN vs FREQUENCY

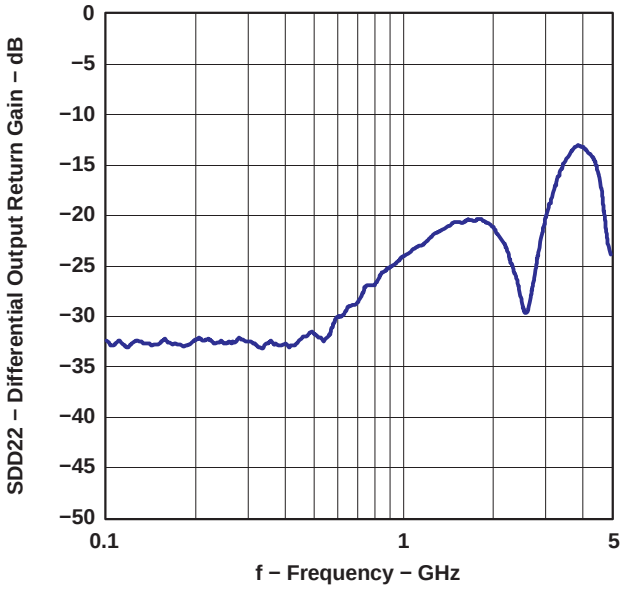


Figure 15

RECEIVE SIGNALS STRENGTH INDICATOR vs DIFFERENTIAL INPUT VOLTAGE

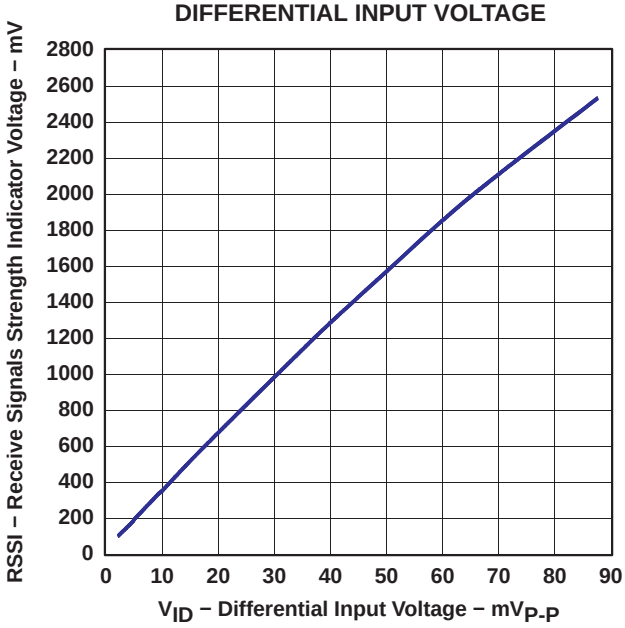


Figure 16

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
ONET3301PARGT	ACTIVE	QFN	RGT	16	121	None	CU NIPDAU	Level-2-220C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2005, Texas Instruments Incorporated

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001
Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
moschip.ru
moschip.ru_4
moschip.ru_6
moschip.ru_9