

EVALUATION KIT
AVAILABLE

Dual/Quad, Unipolar/Bipolar, High-Voltage Digital Pulsers

MAX4940/MAX4940A

General Description

The MAX4940/MAX4940A integrated circuits generate high-voltage, high-frequency, unipolar or bipolar pulses from low-voltage logic inputs. These quad/dual pulsers feature independent logic inputs, independent high-voltage pulser outputs with active clamps and independent high-voltage supply inputs.

The MAX4940/MAX4940A feature quad, high-voltage pulsers with 8.5Ω output impedance for the high-voltage outputs and a 21Ω impedance for the active clamp. The high-voltage outputs can provide 2.0A (typ) output current.

All devices use two logic inputs per channel to control the positive and negative pulses. The MAX4940/MAX4940A have a dedicated input to control the active clamp. All devices feature an independent enable input EN. All digital inputs are CMOS compatible (see the *Ordering Information/Selector Guide*).

The MAX4940/MAX4940A are available in a 56-pin, 8mm x 8mm, TQFN exposed pad package and are specified over the 0°C to $+70^{\circ}\text{C}$ commercial temperature range.

Warning: Exercise caution. The MAX4940/MAX4940A are designed to operate with high voltages.

Applications

Ultrasound Medical Imaging
Flaw Detection
Piezoelectric Drivers
Test Instruments
Cleaning Equipment

Features

- ◆ High-Density Quad-Channel Pulser in One Package
- ◆ 0 to +220V Unipolar or $\pm 110\text{V}$ Bipolar Outputs
- ◆ 8.5Ω (typ) Output Impedance and 2.0A (typ) Output Current
- ◆ 21Ω (typ) Always-On Active Clamp with Integrated Blocking Diodes
- ◆ Integrated Output Diodes (MAX4940A Only)
- ◆ No Special Power-Supply Sequencing Required for Trilevel Applications
- ◆ Matched Rise/Fall Times and Matched Propagation Delays
- ◆ CMOS-Compatible Logic Inputs
- ◆ 56-Pin, 8mm x 8mm, TQFN Package

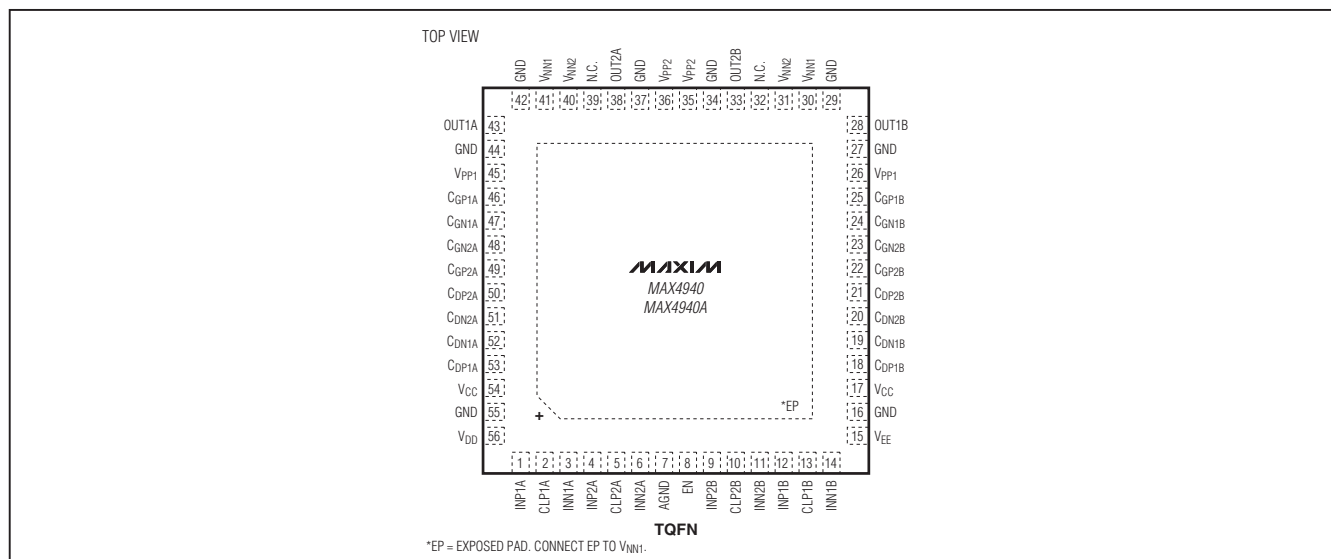
Ordering Information/ Selector Guide

PART	OUTPUT BLOCKING DIODE	OUTPUT CURRENT (A)	PIN- PACKAGE
MAX4940CTN+	None	2.0 (typ)	56 TQFN-EP*
MAX4940ACTN+	OUT2A, OUT2B	2.0 (typ)	56 TQFN-EP*

Note: Devices operate over the 0°C to $+70^{\circ}\text{C}$ temperature range.
+Denotes a lead(Pb)-free/RoHS-compliant package.

*EP = Exposed pad.

Pin Configuration



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ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)

V _{DD} Logic Supply Voltage	-0.3V to +6V
V _{CC} Output Driver Positive Supply Voltage	-0.3V to +15V
V _{EE} Output Driver Negative Supply Voltage	-15V to +0.3V
V _{PP} High-Positive Supply Voltage	-0.3V to (V _{NN} + 220V)
V _{NN} Low-Negative Supply Voltage	-220V to +0.3V
V _{PP1} - V _{NN1} , V _{PP2} - V _{NN2} Supply Voltage	-0.6V to +250V
INP ₋ , INN ₋ , CLP ₋ , EN Logic Input	-0.3V to (V _{DD} + 0.3V)
C _{GN} Voltage	(-0.3V + V _{NN}) to (+15V + V _{NN})
C _{GP} Voltage	(+0.3V + V _{PP}) to (-15V + V _{PP})

C _{DP} , C _{DN} Voltage	-0.3V to V _{CC}
Continuous Power Dissipation (T _A = +70°C)	
56-Pin TQFN (derate 47.6mW/°C above +70°C)	3809mW
Thermal Resistance (Note 1)	
θ _{JA}	21°C/W
θ _{JC}	1°C/W
Operating Temperature Range	0°C to +70°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maxim-ic.com/thermal-tutorial.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +3V, V_{CC} = +12V, V_{EE} = -12V, V_{PP} = +100V, V_{NN} = -100V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY (V_{DD}, V_{CC}, V_{EE}, V_{PP}, V_{NN})						
Logic Supply Voltage	V _{DD}		2.37	3	6	V
Positive Drive Supply Voltage	V _{CC}		4.75	12	12.6	V
Negative Drive Supply Voltage	V _{EE}		1.05 x (-V _{CC})	-V _{CC}	0.95 x (-V _{CC})	V
High-Side Supply Voltage	V _{PP1}		0		+200	V
Low-Side Supply Voltage	V _{NN1}		-200		0	V
High-Side Supply Voltage	V _{PP2}		0		V _{PP1}	V
Low-Side Supply Voltage	V _{NN2}		V _{NN1}		0	V
V _{PP} - V _{NN} Supply Voltage			0		+200	V
SUPPLY CURRENT (for single channel)						
V _{DD} Supply Current	I _{DD}	V _{NN} /V _{INP} /V _{CLP} = 0 or V _{DD} , V _{EN} = 0			1	μA
		V _{EN} = V _{DD} , V _{CLP} = 0 or V _{DD} , V _{NN} = V _{INP} , f = 5MHz, one channel switching		100	200	μA
V _{CC} Supply Current	I _{CC}	V _{EN} = 0 (static)			1	μA
		V _{EN} = V _{DD} (static)			10	μA
		V _{EN} = V _{DD} , V _{CLP} = 0 or V _{DD} , V _{NN} = V _{INP} , f = 5MHz, V _{CC} = +12V, V _{DD} = +3V, one channel switching		36		mA
		V _{EN} = V _{DD} , V _{CLP} = 0 or V _{DD} , V _{NN} = V _{INP} , f = 5MHz, V _{CC} = +5V, V _{DD} = +3V, one channel switching		15		

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ELECTRICAL CHARACTERISTICS (continued)

(VDD = +3V, VCC = +12V, VEE = -12V, VPP_ = +100V, VNN_ = -100V, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
VEE_ Supply Current	IEE_	VEN = 0 or VDD (static)		1			μA
		VEE = -5V, VEN = VDD, VCLP_ = VDD, PRF = 10kHz, f = 5MHz, four pulses, no load, one channel switching		100			
		VEE = -12V, VEN = VDD, VCLP_ = VDD, PRF = 10kHz, f = 5MHz, four pulses, no load, one channel switching		200			
VPP_ Supply Current	IPP_	VEN = 0 or VDD (static)		1			μA
		VEN = VDD, VCLP_ = 0 or VDD, VINN_ = VINP_ , f = 5MHz, VPP_ = +5V, VNN_ = -5V, no load, one channel switching		9			mA
		VEN = VDD, VCLP_ = 0 or VDD, VPP_ = +80V, VNN_ = -80V, PRF = 10kHz, f = 10MHz, four pulses, no load, one channel switching		0.6			
VNN_ Supply Current	INN_	VEN = 0 or VDD (static)		1			μA
		VEN = VDD, VCLP_ = 0 or VDD, VINN_ = VINP_ , f = 5MHz, VPP_ = +5V, VNN_ = -5V, no load, one channel switching		9			mA
		VEN = VDD, VINC_ = 0 or VDD, VPP_ = +80V, VNN_ = -80V, PRF = 10kHz, f = 10MHz, four pulses, no load, one channel switching		0.6			
LOGIC INPUTS (EN, INN_ , INP_ , CLP_)							
Low-Level Input Voltage	VIL			0.25 x VDD			V
High-Level Input Voltage	VIH			0.75 x VDD			V
Logic-Input Capacitance	CIN			5			pF
Logic-Input Leakage	IIN	VIN = 0 or VDD		0 ±1			μA
OUTPUT (OUT_)							
OUT_ Output-Voltage Range	VOUT_	No load at OUT_		VNN_ VPP_		V	
		100mA load (MAX4940), VCC = +12V ±5%		VNN_ + 1.5 VPP_ - 1.5		V	
		100mA load (MAX4940A), VCC = +12V ±5%		VNN_ + 2.5 VPP_ - 2.5		V	
Low-Side Output Impedance (MAX4940)	ROLS	IOUT_ = -50mA	VCC = +12V ±5%	7.5 14		Ω	
			VCC = +5V ±5%	8 18			
High-Side Output Impedance (MAX4940)	ROHS	IOUT_ = -50mA	VCC = +12V ±5%	9 14		Ω	
			VCC = +5V ±5%	10.5 18			

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ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3V, V_{CC} = +12V, V_{EE} = -12V, V_{PP} = +100V, V_{NN} = -100V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Low-Side Output Impedance (MAX4940A)	R _{OLS}	I _{OUT} = -50mA	V _{CC} = +12V ±5% V _{CC} = +5V ±5%	8.5 10.0	17 21	Ω
High-Side Output Impedance (MAX4940A)	R _{OHS}	I _{OUT} = -50mA	V _{CC} = +12V ±5% V _{CC} = +5V ±5%	11.5 13.0	17 21	Ω
Low-Side Signal CLAMP Output Impedance	R _{OLSC}	I _{OUT} = -50mA	V _{CC} = +12V ±5% V _{CC} = +5V ±5%	18.7 20	45 60	Ω
High-Side Signal CLAMP Output Impedance	R _{OHSC}	I _{OUT} = -50mA	V _{CC} = +12V ±5% V _{CC} = +5V ±5%	26.5 37.0	45 60	Ω
PEAK CURRENT						
Low-Side Output Current	I _{OL}	V _{CC} = +12V ±5%, V _{OUT} - V _{NN} = 100V	1.3	2.0		A
High-Side Output Current	I _{OH}	V _{CC} = +12V ±5%, V _{OUT} - V _{PP} = 100V	1.3	2.0		A
Low-Side Output Current Clamp	I _{OLC}	V _{CC} = +12V ±5%, V _{OUT} = +40V	0.47	0.9		A
High-Side Output Current Clamp	I _{OHc}	V _{CC} = +12V ±5%, V _{OUT} = +40V	0.47	0.9		
Off-Output Capacitance	C _{O(OFF)}	MAX4940, MAX4940A (OUT1 ₋)		75		pF
		MAX4940A (OUT2 ₋)		45		
Off-Output Leakage Current	I _{LK}	V _{NN} = -100V, V _{PP} = +100V, V _{EN} = 0, V _{OUT} = -100V to +100V			±1	μA
GATE-SOURCE RESISTANCE						
Gate-Source Resistance	R _{GS}	V _{EN} = V _{DD}	5	7.5	10	kΩ
DYNAMIC CHARACTERISTICS (R_L = 100Ω, C_L = 100pF, unless otherwise noted)						
Logic Input-to-Output Rise Propagation Delay (Figure 1)	t _{PLH}	INN ₋ /INP ₋ at 50% to OUT ₋ 10/90%, V _{CC} = +12V, V _{PP} = +5V, V _{NN} = -5V		15		ns
Logic Input-to-Output Fall Propagation Delay (Figure 1)	t _{PHL}	INN ₋ /INP ₋ at 50% to OUT ₋ 10/90%, V _{CC} = +12V, V _{PP} = +5V, V _{NN} = -5V		15		ns
Logic Input-to-Output Rise Propagation Delay Clamp (Figure 1)	t _{PLO}	INN ₋ /INP ₋ at 50% to OUT ₋ 10/90%, V _{CC} = +12V, V _{PP} = +5V, V _{NN} = -5V		15		ns
Logic Input-to-Output Fall Propagation Delay Clamp (Figure 1)	t _{PHO}	INN ₋ /INP ₋ at 50% to OUT ₋ 10/90%, V _{CC} = +12V, V _{PP} = +5V, V _{NN} = -5V		15		ns
OUT ₋ Rise Time (GND to V _{PP}) (Figure 1)	t _{ROP}	V _{PP} = +100V, V _{NN} = -100V, 10% to 90%, V _{CC} = +12V ±5%, V _{EE} = -V _{CC}		9	20	ns
OUT ₋ Rise Time (V _{NN} to V _{PP}) (Figure 1)	t _{RNP}	V _{PP} = +100V, V _{NN} = -100V, 10% to 90%, V _{CC} = +12V ±5%, V _{EE} = -V _{CC}		10.5	35	ns
OUT ₋ Fall Time (GND to V _{NN}) (Figure 1)	t _{FON}	V _{PP} = +100V, V _{NN} = -100V, 10% to 90%, V _{CC} = +12V ±5%, V _{EE} = -V _{CC}		9	20	ns
OUT ₋ Fall Time (V _{PP} to V _{NN}) (Figure 1)	t _{FPN}	V _{PP} = +100V, V _{NN} = -100V, 10% to 90%, V _{CC} = +12V ±5%, V _{EE} = -V _{CC}		10.5	35	ns
OUT ₋ Rise Time (V _{NN} to GND) (Figure 1)	t _{RNO}	V _{PP} = +100V, V _{NN} = -100V, 10% to 90%, V _{CC} = +12V ±5%, V _{EE} = -V _{CC}		17	35	ns

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MAX4940/MAX4940A

ELECTRICAL CHARACTERISTICS (continued)

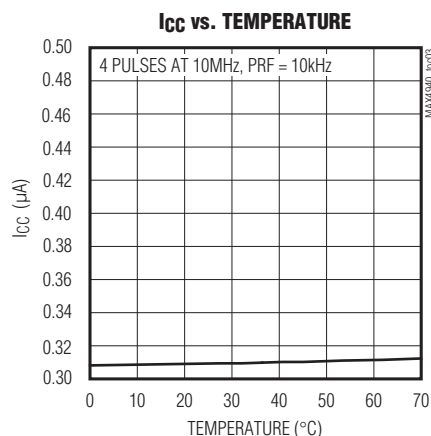
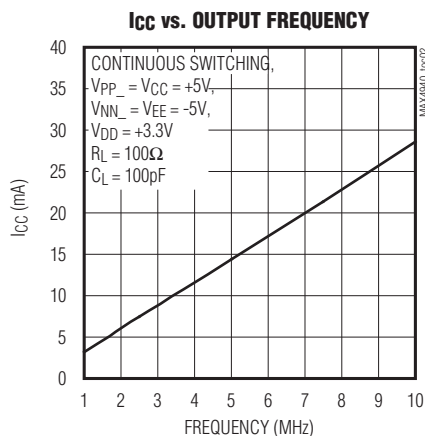
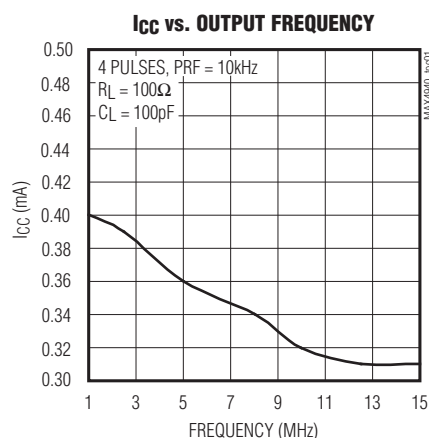
(V_{DD} = +3V, V_{CC} = +12V, V_{EE} = -12V, V_{PP} = +100V, V_{NN} = -100V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUT_ Fall Time (V _{PP} to GND) (Figure 1)	t _{FPO}	V _{PP} = +100V, V _{NN} = -100V, 10% to 90%, V _{CC} = +12V ±5%, V _{EE} = -V _{CC}		17	35	ns
Output Enable Time from EN (Figure 2)	t _{EN}	V _{PP} = +5V, V _{NN} = -5V			100	ns
Output Disable Time from EN (Figure 2)	t _{DI}	V _{PP} = +5V, V _{NN} = -5V			150	ns
2nd Harmonic Distortion LV	THD2_LV	f _{OUT} = 5MHz, V _{PP} = -V _{NN} = +5V, V _{CC} = +12V		-40		dB
2nd Harmonic Distortion HV	THD2_HV	f _{OUT} = 5MHz, V _{PP} = -V _{NN} = +50V, V _{CC} = +12V, 10 periods		-45		dB
Pulse Cancellation	2HD	f _{OUT} = 5MHz, V _{PP} = -V _{NN} = +50V, V _{CC} = +12V, 10 periods, 1st harmonic cancellation		-43		dB
RMS Output Jitter	t _J			10		ps
Crosstalk	CT	Adjacent channels, f = 5MHz		-60		dB

Note 2: Specifications are guaranteed for the stated global conditions, unless otherwise noted. 100% production tested at T_A = +70°C. Specifications at T_A = 0°C are guaranteed by design.

Typical Operating Characteristics

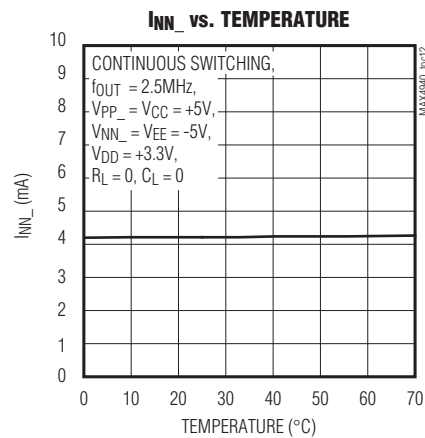
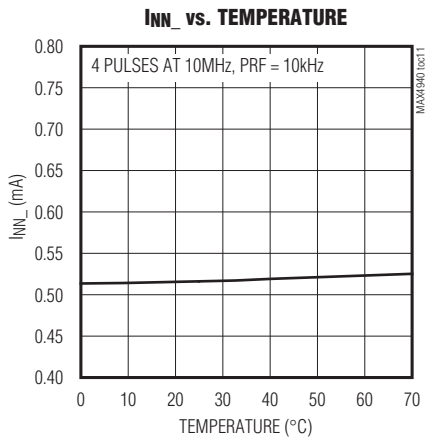
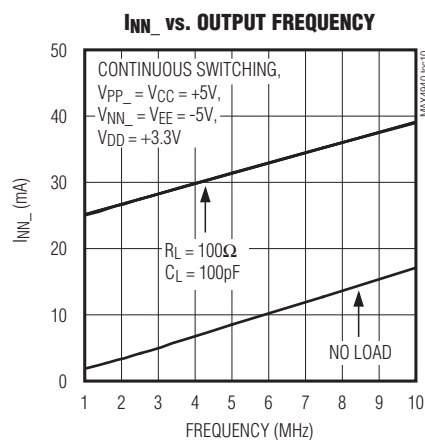
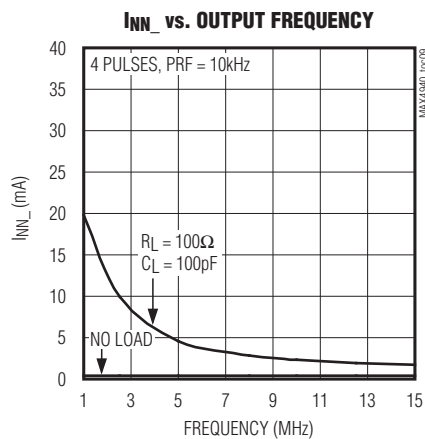
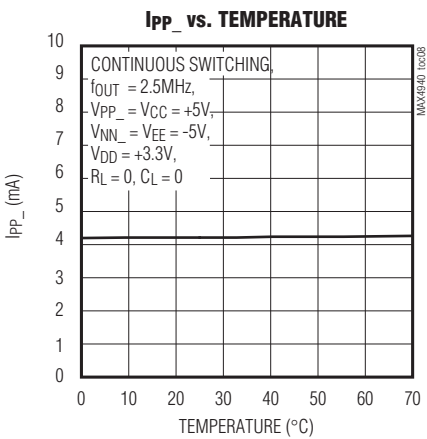
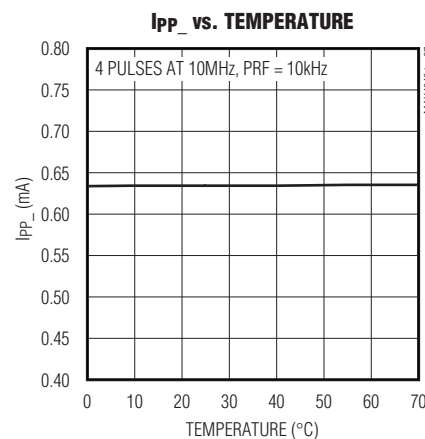
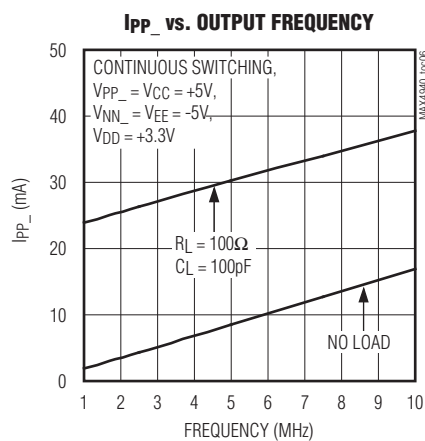
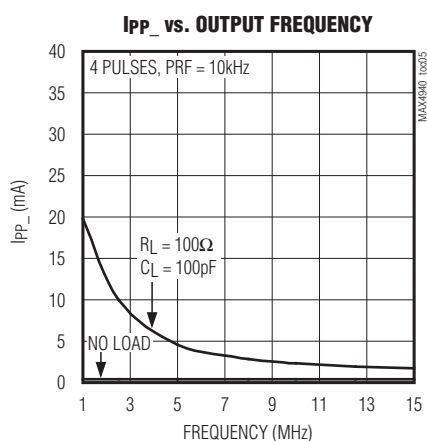
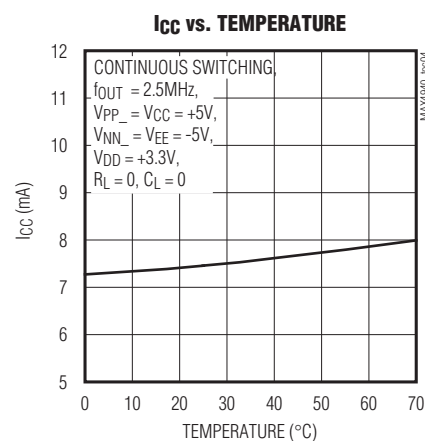
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Typical Operating Characteristics (continued)

($V_{DD} = +3.3V$, $V_{CC} = +12V$, $V_{EE} = -12V$, $V_{PP_} = +100V$, $V_{NN_} = -100V$, $f_{OUT} = 5MHz$, $R_L = 100\Omega$, $C_L = 100pF$, $T_A = +25^\circ C$, unless otherwise noted.)

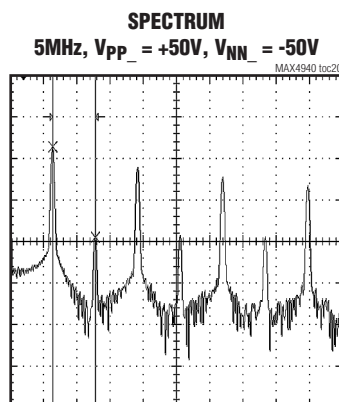
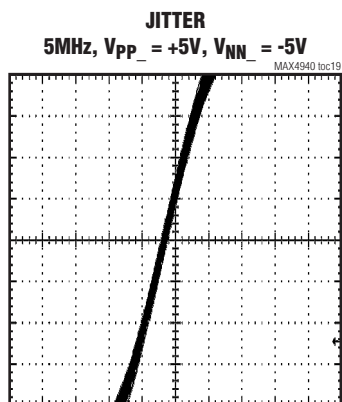
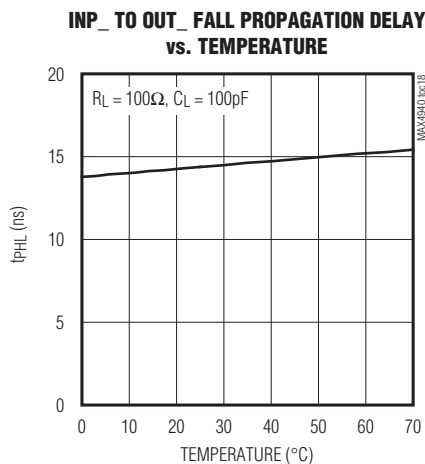
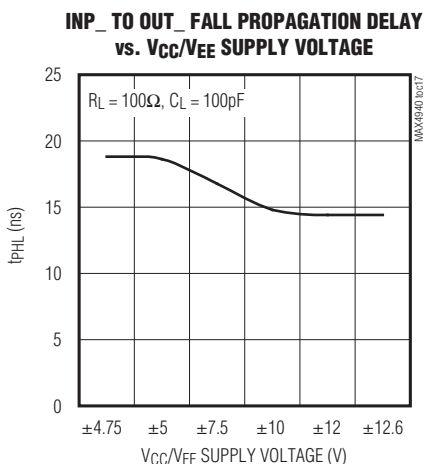
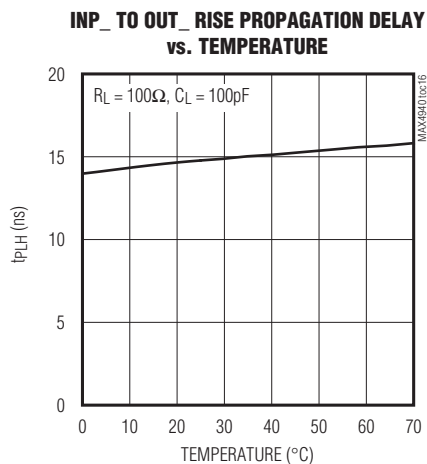
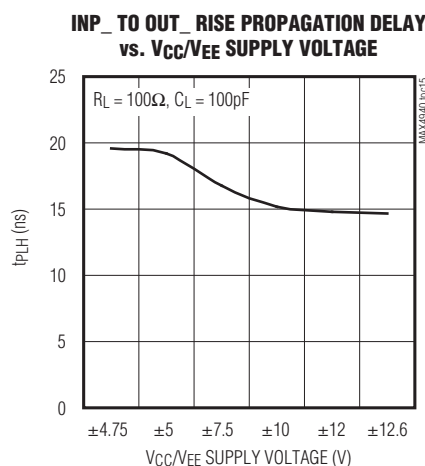
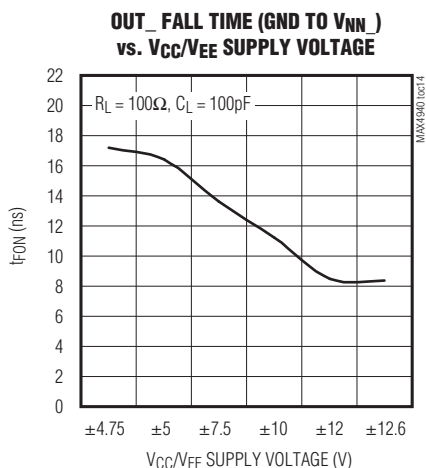
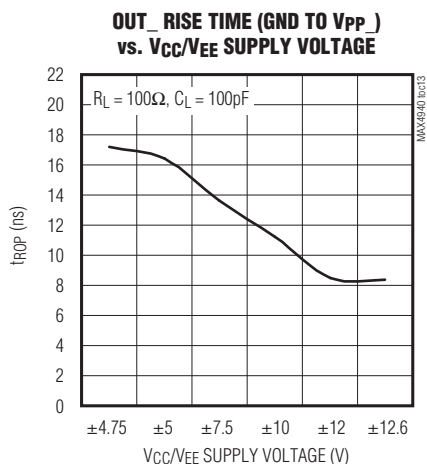


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Typical Operating Characteristics (continued)

($V_{DD} = +3.3V$, $V_{CC} = +12V$, $V_{EE} = -12V$, $V_{PP_} = +100V$, $V_{NN_} = -100V$, $f_{OUT} = 5MHz$, $R_L = 100\Omega$, $C_L = 100pF$, $T_A = +25^\circ C$, unless otherwise noted.)

MAX4940/MAX4940A



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MAX4940/MAX4940A

Pin Description

PIN	NAME	FUNCTION
1	INP1A	Channel 1A High-Side Logic Input. See the <i>Truth Tables</i> section.
2	CLP1A	Channel 1A Clamp Logic Input. Clamp is turned on when CLP1A is high and when INP1A and INN1A are low. See the <i>Truth Table</i> section.
3	INN1A	Channel 1A Low-Side Logic Input. See the <i>Truth Tables</i> section.
4	INP2A	Channel 2A High-Side Logic Input. See the <i>Truth Tables</i> section.
5	CLP2A	Channel 2A Clamp Logic Input. Clamp is turned on when CLP2A is high and when INP2A and INN2A are low. See the <i>Truth Tables</i> section.
6	INN2A	Channel 2A Low-Side Logic Input. See the <i>Truth Tables</i> section.
7	AGND	Analog Ground. Must be connected to common GND.
8	EN	Enable Logic Input. Drive EN high to enable OUT1A, OUT1B, OUT2A, and OUT2B.
9	INP2B	Channel 2B High-Side Logic Input. See the <i>Truth Tables</i> section.
10	CLP2B	Channel 2B Clamp Logic Input. Clamp is turned on when CLP2B is high and when INP2B and INN2B are low. See the <i>Truth Tables</i> section.
11	INN2B	Channel 2B Low-Side Logic Input. See the <i>Truth Tables</i> section.
12	INP1B	Channel 1B High-Side Logic Input. See the <i>Truth Tables</i> section.
13	CLP1B	Channel 1B Clamp Logic Input. Clamp is turned on when CLP1B is high and when INP1B and INN1B are low. See the <i>Truth Tables</i> section.
14	INN1B	Channel 1B Low-Side Logic Input. See the <i>Truth Tables</i> section.
15	VEE	Negative Supply Input. Gate-drive supply voltage for the clamp. Bypass VEE to GND with a 0.1μF capacitor as close as possible to the device.
16, 27, 29, 34, 37, 42, 44, 55	GND	Ground
17, 54	VCC	Gate-Drive Supply Voltage Input. Bypass VCC to GND with a 0.1μF capacitor as close as possible to the device.
18	CDP1B	Channel 1B High-Side Driver Output. Connect a 3.3nF capacitor between CDP1B and CGP1B as close as possible to the device.
19	CDN1B	Channel 1B Low-Side Driver Output. Connect a 3.3nF capacitor between CDN1B and CGN1B as close as possible to the device.
20	CDN2B	Channel 2B Low-Side Driver Output. Connect a 3.3nF capacitor between CDN2B and CGN2B as close as possible to the device.
21	CDP2B	Channel 2B High-Side Driver Output. Connect a 3.3nF capacitor between CDP2B and CGP2B as close as possible to the device.
22	CGP2B	Channel 2B High-Side Gate Input. Connect a 3.3nF capacitor between CDP2B and CGP2B as close as possible to the device.
23	CGN2B	Channel 2B Low-Side Gate Input. Connect a 3.3nF capacitor between CDN2B and CGN2B as close as possible to the device.
24	CGN1B	Channel 1B Low-Side Gate Input. Connect a 3.3nF capacitor between CDN1B and CGN1B as close as possible to the device.
25	CGP1B	Channel 1B High-Side Gate Input. Connect a 3.3nF capacitor between CDP1B and CGP1B as close as possible to the device.

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Pin Description (continued)

PIN	NAME	FUNCTION
26, 45	VPP1	Channel 1A, 1B High-Side Positive Supply Voltage Input. Bypass VPP1 to GND with a 0.1μF capacitor as close as possible to the device.
28	OUT1B	Channel 1B Output
30, 41	VNN1	Channel 1A, 1B Low-Side Negative Supply Voltage Input. Bypass VNN1 to GND with a 0.1μF capacitor as close as possible to the device.
31, 40	VNN2	Channel 2A, 2B Low-Side Negative Supply Voltage Input. Bypass VNN2 to GND with a 0.1μF capacitor as close as possible to the device.
32, 39	N.C.	No Connection. Not connected internally.
33	OUT2B	Channel 2B Output
35, 36	VPP2	Channel 2A, 2B High-Side Positive Supply Voltage Input. Bypass VPP2 to GND with a 0.1μF capacitor as close as possible to the device.
38	OUT2A	Channel 2A Output
43	OUT1A	Channel 1A Output
46	CGP1A	Channel 1A High-Side Gate Input. Connect a 3.3nF capacitor between CDP1A and CGP1A as close as possible to the device.
47	CGN1A	Channel 1A Low-Side Gate Input. Connect a 3.3nF capacitor between CDN1A and CGN1A as close as possible to the device.
48	CGN2A	Channel 2A Low-Side Gate Input. Connect a 3.3nF capacitor between CDN2A and CGN2A as close as possible to the device.
49	CGP2A	Channel 2A High-Side Gate Input. Connect a 3.3nF capacitor between CDP2A and CGP2A as close as possible to the device.
50	CDP2A	Channel 2A High-Side Driver Output. Connect a 3.3nF capacitor between CDP2A and CGP2A as close as possible to the device.
51	CDN2A	Channel 2A Low-Side Driver Output. Connect a 3.3nF capacitor between CDN2A and CGN2A as close as possible to the device.
52	CDN1A	Channel 1A Low-Side Driver Output. Connect a 3.3nF capacitor between CDN1A and CGN1A as close as possible to the device.
53	CDP1A	Channel 1A High-Side Driver Output. Connect a 3.3nF capacitor between CDP1A and CGP1A as close as possible to the device.
56	VDD	Logic-Supply Voltage Input. Bypass VDD to GND with a 0.1μF capacitor as close as possible to the device.
—	EP	Exposed Pad. EP must be connected to VNN1.

MAX4940/MAX4940A

Dual/Quad, Unipolar/Bipolar, High-Voltage Digital Pulsers

Detailed Description

The MAX4940/MAX4940A are quad high-voltage, high-speed pulsers that can be independently configured for either unipolar/bipolar/multilevel pulse outputs (see Figures 5 and 6.). These devices have independent logic inputs for full pulse control and independent active clamps. The clamp input, CLP_, can be set high to activate the clamp automatically when the device is not pulsing to the positive or negative high-voltage supplies.

Logic Inputs (INP_, INN_, CLP_, EN)

INP_ controls the on and off states of the high-side FET, INN_ controls the on and off states of the low-side FET, and CLP_ controls the active clamp. A global enable input (EN) can be used to enable/disable all channels. These signals give complete control of the output stage of each driver (see the *Truth Tables* section for all logic combinations). The MAX4940/MAX4940A logic inputs are **CMOS logic compatible and the logic levels are referenced to V_{DD}** for maximum flexibility. The low 5pF (typ) input capacitance of the logic inputs reduce loading and increase switching speed.

Truth Tables

MAX4940

INPUTS				OUTPUTS	STATE
EN	INP_	INN_	CLP_	OUT_	
0	X	X	X	High impedance	Powered up, INP_/INN_ disabled.
1	0	0	0	High impedance	Powered up, all inputs enabled.
1	0	0	1	GND	Powered up, all inputs enabled.
1	0	1	X	V _{NN_}	Powered up, all inputs enabled.
1	1	0	X	V _{PP_}	Powered up, all inputs enabled.
1	1	1	X	Not allowed	Not allowed.

MAX4940A

INPUTS				OUTPUTS	STATE
EN	INP1A INP1B	INN1A INN1B	CLP1A CLP1B	OUT1A OUT1B	
0	X	X	X	High impedance	Powered up, INP_/INN_ disabled.
1	0	0	0	High impedance	Powered up, all inputs enabled.
1	0	0	1	GND	Powered up, all inputs enabled.
1	0	1	0	V _{NN_}	Powered up, all inputs enabled.
1	1	0	0	V _{PP_}	Powered up, all inputs enabled.
1	1	1	1	Not allowed	Not allowed.

INPUTS				OUTPUTS	STATE
EN	INP2A INP2B	INN2A INN2B	CLP2A CLP2B	OUT2A OUT2B	
0	X	X	X	High impedance	Powered up, INP_/INN_ disabled.
1	0	0	0	High impedance	Powered up, all inputs enabled.
1	0	0	1	GND	Powered up, all inputs enabled.
1	0	1	X	V _{NN_}	Powered up, all inputs enabled.
1	1	0	X	V _{PP_}	Powered up, all inputs enabled.
1	1	1	X	Not allowed	Not allowed.

X = Don't care.

0 = Logic-low.

1 = Logic-high.

Dual/Quad, Unipolar/Bipolar, High-Voltage Digital Pulsers

Active Clamps

The MAX4940/MAX4940A feature an integrated active clamp circuit to improve pulse quality and reduce 2nd harmonic distortion. The clamp circuit consists of an n-channel (DC-coupled) and a p-channel (DC-coupled) high-voltage FETs that are switched on or off by the logic clamp input (CLP_).

The MAX4940/MAX4940A feature protected clamp devices, allowing the clamp circuit to be used in bipolar pulsing circuits (see Figures 3 and 4). A diode in series with the OUT_ output prevents the body diode of the low-side FET from turning on when a voltage lower than GND is present. Another diode in series with the OUT_ output prevents the body diode of the high-side FET from turning on when a voltage higher than ground is present. The MAX4940/MAX4940A have an active clamp on all outputs.

For the MAX4940 only, the user can connect the active clamp input (CLP_) to a logic-high voltage and drive only the INP_ and INN_ inputs to minimize the number of signals used to drive the device. In this case, whenever both the INP_ and INN_ inputs are low and the CLP_ input is high, the active clamp circuit pulls the output to GND (see the *Truth Tables* section for more information).

Integrated Blocking Diodes (MAX4940A Only)

The high-voltage OUT2A/OUT2B outputs of the MAX4940A feature integrated blocking diodes that allow the user to implement multilevel pulsing by connecting the outputs of multiple pulser channels in parallel. Internal diodes in series with the OUT2A and OUT2B outputs prevent the body diode of the high-side and low-side FETs from switching on when a voltage greater than VNN2 or VPP2 is present on the output (see Figure 4).

Thermal Protection

A thermal shutdown circuit with a typical threshold of +155°C prevents damage due to excessive power dissipation. When the junction temperature exceeds $T_J = +155^\circ\text{C}$, all outputs are disabled. Normal operation typically resumes after the IC's junction temperature drops below +130°C.

Applications Information

AC-Coupling Capacitor Selection

The value of all AC-coupling capacitors (between CDP_ and CGP_, and between CDN_ and CGN_) should be between 1nF to 10nF. The voltage rating of the capacitor should be greater than VPP_ and VNN_. The capacitors should be placed as close as possible to the device.

Power Dissipation

The power dissipation of the MAX4940/MAX4940A consists of three major components caused by the current consumption from VCC, VPP_, and VNN_. The sum of these components (PVCC, PVPP_, and PVNN_) must be kept below the maximum power-dissipation limit. See the *Typical Operating Characteristics* section for more information on typical supply currents versus switching frequencies.

The device consumes most of the supply current from VCC supply to charge and discharge internal nodes such as the gate capacitance of the high-side FET (Cp) and the low-side FET (CN). Neglecting the small quiescent supply current and a small amount of current used to charge and discharge the capacitances at the internal gate clamp FETs, the power consumption can be estimated as follows:

$$P_{VCC} = \left[(C_N \times V_{CC}^2 \times f_{IN}) + (C_P \times V_{CC}^2 \times f_{INP}) \right] \times (BRF \times BTD)$$

$$f_{IN} = f_{INN_} + f_{INP_}$$

where $f_{INN_}$ and $f_{INP_}$ are the switching frequency of the inputs INN_, INP_, respectively, and where BRF is the burst response frequency, and BTD is the burst time duration. The typical values of the gate capacitances are $C_N = 1.2\mu\text{F}$, $C_P = 0.4\mu\text{F}$.

See the *Typical Operating Characteristics* for VPP_ and VNN_ power consumption.

Power Supplies and Bypassing

The MAX4940/MAX4940A operate from independent supply voltage sets (only VDD, VCC, and VEE are common to all channels). VPP1/VNN1 supply two channels and VPP2/VNN2 supply the other two channels. The logic input circuit operates from a +2.37V to +6V single supply (VDD). The level-shift driver dual supplies, VCC/VEE operate from $\pm 4.75\text{V}$ to $\pm 12.6\text{V}$.

The VPP_/VNN_ high-side and low-side supplies are driven from a single positive supply up to +220V, from a single negative supply up to -220V, or from $\pm 110\text{V}$ dual supplies. Either VPP_ or VNN_ can be set at 0. Bypass each supply input to ground with a 0.1 μF capacitor as close as possible to the device.

Depending on the applications, additional bypassing may be needed to maintain the input of both VNN_ and VPP_ stable during output transitions. For example, with $C_{OUT} = 100\text{pF}$ and $R_{OUT} = 100\Omega$ load, the use of an additional 10 μF (typ) electrolytic capacitor is recommended.

Dual/Quad, Unipolar/Bipolar, High-Voltage Digital Pulsers

Exposed Pad and Layout Concerns

The MAX940/MAX940A provide an exposed pad (EP) underneath the TQFN package for improved thermal performance. EP is internally connected to V_{NN1}. Connect EP to V_{NN1} externally. To aid heat dissipation, connect EP to a similarly sized pad on the component side of the PCB. This pad should be connected through the solder-side copper by several plated holes to a large heat spreading copper area to conduct heat away from the device.

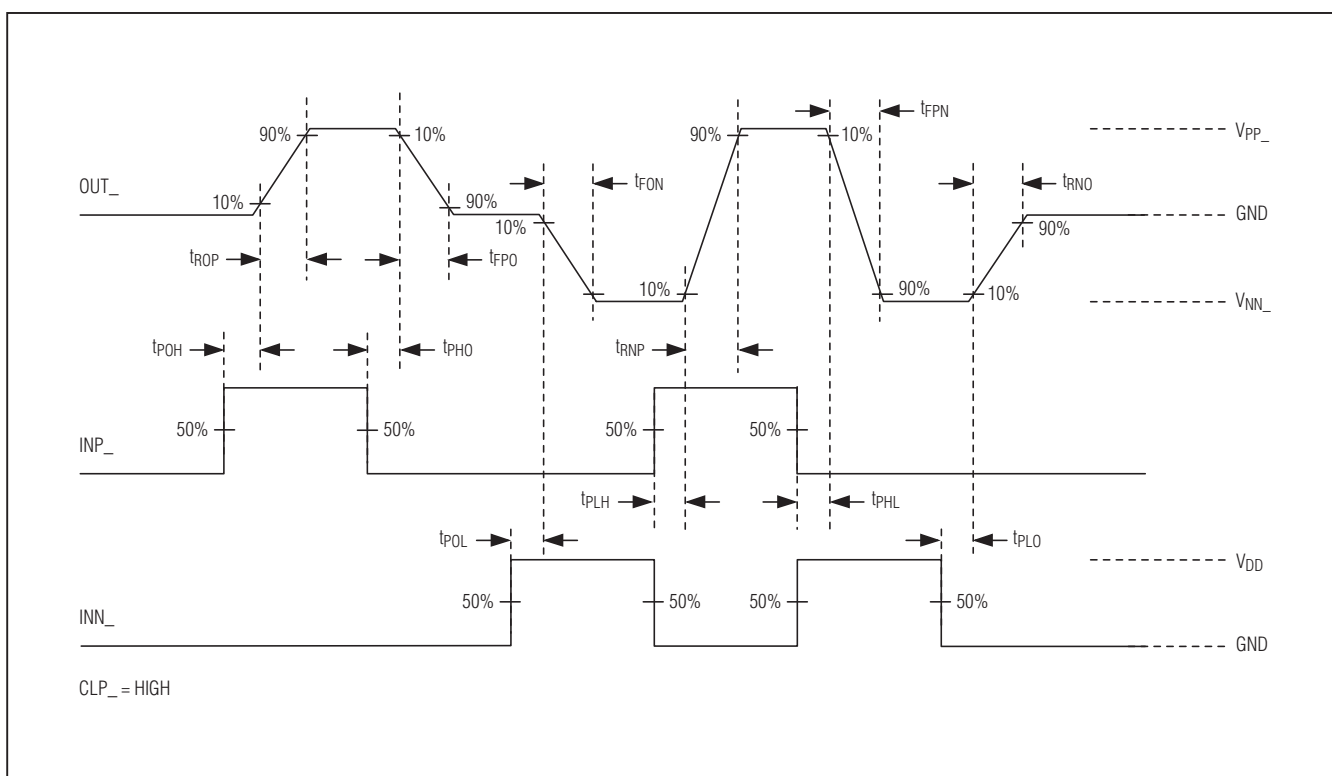
The MAX4940/MAX4940A high-speed pulsers require low-inductance bypass capacitors to their supply inputs. High-speed PCB trace design practices are recommended. Pay

particular attention to **minimize trace lengths and use sufficient trace width** to reduce inductance. Use of surface-mount components is recommended.

Supply Sequencing

In a typical trilevel application when VNN1 and VNN2 are externally shorted ($V_{NN1} = V_{NN2}$), the MAX4940/MAX4940A do not require any power sequencing. In general, and in particular for the multilevel application, VNN1 must be less than or equal to VNN2 ($V_{NN1} \leq V_{NN2}$) at all times. No other power-supply sequencing is required for the MAX4940/MAX4940A.

Timing Diagrams

Figure 1. Detail Timing ($R_L = 100\Omega$, $C_L = 100\text{pF}$)

Dual/Quad, Unipolar/Bipolar, High-Voltage Digital Pulsers

Timing Diagrams (continued)

MAX4940/MAX4940A

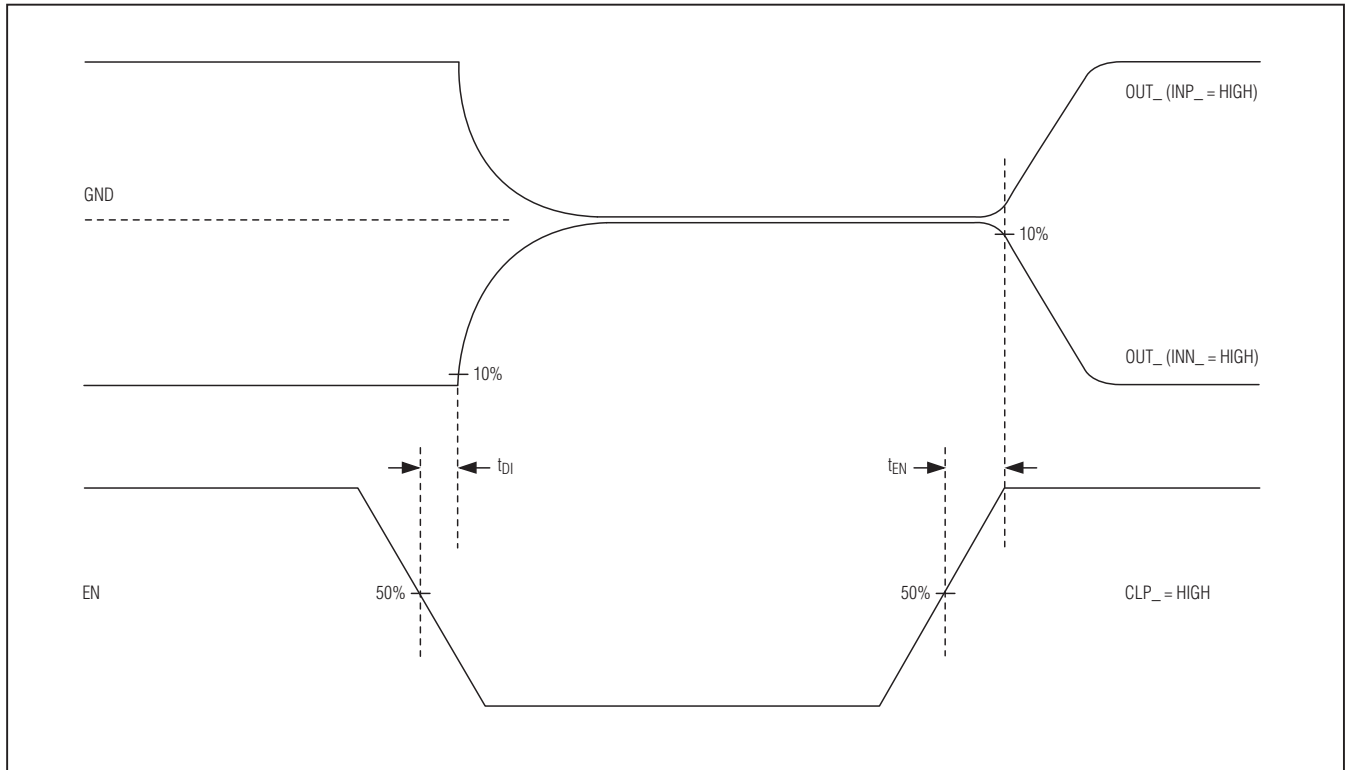


Figure 2. Enable Timing ($R_L = 100\Omega$, $C_L = 100pF$)

MAX4940/MAX4940A

MAX4940/MAX4940A



MAX4940/MAX4940A

MAX4940/MAX4940A

MAX4940/MAX4940A



MAX4940/MAX4940A

Dual/Quad, Unipolar/Bipolar, High-Voltage Digital Pulsers

Typical Application Circuits

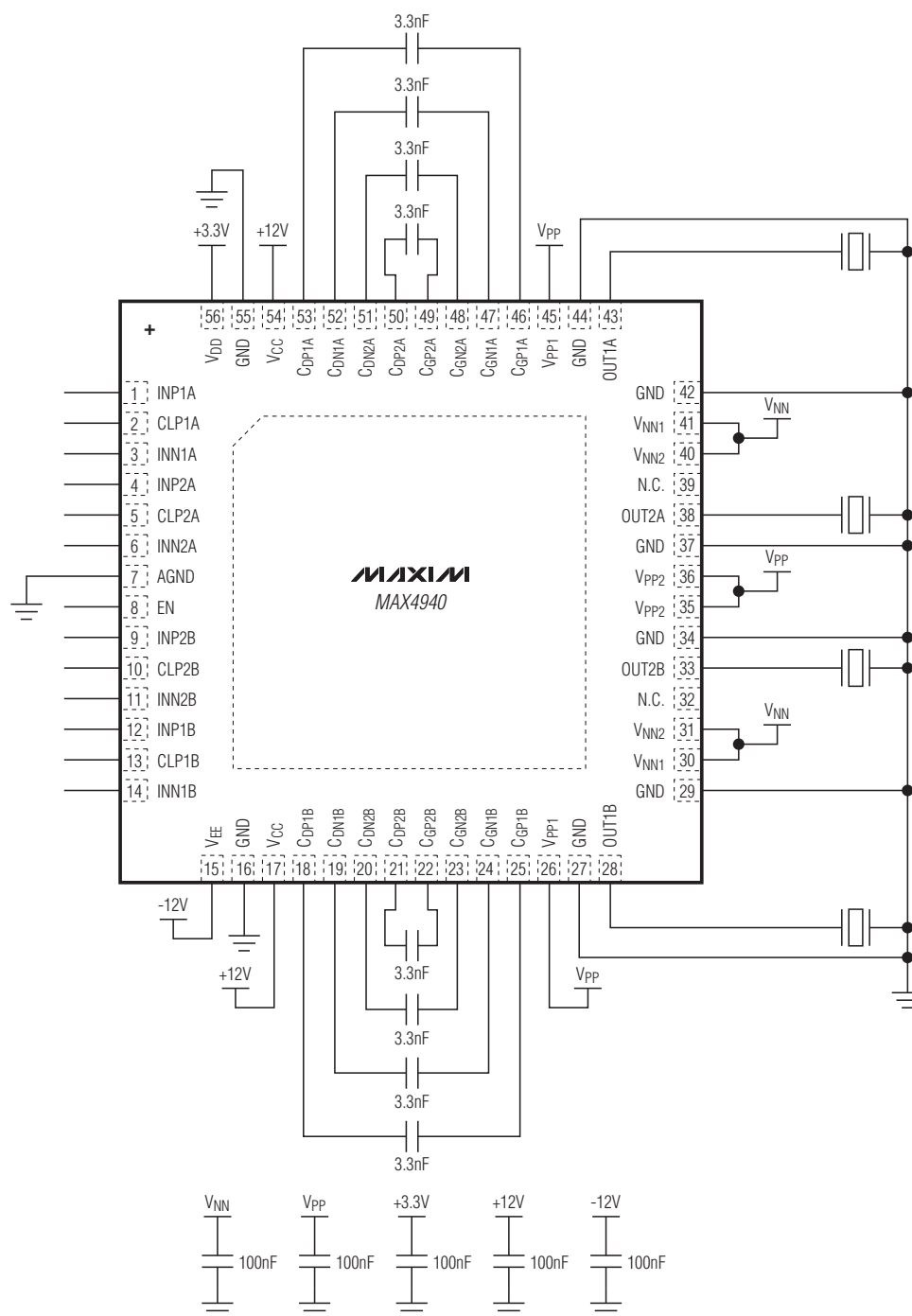


Figure 5. MAX4940 Quad Pulsing with Always-On Active Return-to-Zero

Dual/Quad, Unipolar/Bipolar, High-Voltage Digital Pulsers

Typical Application Circuits (continued)

MAX4940/MAX4940A

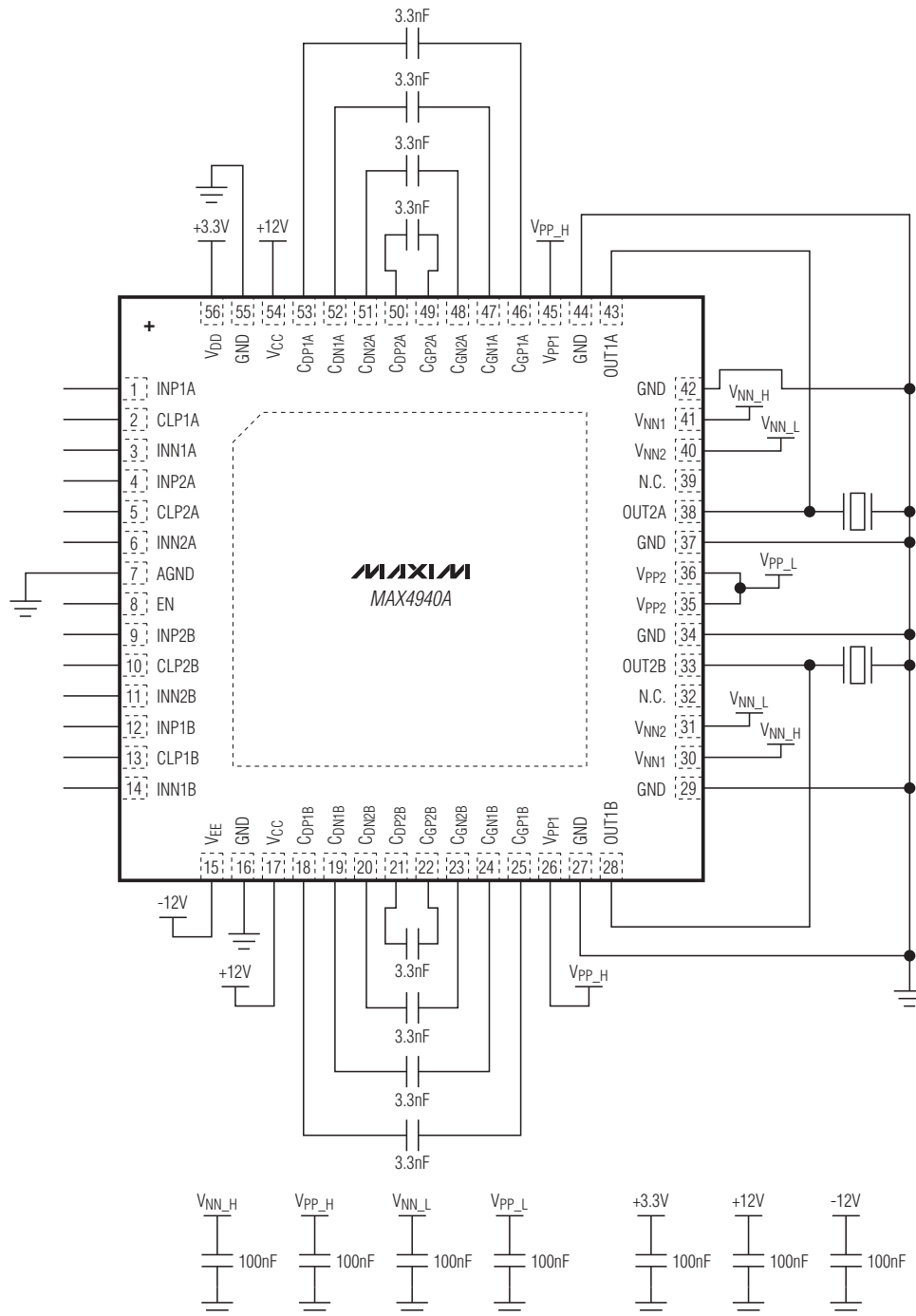


Figure 6. MAX4940A Dual Five-Level Pulsing

Dual/Quad, Unipolar/Bipolar, High-Voltage Digital Pulsers

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
56 TQFN	T5688-3	21-0135

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