# EL5175, EL5375

550MHz Differential Line Receivers

FN7306
Rev 7.00
August 25, 2010

The EL5175 and EL5375 are single and triple high bandwidth amplifiers designed to extract the difference signal from noisy environments. They are primarily targeted for applications such as receiving signals from twisted-pair lines or any application where common mode noise injection is likely to occur.

The EL5175 and EL5375 are stable for a gain of one and requires two external resistors to set the voltage gain for each channel.

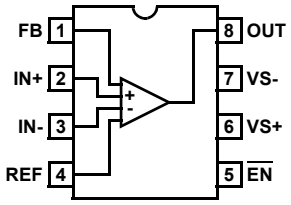
The output common mode level is set by the reference pin ($V_{REF}$), which has a -3dB bandwidth of over 450MHz. Generally, this pin is grounded but it can be tied to any voltage reference.

The output can deliver a maximum of ±60mA and is short circuit protected to withstand a temporary overload condition.

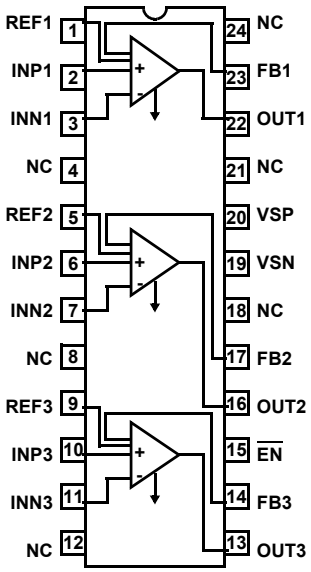
The EL5175 is available in the 8 Ld SOIC and 8 Ld MSOP packages and the EL5375 in the 24 Ld QSOP package. All are specified for operation over the full -40°C to +85°C temperature range.

## Pinouts

**EL5175**
**(8 LD SOIC, MSOP)**
TOP VIEW




**EL5375**
**(24 LD QSOP)**
TOP VIEW




## Features

- Differential input range ±2.3V
- 550MHz 3dB bandwidth
- 900V/µs slew rate
- 60mA maximum output current
- Single 5V or dual ±5V supplies
- Low power, 9.6mA per channel
- Pb-free available (RoHS compliant)

## Applications

- Twisted-pair receivers
- Differential line receivers
- VGA over twisted-pair
- Differential to single-ended amplification
- Reception of analog signals in a noisy environment

## Ordering Information

| PART NUMBER | PART MARKING | PACKAGE | PKG. DWG. # |
|---|---|---|---|
| EL5175IS* | 5175IS | 8 Ld SOIC (150 mil) | MDP0027 |
| EL5175ISZ* (Note) | 5175ISZ | 8 Ld SOIC (Pb-free) (150 mil) | MDP0027 |
| EL5175IY* | 5 | 8 Ld MSOP (3.0mm) | MDP0043 |
| EL5175IYZ* (Note) | BAAAB | 8 Ld MSOP (Pb-free) (3.0mm) | MDP0043 |
| EL5375IU* | EL5375IU | 24 Ld QSOP (150 mil) | MDP0040 |
| EL5375IUZ* (Note) | EL5375IUZ | 24 Ld QSOP (Pb-free) (150 mil) | MDP0040 |

*Add “-T7” or “-T13” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

## Absolute Maximum Ratings ($T_A$ = +25°C)

Supply Voltage ($V_S$+ to $V_S$-) . . . . . .12V
Supply Voltage Rate-of-rise (dV/dT) . . . . . 1V/µs
Input Voltage (IN+, IN- to $V_S$+, $V_S$-). . . . . $V_S$- - 0.3V to $V_S$+ + 0.3V
Differential Input Voltage (IN+ to IN-). . . . . ±4.8V
Maximum Output Current. . . . . ±60mA

## Thermal Information

Operating Junction Temperature . . . . . +135°C
Ambient Operating Temperature . . . . . -40°C to +85°C
Storage Temperature Range . . . . . -65°C to +150°C
Power Dissipation . . . . . See Curves
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

*IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$*

## Electrical Specifications

$V_S$+ = +5V, $V_S$- = -5V, $T_A$ = +25°C, $V_{IN}$ = 0V, $R_L$ = 500Ω, $R_F$ = 0, $R_G$ = OPEN, $C_L$ = 2.7pF, Unless Otherwise Specified.

| PARAMETER | DESCRIPTION | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **AC PERFORMANCE** | | | | | | |
| BW | -3dB Bandwidth | $A_V$ = 1, $C_L$ = 2.7pF | | 550 | | MHz |
| | | $A_V$ = 2, $R_F$ = 806, $C_L$ = 2.7pF | | 190 | | MHz |
| | | $A_V$ = 10, $R_F$ = 806, $C_L$ = 2.7pF | | 20 | | MHz |
| BW | ± 0.1dB Bandwidth | $A_V$ = 1, $C_L$ = 2.7pF | | 60 | | MHz |
| SR | Slew Rate | $V_{OUT}$ = 3$V_{P-P}$, 20% to 80%, $R_L$ = 100Ω | | 600 | | V/µs |
| | | $V_{OUT}$ = 3$V_{P-P}$, 20% to 80%, $R_L$ = 500Ω | | 900 | | V/µs |
| $t_{STL}$ | Settling Time to 0.1% | $V_{OUT}$ = 2$V_{P-P}$ | | 10 | | ns |
| $t_{OVR}$ | Output Overdrive Recovery Time | | | 20 | | ns |
| GBWP | Gain Bandwidth Product | | | 200 | | MHz |
| $V_{REF}$BW (-3dB) | $V_{REF}$ -3dB Bandwidth | $A_V$ = 1, $C_L$ = 2.7pF | | 450 | | MHz |
| $V_{REF}$SR | $V_{REF}$ Slew Rate | $V_{OUT}$ = 2$V_{P-P}$, 20% to 80% | | 1000 | | V/µs |
| $V_N$ | Input Voltage Noise | At f = 10kHz | | 21 | | nV/√Hz |
| $I_N$ | Input Current Noise | At f = 10kHz | | 2.7 | | pA/√Hz |
| HD2 | Second Harmonic Distortion | $V_{OUT}$ = 1$V_{P-P}$, 5MHz | | -70 | | dBc |
| HD2 | Second Harmonic Distortion | $V_{OUT}$ = 1$V_{P-P}$, 5MHz | | -66 | | dBc |
| HD3 | Third Harmonic Distortion | $V_{OUT}$ = 1$V_{P-P}$, 5MHz | | -94 | | dBc |
| HD3 | Third Harmonic Distortion | $V_{OUT}$ = 1$V_{P-P}$, 5MHz | | -84 | | dBc |
| dG | Differential Gain at 3.58MHz | $R_L$ = 150Ω , $A_V$ = 2 | | 0.1 | | % |
| dθ | Differential Phase at 3.58MHz | $R_L$ = 150Ω , $A_V$ = 2 | | 0.1 | | ° |
| $e_S$ | Channel Separation (EL5375) | At f = 100kHz | | 90 | | dB |
| **INPUT CHARACTERISTICS** | | | | | | |
| $V_{OS}$ | Input Referred Offset Voltage | EL5175 | | -3 | ±40 | mV |
| | | EL5375 | | -3 | ±30 | mV |
| $I_{IN}$ | Input Bias Current ($V_{IN}$, $V_{INB}$, $V_{REF}$) | | -25 | -12.5 | -6 | µA |
| $R_{IN}$ | Differential Input Resistance | | | 150 | | kΩ |
| $C_{IN}$ | Differential Input Capacitance | | | 1 | | pF |
| DMIR | Differential Mode Input Range | | ±2.1 | ±2.3 | ±2.5 | V |
| CMIR | Common Mode Input Range at $V_{IN}$+, $V_{IN}$- | | -4.3 | | +3.3 | V |

**Electrical Specifications** $V_S+ = +5V$, $V_S- = -5V$, $T_A = +25°C$, $V_{IN} = 0V$, $R_L = 500\Omega$, $R_F = 0$, $R_G$ = OPEN, $C_L = 2.7pF$, Unless Otherwise Specified. **(Continued)**

| PARAMETER | DESCRIPTION | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{REFIN}+$ | Reference Input - Positive | $V_{IN}+ = V_{IN}- = 0V$ | 3.3 | 3.5 | | V |
| $V_{REFIN}-$ | Reference Input - Negative | $V_{IN}+ = V_{IN}- = 0V$ | | -3.9 | -3.6 | V |
| CMRR | Input Common Mode Rejection Ratio | $V_{IN} = \pm2.5V$ | 75 | 95 | | dB |
| Gain | Gain Accuracy | EL5175, $V_{IN} = 1V$ | 0.979 | 0.994 | 1.009 | V |
| | | EL5375, $V_{IN} = 1V$ | 0.977 | 0.992 | 1.007 | V |
| **OUTPUT CHARACTERISTICS** | | | | | | |
| $V_{OUT}$ | Positive Output Voltage Swing | $R_L = 500\Omega$ to GND | 3.3 | 3.54 | | V |
| | Negative Output Voltage Swing | $R_L = 500\Omega$ to GND | | -3.95 | -3.6 | V |
| $I_{OUT}$(Max) | Maximum Output Current | $R_L = 10\Omega$ | ±40 | ±67 | | mA |
| $R_{OUT}$ | Output Impedance | | | 130 | | mΩ |
| **SUPPLY** | | | | | | |
| $V_{SUPPLY}$ | Supply Operating Range | $V_S+$ to $V_S-$ | 4.75 | | 11 | V |
| $I_{S\ (ON)}$ | Power Supply Current Per Channel - Enabled | | 8 | 9.6 | 11 | mA |
| $I_{S\ (OFF)}+$ | Positive Power Supply Current - Disabled | $\overline{EN}$ pin tied to 4.8V, EL5175 | | 80 | 100 | µA |
| | | $\overline{EN}$ pin tied to 4.8V, EL5375 | | 1.7 | 5 | µA |
| $I_{S\ (OFF)}-$ | Negative Power Supply Current - Disabled | | -150 | -120 | -90 | µA |
| PSRR | Power Supply Rejection Ratio | $V_S$ from ±4.5V to ±5.5V | 45 | 56 | | dB |
| **ENABLE** | | | | | | |
| $t_{EN}$ | Enable Time | | | 80 | | ns |
| $t_{DS}$ | Disable Time | | | 1.2 | | µs |
| $V_{IH}$ | $\overline{EN}$ Pin Voltage for Power-up | | | | $V_S+ - 1.5$ | V |
| $V_{IL}$ | $\overline{EN}$ Pin Voltage for Shutdown | | $V_S+ - 0.5$ | | | V |
| $I_{IH-EN}$ | $\overline{EN}$ Pin Input Current High Per Channel | At $V_{EN} = 5V$ | | 40 | 60 | µA |
| $I_{IL-EN}$ | $\overline{EN}$ Pin Input Current Low Per Channel | At $V_{EN} = 0V$ | -10 | -3 | | µA |

## Pin Descriptions

| EL5175 | EL5375 | PIN NAME | PIN FUNCTION |
|---|---|---|---|
| 1 | | FB | Feedback input |
| 2 | | IN+ | Non-inverting input |
| 3 | | IN- | Inverting input |
| 4 | | REF | Sets the common mode output voltage level to $V_{REF}$ |
| 5 | | $\overline{EN}$ | Enabled when this pin is floating or the applied voltage $\leq V_S+ - 1.5$ |
| 6 | | VS+ | Positive supply voltage |
| 7 | | VS- | Negative supply voltage |
| 8 | | OUT | Output voltage |
| | 1, 5, 9 | REF1, REF2, REF3 | Reference input, controls common-mode output voltage |
| | 2, 6, 10 | INP1, INP2, INP3 | Non-inverting inputs |
| | 3, 7, 11 | INN1, INN2, INN3 | Inverting inputs |
| | 4, 8, 12, 18, 21, 24 | NC | No connect, grounded for best crosstalk performance |
| | 22, 16, 13 | OUT1, OUT2, OUT3 | Non-inverting outputs |
| | 23, 17, 14 | FB1, FB2, FB3 | Feedback from outputs |
| | 15 | $\overline{EN}$ | Enabled when this pin is floating or the applied voltage $\leq V_S+ - 1.5$ |
| | 19 | VSN | Negative supply |
| | 20 | VSP | Positive supply |

## Connection Diagrams

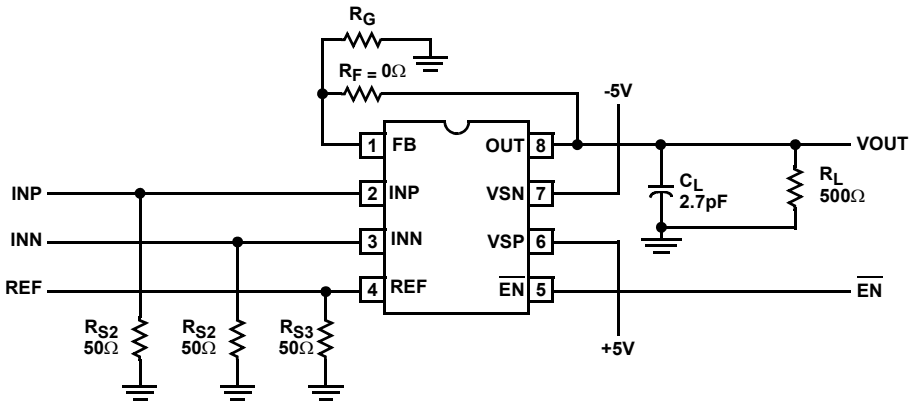



FIGURE 1. EL5175

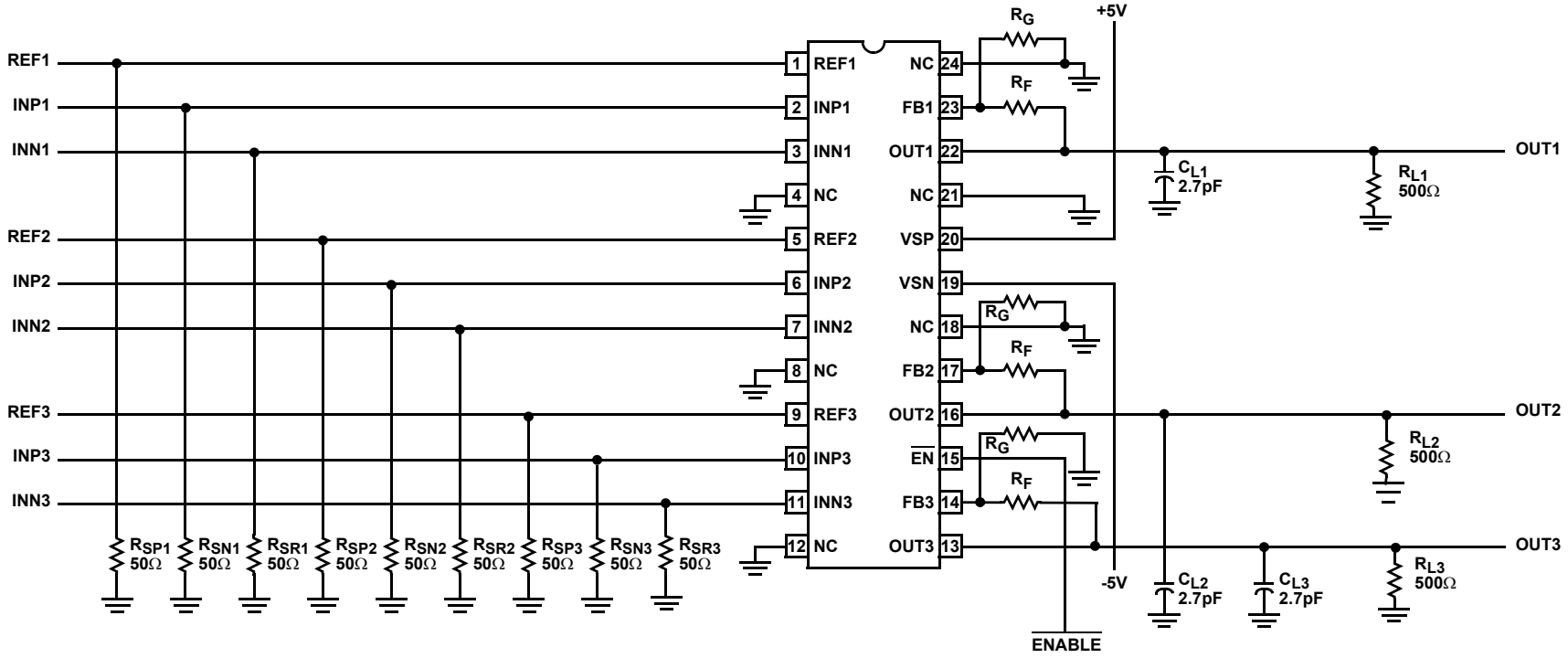



FIGURE 2. EL5375

## *Typical Performance Curves*

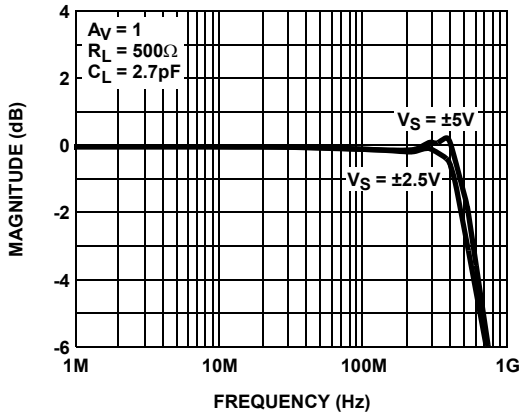



FIGURE 3. FREQUENCY RESPONSE vs SUPPLY VOLTAGE

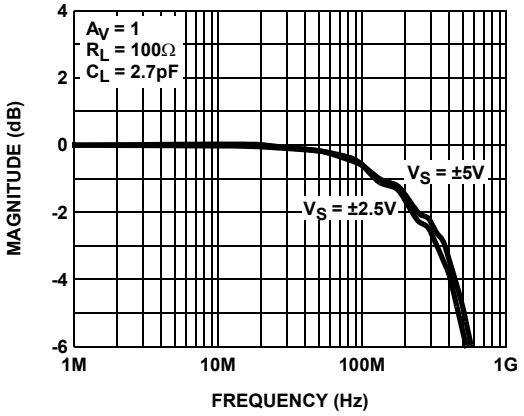



FIGURE 4. FREQUENCY RESPONSE vs SUPPLY VOLTAGE

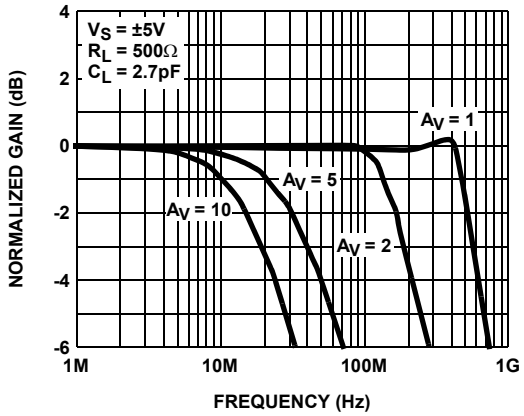



FIGURE 5. FREQUENCY RESPONSE vs VARIOUS GAIN

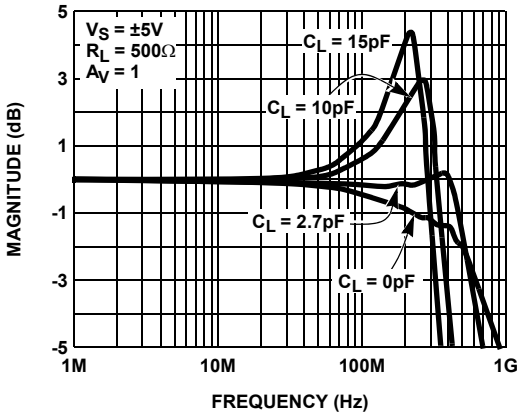



FIGURE 6. FREQUENCY RESPONSE vs $C_L$

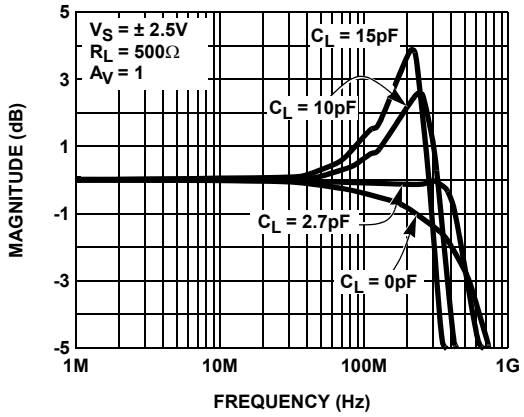



FIGURE 7. FREQUENCY RESPONSE vs $C_L$

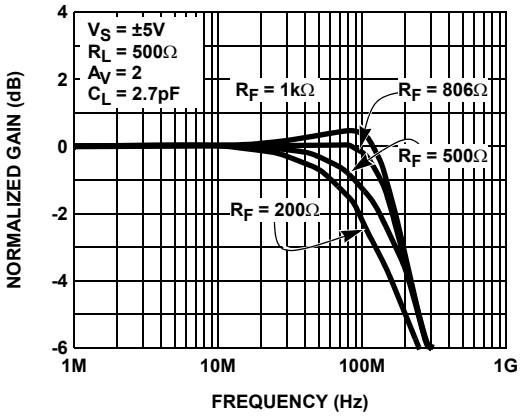



FIGURE 8. FREQUENCY RESPONSE FOR VARIOUS $R_F$

## *Typical Performance Curves* (Continued)

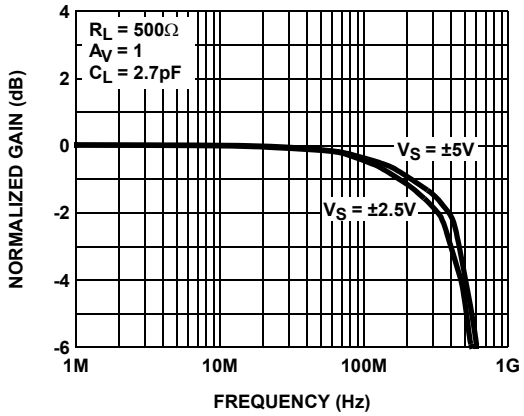



FIGURE 9. FREQUENCY RESPONSE FOR $V_{REF}$

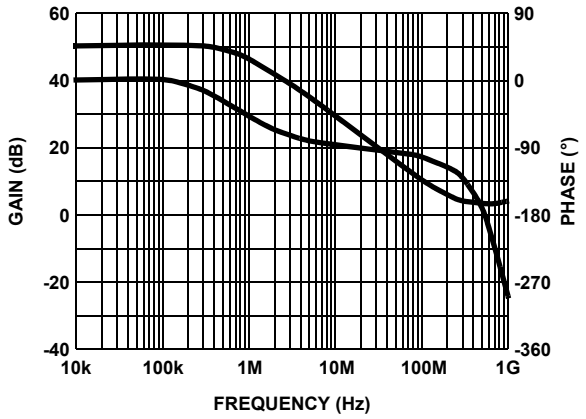



FIGURE 10. OPEN LOOP GAIN

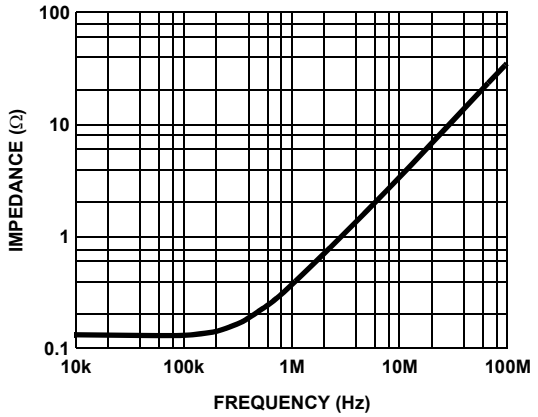



FIGURE 11. OUTPUT IMPEDANCE vs FREQUENCY

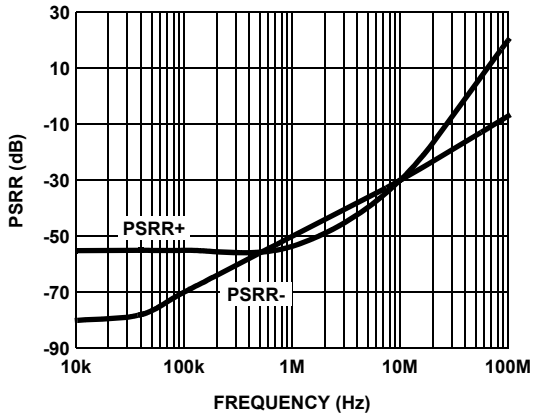



FIGURE 12. PSRR vs FREQUENCY

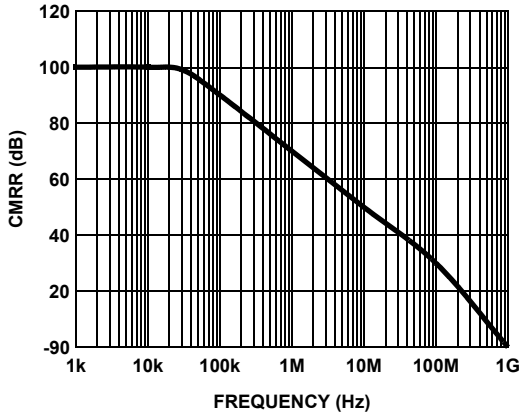



FIGURE 13. CMRR vs FREQUENCY

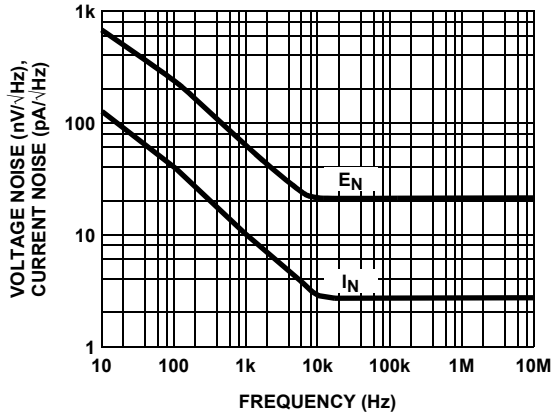



FIGURE 14. VOLTAGE AND CURRENT NOISE vs FREQUENCY

## *Typical Performance Curves* (Continued)

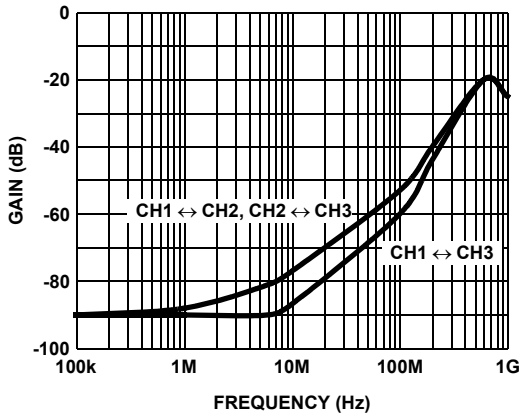



FIGURE 15. CHANNEL ISOLATION vs FREQUENCY (EL5375 ONLY)

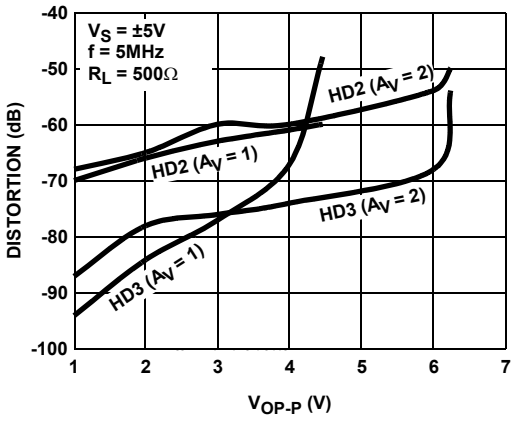



FIGURE 16. HARMONIC DISTORTION vs OUTPUT VOLTAGE

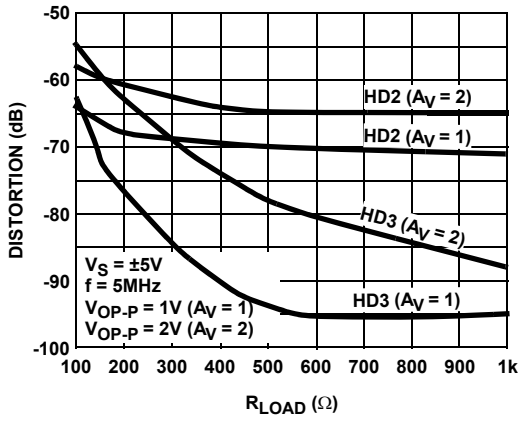



FIGURE 17. HARMONIC DISTORTION vs LOAD RESISTANCE

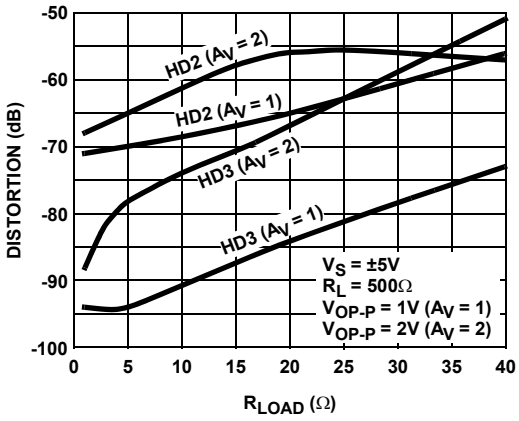



FIGURE 18. HARMONIC DISTORTION vs FREQUENCY

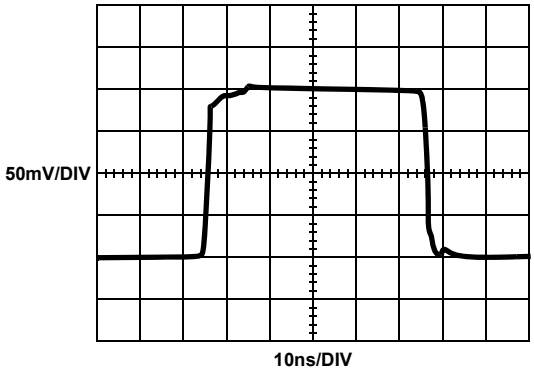



FIGURE 19. SMALL SIGNAL TRANSIENT RESPONSE

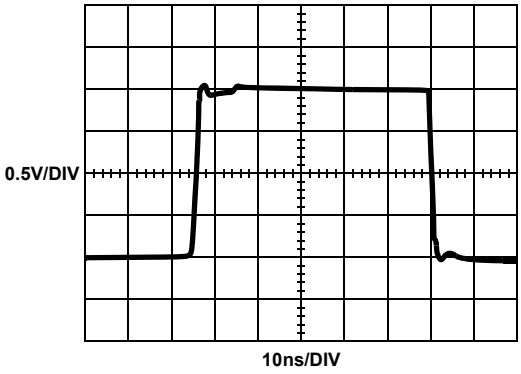



FIGURE 20. LARGE SIGNAL TRANSIENT RESPONSE

## *Typical Performance Curves* (Continued)

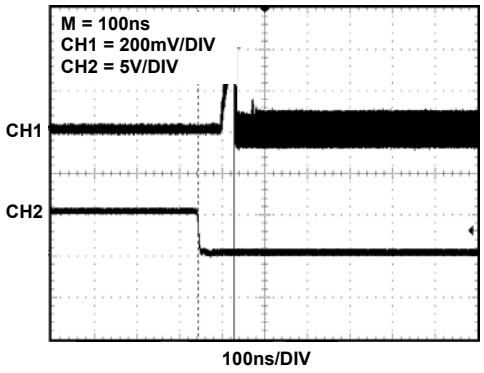



FIGURE 21. ENABLED RESPONSE

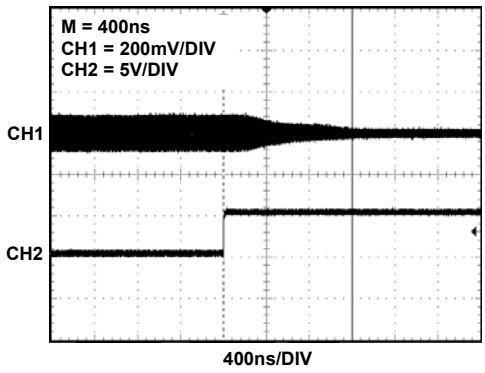



FIGURE 22. DISABLED RESPONSE

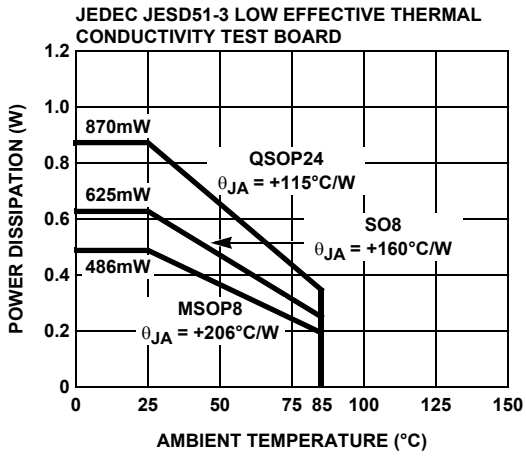



FIGURE 23. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

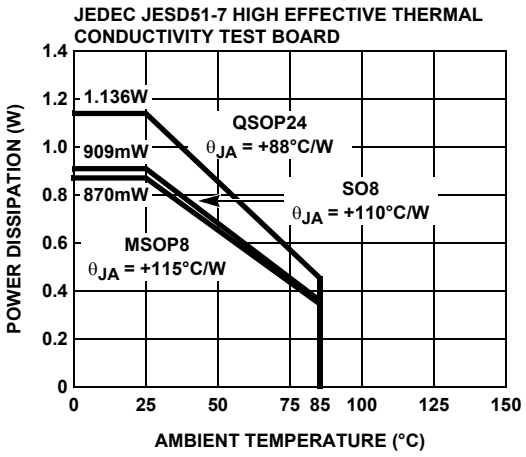
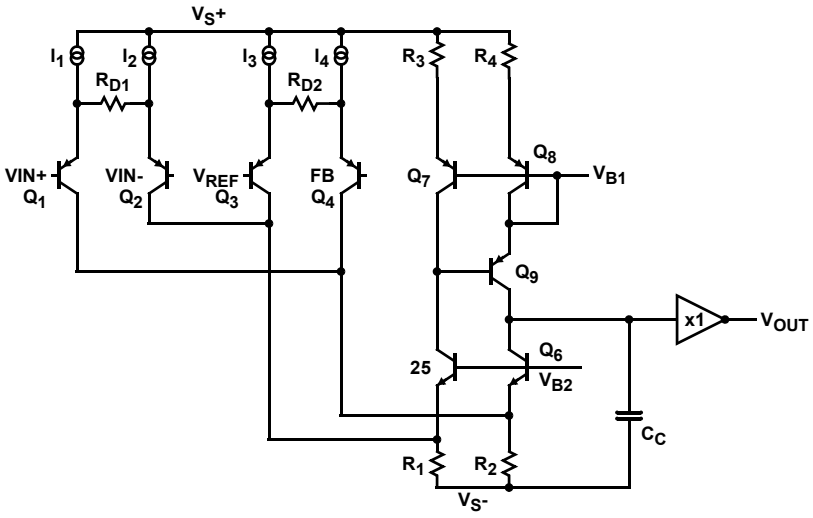



FIGURE 24. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

## *Simplified Schematic*



## Description of Operation and Application Information

### Product Description

The EL5175 and EL5375 are wide bandwidth, low power and single/differential ended to single-ended output amplifiers. The EL5175 is a single channel differential to single-ended amplifier. The EL5375 is a triple channel differential to single ended amplifier. The EL5175 and EL5375 are internally compensated for closed loop gain of +1 orgreater. Connected in gain of 1 and driving a 500Ω load, the EL5175 and EL5375 have a -3dB bandwidth of 550MHz. Driving a 150Ω load at gain of 2, the bandwidth is about 130MHz. The bandwidth at the REF input is about 450MHz. The EL5175 and EL5375 is available with a power-down feature to reduce the power while the amplifier is disabled.

### Input, Output and Supply Voltage Range

The EL5175 and EL5375 have been designed to operate with a single supply voltage of 5V to 10V or a split supplies with its total voltage from 5V to 10V. The amplifiers have an input common mode voltage range from -4.3V to 3.3V for ±5V supply. The differential mode input range (DMIR) between the two inputs is approximately -2.3V to +2.3V. The input voltage range at the REF pin is from -3.6V to 3.3V. If the input common mode or differential mode signal is outside the above-specified ranges, it will cause the output signal to become distorted.

The output of the EL5175 and EL5375 can swing from -3.9V to 3.5V at 500Ω load at ±5V supply. As the load resistance becomes lower, the output swing is reduced respectively.

### Overall Gain Settings

The gain setting for the EL5175 and EL5375 is similar to the conventional operational amplifier. The output voltage is equal to the difference of the inputs plus $V_{REF}$ and then times the gain.

$$V_O = (V_{IN}+ - V_{IN}- + V_{REF}) \times \left(1 + \frac{R_F}{R_G}\right) \quad \text{(EQ. 1)}$$

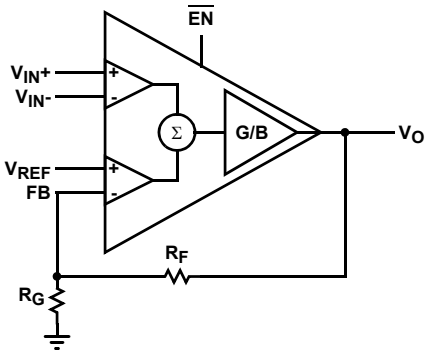



**FIGURE 25.**

### Choice of Feedback Resistor and Gain Bandwidth Product

For applications that require a gain of +1, no feedback resistor is required. Just short the OUT+ pin to FBP pin and OUT- pin to FBN pin. For gains greater than +1, the feedback resistor forms a pole with the parasitic capacitance at the inverting input. As this pole becomes smaller, the amplifier's phase margin is reduced. This causes ringing in the time domain and peaking in the frequency domain. Therefore, $R_F$ has some maximum value that should not be exceeded for optimum performance. If a large value of $R_F$ must be used, a small capacitor in the few Pico farad range in parallel with $R_F$ can help to reduce the ringing and peaking at the expense of reducing the bandwidth.

The bandwidth of the EL5175 and EL5375 depends on the load and the feedback network. $R_F$ and $R_G$ appear in parallel with the load for gains other than +1. As this combination gets smaller, the bandwidth falls off. Consequently, $R_F$ also has a minimum value that should not be exceeded for optimum bandwidth performance. For gain of +1, $R_F$ = 0 is optimum. For the gains other than +1, optimum response is obtained with $R_F$ between 500Ω to 1kΩ. For $A_V$ = 2 and $R_F = R_G$ = 806Ω, the BW is about 190MHz and the frequency response is very flat.

The EL5175 and EL5375 have a gain bandwidth product of 200MHz. For gains ≥5, its bandwidth can be predicted by using Equation 2:

$$\text{Gain} \times \text{BW} = 200\text{MHz} \quad \text{(EQ. 2)}$$

### Driving Capacitive Loads and Cables

The EL5175 and EL5375 can drive 15pF capacitance in parallel with 500Ω load to ground with less than 4.5dB of peaking at a gain of +1. If less peaking is desired in applications, a small series resistor (usually between 5Ω to 50Ω) can be placed in series with each output to eliminate most peaking. However, this will reduce the gain slightly. If the gain setting is greater than 1, the gain resistor $R_G$ can then be chosen to make up for any gain loss, which may be created by the additional series resistor at the output.

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, a back-termination series resistor at the amplifier's output will isolate the amplifier from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. Again, a small series resistor at the output can help to reduce peaking.

### Disable/Power-Down

The EL5175 and EL5375 can be disabled and its outputs placed in a high impedance state. The turn-off time is about 1.2µs and the turn-on time is about 80ns. When disabled, the amplifier's supply current is reduced to 80µA for $I_S$+ and 120µA for $I_S$- typically, thereby effectively eliminating the

power consumption. The amplifier's power-down can be controlled by standard CMOS signal levels at the ENABLE pin. The applied logic signal is relative to the $V_S$+ pin. Letting the $\overline{EN}$ pin float or applying a signal that is less than 1.5V below $V_S$+ will enable the amplifier. The amplifier will be disabled when the signal at the $\overline{EN}$ pin is above $V_S$+ - 0.5V. If a TTL signal is used to control the enabled/disabled function, Figure 26 could be used to convert the TTL signal to CMOS signal.

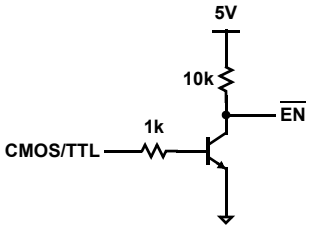



**FIGURE 26. CONVERSION OF TTL SIGNAL TO CMOS SIGNAL**

### *Output Drive Capability*

The EL5175 and EL5375 have internal short circuit protection. Its typical short circuit current is ±67mA. If the output is shorted indefinitely, the power dissipation could easily increase such that the part will be destroyed. Maximum reliability is maintained if the output current never exceeds ±60mA. This limit is set by the design of the internal metal interconnections.

### *Power Dissipation*

With the high output drive capability of the EL5175 and EL5375, it is possible to exceed the +135°C absolute maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if the load conditions or package types need to be modified for the amplifier to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to Equation 3:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}} \quad \text{(EQ. 3)}$$

- $T_{JMAX}$ = Maximum junction temperature
- $T_{AMAX}$ = Maximum ambient temperature
- $\theta_{JA}$ = Thermal resistance of the package

Assume the REF pin is tired to GND for $V_S$ = ±5V application, the maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or:

For sourcing, see Equation 4:

$$PD_{MAX} = \left[V_S \times I_{SMAX} + (V_S+ - V_{OUT}) \times \frac{V_{OUT}}{R_{LOAD}}\right] \times i \quad \text{(EQ. 4)}$$

For sinking, see Equation 5:

$$PD_{MAX} = [V_S \times I_{SMAX} + (V_{OUT} - V_S-) \times I_{LOAD}] \times i \quad \text{(EQ. 5)}$$

Where:

- $V_S$ = Total supply voltage
- $I_{SMAX}$ = Maximum quiescent supply current per channel
- $V_{OUT}$ = Maximum output voltage of the application
- $R_{LOAD}$ = Load resistance
- $I_{LOAD}$ = Load current
- i = Number of channels

By setting the two $PD_{MAX}$ equations equal to each other, we can solve the output current and $R_{LOAD}$ to avoid the device overheat.

### *Power Supply Bypassing and Printed Circuit Board Layout*

As with any high frequency device, a good printed circuit board layout is necessary for optimum performance. Lead lengths should be as short as possible. The power supply pin must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the $V_S$- pin is connected to the ground plane, a single 4.7µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor from $V_S$+ to GND will suffice. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used. In this case, the $V_S$- pin becomes the negative supply rail.

For good AC performance, parasitic capacitance should be kept to a minimum. Use of wire-wound resistors should be avoided because of their additional series inductance. Use of sockets should also be avoided if possible. Sockets add parasitic inductance and capacitance that can result in compromised performance. Minimizing parasitic capacitance at the amplifier's inverting input pin is very important. The feedback resistor should be placed very close to the inverting input pin. Strip line design techniques are recommended for the signal traces.

## Typical Applications

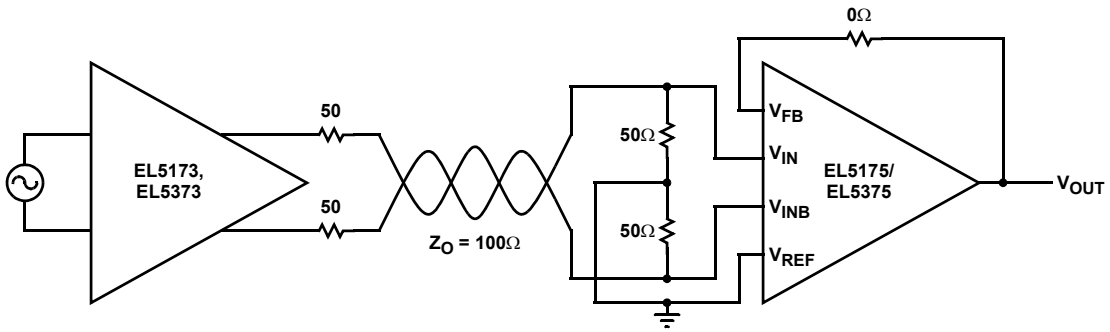



FIGURE 27. TWISTED PAIR CABLE RECEIVER

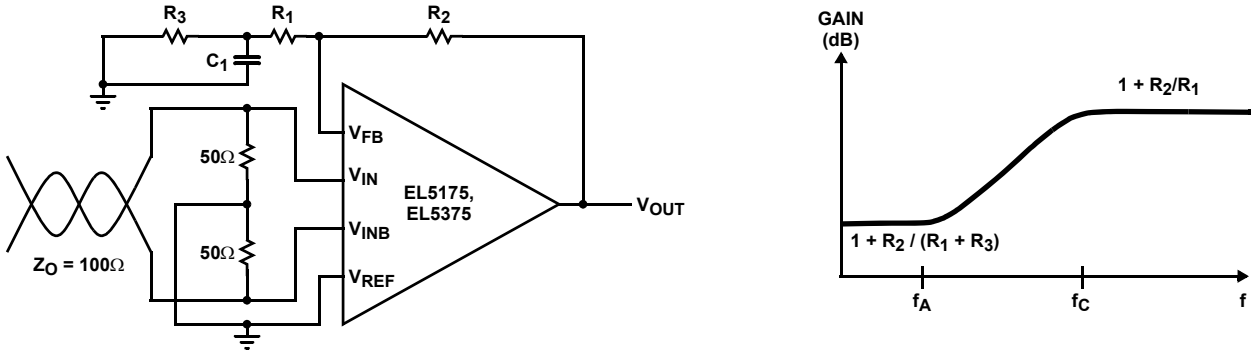



FIGURE 28. COMPENSATED LINE RECEIVER

As the signal is transmitted through a cable, the high frequency signal will be attenuated. One way to compensate this loss is to boost the high frequency gain at the receiver side.

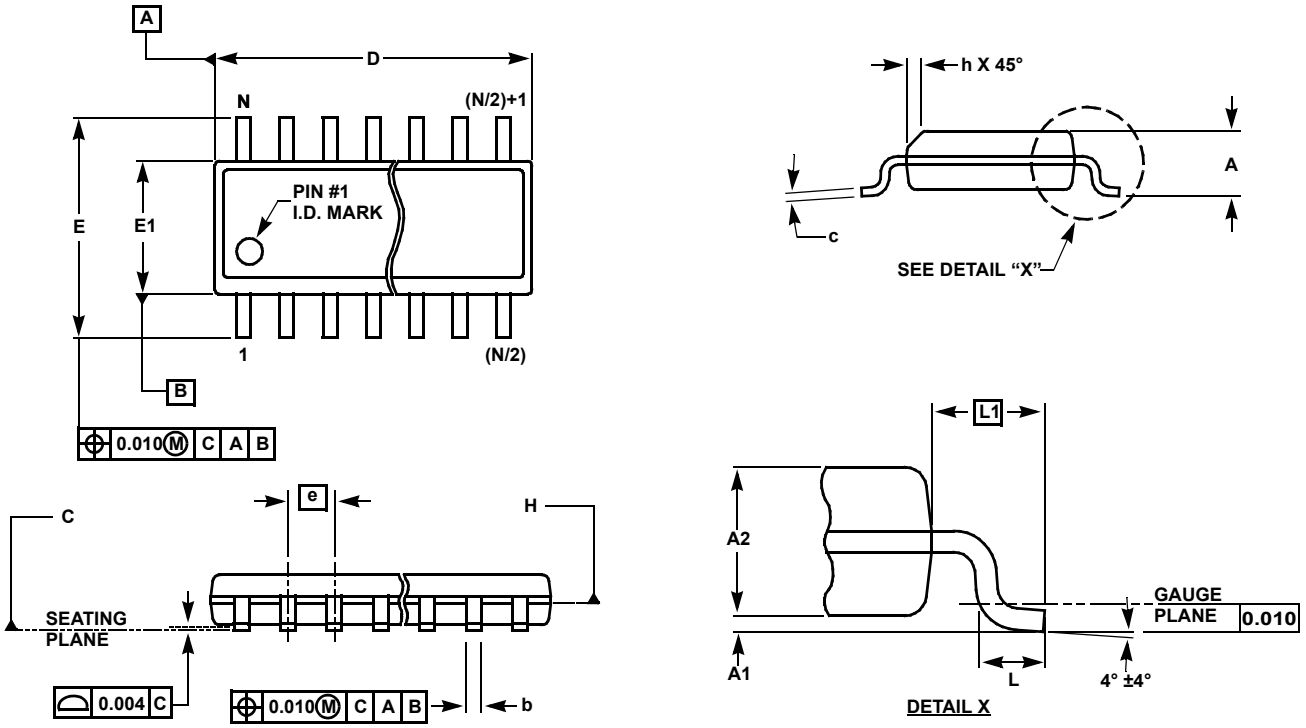
### Level Shifter and Signal Summer

The EL5175 and EL5375 contains two pairs of differential pair input stages. It makes the inputs all high impedance. To take advantage of the two high impedance inputs, the EL5175 and EL5375 can be used as a signal summer to add two signals together. One signal can be applied to $V_{IN}$+; the second signal can be applied to REF and $V_{IN}$- is ground. The output is equal to Equation 6:

$$V_O = (V_{IN}+ + V_{REF}) \times \text{Gain} \quad \text{(EQ. 6)}$$

Also, the EL5175 and EL5375 can be used as a level shifter by applying a level control signal to the REF input.

## *Small Outline Package Family (SO)*




### MDP0027

**SMALL OUTLINE PACKAGE FAMILY (SO)**

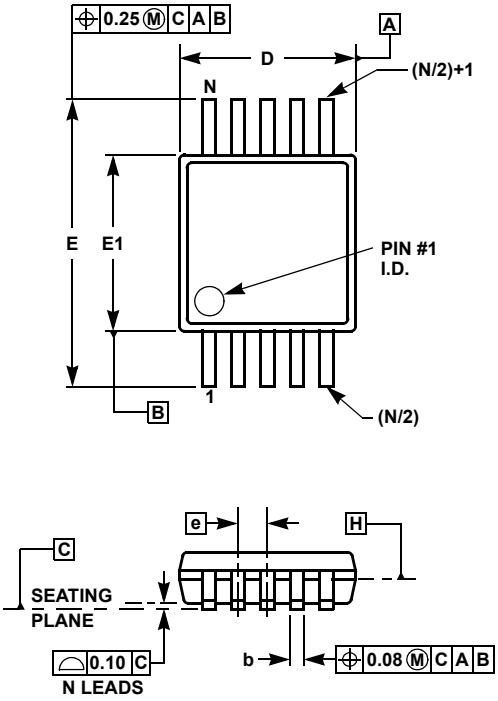
| SYMBOL | INCHES | | | | | | | TOLERANCE | NOTES |
|---|---|---|---|---|---|---|---|---|---|
| | SO-8 | SO-14 | SO16 (0.150") | SO16 (0.300") (SOL-16) | SO20 (SOL-20) | SO24 (SOL-24) | SO28 (SOL-28) | | |
| A | 0.068 | 0.068 | 0.068 | 0.104 | 0.104 | 0.104 | 0.104 | MAX | - |
| A1 | 0.006 | 0.006 | 0.006 | 0.007 | 0.007 | 0.007 | 0.007 | ±0.003 | - |
| A2 | 0.057 | 0.057 | 0.057 | 0.092 | 0.092 | 0.092 | 0.092 | ±0.002 | - |
| b | 0.017 | 0.017 | 0.017 | 0.017 | 0.017 | 0.017 | 0.017 | ±0.003 | - |
| c | 0.009 | 0.009 | 0.009 | 0.011 | 0.011 | 0.011 | 0.011 | ±0.001 | - |
| D | 0.193 | 0.341 | 0.390 | 0.406 | 0.504 | 0.606 | 0.704 | ±0.004 | 1, 3 |
| E | 0.236 | 0.236 | 0.236 | 0.406 | 0.406 | 0.406 | 0.406 | ±0.008 | - |
| E1 | 0.154 | 0.154 | 0.154 | 0.295 | 0.295 | 0.295 | 0.295 | ±0.004 | 2, 3 |
| e | 0.050 | 0.050 | 0.050 | 0.050 | 0.050 | 0.050 | 0.050 | Basic | - |
| L | 0.025 | 0.025 | 0.025 | 0.030 | 0.030 | 0.030 | 0.030 | ±0.009 | - |
| L1 | 0.041 | 0.041 | 0.041 | 0.056 | 0.056 | 0.056 | 0.056 | Basic | - |
| h | 0.013 | 0.013 | 0.013 | 0.020 | 0.020 | 0.020 | 0.020 | Reference | - |
| N | 8 | 14 | 16 | 16 | 20 | 24 | 28 | Reference | - |

Rev. M 2/07

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

## *Mini SO Package Family (MSOP)*




### MDP0043

**MINI SO PACKAGE FAMILY**

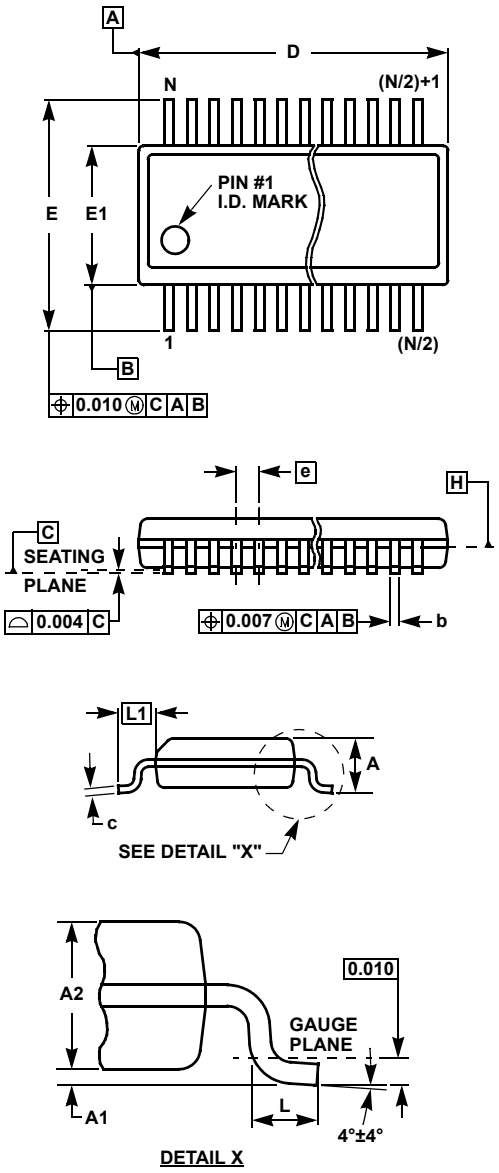
| SYMBOL | MILLIMETERS | | TOLERANCE | NOTES |
|---|---|---|---|---|
| | MSOP8 | MSOP10 | | |
| A | 1.10 | 1.10 | Max. | - |
| A1 | 0.10 | 0.10 | ±0.05 | - |
| A2 | 0.86 | 0.86 | ±0.09 | - |
| b | 0.33 | 0.23 | +0.07/-0.08 | - |
| c | 0.18 | 0.18 | ±0.05 | - |
| D | 3.00 | 3.00 | ±0.10 | 1, 3 |
| E | 4.90 | 4.90 | ±0.15 | - |
| E1 | 3.00 | 3.00 | ±0.10 | 2, 3 |
| e | 0.65 | 0.50 | Basic | - |
| L | 0.55 | 0.55 | ±0.15 | - |
| L1 | 0.95 | 0.95 | Basic | - |
| N | 8 | 10 | Reference | - |

Rev. D 2/07

NOTES:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

## *Quarter Size Outline Plastic Packages Family (QSOP)*




### MDP0040

**QUARTER SIZE OUTLINE PLASTIC PACKAGES FAMILY**

| SYMBOL | INCHES | | | TOLERANCE | NOTES |
|---|---|---|---|---|---|
| | QSOP16 | QSOP24 | QSOP28 | | |
| A | 0.068 | 0.068 | 0.068 | Max. | - |
| A1 | 0.006 | 0.006 | 0.006 | ±0.002 | - |
| A2 | 0.056 | 0.056 | 0.056 | ±0.004 | - |
| b | 0.010 | 0.010 | 0.010 | ±0.002 | - |
| c | 0.008 | 0.008 | 0.008 | ±0.001 | - |
| D | 0.193 | 0.341 | 0.390 | ±0.004 | 1, 3 |
| E | 0.236 | 0.236 | 0.236 | ±0.008 | - |
| E1 | 0.154 | 0.154 | 0.154 | ±0.004 | 2, 3 |
| e | 0.025 | 0.025 | 0.025 | Basic | - |
| L | 0.025 | 0.025 | 0.025 | ±0.009 | - |
| L1 | 0.041 | 0.041 | 0.041 | Basic | - |
| N | 16 | 24 | 28 | Reference | - |

Rev. F 2/07

NOTES:

1. Plastic or metal protrusions of 0.006” maximum per side are not included.
2. Plastic interlead protrusions of 0.010” maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

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