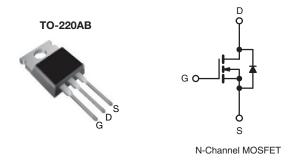
COMPLIANT HALOGEN

FREE



E Series Power MOSFET

PRODUCT SUMMARY				
V _{DS} (V) at T _J max.	550			
R _{DS(on)} max. at 25 °C (Ω)	V _{GS} = 10 V	0.380		
Q _g max. (nC)	50			
Q _{gs} (nC)	6			
Q _{gd} (nC)	10			
Configuration	Single			



FEATURES

- Low figure-of-merit (FOM) Ron x Qq
- Low input capacitance (Ciss)
- · Reduced switching and conduction losses
- Low gate charge (Q_q)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see <u>www.vishav.com/doc?99912</u>

APPLICATIONS

- Computing
 - PC silver box / ATX power supplies
- Lighting
 - Two stage LED lighting
- Consumer electronics
- · Applications using hard switched topologies
 - Power factor correction (PFC)
 - Two switch forward converter
 - Flyback converter
- Switch mode power supplies (SMPS)

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free and Halogen-free	SiHP12N50E-GE3

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)						
PARAMETER		SYMBOL	LIMIT	UNIT		
Drain-Source Voltage	V_{DS}	500	V			
Gate-Source Voltage	V _{GS}	± 20				
Gate-Source Voltage AC (f > 1 Hz)		30				
Continuous Drain Current (T _J = 150 °C)	V_{GS} at 10 V $T_{C} = 25 ^{\circ}C$ $T_{C} = 100 ^{\circ}C$	I-	10.5	А		
	V_{GS} at 10 V $T_C = 100 ^{\circ}C$	I _D	6.6			
Pulsed Drain Current ^a	I _{DM}	21				
Linear Derating Factor		0.91	W/°C			
Single Pulse Avalanche Energy b	E _{AS}	103	mJ			
Maximum Power Dissipation	P_{D}	114	W			
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to +150	°C		
Drain-Source Voltage Slope	$V_{DS} = 0 \text{ V to } 80 \text{ % } V_{DS}$	dV/dt 70		V/ns		
Reverse Diode dV/dt ^d		uv/ut	27	V/115		
Soldering Recommendations (Peak Temperature) ^c	for 10 s		300	°C		

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature.
- b. V_{DD} = 50 V, starting T_J = 25 °C, L = 28.2 mH, R_q = 25 Ω , I_{AS} = 2.7 A.
- c. 1.6 mm from case.
- d. $I_{SD} \le I_D$, dI/dt = 100 A/ μ s, starting $T_J = 25$ °C.

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.1	C/ VV	



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PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static				•	•	•	
Drain-Source Breakdown Voltage	V_{DS}	V _{GS} = 0 V, I _D = 250 μA		500	-	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference to 25 °C, I _D = 1 mA		-	0.60	-	V/°C
Gate-Source Threshold Voltage (N)	V _{GS(th)}	V _{DS} =	= V _{GS} , I _D = 250 μA	2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 500 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = 400 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 125 \text{ °C}$		-	-	1 10	μΑ
Drain-Source On-State Resistance	R _{DS(on)}	$V_{DS} = 400 \text{ V}$ $V_{GS} = 10 \text{ V}$	$I_D = 6 \text{ A}$	_	0.330	0.380	Ω
Forward Transconductance			$I_D = 0.7$ $I_D = 0.7$	_	3.1	0.000	S
Dynamic	9 _{fs}	V DS	; = 00 V, ID = 0 A		0.1		
Input Capacitance	C _{iss}			_	886	T _	I
Output Capacitance	C _{oss}	-	$V_{GS} = 0 \text{ V},$ $V_{DS} = 100 \text{ V},$		52	_	
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		-	6	_	pF
Effective Output Capacitance, Energy Related ^a	C _{o(er)}	V _{DS} = 0 V to 400 V, V _{GS} = 0 V		-	45	-	
Effective Output Capacitance, Time Related ^b	C _{o(tr)}			-	131	-	
Total Gate Charge	Qg			-	25	50	
Gate-Source Charge	Q _{gs}	V _{GS} = 10 V	$V_{GS} = 10 \text{ V}$ $I_D = 6 \text{ A}, V_{DS} = 400 \text{ V}$	-	6	-	nC
Gate-Drain Charge	Q _{gd}				10	-	1
Turn-On Delay Time	t _{d(on)}		1		13	26	- ns
Rise Time	t _r	$V_{DD} = 400 \text{ V}, I_D = 6 \text{ A},$		-	16	32	
Turn-Off Delay Time	t _{d(off)}	V _{GS} :	$V_{DD} = 400 \text{ V}, I_D = 6 \text{ A},$ $V_{GS} = 10 \text{ V}, R_a = 9.1 \Omega$		29	58	
Fall Time	t _f			-	12	24	
Gate Input Resistance	R _g	f = 1 MHz, open drain		-	0.92	-	Ω
Drain-Source Body Diode Characteristic	s						
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	10.5	
Pulsed Diode Forward Current	I _{SM}			-	-	21	A
Diode Forward Voltage	V _{SD}	$T_J = 25 ^{\circ}\text{C}, I_S = 7.5 \text{A}, V_{GS} = 0 \text{V}$		-	-	1.2	V
Reverse Recovery Time	t _{rr}	$T_J = 25 \text{ °C}, I_F = I_S = 6 \text{ A},$ $dI/dt = 100 \text{ A/}\mu\text{s}, V_R = 25 \text{ V}$		-	244	-	ns
Reverse Recovery Charge	Q _{rr}			-	2.5	-	μC
Reverse Recovery Current	I _{RRM}			-	19	-	A

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} . b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

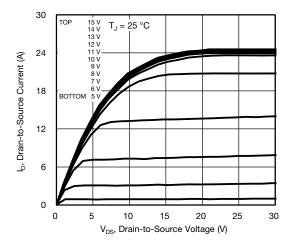


Fig. 1 - Typical Output Characteristics

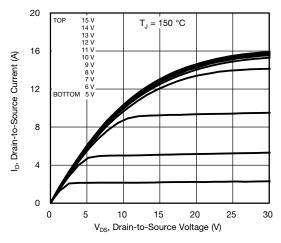


Fig. 2 - Typical Output Characteristics

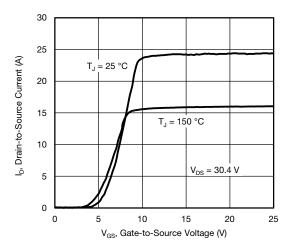


Fig. 3 - Typical Transfer Characteristics

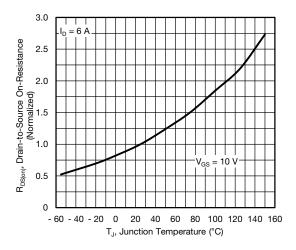


Fig. 4 - Normalized On-Resistance vs. Temperature

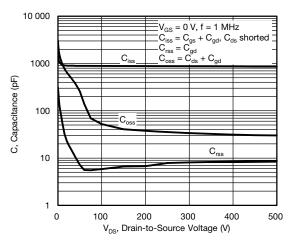


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

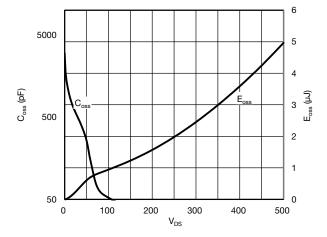


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}



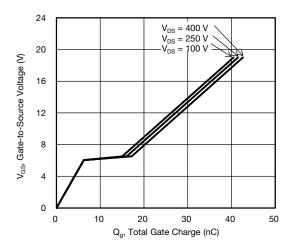


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

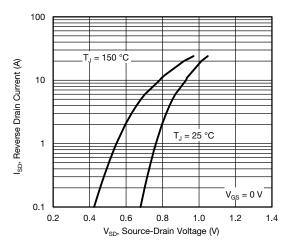


Fig. 8 - Typical Source-Drain Diode Forward Voltage

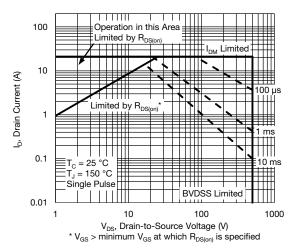


Fig. 9 - Maximum Safe Operating Area

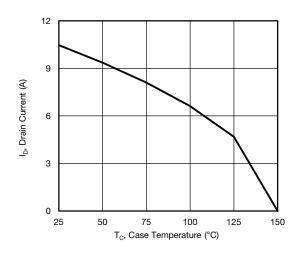


Fig. 10 - Maximum Drain Current vs. Case Temperature

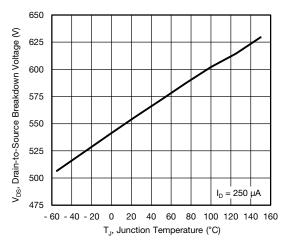


Fig. 11 - Temperature vs. Drain-to-Source Voltage



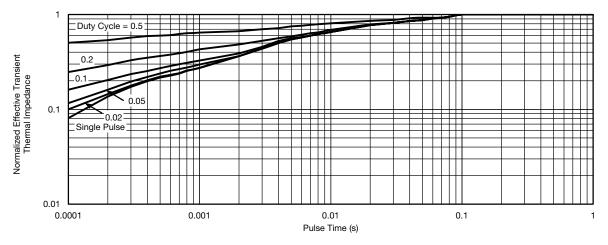


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

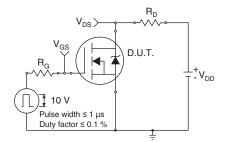


Fig. 13 - Switching Time Test Circuit

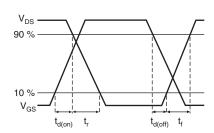


Fig. 14 - Switching Time Waveforms

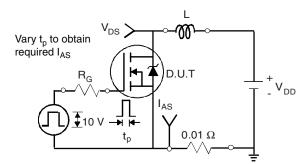


Fig. 15 - Unclamped Inductive Test Circuit

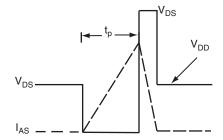


Fig. 16 - Unclamped Inductive Waveforms

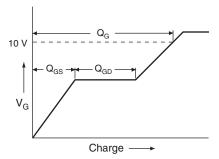


Fig. 17 - Basic Gate Charge Waveform

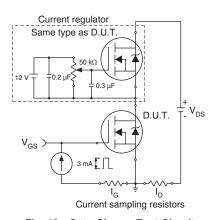
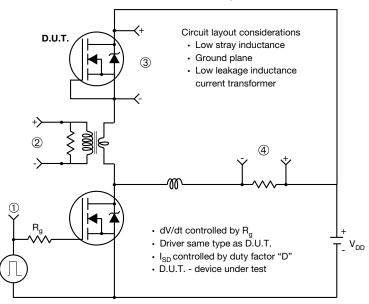


Fig. 18 - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



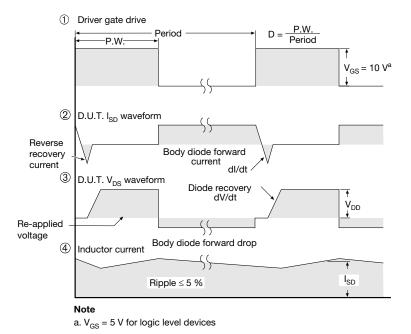


Fig. 19 - For N-Channel

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Revision: 02-Oct-12 Document Number: 91000

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многоканальный

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