



ANALOG DEVICES User Defined Fault Protection and Detection, 0.8 pC Q_{INJ} , 8:1/Dual 4:1 Multiplexers

Data Sheet

ADG5248F/ADG5249F

FEATURES

- User defined secondary supplies set overvoltage level
- Overvoltage protection up to -55 V and $+55\text{ V}$
- Power-off protection up to -55 V and $+55\text{ V}$
- Overvoltage detection on source pins
- Minimum secondary supply level: 4.5 V single-supply
- Interrupt flags indicate fault status
- Low charge injection (Q_{INJ}): 0.8 pC
- Low drain/source on capacitance
- ADG5248F: 19 pF
- ADG5249F: 14 pF
- Latch-up immune under any circumstance
- Known state without digital inputs present
- V_{SS} to V_{DD} analog signal range
- $\pm 5\text{ V}$ to $\pm 22\text{ V}$ dual-supply operation
- 8 V to 44 V single-supply operation
- Fully specified at $\pm 15\text{ V}$, $\pm 20\text{ V}$, $+12\text{ V}$, and $+36\text{ V}$

APPLICATIONS

- Analog input/output modules
- Process control/distributed control systems
- Data acquisition
- Instrumentation
- Avionics
- Automatic test equipment
- Communication systems
- Relay replacement

GENERAL DESCRIPTION

The ADG5248F and ADG5249F are 8:1 and dual 4:1 analog multiplexers. The ADG5248F switches one of eight inputs to a common output, and the ADG5249F switches one of four differential inputs to a common differential output. Each channel conducts equally well in both directions when on, and each channel has an input signal range that extends to the supplies. The primary supply voltages define the on-resistance profile, whereas the secondary supply voltages define the voltage level at which the overvoltage protection engages.

When no power supplies are present, the channel remains in the off condition, and the switch inputs are high impedance. Under normal operating conditions, if the analog input signal levels on any S_x pin exceed positive fault voltage (POSFV) or negative fault voltage (NEGFV) by a threshold voltage (V_T), the channel turns off and that S_x pin becomes high impedance. If the switch on, the drain pin is pulled to the secondary supply voltage that was exceeded. Input signal levels up to $+55\text{ V}$ or -55 V relative to ground are blocked, in both the powered and unpowered conditions.

Rev. A

Document Feedback

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FUNCTIONAL BLOCK DIAGRAMS

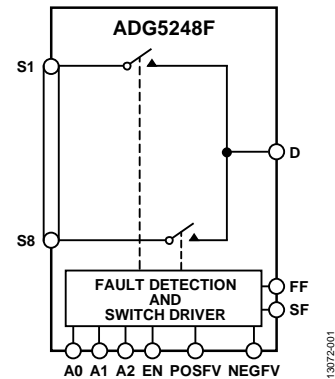


Figure 1. ADG5248F Functional Block Diagram

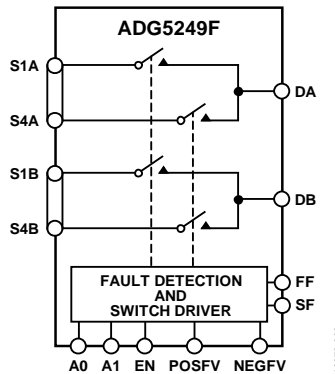


Figure 2. ADG5249F Functional Block Diagram

The low capacitance and charge injection of these switches make them ideal solutions for data acquisition and sample-and-hold applications, where low glitch switching and fast settling times are required.

Note that, throughout this data sheet, multifunction pins, such as A0/F0, are referred to either by the entire pin name or by a single function of the pin, for example, A0, when only that function is relevant.

PRODUCT HIGHLIGHTS

1. Source pins are protected against voltages greater than the secondary supply rails, up to -55 V and $+55\text{ V}$.
2. Source pins are protected against voltages between -55 V and $+55\text{ V}$ in an unpowered state.
3. Overvoltage detection with digital output indicates operating state of switches.
4. Trench isolation guards against latch-up.
5. Optimized for low charge injection and on capacitance.
6. The ADG5248F/ADG5249F can be operated from a dual supply of $\pm 5\text{ V}$ to $\pm 22\text{ V}$ or a single power supply of 8 V to 44 V .

TABLE OF CONTENTS

| | | | |
|--|----|--|----|
| Features | 1 | Test Circuits..... | 23 |
| Applications..... | 1 | Terminology..... | 28 |
| Functional Block Diagrams..... | 1 | Theory of Operation | 30 |
| General Description | 1 | Switch Architecture..... | 30 |
| Product Highlights | 1 | User Defined Fault Protection..... | 31 |
| Revision History | 2 | Applications Information | 32 |
| Specifications..... | 3 | Power Supply Rails | 32 |
| ±15 V Dual Supply | 3 | Power Supply Sequencing Protection | 32 |
| ±20 V Dual Supply | 5 | Signal Range..... | 32 |
| 12 V Single Supply..... | 7 | Power Supply Recommendations..... | 32 |
| 36 V Single Supply..... | 9 | High Voltage Surge Suppression | 32 |
| Continuous Current per Channel, Sx, D, or Dx..... | 12 | Intelligent Fault Detection | 33 |
| Absolute Maximum Ratings..... | 13 | Large Voltage, High Frequency Signals..... | 33 |
| ESD Caution..... | 13 | Outline Dimensions..... | 34 |
| Pin Configurations and Function Descriptions | 14 | Ordering Guide | 34 |
| Typical Performance Characteristics | 18 | | |

REVISION HISTORY

7/2016—Rev. 0 to Rev. A

| | |
|---|-----------|
| Added 20-Lead LFCSP | Universal |
| Changes to Table 5..... | 12 |
| Changes to Table 6..... | 13 |
| Added Figure 4; Renumbered Sequentially | 14 |
| Changes to Table 7..... | 14 |
| Added Figure 6..... | 16 |
| Changes to Table 10..... | 16 |
| Updated Outline Dimensions | 34 |
| Changes to Ordering Guide | 34 |

4/2015—Revision 0: Initial Version

SPECIFICATIONS

±15 V DUAL SUPPLY

$V_{DD} = 15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V} \pm 10\%$, $GND = 0\text{ V}$, $C_{DECOUPLING} = 0.1\text{ }\mu\text{F}$, unless otherwise noted.

Table 1.

| Parameter | +25°C | -40°C to +85°C | -40°C to +125°C | Unit | Test Conditions/Comments |
|---|-----------|----------------|----------------------|-------------------|--|
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | V_{DD} to V_{SS} | V | $V_{DD} = +13.5\text{ V}$, $V_{SS} = -13.5\text{ V}$, see Figure 38 |
| On Resistance, R_{ON} | 250 | | | Ω typ | $V_S = \pm 10\text{ V}$, $I_S = -1\text{ mA}$ |
| | 270 | 335 | 395 | Ω max | |
| | 250 | | | Ω typ | $V_S = \pm 9\text{ V}$, $I_S = -1\text{ mA}$ |
| | 270 | 335 | 395 | Ω max | |
| On-Resistance Match Between Channels, ΔR_{ON} | 2.5 | | | Ω typ | $V_S = \pm 10\text{ V}$, $I_S = -1\text{ mA}$ |
| | 6 | 12 | 13 | Ω max | |
| | 2.5 | | | Ω typ | $V_S = \pm 9\text{ V}$, $I_S = -1\text{ mA}$ |
| | 6 | 12 | 13 | Ω max | |
| On-Resistance Flatness, $R_{FLAT(ON)}$ | 6.5 | | | Ω typ | $V_S = \pm 10\text{ V}$, $I_S = -1\text{ mA}$ |
| | 8 | 9 | 9 | Ω max | |
| | 1.5 | | | Ω typ | $V_S = \pm 9\text{ V}$, $I_S = -1\text{ mA}$ |
| | 3.5 | 4 | 4 | Ω max | |
| Threshold Voltage, V_T | 0.7 | | | V typ | See Figure 30 |
| LEAKAGE CURRENTS | | | | | |
| Source Off Leakage, I_S (Off) | ± 0.1 | | | nA typ | $V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$ |
| | ± 1 | ± 2 | ± 5 | nA max | $V_S = \pm 10\text{ V}$, $V_D = \mp 10\text{ V}$, see Figure 36 |
| Drain Off Leakage, I_D (Off) | ± 0.1 | | | nA typ | $V_S = \pm 10\text{ V}$, $V_D = \mp 10\text{ V}$, see Figure 36 |
| | ± 1 | ± 5 | ± 10 | nA max | |
| Channel On Leakage, I_D (On), I_S (On) | ± 0.3 | | | nA typ | $V_S = V_D = \pm 10\text{ V}$, see Figure 37 |
| | ± 1.5 | ± 20 | ± 25 | nA max | |
| FAULT | | | | | |
| Source Leakage Current, I_S With Overvoltage | ± 66 | | ± 78 | μA typ | $V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$, $GND = 0\text{ V}$, $V_S = \pm 55\text{ V}$, see Figure 35 |
| Power Supplies Grounded or Floating | ± 25 | | ± 40 | μA typ | $V_{DD} = 0\text{ V}$ or floating, $V_{SS} = 0\text{ V}$ or floating, $GND = 0\text{ V}$, $A_X = 0\text{ V}$ or floating, $V_S = \pm 55\text{ V}$, see Figure 34 |
| Drain Leakage Current, I_D With Overvoltage | ± 10 | | | nA typ | $V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$, $GND = 0\text{ V}$, $V_S = \pm 55\text{ V}$, see Figure 35 |
| | ± 50 | ± 70 | ± 90 | nA max | |
| Power Supplies Grounded | ± 500 | | | nA typ | $V_{DD} = 0\text{ V}$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, $V_S = \pm 55\text{ V}$, $A_X = 0\text{ V}$, see Figure 34 |
| | ± 700 | ± 700 | ± 700 | nA max | |
| Power Supplies Floating | ± 50 | ± 50 | ± 50 | μA typ | $V_{DD} = \text{floating}$, $V_{SS} = \text{floating}$, $GND = 0\text{ V}$, $V_S = \pm 55\text{ V}$, $A_X = 0\text{ V}$, see Figure 34 |
| DIGITAL INPUTS | | | | | |
| Input Voltage High, V_{INH} | | | 2.0 | V min | |
| Input Voltage Low, V_{INL} | | | 0.8 | V max | |
| Input Current, I_{INL} or I_{INH} | ± 0.7 | | | μA typ | $V_{IN} = GND$ or V_{DD} |
| | ± 1.1 | | ± 1.2 | μA max | |
| Digital Input Capacitance, C_{IN} | 5.0 | | | pF typ | |

| Parameter | +25°C | −40°C to +85°C | −40°C to +125°C | Unit | Test Conditions/Comments |
|---|-------|----------------|-----------------|-------------------|--|
| Output Voltage | | | | | |
| High, V_{OH} | 2.0 | | | V min | |
| Low, V_{OL} | 0.8 | | | V max | |
| DYNAMIC CHARACTERISTICS¹ | | | | | |
| Transition Time, $t_{TRANSITION}$ | 210 | | | ns typ | $R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$ |
| | 290 | 305 | 310 | ns max | $V_S = 10\text{ V}$, see Figure 50 |
| t_{ON} (EN) | 200 | | | ns typ | $R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$ |
| | 280 | 295 | 315 | ns max | $V_S = 10\text{ V}$, see Figure 49 |
| t_{OFF} (EN) | 105 | | | ns typ | $R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$ |
| | 120 | 160 | 160 | ns max | $V_S = 10\text{ V}$, see Figure 49 |
| Break-Before-Make Time Delay, t_D | 155 | | | ns typ | $R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$ |
| | | | 90 | ns min | $V_S = 10\text{ V}$, see Figure 48 |
| Overvoltage Response Time, $t_{RESPONSE}$ | 90 | | | ns typ | $R_L = 1\text{ k}\Omega$, $C_L = 5\text{ pF}$, see Figure 43 |
| | 115 | 130 | 130 | ns max | |
| Overvoltage Recovery Time, $t_{RECOVERY}$ | 745 | | | ns typ | $R_L = 1\text{ k}\Omega$, $C_L = 5\text{ pF}$, see Figure 44 |
| | 945 | 965 | 970 | ns max | |
| Interrupt Flag Response Time, $t_{DIGRESP}$ | 90 | | | ns typ | $C_L = 12\text{ pF}$, see Figure 45 |
| Interrupt Flag Recovery Time, t_{DIGREC} | 65 | | | μs typ | $C_L = 12\text{ pF}$, see Figure 46 |
| | 900 | | | ns typ | $C_L = 12\text{ pF}$, $R_{PULLUP} = 1\text{ k}\Omega$, see Figure 47 |
| Charge Injection, Q_{INU} | −0.8 | | | pC typ | $V_S = 0\text{ V}$, $R_S = 0\text{ }\Omega$, $C_L = 1\text{ nF}$, see Figure 51 |
| Off Isolation | −75 | | | dB typ | $R_L = 50\text{ }\Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, see Figure 41, worst case channel |
| Channel-to-Channel Crosstalk | | | | | $R_L = 50\text{ }\Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, see Figure 40 |
| Adjacent Channels | −75 | | | dB typ | |
| Nonadjacent Channels | −88 | | | dB typ | |
| Total Harmonic Distortion Plus Noise, THD + N | 0.005 | | | % typ | $R_L = 10\text{ k}\Omega$, $V_S = 15\text{ V p-p}$, $f = 20\text{ Hz to }20\text{ kHz}$, see Figure 39 |
| −3 dB Bandwidth | | | | | $R_L = 50\text{ }\Omega$, $C_L = 5\text{ pF}$, see Figure 42 |
| ADG5248F | 190 | | | MHz typ | |
| ADG5249F | 320 | | | MHz typ | |
| Insertion Loss | 10.5 | | | dB typ | $R_L = 50\text{ }\Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, see Figure 42 |
| C_S (Off) | 4 | | | pF typ | $V_S = 0\text{ V}$, $f = 1\text{ MHz}$ |
| C_D (Off) | | | | | $V_S = 0\text{ V}$, $f = 1\text{ MHz}$ |
| ADG5248F | 13 | | | pF typ | |
| ADG5249F | 8 | | | pF typ | |
| C_D (On), C_S (On) | | | | | $V_S = 0\text{ V}$, $f = 1\text{ MHz}$ |
| ADG5248F | 19 | | | pF typ | |
| ADG5249F | 14 | | | pF typ | |
| POWER REQUIREMENTS | | | | | |
| Normal Mode | | | | | $V_{DD} = \text{POSFV} = +16.5\text{ V}$; $V_{SS} = \text{NEGFV} = -16.5\text{ V}$; $\text{GND} = 0\text{ V}$; digital inputs = 0 V, 5 V, or V_{DD} |
| I_{DD} | 1.15 | | | mA typ | |
| I_{POSFV} | 0.15 | | | mA typ | |
| $I_{DD} + I_{\text{POSFV}}$ | 2 | | 2 | mA max | |
| I_{GND} | 0.75 | | | mA typ | |
| | 1.25 | | 1.25 | mA max | |
| I_{SS} | 0.45 | | | mA typ | |
| I_{NEGFV} | 0.2 | | | mA typ | |
| $I_{SS} + I_{\text{NEGFV}}$ | 0.8 | | 0.85 | mA max | |

| Parameter | +25°C | -40°C to +85°C | -40°C to +125°C | Unit | Test Conditions/Comments |
|----------------------|-------|----------------|-----------------|--------|--------------------------|
| Fault Mode | | | | | $V_S = \pm 55\text{ V}$ |
| I_{DD} | 1.4 | | | mA typ | |
| I_{POSFV} | 0.2 | | | mA typ | |
| $I_{DD} + I_{POSFV}$ | 2.2 | | 2.3 | mA max | |
| I_{GND} | 0.9 | | | mA typ | |
| | 1.6 | | 1.7 | mA max | |
| I_{SS} | 0.45 | | | mA typ | |
| I_{NEGFV} | 0.2 | | | mA typ | |
| $I_{SS} + I_{NEGFV}$ | 1.0 | | 1.1 | mA max | |
| V_{DD}/V_{SS} | | | ± 5 | V min | GND = 0 V |
| | | | ± 22 | V max | GND = 0 V |

¹ Guaranteed by design; not subject to production test.

±20 V DUAL SUPPLY

$V_{DD} = 20\text{ V} \pm 10\%$, $V_{SS} = -20\text{ V} \pm 10\%$, GND = 0 V, $C_{DECOUPLING} = 0.1\ \mu\text{F}$, unless otherwise noted.

Table 2.

| Parameter | +25°C | -40°C to +85°C | -40°C to +125°C | Unit | Test Conditions/Comments |
|---|-----------|----------------|----------------------|-------------------|--|
| ANALOG SWITCH | | | | | $V_{DD} = +18\text{ V}$, $V_{SS} = -18\text{ V}$, see Figure 38 |
| Analog Signal Range | | | V_{DD} to V_{SS} | V | |
| On Resistance, R_{ON} | 260 | | | Ω typ | $V_S = \pm 15\text{ V}$, $I_S = -1\text{ mA}$ |
| | 280 | 345 | 405 | Ω max | |
| | 250 | | | Ω typ | $V_S = \pm 13.5\text{ V}$, $I_S = -1\text{ mA}$ |
| | 270 | 335 | 395 | Ω max | |
| On-Resistance Match Between Channels, ΔR_{ON} | 2.5 | | | Ω typ | $V_S = \pm 15\text{ V}$, $I_S = -1\text{ mA}$ |
| | 6 | 12 | 13 | Ω max | |
| | 2.5 | | | Ω typ | $V_S = \pm 13.5\text{ V}$, $I_S = -1\text{ mA}$ |
| | 6 | 12 | 13 | Ω max | |
| On-Resistance Flatness, $R_{FLAT(ON)}$ | 12.5 | | | Ω typ | $V_S = \pm 15\text{ V}$, $I_S = -1\text{ mA}$ |
| | 14 | 15 | 15 | Ω max | |
| | 1.5 | | | Ω typ | $V_S = \pm 13.5\text{ V}$, $I_S = -1\text{ mA}$ |
| | 3.5 | 4 | 4 | Ω max | |
| Threshold Voltage, V_T | 0.7 | | | V typ | See Figure 30 |
| LEAKAGE CURRENTS | | | | | $V_{DD} = +22\text{ V}$, $V_{SS} = -22\text{ V}$ |
| Source Off Leakage, I_S (Off) | ± 0.1 | | | nA typ | $V_S = \pm 15\text{ V}$, $V_D = \mp 15\text{ V}$, see Figure 36 |
| | ± 1 | ± 2 | ± 5 | nA max | |
| Drain Off Leakage, I_D (Off) | ± 0.1 | | | nA typ | $V_S = \pm 15\text{ V}$, $V_D = \mp 15\text{ V}$, see Figure 36 |
| | ± 1 | ± 5 | ± 10 | nA max | |
| Channel On Leakage, I_D (On), I_S (On) | ± 0.3 | | | nA typ | $V_S = V_D = \pm 15\text{ V}$, see Figure 37 |
| | ± 1.5 | ± 20 | ± 25 | nA max | |
| FAULT | | | | | |
| Source Leakage Current, I_S With Overvoltage | ± 66 | | | μA typ | $V_{DD} = 22\text{ V}$, $V_{SS} = -22\text{ V}$, GND = 0 V, $V_S = \pm 55\text{ V}$, see Figure 35 |
| Power Supplies Grounded or Floating | ± 25 | | | μA typ | $V_{DD} = 0\text{ V}$ or floating, $V_{SS} = 0\text{ V}$ or floating, GND = 0 V, $A_x = 0\text{ V}$ or floating, $V_S = \pm 55\text{ V}$, see Figure 34 |

| Parameter | +25°C | -40°C to +85°C | -40°C to +125°C | Unit | Test Conditions/Comments |
|---|--------------|----------------|-----------------|------------------|---|
| Drain Leakage Current, I_D With Overvoltage | ±10 | | | nA typ | $V_{DD} = +22\text{ V}$, $V_{SS} = -22\text{ V}$, $GND = 0\text{ V}$, $V_S = \pm 55\text{ V}$, see Figure 35 |
| Power Supplies Grounded | ±2 ±500 | ±2 | ±2 | µA max nA typ | $V_{DD} = 0\text{ V}$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, $V_S = \pm 55\text{ V}$, $A_x = 0\text{ V}$, see Figure 34 |
| Power Supplies Floating | ±700 ±50 | ±700 ±50 | ±700 ±50 | nA max µA typ | $V_{DD} = \text{floating}$, $V_{SS} = \text{floating}$, $GND = 0\text{ V}$, $V_S = \pm 55\text{ V}$, $A_x = 0\text{ V}$, see Figure 34 |
| DIGITAL INPUTS | | | | | |
| Input Voltage High, V_{INH} Low, V_{INL} | | | 2.0 0.8 | V min V max | $V_{IN} = GND$ or V_{DD} |
| Input Current, I_{INL} or I_{INH} | ±0.7 ±1.1 | | ±1.2 | µA typ µA max | |
| Digital Input Capacitance, C_{IN} | 5.0 | | | pF typ | |
| Output Voltage High, V_{OH} Low, V_{OL} | 2.0 0.8 | | | V min V max | |
| DYNAMIC CHARACTERISTICS¹ | | | | | |
| Transition Time, $t_{TRANSITION}$ | 230 335 | 340 | 340 | ns typ ns max | $R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$ $V_S = 10\text{ V}$, see Figure 50 |
| t_{ON} (EN) | 225 325 | 340 | 340 | ns typ ns max | $R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$ $V_S = 10\text{ V}$, see Figure 49 |
| t_{OFF} (EN) | 100 135 | 155 | 155 | ns typ ns max | $R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$ $V_S = 10\text{ V}$, see Figure 49 |
| Break-Before-Make Time Delay, t_D | 175 | | | ns typ ns min | $R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$ $V_S = 10\text{ V}$, see Figure 48 |
| Overvoltage Response Time, $t_{RESPONSE}$ | 75 105 | 105 | 105 | ns typ ns max | $R_L = 1\text{ k}\Omega$, $C_L = 5\text{ pF}$, see Figure 43 |
| Overvoltage Recovery Time, $t_{RECOVERY}$ | 820 1100 | 1250 | 1400 | ns typ ns max | $R_L = 1\text{ k}\Omega$, $C_L = 5\text{ pF}$, see Figure 44 |
| Interrupt Flag Response Time, $t_{DIGRESP}$ | 75 | | | ns typ | $C_L = 12\text{ pF}$, see Figure 45 |
| Interrupt Flag Recovery Time, t_{DIGREC} | 65 1000 | | | µs typ ns typ | $C_L = 12\text{ pF}$, see Figure 46 $C_L = 12\text{ pF}$, $R_{PULLUP} = 1\text{ k}\Omega$, see Figure 47 |
| Charge Injection, Q_{INJ} | -1.2 | | | pC typ | $V_S = 0\text{ V}$, $R_S = 0\text{ }\Omega$, $C_L = 1\text{ nF}$, see Figure 51 |
| Off Isolation | -75 | | | dB typ | $R_L = 50\text{ }\Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, see Figure 41, worst case channel |
| Channel-to-Channel Crosstalk Adjacent Channels Nonadjacent Channels | -75 -88 | | | dB typ dB typ | $R_L = 50\text{ }\Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, see Figure 40 |
| Total Harmonic Distortion Plus Noise, THD + N | 0.005 | | | % typ | $R_L = 10\text{ k}\Omega$, $V_S = 20\text{ V p-p}$, $f = 20\text{ Hz to } 20\text{ kHz}$, see Figure 39 |
| -3 dB Bandwidth | | | | | $R_L = 50\text{ }\Omega$, $C_L = 5\text{ pF}$, see Figure 42 |
| ADG5248F | 190 | | | MHz typ | |
| ADG5249F | 320 | | | MHz typ | |
| Insertion Loss | 10.5 | | | dB typ | $R_L = 50\text{ }\Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, see Figure 42 |
| C_S (Off) | 4 | | | pF typ | $V_S = 0\text{ V}$, $f = 1\text{ MHz}$ |
| C_D (Off) | | | | | $V_S = 0\text{ V}$, $f = 1\text{ MHz}$ |
| ADG5248F | 13 | | | pF typ | |
| ADG5249F | 8 | | | pF typ | |

| Parameter | +25°C | -40°C to +85°C | -40°C to +125°C | Unit | Test Conditions/Comments | |
|-----------------------------|-------|----------------|-----------------|--------|---|--|
| C_D (On), C_S (On) | | | | | $V_S = 0\text{ V}$, $f = 1\text{ MHz}$ | |
| ADG5248F | 19 | | | pF typ | | |
| ADG5249F | 14 | | | pF typ | | |
| POWER REQUIREMENTS | | | | | | |
| Normal Mode | | | | | | |
| I_{DD} | 1.15 | | | mA typ | $V_{DD} = \text{POSFV} = +22\text{ V}$; $V_{SS} = \text{NEGFV} = -22\text{ V}$; digital inputs = 0 V, 5 V, or V_{DD} | |
| I_{POSFV} | 0.15 | | | mA typ | | |
| $I_{DD} + I_{\text{POSFV}}$ | 2 | | 2 | mA max | | |
| I_{GND} | 0.75 | | | mA typ | | |
| | 1.25 | | 1.25 | mA max | | |
| I_{SS} | 0.45 | | | mA typ | | |
| I_{NEGFV} | 0.2 | | | mA typ | | |
| $I_{SS} + I_{\text{NEGFV}}$ | 0.8 | | 0.85 | mA max | | |
| Fault Mode | | | | | | |
| I_{DD} | 1.4 | | | mA typ | | |
| I_{POSFV} | 0.2 | | | mA typ | | |
| $I_{DD} + I_{\text{POSFV}}$ | 2.2 | | 2.3 | mA max | | |
| I_{GND} | 0.9 | | | mA typ | | |
| | 1.6 | | 1.7 | mA max | | |
| I_{SS} | 0.45 | | | mA typ | | |
| I_{NEGFV} | 0.2 | | | mA typ | | |
| $I_{SS} + I_{\text{NEGFV}}$ | 1.0 | | 1.1 | mA max | | |
| V_{DD}/V_{SS} | | | ± 5 | V min | $V_S = \pm 55\text{ V}$ | |
| | | | ± 22 | V max | $GND = 0\text{ V}$ | |

¹ Guaranteed by design; not subject to production test.

12 V SINGLE SUPPLY

$V_{DD} = 12\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, $C_{\text{DECOUPLING}} = 0.1\text{ }\mu\text{F}$, unless otherwise noted.

Table 3.

| Parameter | +25°C | -40°C to +85°C | -40°C to +125°C | Unit | Test Conditions/Comments |
|---|-----------|----------------|-----------------|--------------|---|
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | 0 V to V_{DD} | V | $V_{DD} = 10.8\text{ V}$, $V_{SS} = 0\text{ V}$, see Figure 38 |
| On Resistance, R_{ON} | 630 | | | Ω typ | $V_S = 0\text{ V to } 10\text{ V}$, $I_S = -1\text{ mA}$ |
| | 690 | 710 | 730 | Ω max | |
| | 270 | | | Ω typ | $V_S = 3.5\text{ V to } 8.5\text{ V}$, $I_S = -1\text{ mA}$ |
| | 290 | 355 | 410 | Ω max | |
| On-Resistance Match Between Channels, ΔR_{ON} | 6 | | | Ω typ | $V_S = 0\text{ V to } 10\text{ V}$, $I_S = -1\text{ mA}$ |
| | 17 | 19 | 19 | Ω max | |
| | 3 | | | Ω typ | $V_S = 3.5\text{ V to } 8.5\text{ V}$, $I_S = -1\text{ mA}$ |
| | 6.5 | 11 | 12 | Ω max | |
| On-Resistance Flatness, $R_{\text{FLAT(ON)}}$ | 380 | | | Ω typ | $V_S = 0\text{ V to } 10\text{ V}$, $I_S = -1\text{ mA}$ |
| | 440 | 460 | 460 | Ω max | |
| | 25 | | | Ω typ | $V_S = 3.5\text{ V to } 8.5\text{ V}$, $I_S = -1\text{ mA}$ |
| | 27 | 28 | 28 | Ω max | |
| Threshold Voltage, V_T | 0.7 | | | V typ | See Figure 30 |
| LEAKAGE CURRENTS | | | | | |
| Source Off Leakage, I_S (Off) | ± 0.1 | | | nA typ | $V_{DD} = 13.2\text{ V}$, $V_{SS} = 0\text{ V}$ |
| | ± 1 | ± 2 | ± 5 | nA max | $V_S = 1\text{ V}/10\text{ V}$, $V_D = 10\text{ V}/1\text{ V}$, see Figure 36 |

| Parameter | +25°C | -40°C to +85°C | -40°C to +125°C | Unit | Test Conditions/Comments |
|--|------------|----------------|-----------------|----------------|--|
| Drain Off Leakage, I_D (Off) | ±0.1 | | | nA typ | $V_S = 1\text{ V}/10\text{ V}, V_D = 10\text{ V}/1\text{ V}$, see Figure 36 |
| Channel On Leakage, I_D (On), I_S (On) | ±1 | ±5 | ±10 | nA max | $V_S = V_D = 1\text{ V}/10\text{ V}$, see Figure 37 |
| | ±0.3 | | | nA typ | |
| | ±1.5 | ±20 | ±25 | nA max | |
| FAULT | | | | | |
| Source Leakage Current, I_S With Overvoltage | ±63 | | | µA typ | $V_{DD} = 13.2\text{ V}, V_{SS} = 0\text{ V}, \text{GND} = 0\text{ V}, V_S = \pm 55\text{ V}$, see Figure 35 |
| Power Supplies Grounded or Floating | ±25 | | | µA typ | $V_{DD} = 0\text{ V}$ or floating, $V_{SS} = 0\text{ V}$ or floating, $\text{GND} = 0\text{ V}, A_X = 0\text{ V}$ or floating, $V_S = \pm 55\text{ V}$, see Figure 34 |
| Drain Leakage Current, I_D With Overvoltage | ±10 | | | nA typ | $V_{DD} = 13.2\text{ V}, V_{SS} = 0\text{ V}, \text{GND} = 0\text{ V}, V_S = \pm 55\text{ V}$, see Figure 35 |
| Power Supplies Grounded | ±50 | ±70 | ±90 | nA max | $V_{DD} = 0\text{ V}, V_{SS} = 0\text{ V}, \text{GND} = 0\text{ V}, V_S = \pm 55\text{ V}, A_X = 0\text{ V}$, see Figure 34 |
| | ±500 | | | nA typ | |
| Power Supplies Floating | ±700 | ±700 | ±700 | nA max | $V_{DD} = \text{floating}, V_{SS} = \text{floating}, \text{GND} = 0\text{ V}, V_S = \pm 55\text{ V}, A_X = 0\text{ V}$, see Figure 34 |
| | ±50 | ±50 | ±50 | µA typ | |
| DIGITAL INPUTS | | | | | |
| Input Voltage High, V_{INH} Low, V_{INL} | | | 2.0 0.8 | V min V max | $V_{IN} = \text{GND}$ or V_{DD} |
| Input Current, I_{INL} or I_{INH} | ±0.7 | | | µA typ | |
| | ±1.1 | | ±1.2 | µA max | |
| Digital Input Capacitance, C_{IN} | 5.0 | | | pF typ | |
| Output Voltage High, V_{OH} Low, V_{OL} | 2.0 0.8 | | | V min V max | |
| DYNAMIC CHARACTERISTICS¹ | | | | | |
| Transition Time, $t_{TRANSITION}$ | 165 | | | ns typ | $R_L = 1\text{ k}\Omega, C_L = 35\text{ pF}$ |
| | 205 | 215 | 230 | ns max | $V_S = 8\text{ V}$, see Figure 50 |
| t_{ON} (EN) | 160 | | | ns typ | $R_L = 1\text{ k}\Omega, C_L = 35\text{ pF}$ |
| | 200 | 215 | 230 | ns max | $V_S = 8\text{ V}$, see Figure 49 |
| t_{OFF} (EN) | 125 | | | ns typ | $R_L = 1\text{ k}\Omega, C_L = 35\text{ pF}$ |
| | 150 | 155 | 155 | ns max | $V_S = 8\text{ V}$, see Figure 49 |
| Break-Before-Make Time Delay, t_D | 100 | | | ns typ | $R_L = 1\text{ k}\Omega, C_L = 35\text{ pF}$ |
| | | | 60 | ns min | $V_S = 8\text{ V}$, see Figure 48 |
| Overvoltage Response Time, $t_{RESPONSE}$ | 110 | | | ns typ | $R_L = 1\text{ k}\Omega, C_L = 5\text{ pF}$, see Figure 43 |
| | 145 | 145 | 145 | ns max | |
| Overvoltage Recovery Time, $t_{RECOVERY}$ | 500 | | | ns typ | $R_L = 1\text{ k}\Omega, C_L = 5\text{ pF}$, see Figure 44 |
| | 655 | 720 | 765 | ns max | |
| Interrupt Flag Response Time, $t_{DIGRESP}$ | 95 | | | ns typ | $C_L = 12\text{ pF}$, see Figure 45 |
| Interrupt Flag Recovery Time, t_{DIGREC} | 65 | | | µs typ | $C_L = 12\text{ pF}$, see Figure 46 |
| | 900 | | | ns typ | $C_L = 12\text{ pF}, R_{PULLUP} = 1\text{ k}\Omega$, see Figure 47 |
| Charge Injection, Q_{INJ} | 0.2 | | | pC typ | $V_S = 6\text{ V}, R_S = 0\text{ }\Omega, C_L = 1\text{ nF}$, see Figure 51 |
| Off Isolation | -75 | | | dB typ | $R_L = 50\text{ }\Omega, C_L = 5\text{ pF}, f = 1\text{ MHz}$, see Figure 41, worst case channel |
| Channel-to-Channel Crosstalk Adjacent Channels | -75 | | | dB typ | $R_L = 50\text{ }\Omega, C_L = 5\text{ pF}, f = 1\text{ MHz}$, see Figure 40 |
| Nonadjacent Channels | -88 | | | dB typ | |
| Total Harmonic Distortion Plus Noise, THD + N | 0.044 | | | % typ | $R_L = 10\text{ k}\Omega, V_S = 6\text{ V p-p}, f = 20\text{ Hz}$ to 20 kHz , see Figure 39 |

| Parameter | +25°C | −40°C to +85°C | −40°C to +125°C | Unit | Test Conditions/Comments |
|---------------------------|-------|----------------|-----------------|---------|---|
| −3 dB Bandwidth | | | | | $R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, see Figure 42 |
| ADG5248F | 175 | | | MHz typ | |
| ADG5249F | 290 | | | MHz typ | |
| Insertion Loss | 10.5 | | | dB typ | $R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 1 \text{ MHz}$, see Figure 42 |
| C_S (Off) | 4 | | | pF typ | $V_S = 6 \text{ V}$, $f = 1 \text{ MHz}$ |
| C_D (Off) | | | | | $V_S = 6 \text{ V}$, $f = 1 \text{ MHz}$ |
| ADG5248F | 14 | | | pF typ | |
| ADG5249F | 8 | | | pF typ | |
| C_D (On), C_S (On) | | | | | $V_S = 6 \text{ V}$, $f = 1 \text{ MHz}$ |
| ADG5248F | 20 | | | pF typ | |
| ADG5249F | 14 | | | pF typ | |
| POWER REQUIREMENTS | | | | | $V_{DD} = 13.2 \text{ V}$; $V_{SS} = 0 \text{ V}$; digital inputs = 0 V, 5 V, or V_{DD} |
| Normal Mode | | | | | |
| I_{DD} | 1.15 | | | mA typ | |
| I_{POSFV} | 0.15 | | | mA typ | |
| $I_{DD} + I_{POSFV}$ | 2 | | 2 | mA max | |
| I_{GND} | 0.75 | | | mA typ | |
| | 1.4 | | 1.4 | mA max | |
| I_{SS} | 0.3 | | | mA typ | |
| I_{NEGFV} | 0.2 | | | mA typ | |
| $I_{SS} + I_{NEGFV}$ | 0.65 | | 0.7 | mA max | |
| Fault Mode | | | | | $V_S = \pm 55 \text{ V}$ |
| I_{DD} | 1.4 | | | mA typ | |
| I_{POSFV} | 0.2 | | | mA typ | |
| $I_{DD} + I_{POSFV}$ | 2.2 | | 2.3 | mA max | |
| I_{GND} | 0.9 | | | mA typ | |
| | 1.6 | | 1.7 | mA max | |
| I_{SS} | 0.45 | | | mA typ | Digital inputs = 5 V |
| I_{NEGFV} | 0.2 | | | mA typ | |
| $I_{SS} + I_{NEGFV}$ | 1.0 | | 1.1 | mA max | $V_S = \pm 55 \text{ V}$, $V_D = 0 \text{ V}$ |
| V_{DD} | | | 8 | V min | $GND = 0 \text{ V}$ |
| | | | 44 | V max | $GND = 0 \text{ V}$ |

¹ Guaranteed by design; not subject to production test.

36 V SINGLE SUPPLY

$V_{DD} = 36 \text{ V} \pm 10\%$, $V_{SS} = 0 \text{ V}$, $GND = 0 \text{ V}$, $C_{DECOUPLING} = 0.1 \mu\text{F}$, unless otherwise noted.

Table 4.

| Parameter | +25°C | −40°C to +85°C | −40°C to +125°C | Unit | Test Conditions/Comments |
|---|-------|----------------|-----------------|--------------|--|
| ANALOG SWITCH | | | | | $V_{DD} = 32.4 \text{ V}$, $V_{SS} = 0 \text{ V}$, see Figure 38 |
| Analog Signal Range | | | 0 V to V_{DD} | V | |
| On Resistance, R_{ON} | 310 | | | Ω typ | $V_S = 0 \text{ V}$ to 30 V, $I_S = -1 \text{ mA}$ |
| | 335 | 415 | 480 | Ω max | |
| | 250 | | | Ω typ | $V_S = 4.5 \text{ V}$ to 28 V, $I_S = -1 \text{ mA}$ |
| | 270 | 335 | 395 | Ω max | |
| On-Resistance Match Between Channels, ΔR_{ON} | 3 | | | Ω typ | $V_S = 0 \text{ V}$ to 30 V, $I_S = -1 \text{ mA}$ |
| | 7 | 16 | 18 | Ω max | |
| | 3 | | | Ω typ | $V_S = 4.5 \text{ V}$ to 28 V, $I_S = -1 \text{ mA}$ |
| | 6.5 | 11 | 12 | Ω max | |

| Parameter | +25°C | -40°C to +85°C | -40°C to +125°C | Unit | Test Conditions/Comments |
|--|------------------------|-----------------------|-----------------------|--|---|
| On-Resistance Flatness, $R_{FLAT(ON)}$ | 62 70 1.5 3.5 | 85 | 100 | Ω typ Ω max Ω typ Ω max | $V_S = 0\text{ V to }30\text{ V}$, $I_S = -1\text{ mA}$ $V_S = 4.5\text{ V to }28\text{ V}$, $I_S = -1\text{ mA}$ |
| Threshold Voltage, V_T | 0.7 | 4 | 4 | Ω max V typ | See Figure 30 |
| LEAKAGE CURRENTS | | | | | |
| Source Off Leakage, I_S (Off) | ± 0.1 ± 1 | ± 2 | ± 5 | nA typ nA max | $V_{DD} = 39.6\text{ V}$, $V_{SS} = 0\text{ V}$ $V_S = 1\text{ V}/30\text{ V}$, $V_D = 30\text{ V}/1\text{ V}$, see Figure 36 |
| Drain Off Leakage, I_D (Off) | ± 0.1 ± 1 | ± 5 | ± 10 | nA typ nA max | $V_S = 1\text{ V}/30\text{ V}$, $V_D = 30\text{ V}/1\text{ V}$, see Figure 36 |
| Channel On Leakage, I_D (On), I_S (On) | ± 0.3 ± 1.5 | ± 20 | ± 25 | nA typ nA max | $V_S = V_D = 1\text{ V}/30\text{ V}$, see Figure 37 |
| FAULT | | | | | |
| Source Leakage Current, I_S With Overvoltage | ± 58 | | | μA typ | $V_{DD} = 39.6\text{ V}$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, $V_S = +55\text{ V}$, -40 V, see Figure 35 |
| Power Supplies Grounded or Floating | ± 25 | | | μA typ | $V_{DD} = 0\text{ V}$ or floating, $V_{SS} = 0\text{ V}$ or floating, $GND = 0\text{ V}$, $A_X = 0\text{ V}$ or floating, $V_S = \pm 55\text{ V}$, see Figure 34 |
| Drain Leakage Current, I_D With Overvoltage | ± 10 | | | nA typ | $V_{DD} = 39.6\text{ V}$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, $V_S = +55\text{ V}$, -40 V, see Figure 35 |
| Power Supplies Grounded | ± 50 ± 500 | ± 70 | ± 90 | nA max nA typ | $V_{DD} = 0\text{ V}$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, $V_S = \pm 55\text{ V}$, $A_X = 0\text{ V}$, see Figure 34 |
| Power Supplies Floating | ± 700 ± 50 | ± 700 ± 50 | ± 700 ± 50 | nA max μA typ | $V_{DD} = \text{floating}$, $V_{SS} = \text{floating}$, $GND = 0\text{ V}$, $V_S = \pm 55\text{ V}$, $A_X = 0\text{ V}$, see Figure 34 |
| DIGITAL INPUTS | | | | | |
| Input Voltage High, V_{INH} Low, V_{INL} | | | 2.0 0.8 | V min V max | |
| Input Current, I_{INL} or I_{INH} | ± 0.7 ± 1.1 | | ± 1.2 | μA typ μA max | $V_{IN} = V_{GND}$ or V_{DD} |
| Digital Input Capacitance, C_{IN} | 5.0 | | | pF typ | |
| Output Voltage High, V_{OH} Low, V_{OL} | 2.0 0.8 | | | V min V max | |
| DYNAMIC CHARACTERISTICS ¹ | | | | | |
| Transition Time, $t_{TRANSITION}$ | 195 255 | 275 | 285 | ns typ ns max | $R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$ $V_S = 18\text{ V}$, see Figure 50 |
| t_{ON} (EN) | 190 245 | 270 | 280 | ns typ ns max | $R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$ $V_S = 18\text{ V}$, see Figure 49 |
| t_{OFF} (EN) | 105 135 | 145 | 145 | ns typ ns max | $R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$ $V_S = 18\text{ V}$, see Figure 49 |
| Break-Before-Make Time Delay, t_D | 110 | | 60 | ns typ ns min | $R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$ $V_S = 18\text{ V}$, see Figure 48 |
| Overvoltage Response Time, $t_{RESPONSE}$ | 60 80 | 85 | 85 | ns typ ns max | $R_L = 1\text{ k}\Omega$, $C_L = 5\text{ pF}$, see Figure 43 |
| Overvoltage Recovery Time, $t_{RECOVERY}$ | 1400 1900 | 2100 | 2200 | ns typ ns max | $R_L = 1\text{ k}\Omega$, $C_L = 5\text{ pF}$, see Figure 44 |

| Parameter | +25°C | -40°C to +85°C | -40°C to +125°C | Unit | Test Conditions/Comments |
|---|-------|----------------|-----------------|-------------|--|
| Interrupt Flag Response Time, $t_{DIGRESP}$ | 85 | | | ns typ | $C_L = 12$ pF, see Figure 45 |
| Interrupt Flag Recovery Time, t_{DIGREC} | 65 | | | μ s typ | $C_L = 12$ pF, see Figure 46 |
| | 1600 | | | ns typ | $C_L = 12$ pF, $R_{PULLUP} = 1$ k Ω , see Figure 47 |
| Charge Injection, Q_{INJ} | -1.2 | | | pC typ | $V_S = 18$ V, $R_S = 0$ Ω , $C_L = 1$ nF, see Figure 51 |
| Off Isolation | -75 | | | dB typ | $R_L = 50$ Ω , $C_L = 5$ pF, $f = 1$ MHz, see Figure 41, worst case channel |
| Channel-to-Channel Crosstalk | | | | | $R_L = 50$ Ω , $C_L = 5$ pF, $f = 1$ MHz, see Figure 40 |
| Adjacent Channels | -75 | | | dB typ | |
| Nonadjacent Channels | -88 | | | dB typ | |
| Total Harmonic Distortion Plus Noise, THD + N | 0.007 | | | % typ | $R_L = 10$ k Ω , $V_S = 18$ V p-p, $f = 20$ Hz to 20 kHz, see Figure 39 |
| -3 dB Bandwidth | | | | | $R_L = 50$ Ω , $C_L = 5$ pF, see Figure 42 |
| ADG5248F | 200 | | | MHz typ | |
| ADG5249F | 320 | | | MHz typ | |
| Insertion Loss | 10.5 | | | dB typ | $R_L = 50$ Ω , $C_L = 5$ pF, $f = 1$ MHz, see Figure 42 |
| C_S (Off) | 4 | | | pF typ | $V_S = 18$ V, $f = 1$ MHz |
| C_D (Off) | | | | | $V_S = 18$ V, $f = 1$ MHz |
| ADG5248F | 13 | | | pF typ | |
| ADG5249F | 7 | | | pF typ | |
| C_D (On), C_S (On) | | | | | $V_S = 18$ V, $f = 1$ MHz |
| ADG5248F | 18 | | | pF typ | |
| ADG5249F | 12 | | | pF typ | |
| POWER REQUIREMENTS | | | | | $V_{DD} = 39.6$ V; $V_{SS} = 0$ V; digital inputs = 0 V, 5 V, or V_{DD} |
| Normal Mode | | | | | |
| I_{DD} | 1.15 | | | mA typ | |
| I_{POSFV} | 0.15 | | | mA typ | |
| $I_{DD} + I_{POSFV}$ | 2 | | 2 | mA max | |
| I_{GND} | 0.75 | | | mA typ | |
| I_{SS} | 1.4 | | 1.4 | mA max | |
| I_{SS} | 0.3 | | | mA typ | |
| I_{NEGFV} | 0.2 | | | mA typ | |
| $I_{SS} + I_{NEGFV}$ | 0.65 | | 0.7 | mA max | |
| Fault Mode | | | | | $V_S = +55$ V, -40 V |
| I_{DD} | 1.4 | | | mA typ | |
| I_{POSFV} | 0.2 | | | mA typ | |
| $I_{DD} + I_{POSFV}$ | 2.2 | | 2.3 | mA max | |
| I_{GND} | 0.9 | | | mA typ | |
| I_{SS} | 1.6 | | 1.7 | mA max | |
| I_{SS} | 0.45 | | | mA typ | |
| I_{NEGFV} | 0.2 | | | mA typ | |
| $I_{SS} + I_{NEGFV}$ | 1.0 | | 1.1 | mA max | |
| V_{DD} | | | 8 | V min | GND = 0 V |
| | | | 44 | V max | GND = 0 V |

¹ Guaranteed by design; not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, S_x,¹ D, OR D_x

Table 5.

| Parameter | 25°C | 85°C | 125°C | Unit | Test Conditions/Comments |
|--|------|------|-------|--------|---|
| ADG5248F | | | | | |
| 20-Lead TSSOP, $\theta_{JA} = 112.6^{\circ}\text{C/W}$ | 27 | 16 | 8 | mA max | $V_S = V_{SS}$ to $V_{DD} - 4.5\text{ V}$ |
| | 16 | 11 | 7 | mA max | $V_S = V_{SS}$ to V_{DD} |
| 20-Lead LFCSP, $\theta_{JA} = 30.4^{\circ}\text{C/W}$ | 48 | 25 | 11 | mA max | $V_S = V_{SS}$ to $V_{DD} - 4.5\text{ V}$ |
| | 27 | 17 | 9 | mA max | $V_S = V_{SS}$ to V_{DD} |
| ADG5249F | | | | | |
| 20-Lead TSSOP, $\theta_{JA} = 112.6^{\circ}\text{C/W}$ | 20 | 13 | 8 | mA max | $V_S = V_{SS}$ to $V_{DD} - 4.5\text{ V}$ |
| | 12 | 8 | 6 | mA max | $V_S = V_{SS}$ to V_{DD} |
| 20-Lead LFCSP, $\theta_{JA} = 30.4^{\circ}\text{C/W}$ | 36 | 20 | 10 | mA max | $V_S = V_{SS}$ to $V_{DD} - 4.5\text{ V}$ |
| | 21 | 13 | 8 | mA max | $V_S = V_{SS}$ to V_{DD} |

¹ S_x is the S1 to S8 pins on the [ADG5248F](#), and the S1A to S4A and S1B to S4B pins on the [ADG5249F](#).

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

| Parameter | Rating |
|--|---|
| V _{DD} to V _{SS} | 48 V |
| V _{DD} to GND | -0.3 V to +48 V |
| V _{SS} to GND | -48 V to +0.3 V |
| POSFV to GND | -0.3 V to V _{DD} + 0.3 V |
| NEGFV to GND | V _{SS} - 0.3 V to + 0.3 V |
| Sx Pins | -55 V to +55 V |
| Sx to V _{DD} or V _{SS} | 80 V |
| V _S to V _D | 80 V |
| D or Dx Pins ¹ | NEGFV - 0.7 V to POSFV + 0.7 V or 30 mA, whichever occurs first |
| Digital Inputs | GND - 0.7 V to 48 V or 30 mA, whichever occurs first |
| Peak Current, Sx, D, or Dx Pins | 72.5 mA (pulsed at 1 ms, 10% duty cycle maximum) |
| Continuous Current, Sx, D, or Dx Pins | Data ² + 15% |
| Digital Outputs | GND - 0.7 V to 6 V or 30 mA, whichever occurs first |
| D or Dx Pins, Overvoltage State, Load Current | 1 mA |
| Operating Temperature Range | -40°C to +125°C |
| Storage Temperature Range | -65°C to +150°C |
| Junction Temperature | 150°C |
| Thermal Impedance, θ_{JA} (4-Layer Board) | |
| 20-Lead TSSOP | 112.6°C/W |
| 20-Lead LFCSP | 30.4°C/W |
| Reflow Soldering Peak Temperature, Pb-Free | As per JEDEC J-STD-020 |

¹ Overvoltages at the D or Dx pins are clamped by internal diodes. Limit the current to the maximum ratings given.

² See Table 5.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

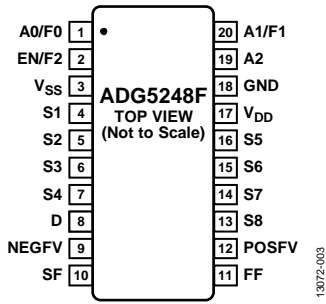
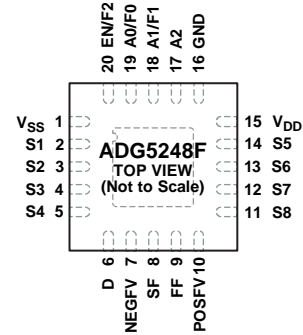


Figure 3. ADG5248F Pin Configuration (TSSOP)



NOTES
 1. THE EXPOSED PAD IS CONNECTED INTERNALLY. FOR INCREASED RELIABILITY OF THE SOLDER JOINTS AND MAXIMUM THERMAL CAPABILITY, IT IS RECOMMENDED THAT THE PAD BE SOLDERED TO THE SUBSTRATE, V_{SS}.

Figure 4. ADG5248F Pin Configuration (LFCSP)

Table 7. ADG5248F Pin Function Descriptions

| Pin No. | | Mnemonic | Description |
|----------------|-------------|-----------------|--|
| TSSOP | LFCSP | | |
| 1 | 19 | A0/F0 | Logic Control Input (A0). See Table 8. Decoder Pin (F0). This pin is used together with the specific fault pin (SF) to indicate which input is in a fault condition. See Table 9. |
| 2 | 20 | EN/F2 | Active High Digital Input (EN). When this pin is low, the device is disabled and all switches are off. When this pin is high, the Ax logic inputs determine the on switches. Decoder Pin (F2). This pin is used together with the specific fault pin (SF) to indicate which input is in a fault condition. See Table 9. |
| 3 | 1 | V _{SS} | Most Negative Power Supply Potential. |
| 4 | 2 | S1 | Overvoltage Protected Source Terminal 1. This pin can be an input or an output. |
| 5 | 3 | S2 | Overvoltage Protected Source Terminal 2. This pin can be an input or an output. |
| 6 | 4 | S3 | Overvoltage Protected Source Terminal 3. This pin can be an input or an output. |
| 7 | 5 | S4 | Overvoltage Protected Source Terminal 4. This pin can be an input or an output. |
| 8 | 6 | D | Drain Terminal. This pin can be an input or an output. |
| 9 | 7 | NEGFV | Negative Fault Voltage. This pin is the negative supply voltage that determines the overvoltage protection level. If a secondary supply is not used, connect this pin to V _{SS} . |
| 10 | 8 | SF | Specific Fault Digital Output. This pin has a high output (weak internal pull-up resistor, nominally 3 V output) when the device is in normal operation, or a low output when a fault condition is detected on a specific pin, depending on the state of F0, F1, and F2 as shown in Table 9. |
| 11 | 9 | FF | Fault Flag Digital Output. This pin has a high output when the device is in normal operation, or a low output when a fault condition occurs on any of the Sx inputs. The FF pin has a weak internal pull-up resistor that allows multiple signals to be combined into a single interrupt for larger modules that contain multiple devices. |
| 12 | 10 | POSFV | Positive Fault Voltage. This pin is the positive supply voltage that determines the overvoltage protection level. If a secondary supply is not used, connect this pin to V _{DD} . |
| 13 | 11 | S8 | Overvoltage Protected Source Terminal 8. This pin can be an input or an output. |
| 14 | 12 | S7 | Overvoltage Protected Source Terminal 7. This pin can be an input or an output. |
| 15 | 13 | S6 | Overvoltage Protected Source Terminal 6. This pin can be an input or an output. |
| 16 | 14 | S5 | Overvoltage Protected Source Terminal 5. This pin can be an input or an output. |
| 17 | 15 | V _{DD} | Most Positive Power Supply Potential. |
| 18 | 16 | GND | Ground (0 V) Reference. |
| 19 | 17 | A2 | Logic Control Input. |
| 20 | 18 | A1/F1 | Logic Control Input (A1). See Table 8. Decoder Pin (F1). This pin is used together with the specific fault pin (SF) to indicate which input is in a fault condition. See Table 9. |
| Not Applicable | Exposed Pad | EP | Exposed Pad. The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V _{SS} . |

Table 8. ADG5248F Switch Selection Truth Table

| A2 | A1 | A0 | EN | On Switch |
|----------------|----------------|----------------|----|-----------|
| X ¹ | X ¹ | X ¹ | 0 | None |
| 0 | 0 | 0 | 1 | S1 |
| 0 | 0 | 1 | 1 | S2 |
| 0 | 1 | 0 | 1 | S3 |
| 0 | 1 | 1 | 1 | S4 |
| 1 | 0 | 0 | 1 | S5 |
| 1 | 0 | 1 | 1 | S6 |
| 1 | 1 | 0 | 1 | S7 |
| 1 | 1 | 1 | 1 | S8 |

¹ X is don't care.

Table 9. ADG5248F Fault Diagnostic Output Truth Table

| Switch in Fault ¹ | State of Specific Flag (SF) with Control Inputs (F2, F1, F0) | | | | | | | | State of the Fault Flag (FF) |
|------------------------------|--|---------|---------|---------|---------|---------|---------|---------|------------------------------|
| | 0, 0, 0 | 0, 0, 1 | 0, 1, 0 | 0, 1, 1 | 1, 0, 0 | 1, 0, 1 | 1, 1, 0 | 1, 1, 1 | |
| None | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| S1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| S2 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| S3 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| S4 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| S5 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| S6 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| S7 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| S8 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |

¹ More than one switch can be in fault. See the Applications Information section for more information.

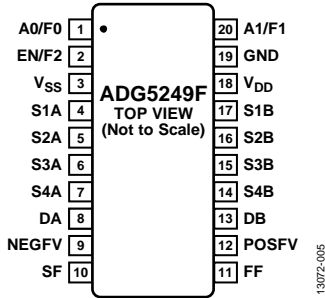
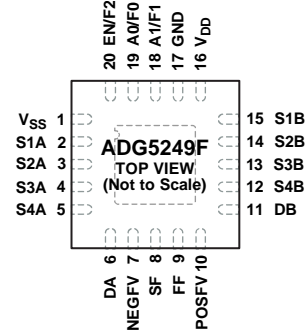


Figure 5. ADG5249F Pin Configuration (TSSOP)



NOTES
 1. THE EXPOSED PAD IS CONNECTED INTERNALLY. FOR INCREASED RELIABILITY OF THE SOLDER JOINTS AND MAXIMUM THERMAL CAPABILITY, IT IS RECOMMENDED THAT THE PAD BE SOLDERED TO THE SUBSTRATE, V_{SS}.

Figure 6. ADG5249F Pin Configuration (LFCSP)

Table 10. ADG5249F Pin Function Descriptions

| Pin No. | | Mnemonic | Description |
|----------------|-------------|-----------------|--|
| TSSOP | LFCSP | | |
| 1 | 19 | A0/F0 | Logic Control Input (A0). See Table 11. Decoder Pin (F0). This pin is used together with the specific fault pin (SF) to indicate which input is in a fault condition. See Table 12. |
| 2 | 20 | EN/F2 | Active High Digital Input (EN). When this pin is low, the device is disabled and all switches are off. When this pin is high, the Ax logic inputs determine the on switches. Decoder Pin (F2). This pin is used together with the specific fault pin (SF) to indicate which input is in a fault condition. See Table 12. |
| 3 | 1 | V _{SS} | Most Negative Power Supply Potential. |
| 4 | 2 | S1A | Overvoltage Protected Source Terminal 1A. This pin can be an input or an output. |
| 5 | 3 | S2A | Overvoltage Protected Source Terminal 2A. This pin can be an input or an output. |
| 6 | 4 | S3A | Overvoltage Protected Source Terminal 3A. This pin can be an input or an output. |
| 7 | 5 | S4A | Overvoltage Protected Source Terminal 4A. This pin can be an input or an output. |
| 8 | 6 | DA | Drain Terminal A. This pin can be an input or an output. |
| 9 | 7 | NEG FV | Negative Fault Voltage. This pin is the negative supply voltage that determines the overvoltage protection level. If a secondary supply is not used, connect this pin to V _{SS} . |
| 10 | 8 | SF | Specific Fault Digital Output. This pin has a high output (weak internal pull-up resistor, nominally 3 V output) when the device is in normal operation, or a low output when a fault condition is detected on a specific pin, depending on the state of F0, F1, and, F2 as shown in Table 12. |
| 11 | 9 | FF | Fault Flag Digital Output. This pin has a high output when the device is in normal operation, or a low output when a fault condition occurs on any of the Sx inputs. The FF pin has a weak internal pull-up resistor that allows multiple signals to be combined into a single interrupt for larger modules that contain multiple devices. |
| 12 | 10 | POS FV | Positive Fault Voltage. This pin is the positive supply voltage that determines the overvoltage protection level. If a secondary supply is not used, connect this pin to V _{DD} . |
| 13 | 11 | DB | Drain Terminal B. This pin can be an input or an output. |
| 14 | 12 | S4B | Overvoltage Protected Source Terminal 4B. This pin can be an input or an output. |
| 15 | 13 | S3B | Overvoltage Protected Source Terminal 3B. This pin can be an input or an output. |
| 16 | 14 | S2B | Overvoltage Protected Source Terminal 2B. This pin can be an input or an output. |
| 17 | 15 | S1B | Overvoltage Protected Source Terminal 1B. This pin can be an input or an output. |
| 18 | 16 | V _{DD} | Most Positive Power Supply Potential. |
| 19 | 17 | GND | Ground (0 V) Reference. |
| 20 | 18 | A1/F1 | Logic Control Input (A1). See Table 11. Decoder Pin (F1). This pin is used together with the specific fault pin (SF) to indicate which input is in a fault condition. See Table 12. |
| Not Applicable | Exposed Pad | EP | Exposed Pad. The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V _{SS} . |

Table 11. ADG5249F Switch Selection Truth Table

| A1 | A0 | EN | On Switch Pair |
|----------------|----------------|----|----------------|
| X ¹ | X ¹ | 0 | None |
| 0 | 0 | 1 | S1x |
| 0 | 1 | 1 | S2x |
| 1 | 0 | 1 | S3x |
| 1 | 1 | 1 | S4x |

¹ X is don't care.

Table 12. ADG5249F Fault Diagnostic Output Truth Table

| Switch in Fault ¹ | State of Specific Flag (SF) with Control Inputs (F2, F1, F0) | | | | | | | | State of the Fault Flag (FF) |
|------------------------------|--|---------|---------|---------|---------|---------|---------|---------|------------------------------|
| | 0, 0, 0 | 0, 0, 1 | 0, 1, 0 | 0, 1, 1 | 1, 0, 0 | 1, 0, 1 | 1, 1, 0 | 1, 1, 1 | |
| None | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| S1A | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| S2A | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| S3A | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| S4A | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| S1B | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| S2B | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| S3B | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| S4B | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |

¹ More than one switch can be in fault. See the Applications Information section for more information.

TYPICAL PERFORMANCE CHARACTERISTICS

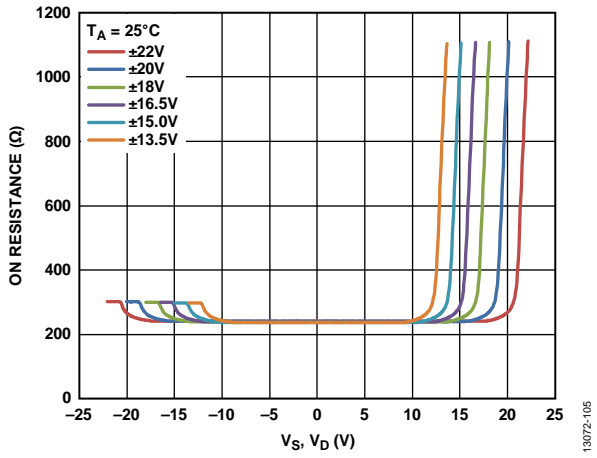


Figure 7. R_{ON} as a Function of V_S, V_D , Dual Supply

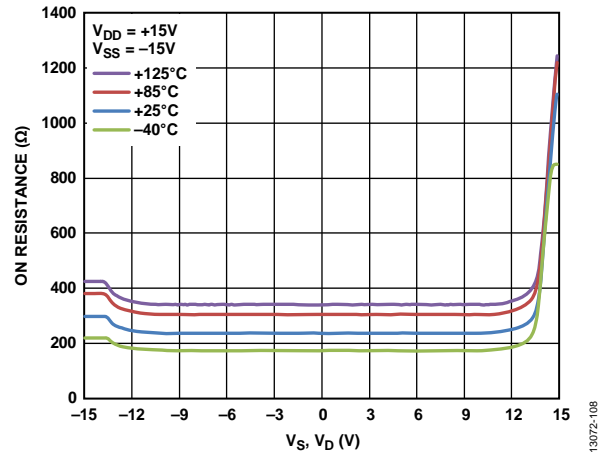


Figure 10. R_{ON} as a Function of V_S, V_D for Different Temperatures, ± 15 V Dual Supply

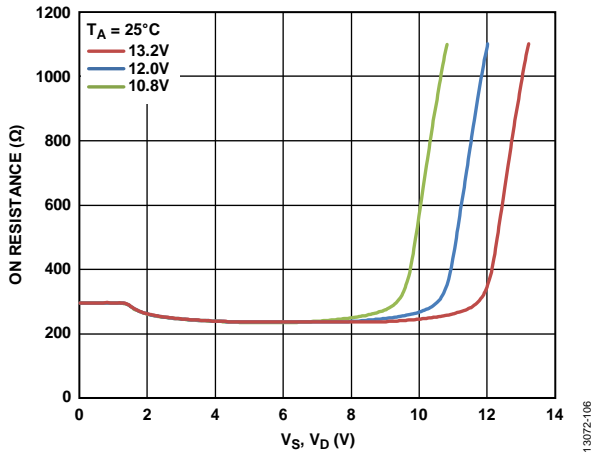


Figure 8. R_{ON} as a Function of V_S, V_D , 12 V Single Supply

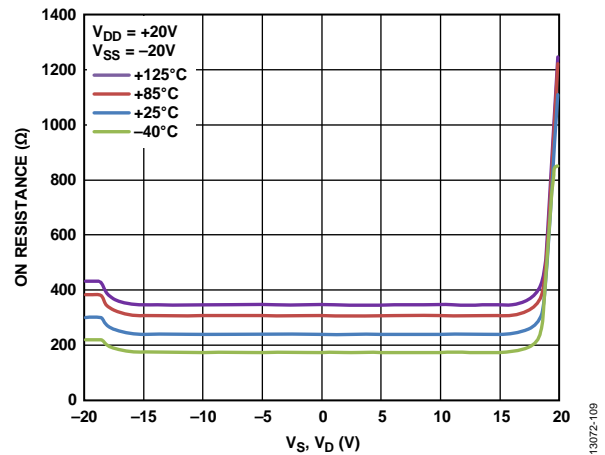


Figure 11. R_{ON} as a Function of V_S, V_D for Different Temperatures, ± 20 V Dual Supply

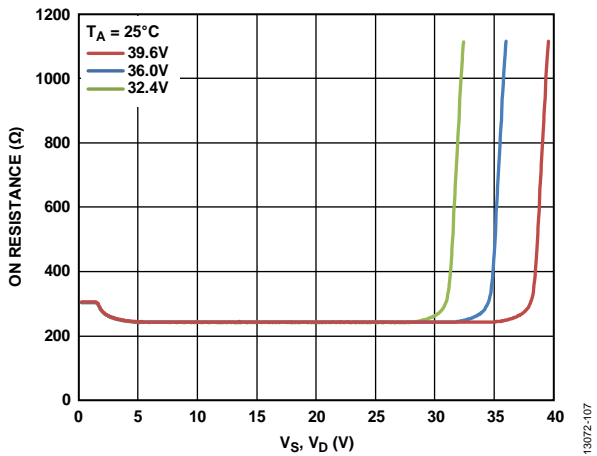


Figure 9. R_{ON} as a Function of V_S, V_D , 36 V Single Supply

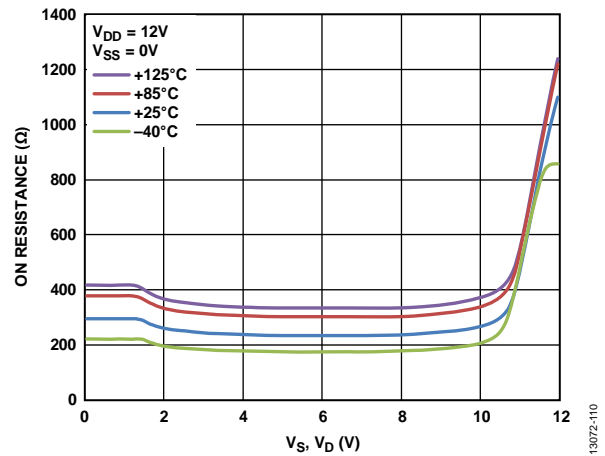


Figure 12. R_{ON} as a Function of V_S, V_D for Different Temperatures, 12 V Single Supply

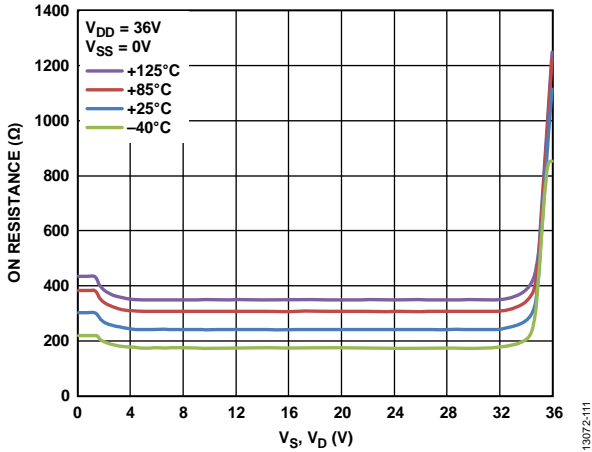


Figure 13. R_{ON} as a Function of V_S , V_D for Different Temperatures, 36 V Single Supply

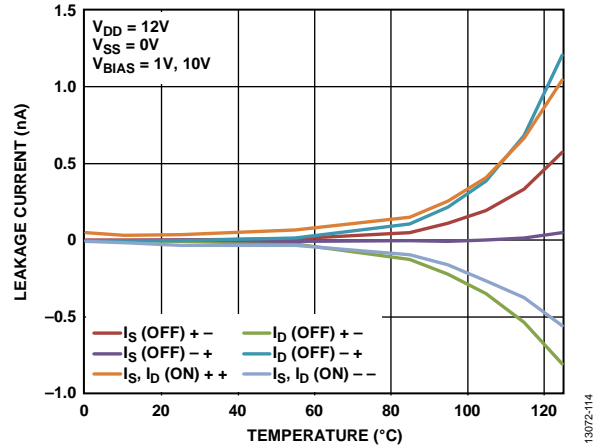


Figure 16. Leakage Current vs. Temperature, 12 V Single Supply

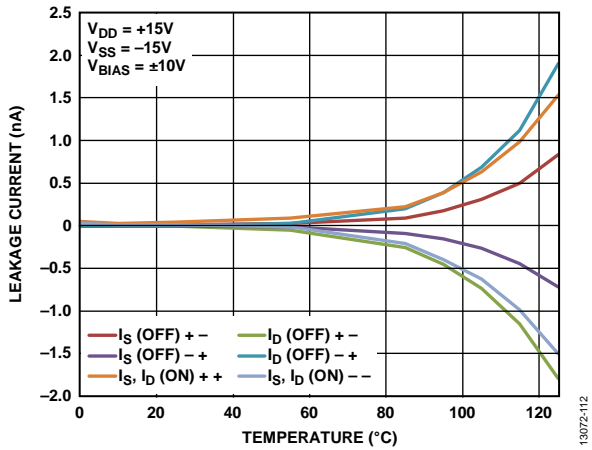


Figure 14. Leakage Current vs. Temperature, ±15 V Dual Supply

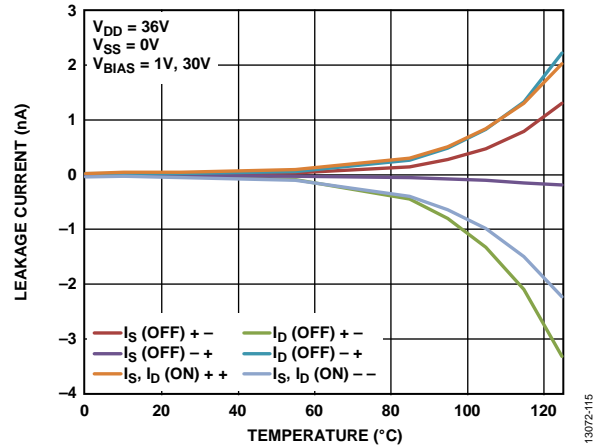


Figure 17. Leakage Current vs. Temperature, 36 V Single Supply

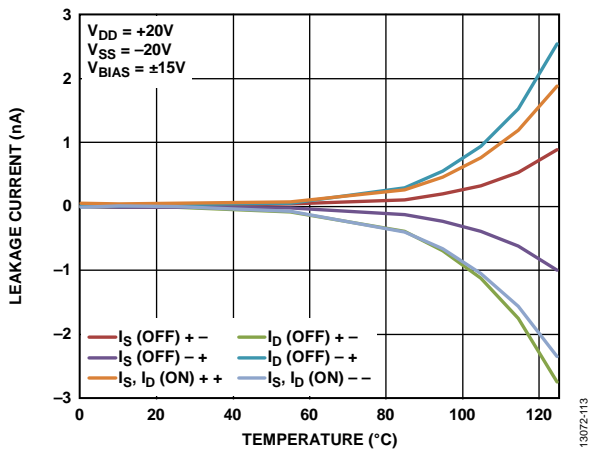


Figure 15. Leakage Current vs. Temperature, ±20 V Dual Supply

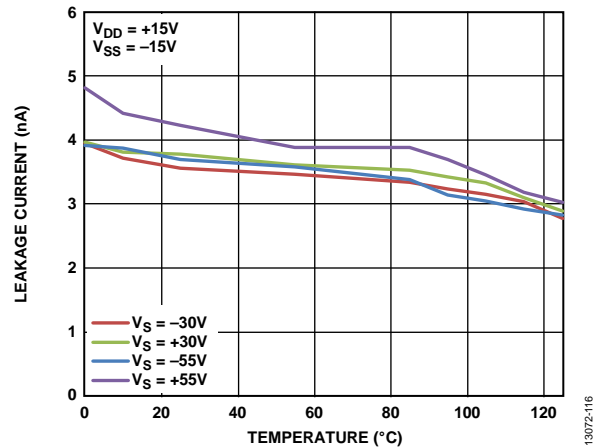


Figure 18. Overvoltage Leakage Current vs. Temperature, ±15 V Dual Supply

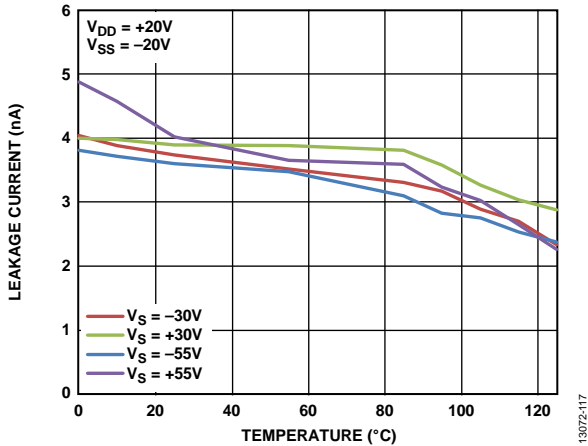


Figure 19. Overvoltage Leakage Current vs. Temperature, ±20 V Dual Supply

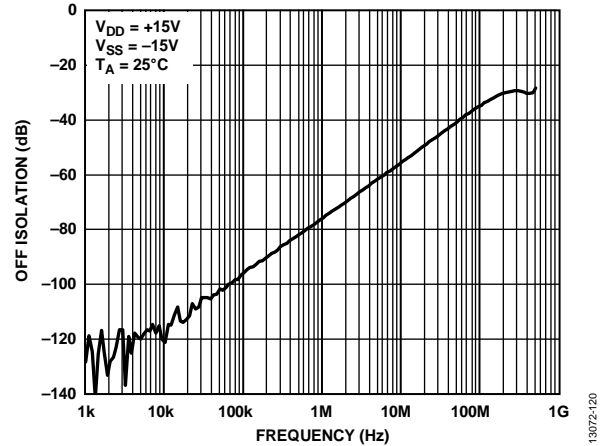


Figure 22. Off Isolation vs. Frequency, ±15 V Dual Supply

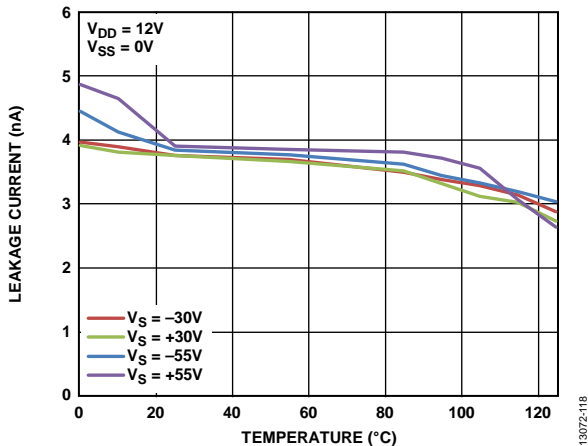


Figure 20. Overvoltage Leakage Current vs. Temperature, 12 V Single Supply

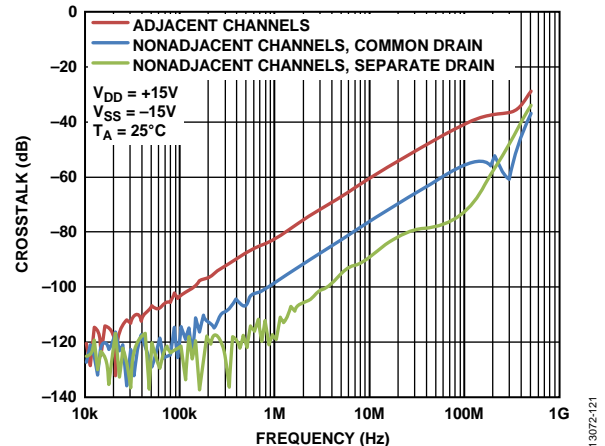


Figure 23. Crosstalk vs. Frequency, ±15 V Dual Supply

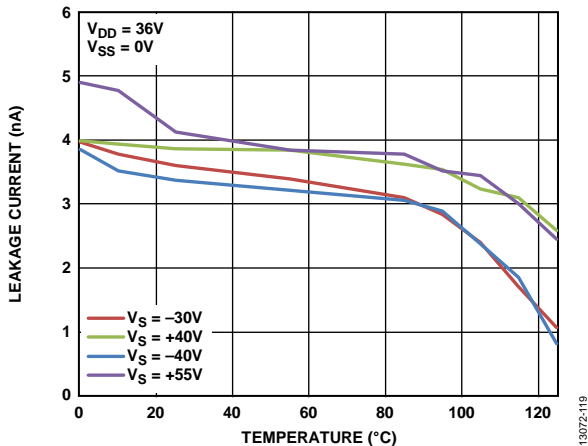


Figure 21. Overvoltage Leakage Current vs. Temperature, 36 V Single Supply

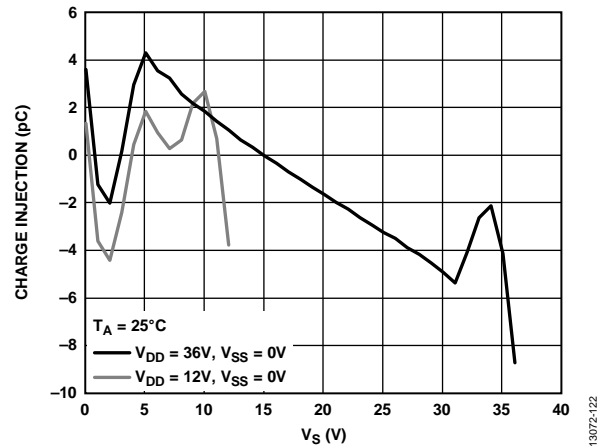


Figure 24. Charge Injection vs. Source Voltage (V_S), Single Supply

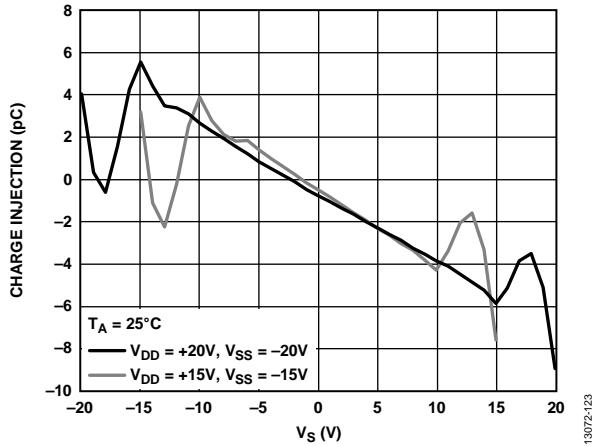


Figure 25. Charge Injection vs. Source Voltage (V_S), Dual Supply

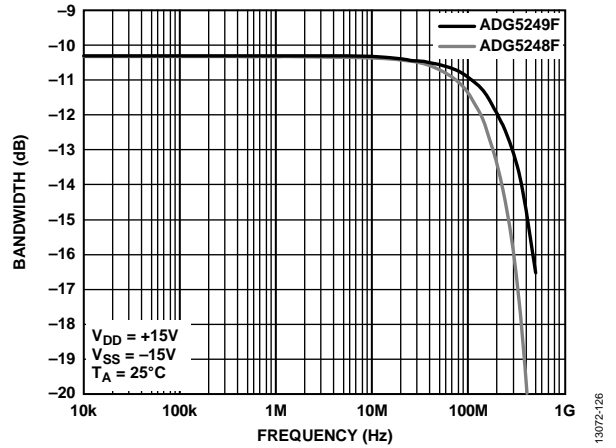


Figure 28. Bandwidth vs. Frequency

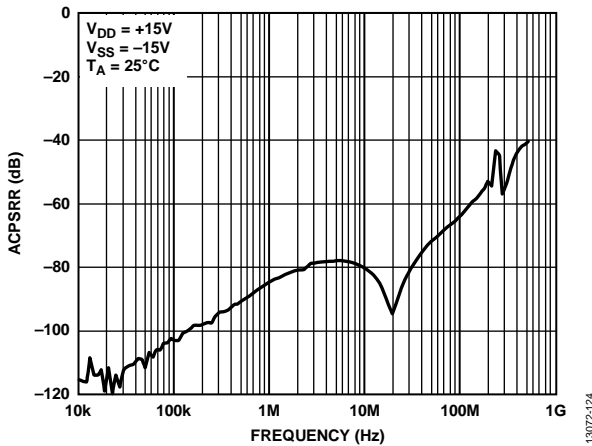


Figure 26. ACPSRR vs. Frequency, ± 15 V Dual Supply

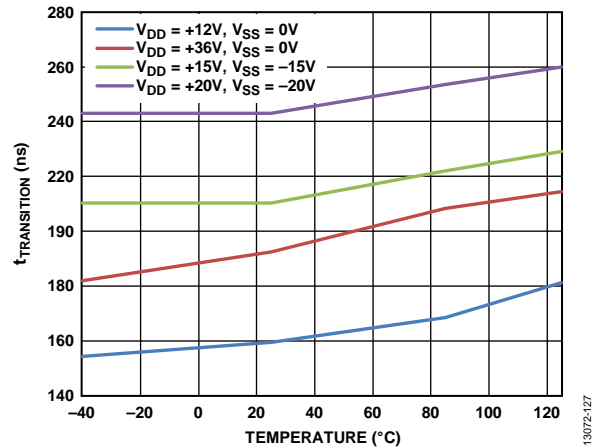


Figure 29. $t_{TRANSITION}$ vs. Temperature

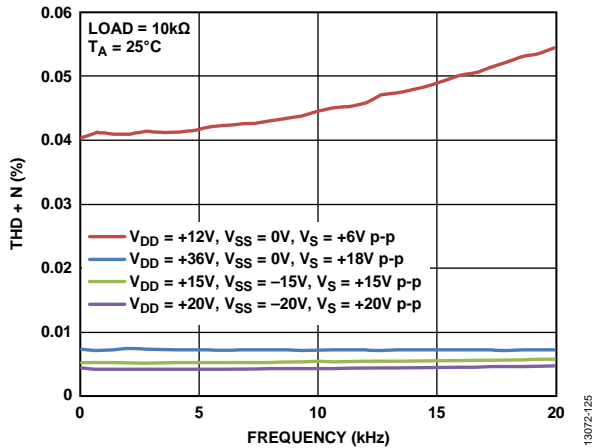


Figure 27. THD + N vs. Frequency

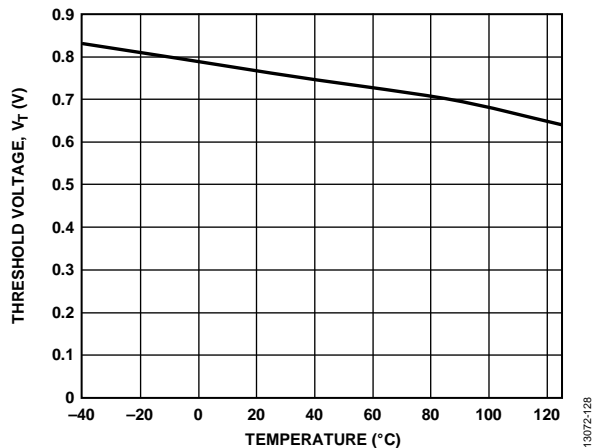


Figure 30. Threshold Voltage (V_T) vs. Temperature

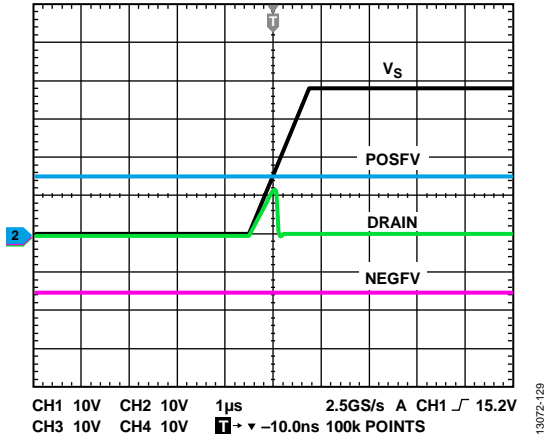


Figure 31. Drain Output Response to Positive Overvoltage

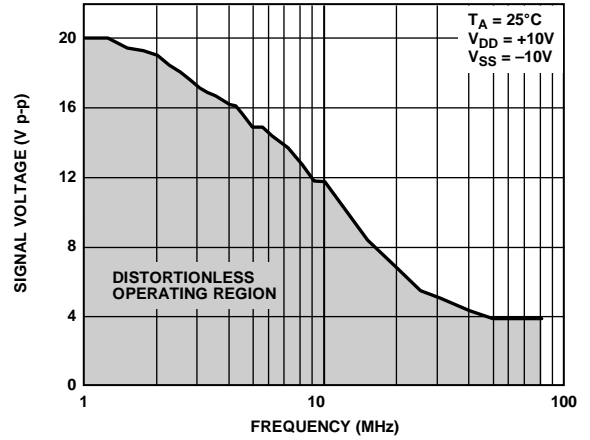


Figure 33. Large Signal Voltage Tracking vs. Frequency

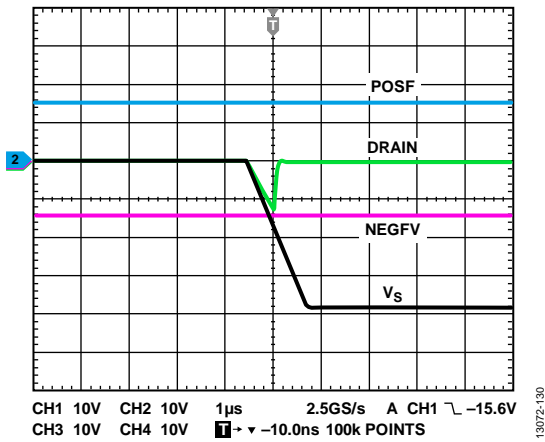


Figure 32. Drain Output Response to Negative Overvoltage

TEST CIRCUITS

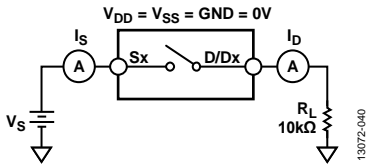


Figure 34. Switch Unpowered Leakage

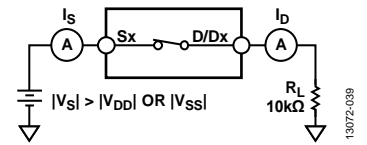
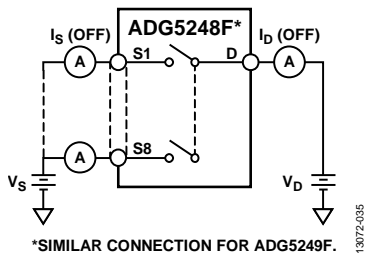


Figure 35. Switch Overvoltage Leakage



*SIMILAR CONNECTION FOR ADG5249F.

Figure 36. Off Leakage

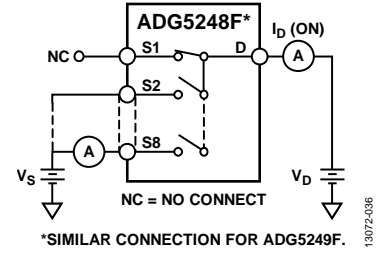


Figure 37. On Leakage

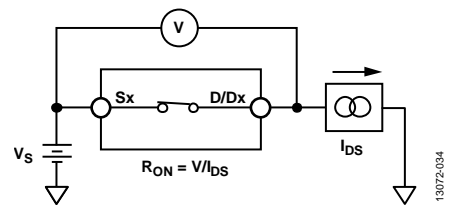


Figure 38. On Resistance

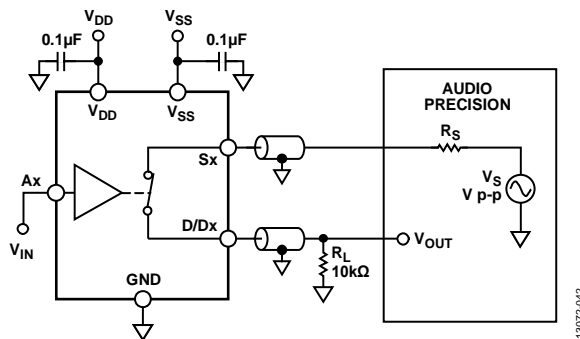
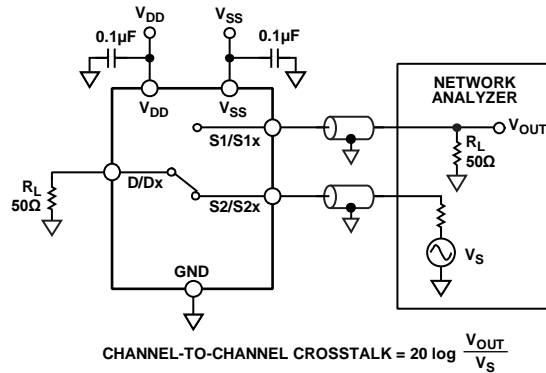
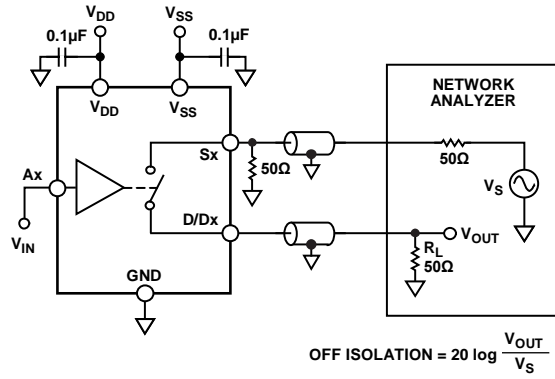


Figure 39. THD + N



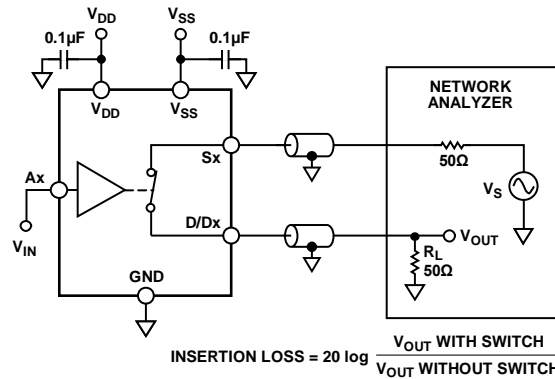
$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \log \frac{V_{OUT}}{V_S}$$

Figure 40. Channel-to-Channel Crosstalk



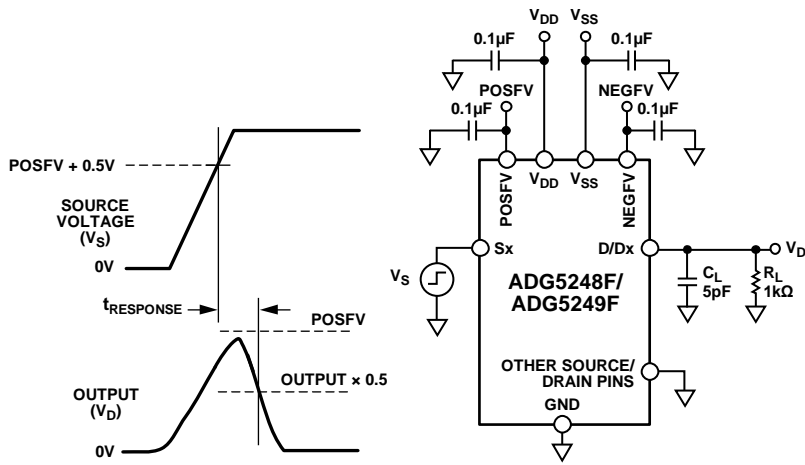
13072-037

Figure 41. Off Isolation



13072-041

Figure 42. Bandwidth

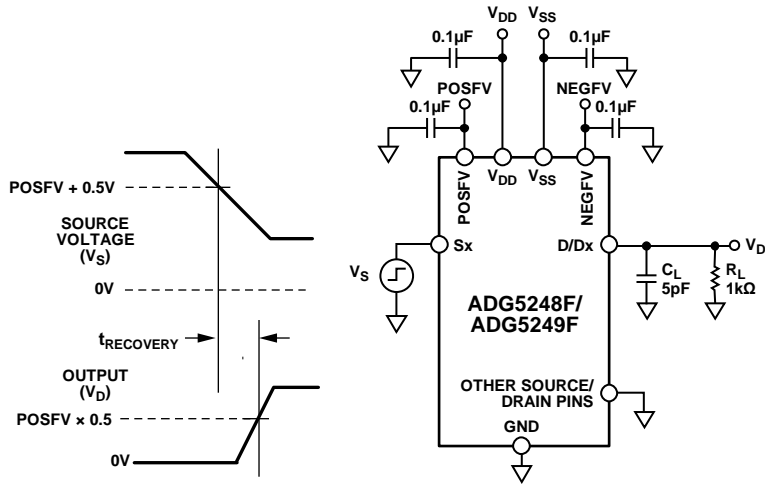


NOTES

1. THE OUTPUT PULLS TO V_{DD} WITHOUT A 1kΩ RESISTOR (INTERNAL 40kΩ PULL-UP RESISTOR TO THE SUPPLY RAIL DURING A FAULT).

Figure 43. Overtolerance Response Time, $t_{RESPONSE}$

13072-043



NOTES
 1. THE OUTPUT STARTS FROM THE POSFV CLAMP LEVEL WITHOUT A 1kΩ RESISTOR (INTERNAL 40kΩ PULL-UP RESISTOR TO THE POSFV SUPPLY RAIL DURING A FAULT).

Figure 44. Overtolerance Recovery Time, $t_{RECOVERY}$

13072-044

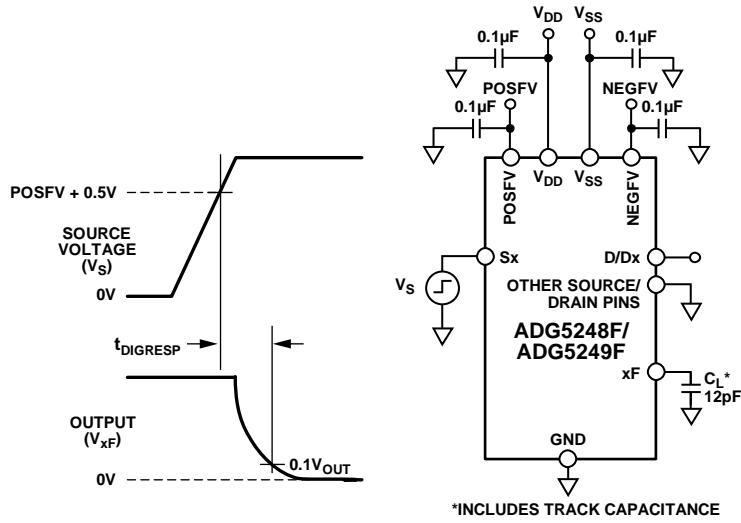


Figure 45. Interrupt Flag Response Time, $t_{DIGRESP}$

13072-058

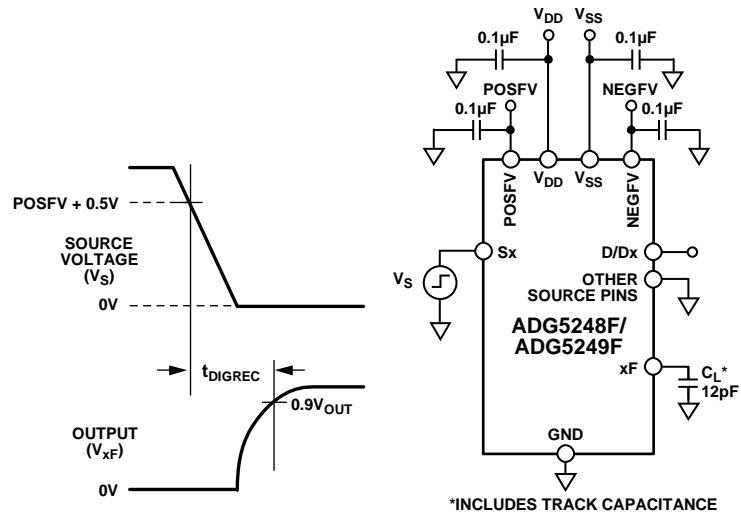


Figure 46. Interrupt Flag Recovery Time, t_{DIGREC}

13072-056

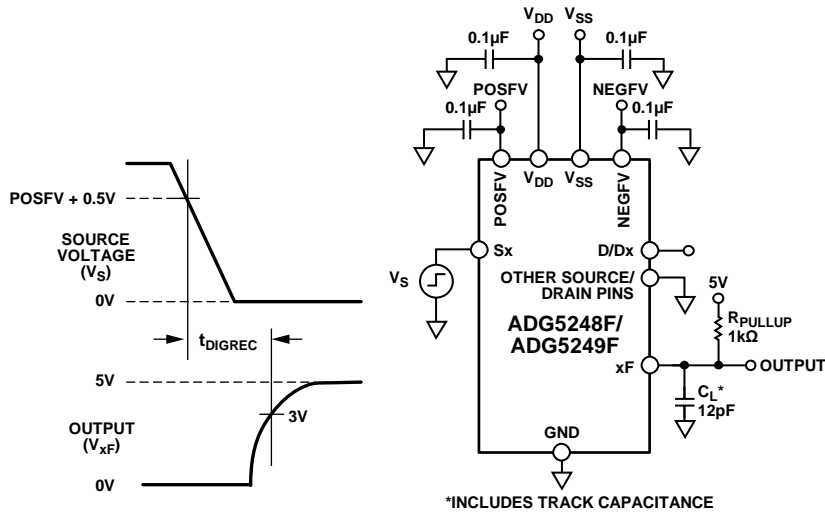


Figure 47. Interrupt Flag Recovery Time, t_{DIGREC} , with a 1 kΩ Pull-Up Resistor

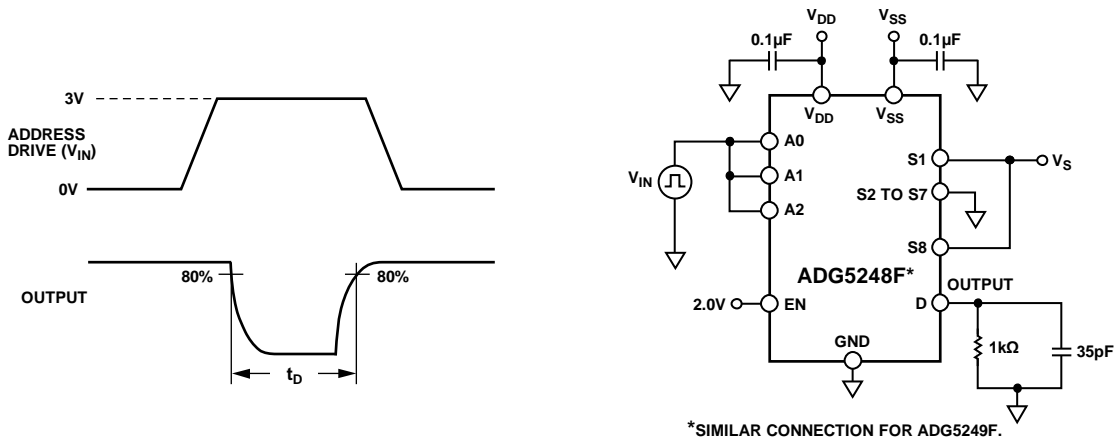


Figure 48. Break-Before-Make Time Delay, t_D

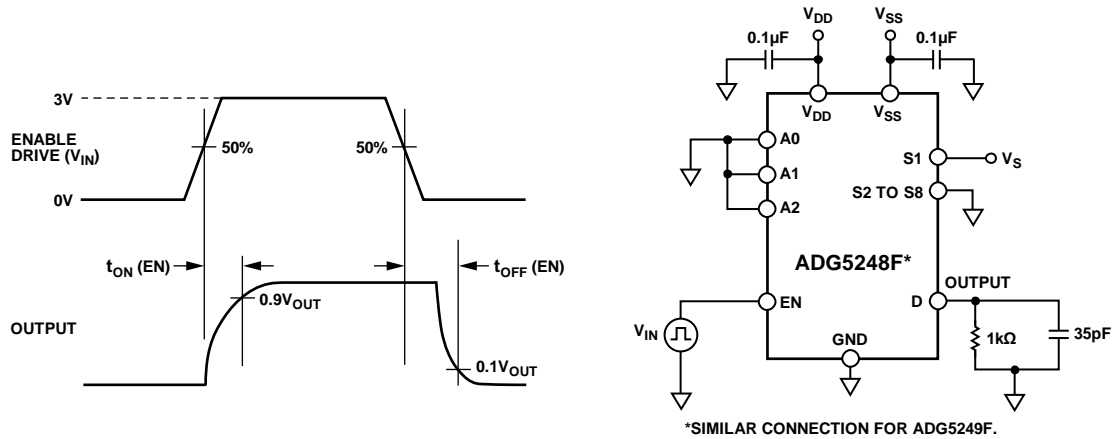


Figure 49. Enable Delay, $t_{ON}(EN)$, $t_{OFF}(EN)$

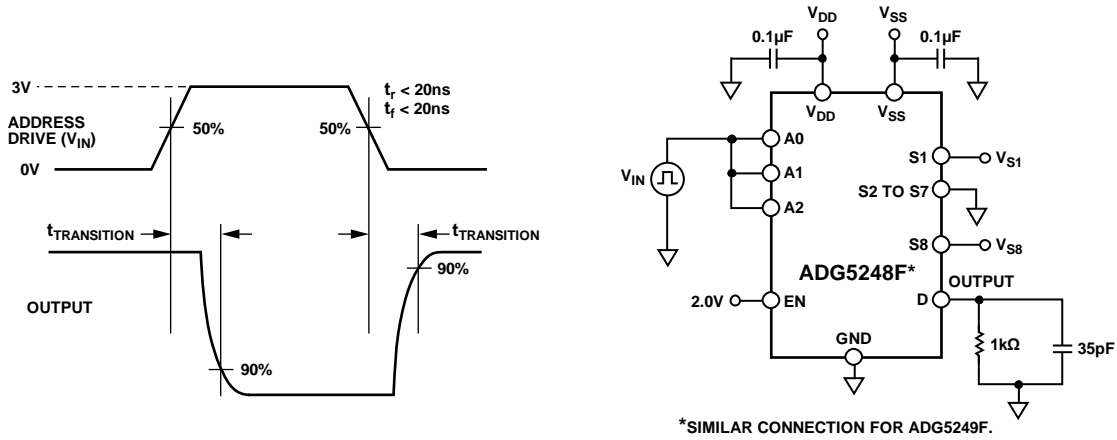


Figure 50. Address to Output Switching Time, $t_{TRANSITION}$

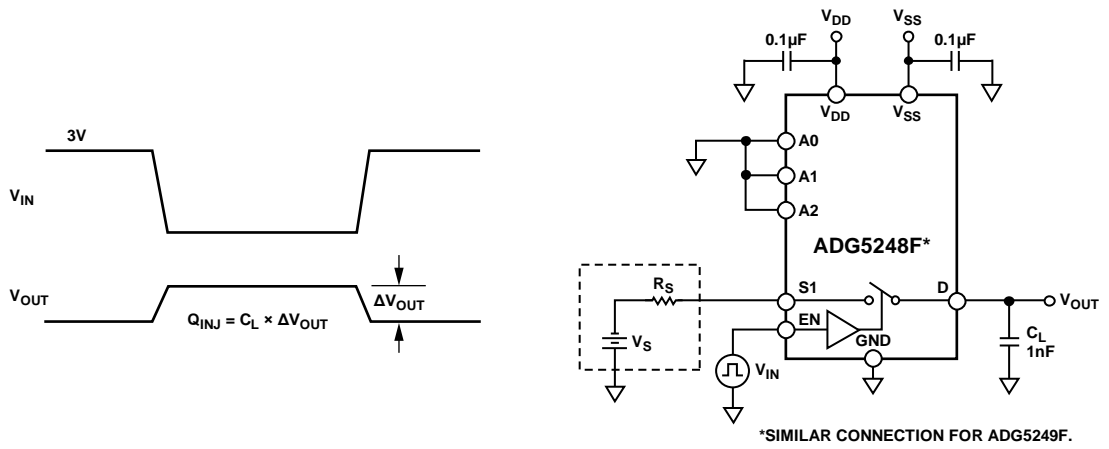


Figure 51. Charge Injection, Q_{INJ}

TERMINOLOGY

I_{DD}

I_{DD} represents the positive supply current.

I_{SS}

I_{SS} represents the negative supply current.

I_{POSFV}

I_{POSFV} represents the positive secondary supply current.

I_{NEGFV}

I_{NEGFV} represents the negative secondary supply current.

V_D, V_S

V_D and V_S represent the analog voltage on the D or Dx pins and the Sx pins, respectively.

R_{ON}

R_{ON} represents the ohmic resistance between the D or Dx pins and the Sx pins.

ΔR_{ON}

ΔR_{ON} represents the difference between the R_{ON} of any two channels.

$R_{FLAT(ON)}$

$R_{FLAT(ON)}$ is the flatness that is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range.

I_S (Off)

I_S (off) is the source leakage current with the switch off.

I_D (Off)

I_D (off) is the drain leakage current with the switch off.

I_D (On), I_S (On)

I_D (on) and I_S (on) represent the channel leakage currents with the switch on.

V_{INL}

V_{INL} is the maximum input voltage for Logic 0.

V_{INH}

V_{INH} is the minimum input voltage for Logic 1.

I_{INL}, I_{INH}

I_{INL} and I_{INH} represent the low and high input currents of the digital inputs.

C_D (Off)

C_D (off) represents the off switch drain capacitance, which is measured with reference to ground.

C_S (Off)

C_S (off) represents the off switch source capacitance, which is measured with reference to ground.

C_D (On), C_S (On)

C_D (on) and C_S (on) represent the on switch capacitances, which are measured with reference to ground.

C_{IN}

C_{IN} is the digital input capacitance.

t_{ON} (EN)

t_{ON} (EN) represents the delay between applying the digital control input and the output switching on (see Figure 49).

t_{OFF} (EN)

t_{OFF} (EN) represents the delay between applying the digital control input and the output switching off (see Figure 49).

$t_{TRANSITION}$

$t_{TRANSITION}$ represents the delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

t_D

t_D represents the off time measured between the 90% points of both switches when switching from one address state to another.

$t_{DIGRESP}$

$t_{DIGRESP}$ is the time required for the FF pin to go low (0.3 V), measured with respect to the voltage on the source pin exceeding the supply voltage by 0.5 V.

t_{DIGREC}

t_{DIGREC} is the time required for the FF pin to return high, measured with respect to voltage on the Sx pin falling below the supply voltage plus 0.5 V.

$t_{RESPONSE}$

$t_{RESPONSE}$ represents the delay between the source voltage exceeding the supply voltage by 0.5 V and the drain voltage falling to 50% of its peak voltage.

$t_{RESPONSE}$ (EN)

$t_{RESPONSE}$ (EN) represents the delay between the enable pin being asserted and the drain reaching 90% of POSFV or NEGFV for a switch that is in fault.

$t_{RECOVERY}$

$t_{RECOVERY}$ represents the delay between an overvoltage on the Sx pin falling below the supply voltage plus 0.5 V and the drain voltage rising from 0 V to 50% of its voltage.

Off Isolation

Off isolation is a measure of unwanted signal coupling through an off switch.

Charge Injection

Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

Channel-to-Channel Crosstalk

Crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Insertion Loss

Insertion loss is the loss due to the on resistance of the switch.

-3 dB Bandwidth

Bandwidth is the frequency at which the output is attenuated by 3 dB.

AC Power Supply Rejection Ratio (ACPSRR)

ACPSRR is the ratio of the amplitude of signal on the output to the amplitude of the modulation. ACPSRR is a measure of the ability of the device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p.

On Response

On response is the frequency response of the on switch.

 V_T

V_T is the voltage threshold at which the overvoltage protection circuitry engages (see Figure 30).

Total Harmonic Distortion Plus Noise (THD + N)

THD + N is the ratio of the harmonic amplitude plus noise of the signal to the fundamental.

THEORY OF OPERATION

SWITCH ARCHITECTURE

Each channel of the [ADG5248F/ADG5249F](#) consists of a parallel pair of N-channel DMOS (NDMOS) and P-channel DMOS (PDMOS) transistors. This construction provides excellent performance across the signal range. The [ADG5248F/ADG5249F](#) channels operate as standard switches when input signals with a voltage between POSFV and NEGFV are applied. For example, the on resistance is 250 Ω typically and opening or closing the switch is controlled using the appropriate address pins.

Additional internal circuitry enables the switch to detect overvoltage inputs by comparing the voltage on a source pin (Sx) with POSFV and NEGFV. A signal is considered overvoltage if it exceeds these secondary supply voltages by the voltage threshold, V_T . The threshold voltage is typically 0.7 V, but can range from 0.8 V at -40°C down to 0.6 V at +125°C. See Figure 30 to see the change in V_T with operating temperature.

The maximum voltage that can be applied to any source input is +55 V or -55 V. When the device is powered using a single supply of 25 V or greater, the maximum negative signal level is reduced. It reduces from -55 V at $V_{DD} = +25$ V to -40 V at $V_{DD} = +40$ V to remain within the 80 V maximum rating. Construction of the process allows the channel to withstand 80 V across the switch when it is opened. These overvoltage limits apply whether the power supplies are present or not.

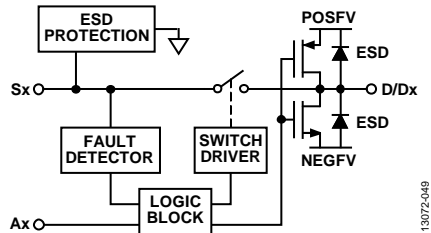


Figure 52. Switch Channel and Control Function

When an overvoltage condition is detected on a source pin (Sx), the switch automatically opens regardless of the digital logic state. The source pin becomes high impedance and ensures that no current flows through the switch. If a source pin is selected that is in fault, the drain pin is pulled to the supply that was exceeded. For example, if the source voltage exceeds POSFV, the drain output pulls to POSFV. If the source voltage exceeds NEGFV, the drain output pulls to NEGFV. In Figure 31, the voltage on the drain pin can be seen to follow the voltage on the source pin until the switch turns off completely. The drain pin then pulls to GND due to the 1 kΩ load resistor; otherwise, it pulls to the POSFV supply. The maximum voltage on the drain is limited by the internal ESD diodes, and the rate at which the output voltage discharges is dependent on the load at the pin.

During overvoltage conditions, the leakage current into and out of the source pins is limited to tens of microamperes. If the source pin is unselected, only nanoamperes of leakage appear on the drain pin. However, if the source is selected, the pin is pulled to the supply rail. The device that pulls the drain pin to the rail has an impedance of approximately 40 kΩ; thus, the D or Dx pin current is limited to approximately 1 mA during a shorted load condition. This internal impedance also determines the minimum external load resistance required to ensure that the drain pin is pulled to the desired voltage level during a fault.

When an overvoltage event occurs, the channels undisturbed by the overvoltage input continue to operate normally without additional crosstalk.

ESD Performance

The drain pins have ESD protection diodes to the secondary supply rails and the voltage at these pins must not exceed the secondary supply voltages, POSFV and NEGFV. The source pins have specialized ESD protection that allows the signal voltage to reach ±55 V regardless of supply voltage level. Exceeding ±55 V on any source input may damage the ESD protection circuitry on the device. See Figure 52 for an overview of the switch channel.

Trench Isolation

In the [ADG5248F](#) and [ADG5249F](#), an insulating oxide layer (trench) is placed between the NDMOS and the PDMOS transistors of each switch. Parasitic junctions, which occur between the transistors in junction isolated switches, are eliminated, and the result is a switch that is latch-up immune under all circumstances.

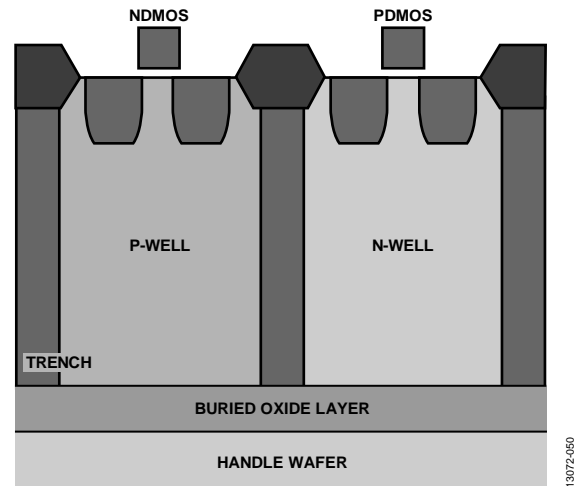


Figure 53. Trench Isolation

USER DEFINED FAULT PROTECTION

POSFV and NEGFV are required secondary power supplies that set the level at which the overvoltage protection is engaged. POSFV can be supplied from 4.5 V to V_{DD} , and NEGFV can be supplied from V_{SS} to 0 V. If a secondary supply is not available, the POSFV and NEGFV pins must be connected to V_{DD} (POSFV) and V_{SS} (NEGFV). The overvoltage protection then engages at the primary supply voltages. When the voltages at the source inputs exceed POSFV or NEGFV by V_T , the switch turns off or, if the device is unpowered, the switch remains off. The switch input remains high impedance regardless of the digital input state and if it is selected, the drain pulls to either POSFV or NEGFV. Signal levels up to +55 V and -55 V are blocked in both the powered and unpowered condition as long as the 80 V limitation between the source and supply pins is met.

Power-On Protection

The following conditions must be satisfied for the switch to be in the on condition:

- The primary supply must be V_{DD} to $V_{SS} \geq 8$ V
- For POSFV, the secondary supply must be between 4.5 V and V_{DD} , and for NEGFV, the secondary supply must be between V_{SS} and 0 V
- The input signal must be between $NEGFV - V_T$ and $POSFV + V_T$
- The digital logic control input has selected the switch

When the switch is turned on, signal levels up to the secondary supply rails are passed.

The switch responds to an analog input that exceeds POSFV or NEGFV by a threshold voltage, V_T , by turning off. The absolute input voltage limits are -55 V and +55 V, while maintaining an 80 V limit between the source pin and the supply rails. The switch remains off until the voltage at the source pin returns to between POSFV and NEGFV.

The fault response time ($t_{RESPONSE}$) when powered by a ± 15 V dual supply is typically 90 ns and the fault recovery time ($t_{RECOVERY}$) is 745 ns. These vary with supply voltages and output load conditions.

The maximum stress across the switch channel is 80 V; therefore, the user must pay close attention to this limit under a fault condition.

For example, consider the case where the device is set up in a multiplexer configuration as shown in Figure 54.

- V_{DD}/V_{SS} and POSFV/NEGFV = ± 22 V, S1 = +22 V, S1 is selected
- S2 has a -55 V fault and S3 has a +55 V fault
- The voltage between S2 and D = $+22$ V - (-55 V) = +77 V
- The voltage between S3 and D = 55 V - 22 V = 33 V

These calculations are all within device specifications: a 55 V maximum fault on the source inputs and a maximum of 80 V across the off switch channel.

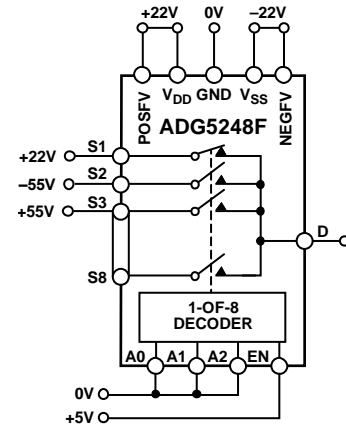


Figure 54. ADG5248F in an Overvoltage Condition

Power-Off Protection

When no power supplies are present, the switch remains in the off condition, and the switch inputs are high impedance. This state ensures that no current flows and prevents damage to the switch or downstream circuitry. The switch output is a virtual open circuit.

The switch remains off regardless of whether the V_{DD} and V_{SS} supplies are 0 V or floating. A GND reference must always be present to ensure proper operation. Signal levels of up to ± 55 V are blocked in the unpowered condition.

Digital Input Protection

The ADG5248F and the ADG5249F can tolerate digital input signals being present on the device without power. When the device is unpowered, the switch is guaranteed to be in the off state, regardless of the state of the digital logic signals.

The digital inputs are protected against positive faults of up to 44 V. The digital inputs do not offer protection against negative overvoltages. ESD protection diodes connected to GND are present on the digital inputs.

Overvoltage Interrupt Flag

The voltages on the source inputs of the ADG5248F and ADG5249F are continuously monitored, and the state of the switches is indicated by an active low digital output pin, FF.

The voltage on the FF pin indicates if any of the source input pins are experiencing a fault condition. The output of the FF pin is a nominal 3 V when all source pins are within normal operating range. If any source pin voltage exceeds the secondary supply voltage by V_T , the FF output reduces to below 0.8 V.

Use the specific fault digital output pin, SF, to decode which inputs are experiencing a fault condition. The SF pin reduces to below 0.8 V when a fault condition is detected on a specific pin, depending on the state of the F0, F1, and F2 pins (see Table 9 and Table 12).

APPLICATIONS INFORMATION

The overvoltage protected family of switches and multiplexers provides robust solutions for instrumentation, industrial, automotive, aerospace, and other harsh environments where overvoltage signals can be present and the system must remain operational both during and after the overvoltage has occurred.

POWER SUPPLY RAILS

To guarantee correct operation of the device, 0.1 μF decoupling capacitors are required on the primary and secondary supplies. If they are driven from the same supply, one set of 0.1 μF decoupling capacitors is sufficient.

The secondary supplies (POSFV and NEGFV) provide the current required to operate the fault protection and, thus, must be low impedance supplies. Therefore, they can be derived from the primary supplies by using a resistor divider and buffer.

The secondary supply rails (POSFV and NEGFV) must not exceed the primary supply rails (V_{DD} and V_{SS}) because this may lead to a signal passing through the switch unintentionally.

The ADG5248F and the ADG5249F can operate with bipolar supplies between $\pm 5\text{ V}$ and $\pm 22\text{ V}$. The supplies on V_{DD} and V_{SS} need not be symmetrical but the V_{DD} to V_{SS} range must not exceed 44 V. The ADG5248F and the ADG5249F can also operate with single supplies between 8 V and 44 V with V_{SS} connected to GND.

The ADG5248F and ADG5249F devices are fully specified at $\pm 15\text{ V}$, $\pm 20\text{ V}$, $+12\text{ V}$, and $+36\text{ V}$ supply ranges.

POWER SUPPLY SEQUENCING PROTECTION

The switch channel remains open when the devices are unpowered and signals from -55 V to $+55\text{ V}$ can be applied without damaging the devices. The switch channel closes only when the supplies are connected, a suitable digital control signal is placed on the address pins, and the signal is within normal operating range. Placing the ADG5248F/ADG5249F between external connectors and sensitive components offers protection in systems where a signal is presented to the source pins before the supply voltages are available.

SIGNAL RANGE

The primary supplies define the on-resistance profile of the channel, whereas the secondary supplies define the signal range. Using voltages on POSFV and NEGFV that are lower than V_{DD} and V_{SS} , the required signal can benefit from the flat on resistance in the center of the full signal capabilities of the device.

POWER SUPPLY RECOMMENDATIONS

Analog Devices, Inc., has a wide range of power management products to meet the requirements of most high performance signal chains.

An example of a bipolar power solution is shown in Figure 55. The ADP7118 and ADP7182 can be used to generate clean positive and negative rails from the ADP5070 (dual switching regulator) output. These rails can power the ADG5248F, the ADG5249F, an amplifier, and/or a precision converter in a typical signal chain.

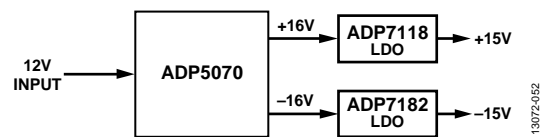


Figure 55. Bipolar Power Solution

Table 13. Recommended Power Management Devices

| Product | Description |
|---------|--|
| ADP5070 | 1 A/0.6 A, dc-to-dc switching regulator with independent positive and negative outputs |
| ADP7118 | 20 V, 200 mA, low noise, CMOS LDO |
| ADP7142 | 40 V, 200 mA, low noise, CMOS LDO |
| ADP7182 | -28 V, -200 mA, low noise, linear regulator |

HIGH VOLTAGE SURGE SUPPRESSION

The ADG5248F/ADG5249F are not intended for use in very high voltage applications. The maximum operating voltage of the transistor is 80 V. In applications where the inputs are likely to be subject to overvoltages exceeding the breakdown voltage, use transient voltage suppressors (TVSs) or similar.

INTELLIGENT FAULT DETECTION

The [ADG5248F](#) and [ADG5249F](#) digital output pin, FF, can interface with a microprocessor or control system and can be used as an interrupt flag. This feature provides real-time diagnostic information on the state of the device and the system to which it connects.

The control system can use the digital interrupt, FF, to start a variety of actions, as follows:

- Initiating an investigation into the source of an overvoltage fault.
- Shutting down critical systems in response to the overvoltage condition.
- Using data recorders to mark data during these events as unreliable or out of specification.

For systems sensitive during a start-up sequence, the active low operation of the flag allows the system to ensure that the [ADG5248F](#) or [ADG5249F](#) is powered on and that all input voltages are within the normal operating range before initiating operation.

The FF pin has a weak internal pull-up resistor, which allows the signals to combine into a single interrupt for larger modules that contain multiple devices.

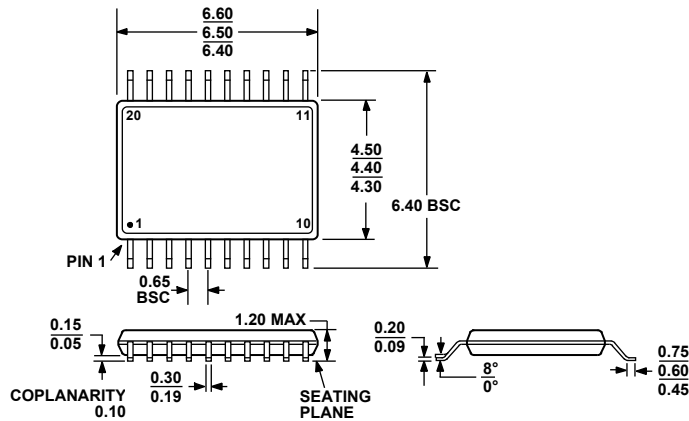
The recovery time, t_{DIGREC} , can be decreased from a typical 65 μ s to 900 ns by using a 1 k Ω pull-up resistor.

The specific fault digital output, SF, decodes which inputs are experiencing a fault condition. The SF pin reduces to below 0.8 V when a fault condition is detected on a specific pin, depending on the state of the F0, F1, and F2 pins (see Table 9 and Table 12). The specific fault feature also works with the switches disabled (EN pin low), which allows the user to cycle through and check the fault conditions without connecting the fault to the drain output.

LARGE VOLTAGE, HIGH FREQUENCY SIGNALS

Figure 33 illustrates the voltage range and frequencies that the [ADG5248F/ADG5249F](#) can reliably convey. For signals that extend across the full signal range from V_{SS} to V_{DD} , keep the frequency below 1 MHz. If the required frequency is greater than 1 MHz, decrease the signal range appropriately to ensure signal integrity.

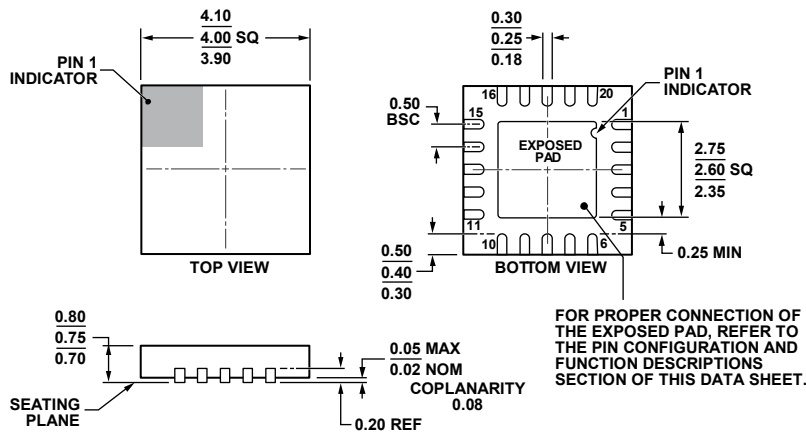
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AC

Figure 56. 20-Lead Thin Shrink Small Outline Package [TSSOP] (RU-20)

Dimensions shown in millimeters



FOR PROPER CONNECTION OF THE EXPOSED PAD, REFER TO THE PIN CONFIGURATION AND FUNCTION DESCRIPTIONS SECTION OF THIS DATA SHEET.

COMPLIANT TO JEDEC STANDARDS MO-220-WGGD.

Figure 57. 20-Lead Lead Frame Chip Scale Package [LFCSP] 4 mm × 4 mm Body and 0.75 mm Package Height (CP-20-8)

Dimensions shown in millimeters

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option |
|--------------------|-------------------|---|----------------|
| ADG5248FBCPZ-RL7 | -40°C to +125°C | 20-Lead Lead Frame Chip Scale Package [LFCSP] | CP-20-8 |
| ADG5248FBRUZ | -40°C to +125°C | 20-Lead Thin Shrink Small Outline Package [TSSOP] | RU-20 |
| ADG5248FBRUZ-RL7 | -40°C to +125°C | 20-Lead Thin Shrink Small Outline Package [TSSOP] | RU-20 |
| ADG5249FBCPZ-RL7 | -40°C to +125°C | 20-Lead Lead Frame Chip Scale Package [LFCSP] | CP-20-8 |
| ADG5249FBRUZ | -40°C to +125°C | 20-Lead Thin Shrink Small Outline Package [TSSOP] | RU-20 |
| ADG5249FBRUZ-RL7 | -40°C to +125°C | 20-Lead Thin Shrink Small Outline Package [TSSOP] | RU-20 |

¹ Z = RoHS Compliant Part.

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