

Product Description

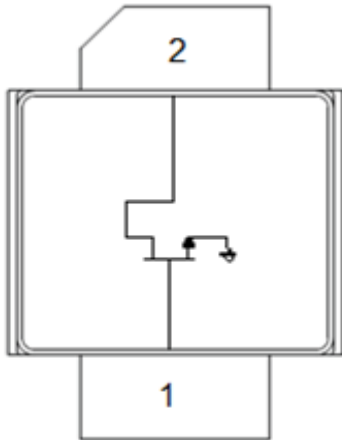
The QPD3601 is a discrete GaN on SiC HEMT which operates from 3.4 to 3.6 GHz. The device is a single stage matched power amplifier transistor.

The QPD3601 can be used in Doherty architecture for the final stage of a base station power amplifier for macrocell high efficiency systems.

QPD3601 can deliver P_{SAT} of 206 W at +50 V operation.

RoHS compliant.

Functional Block Diagram



2 Lead NI400 Package

Product Features

- Operating Frequency Range: 3.4 – 3.6 GHz
- Operating Drain Voltage: +50 V
- Output Power (P_{SAT}): 206 W
- Drain Efficiency: 57.9%
- Efficiency-Tuned P3dB Gain: 16.3 dB
- 2-lead, earless, ceramic flange NI400 package

Applications

- W-CDMA / LTE
- Macrocell Base Station
- Active Antenna

Ordering Information

Part No.	Description
QPD3601	200 W, 3.4 – 3.6 GHz, GaN Discrete
QPD3601-EVB	3.4-3.6 GHz Evaluation Board

Absolute Maximum Ratings

Parameter	Value / Range
Gate Voltage (V_G)	-10 V
Drain Voltage (V_D)	+55 V
Maximum RF Input Power	42 dBm
VSWR Mismatch, P1dB Pulse (20 % duty cycle, 100 μ width), T = 25 °C	10:1
Storage Temperature	-65 to +150°C

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Gate Current (I_G)			15	mA
Gate Voltage (V_G)	-3.3	-2.7	-2.5	V
Drain Voltage (V_D)		50		V
Quiescent Current (I_{DQ})		360		mA

Electrical performance is measured under conditions noted in the electrical specifications table. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Conditions	Min	Typ	Max	Units
Frequency Range		3400		3600	MHz
Quiescent Current			360		mA
Gain	P3dB	15.0	16.3		dB
P3dB		52.5	53.1		dBm
Drain Efficiency	P3dB	51.0	57.9		%
Gate Leakage	$V_D = +50$ V, $V_G = -5$ V	-10.0	-3.5		mA

Test conditions unless otherwise noted: $V_D = +50$ V, $I_{DQ} = 360$ mA, T = 25°C, Pulsed (10 % duty cycle, 100 μ s width), on Class AB single-ended EVB at 3500 MHz

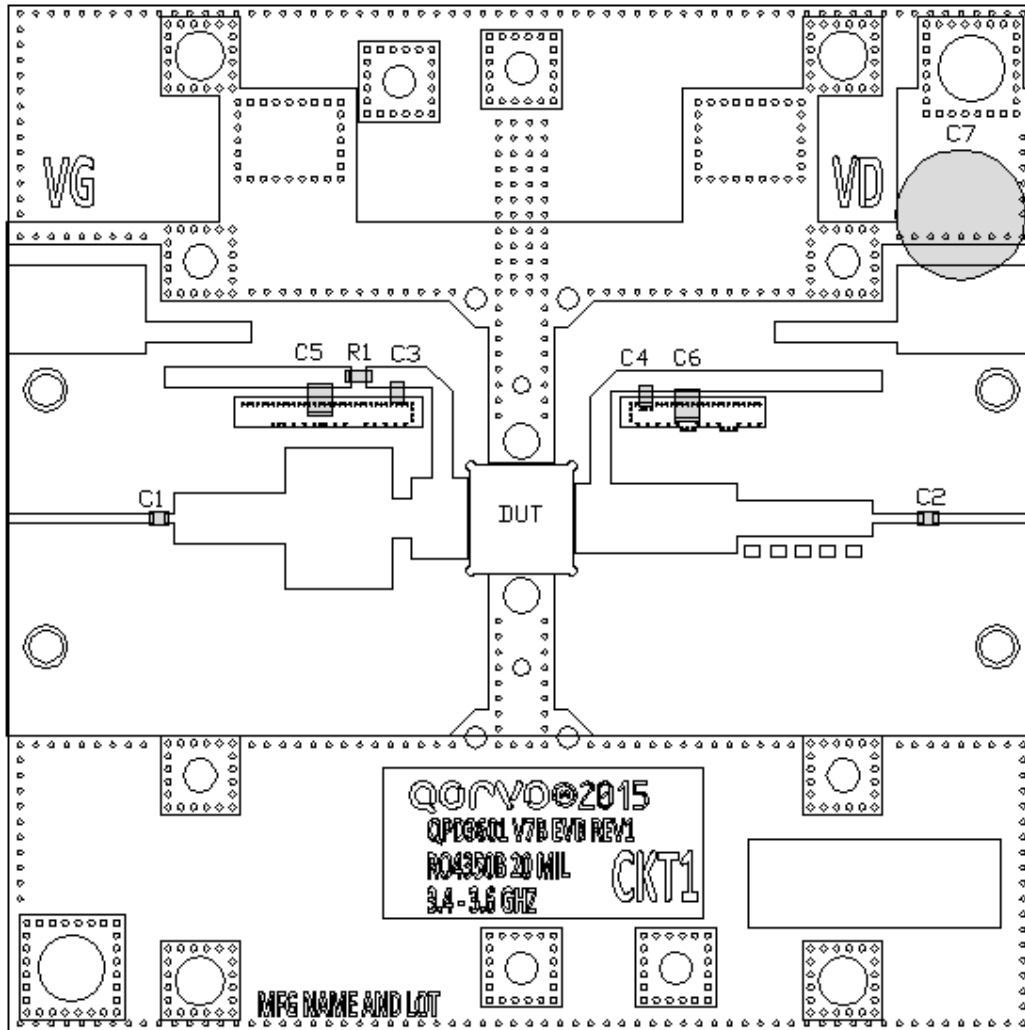
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	$T_{CASE} = 85^\circ\text{C}$, $T_{CH} = 134^\circ\text{C}$ CW: $P_{DISS} = 51$ W, $P_{OUT} = 45$ W	0.96	°C/W

Notes:

1. Thermal resistance measured to package backside.
2. Based on expected carrier amplifier efficiency of Doherty.
3. Pout assumes 20% peaking amplifier contribution of total average Doherty rated power.
4. Refer to the following document: [GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimate](#)

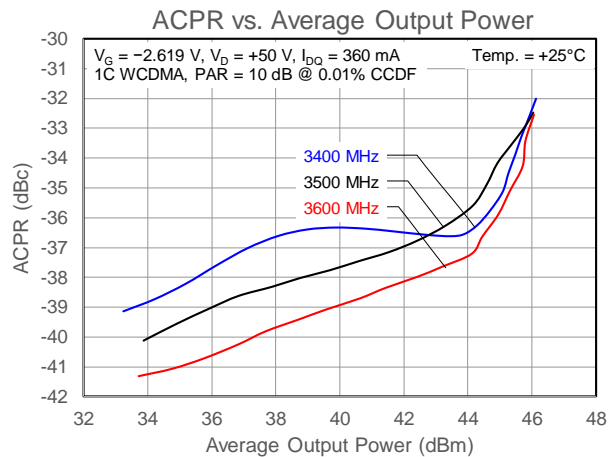
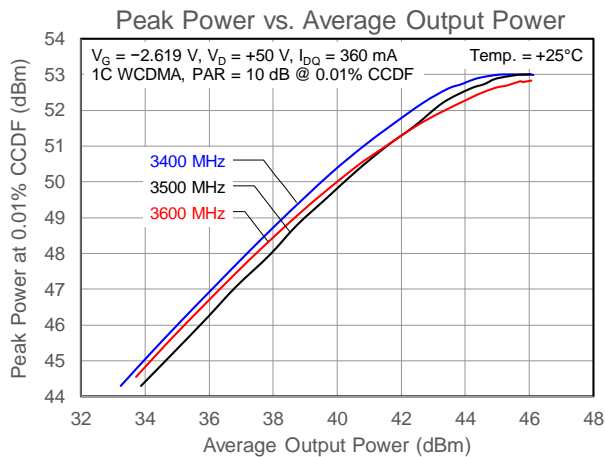
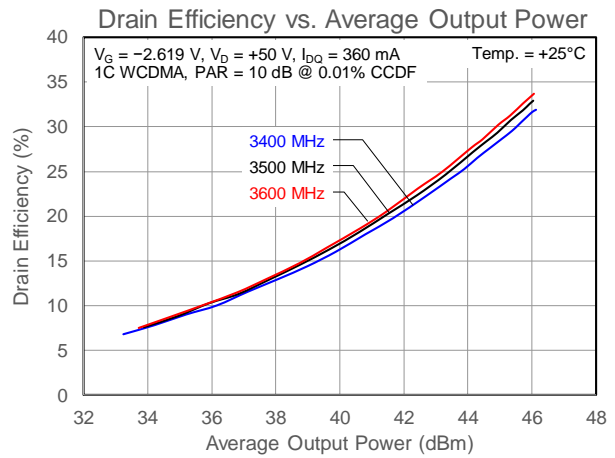
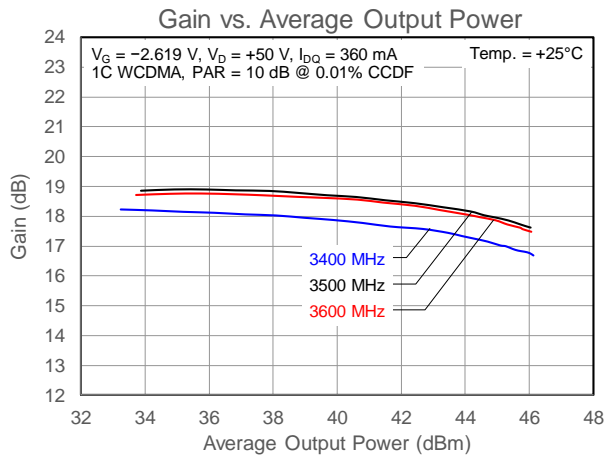
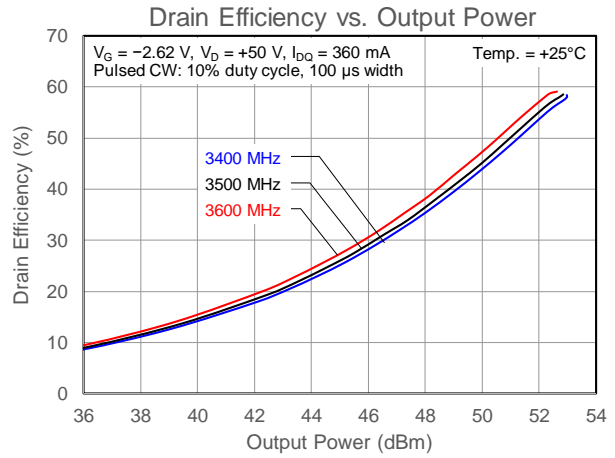
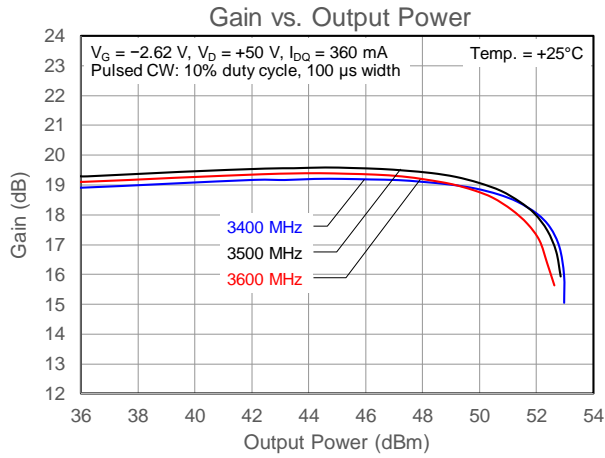
Single-Ended Evaluation Board Layout



Bill of Materials

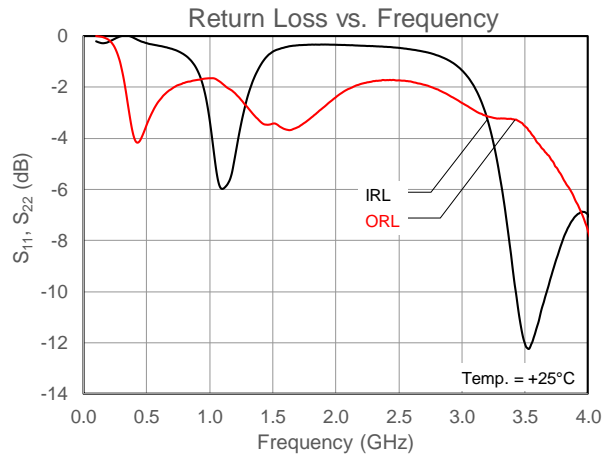
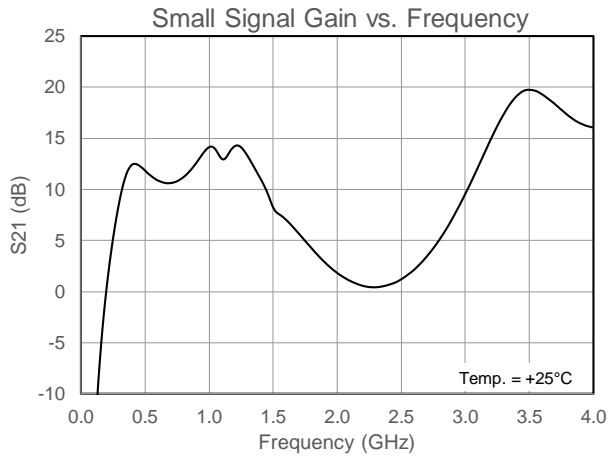
Reference	Value	Description	Manuf.	Part Number
C1, C2, C3, C4	8.2 pF	Capacitor, 8.2 pF	ATC	600F8R2BW250T
C5	10 μF	Capacitor, 10 μF, 50 V	TDK	C5750X7R1H106K230KB
C6	10 μF	Capacitor, 10 μF, 100 V	TDK	C5750X7S2A106M230KB
C7	220 μF	Capacitor, 220 μF, electrolytic, 100 V	Cornell D.	AFK227M2AR44T-F
R1	10 Ω	Resistor, 10 Ω, 1/8 W	Vishay/Dale	CRCW060310R0FKEA

Single-Ended Evaluation Board Performance Plots



Test conditions unless otherwise noted: $V_D = +50 \text{ V}$, $I_{DQ} = 360 \text{ mA}$, $T = 25^\circ\text{C}$, on Class AB single-ended EVB at 3500 MHz

Single-Ended Evaluation Board Performance Plots



Test conditions unless otherwise noted: $V_D = +50\text{ V}$, $I_{DQ} = 360\text{ mA}$, $T = 25^\circ\text{C}$, on Class AB single-ended EVB at 3500 MHz

**RF Characterization – Power-Tuned Load Pull Performance**

Frequency (MHz)	Source Impedance	Load Impedance	Gain @ P3dB (dB)	P3dB (dBm)	Drain Efficiency (%)
3400	11.50 – j15.57	7.76 – j0.96	16.2	53.2	53.3
3500	18.05 – j10.41	6.01 – j0.73	16.6	53.3	55.4
3600	13.17 – j1.70	6.01 – j0.73	16.7	53.4	60.4

Test conditions unless otherwise noted: $V_D = +50$ V, $I_{DQ} = 360$ mA, $T = 25^\circ\text{C}$, Pulsed 10% duty cycle, 100 μs width)

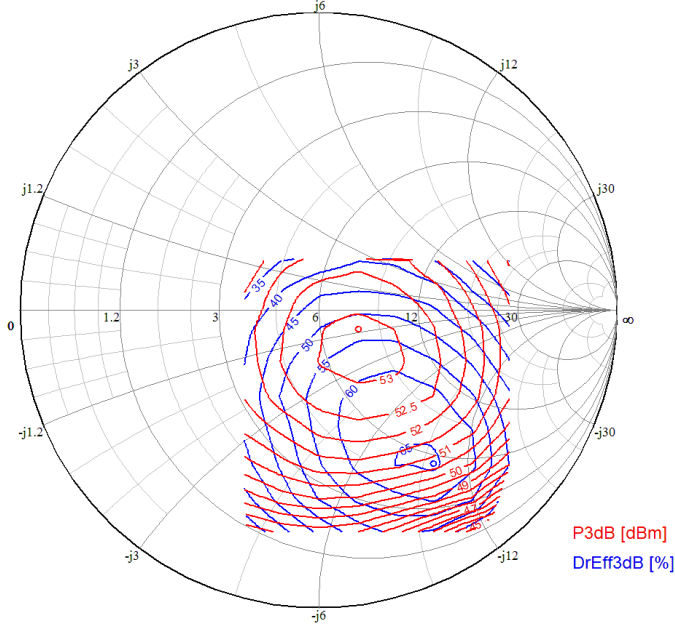
RF Characterization – Efficiency-Tuned Load Pull Performance

Frequency (MHz)	Source Impedance	Load Impedance	Gain @ P3dB (dB)	P3dB (dBm)	Drain Efficiency (%)
3400	11.50 – j15.57	5.38 – j9.66	19.0	50.7	65.9
3500	18.05 – j10.41	6.47 – j6.83	19.2	51.7	67.2
3600	13.17 + j1.70	8.05 – j5.51	18.7	52.0	69.9

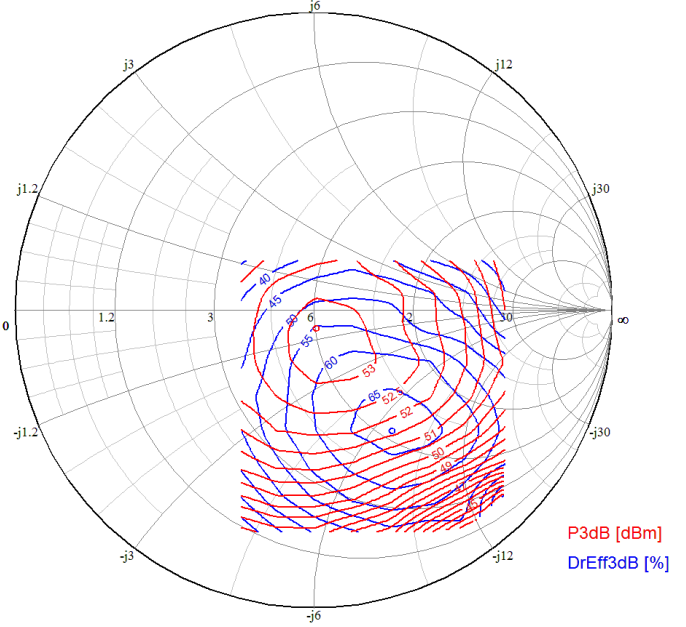
Test conditions unless otherwise noted: $V_D = +50$ V, $I_{DQ} = 360$ mA, $T = 25^\circ\text{C}$, Pulsed 10% duty cycle, 100 μs width)

Load Pull Plots

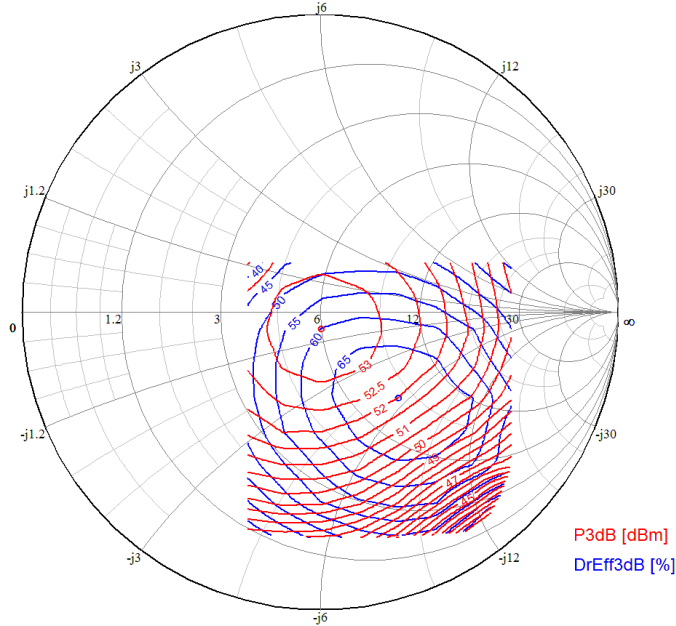
Load Pull at 3.4 GHz



Load Pull at 3.5 GHz

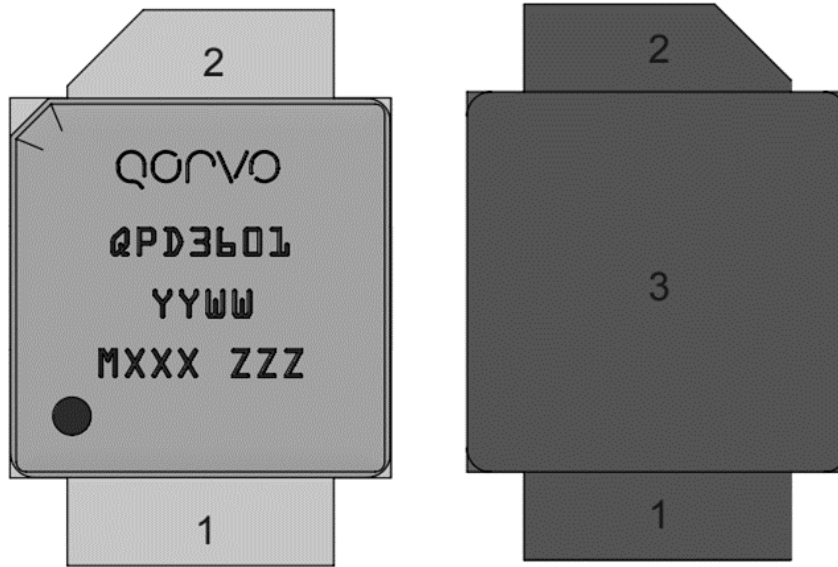


Load Pull at 3.6 GHz



Test conditions unless otherwise noted: $V_D = +50$ V, $I_{DQ} = 360$ mA, $T = 25^\circ\text{C}$, Pulsed 10% duty cycle, 100 μs width)

Pin Configuration

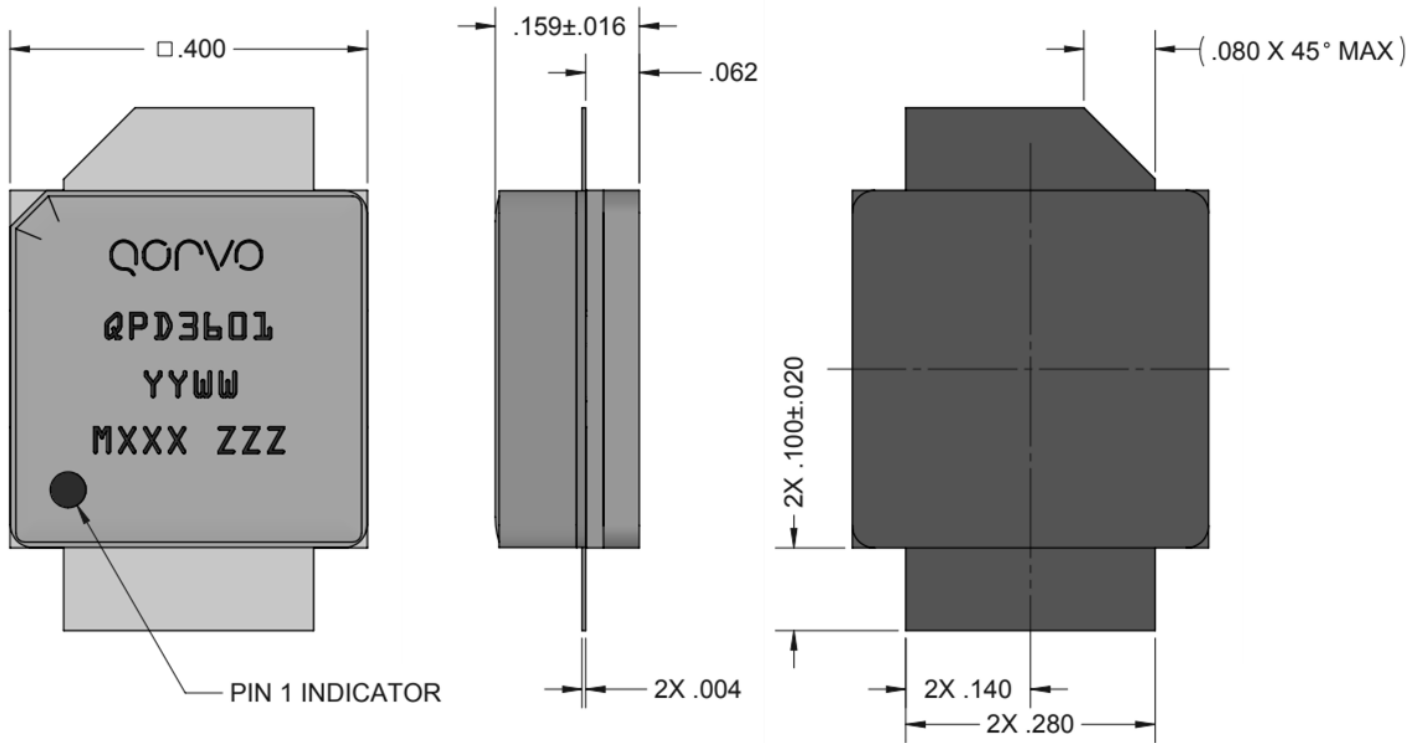


Pin Description

Pin No.	Label	Description
1	RF IN, V_G	RF Input, Gate Bias
2	RF OUT, V_D	RF Output, Drain Bias
3 (Backside Paddle)	RF/DC GND	RF/DC Ground

Package Marking and Dimensions

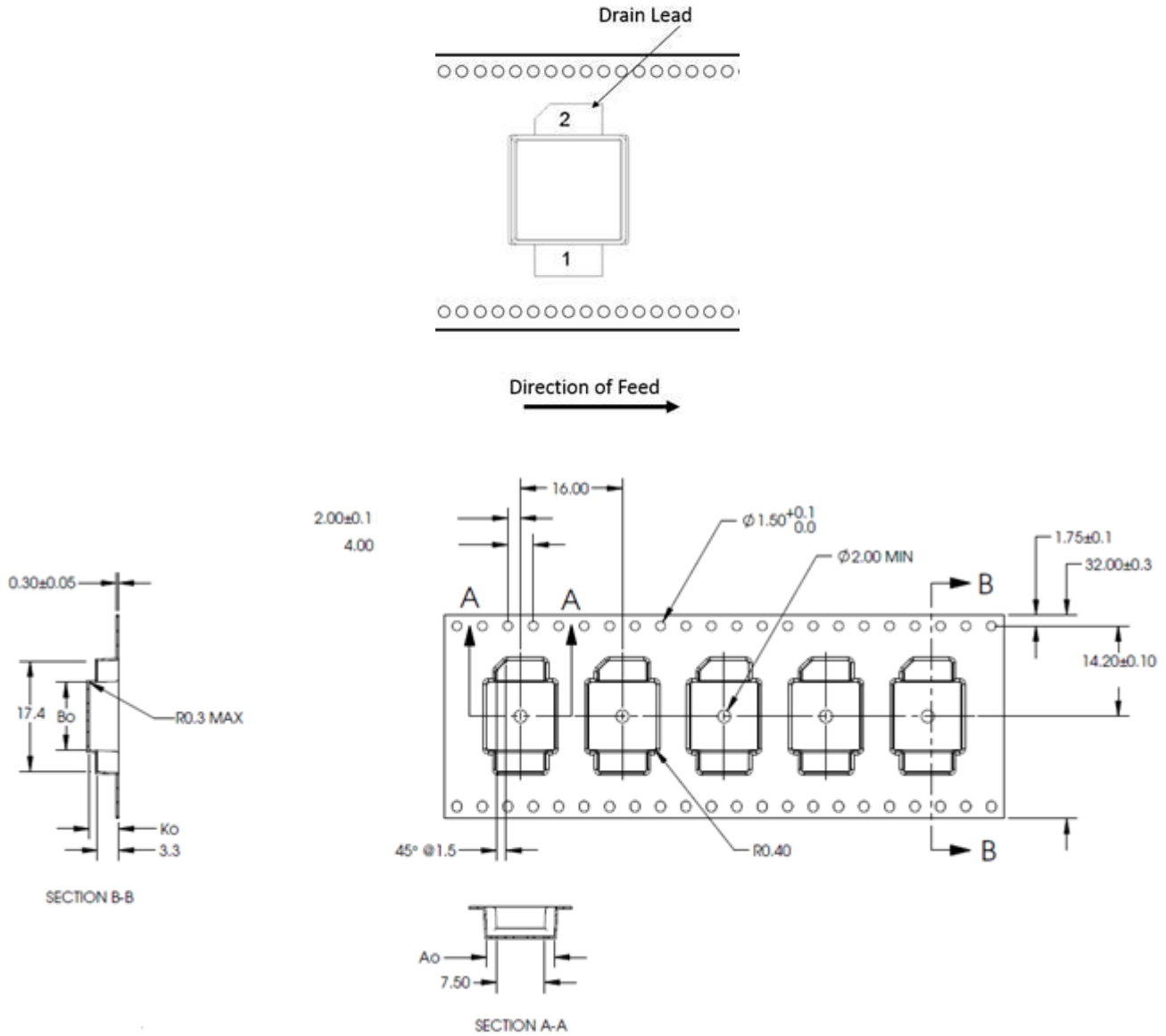
Marking: Qorvo Logo
 Part Number – QPD3601
 Date Code – YYWW
 Production Lot Number – MXXX
 Serial Number – ZZZ



Notes: Unless Otherwise Specified;

1. Material:
 - Package Base: Ceramic/Metal
 - Package Lid: Ceramic
2. Package exposed metallization is NiAu plated. Au thickness is minimum 60 μm .
3. Part is epoxy sealed.
4. Part meets industry NI400 footprint.
5. Body dimensions do not include lid shift or epoxy run out, which can be up to 0.020 per side.
6. Dimensions are in inches. General tolerance is ± 0.005 .

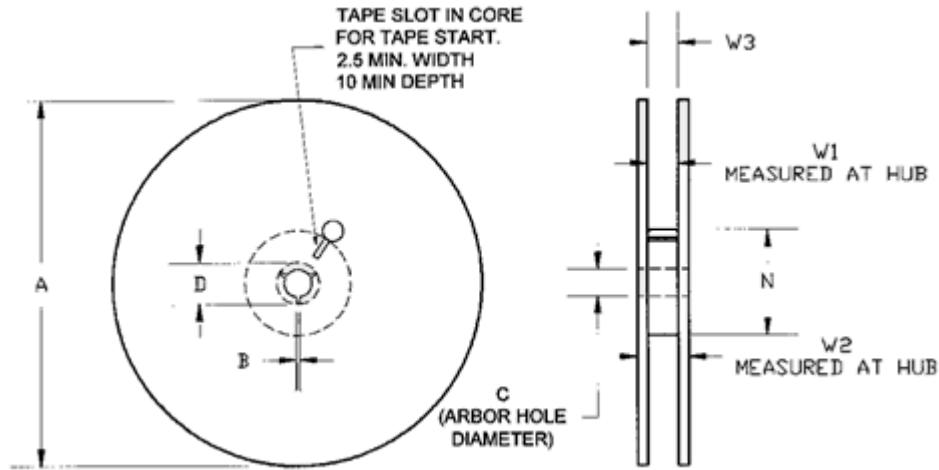
Tape and Reel Information – Carrier and Cover Tape Dimensions



Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.417	10.60
	Width	B0	0.419	10.65
	Depth	K0	0.181	4.60
	Pitch	P1	0.630	16
Centerline Distance	Cavity to Perforation – Length Direction	P2	0.079	2.00
	Cavity to Perforation – Width Direction	F	0.559	14.20
Cover Tape	Width	C	1.004	25.50
Carrier Tape	Width	W	1.260	32

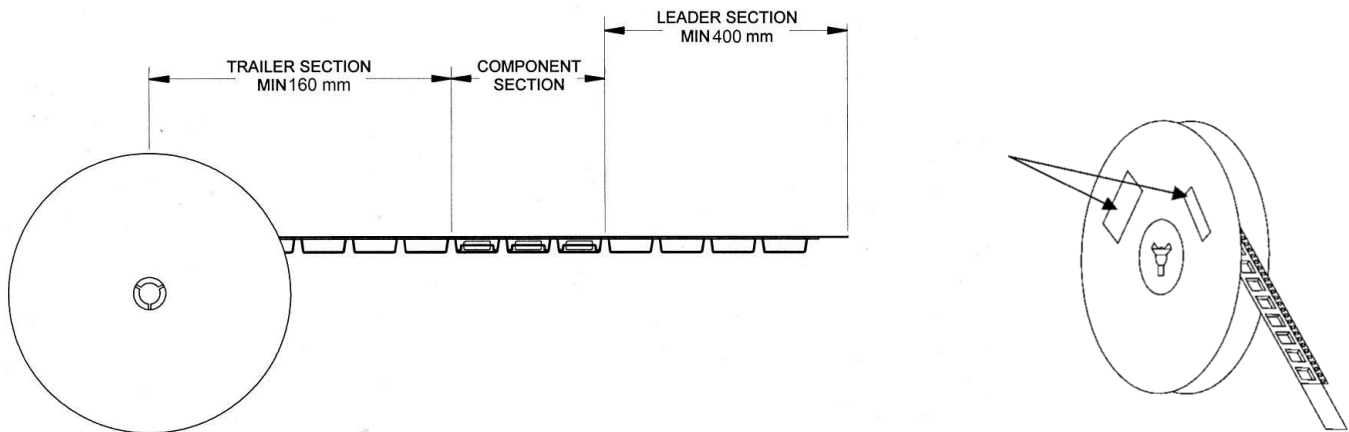
Tape and Reel Information – Reel Dimensions

Standard T/R size = 250 pieces on a 13" reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	12.992	330.0
	Thickness	W2	1.504	38.2
	Space Between Flange	W1	1.291	32.8
Hub	Outer Diameter	N	4.016	102.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.787	20.0

Tape and Reel Information – Tape Length and Label Placement



Notes:

1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1B	ANSI/ESDA/JEDEC Standard JS-
ESD – Charged Device Model (CDM)	Class C3	ANSI/ESDA/JEDEC Standard JS-
MSL – 260°C Convection Reflow	MSL3	IPC/JEDEC Standard J-STD-020



Solderability

Compatible with both lead-free (260°C maximum reflow temperature) soldering processes. The use of no-clean solder to avoid washing after soldering is recommended. Contact plating is NiAu. Au thickness is minimum 60 µin.

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU. This product also has the following attributes:

- Product uses RoHS Exemption 7c-II to meet RoHS Compliance requirements.
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free

Contact Information

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