

MC74LVX4245

Dual Supply Octal Translating Transceiver

with 3-State Outputs

The 74LVX4245 is a 24-pin dual-supply, octal translating transceiver that is designed to interface between a 5.0 V bus and a 3.0 V bus in a mixed 3.0 V / 5.0 V supply environment such as laptop computers using a 3.3 V CPU and 5.0 V LCD display. The A port interfaces with the 5V bus; the B port interfaces with the 3.0 V bus.

The Transmit/Receive (T/\bar{R}) input determines the direction of data flow. Transmit (active-High) enables data from the A port to the B port. Receive (active-Low) enables data from the B port to the A port. The Output Enable (\overline{OE}) input, when High, disables both A and B ports by placing them in 3-State.

Features

- Bi-directional Interface Between 5.0 V and 3.0 V Buses
- Control Inputs Compatible with TTL Level
- 5.0 V Data Flow at A Port and 3.0 V Data Flow at B Port
- Outputs Source/Sink 24 mA at 5.0 V Bus and 12 mA at 3.0 V Bus
- Guaranteed Simultaneous Switching Noise Level and Dynamic Threshold Performance
- Available in SOIC and TSSOP Packages
- Functionally Compatible with the 74 Series 245
- These Devices are Pb-Free and are RoHS Compliant

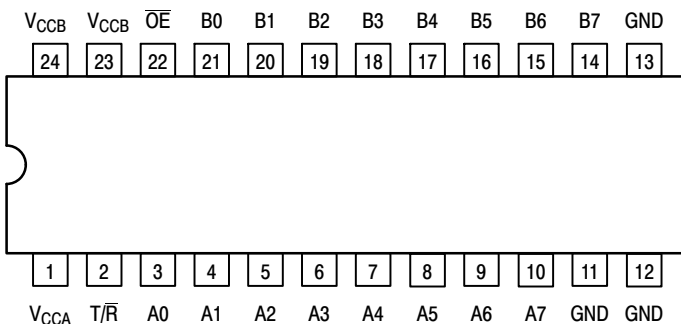


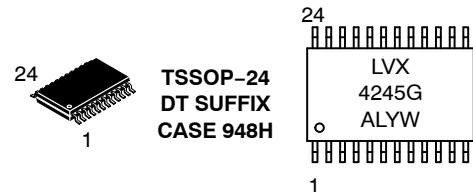
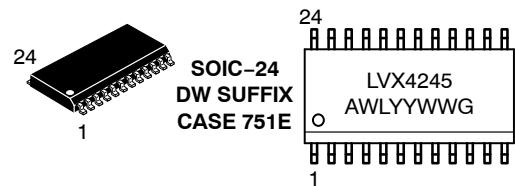
Figure 1. 24-Lead Pinout
(Top View)



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MARKING DIAGRAMS



LVX4245 = Specific Device Code
 A = Assembly Location
 WL, L = Wafer Lot
 Y = Year
 WW, W = Work Week
 G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

PIN NAMES

| Pins | Function |
|-----------------|--|
| \overline{OE} | Output Enable Input |
| T/\bar{R} | Transmit/Receive Input |
| A0-A7 | Side A 3-State Inputs or 3-State Outputs |
| B0-B7 | Side B 3-State Inputs or 3-State Outputs |

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

MC74LVX4245

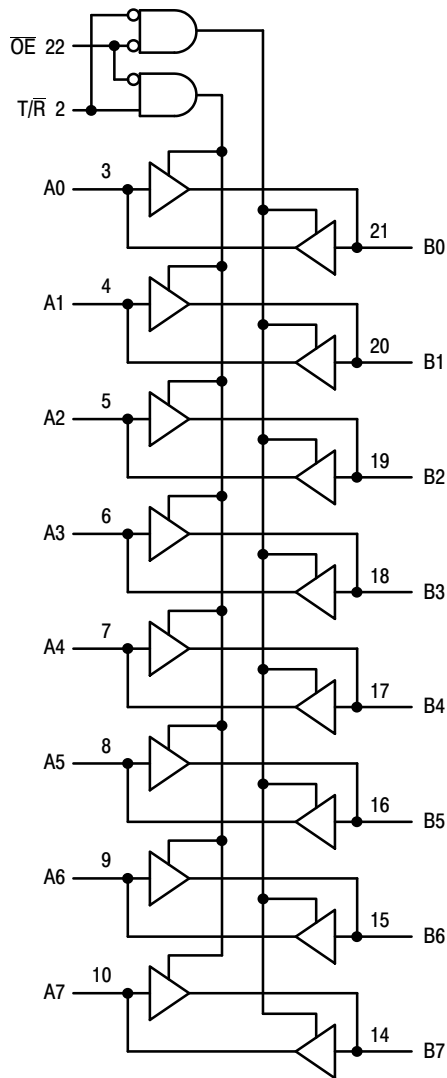


Figure 2. Logic Diagram

| INPUTS | | OPERATING MODE Non-Inverting |
|--------|-----|---------------------------------|
| OE | T/R | |
| L | L | B Data to A Bus |
| L | H | A Data to B Bus |
| H | X | Z |

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; X = High or Low Voltage Level and Transitions are Acceptable; For I_{CC} reasons, Do Not Float Inputs

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ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Condition | Unit |
|--------------------|--------------------------------|--|------------------------------------|---------------------------------|
| V_{CCA}, V_{CCB} | DC Supply Voltage | -0.5 to +7.0 | | V |
| V_I | DC Input Voltage | $\overline{OE}, T/R$ | -0.5 to $V_{CCA} + 0.5$ | V |
| $V_{I/O}$ | DC Input/Output Voltage | An | -0.5 to $V_{CCA} + 0.5$ | V |
| | | Bn | -0.5 to $V_{CCB} + 0.5$ | V |
| I_{IK} | DC Input Diode Current | $\overline{OE}, T/R$ | ± 20 | $V_I < GND$ mA |
| I_{OK} | DC Output Diode Current | | ± 50 | $V_O < GND; V_O > V_{CC}$ mA |
| I_O | DC Output Source/Sink Current | | ± 50 | mA |
| I_{CC}, I_{GND} | DC Supply Current | Per Output Pin Maximum Current at I_{CCA} Maximum Current at I_{CCB} | ± 50 ± 200 ± 100 | mA |
| T_{STG} | Storage Temperature Range | | -65 to +150 | °C |
| Latchup | DC Latchup Source/Sink Current | | ± 300 | mA |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|---------------------|--|--------------------------------------|----------------|------|
| V_{CCA}, V_{CCB} | Supply Voltage | V_{CCA} 4.5 V_{CCB} 2.7 | 5.5 3.6 | V |
| V_I | Input Voltage | $\overline{OE}, T/R$ | 0 V_{CCA} | V |
| $V_{I/O}$ | Input/Output Voltage | An | 0 V_{CCA} | V |
| | | Bn | 0 V_{CCB} | V |
| T_A | Operating Free-Air Temperature | -40 | +85 | °C |
| $\Delta t/\Delta V$ | Minimum Input Edge Rate V_{IN} from 30% to 70% of V_{CC} ; V_{CC} at 3.0V, 4.5V, 5.5V | 0 | 8 | ns/V |

DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Condition | V_{CCA} | V_{CCB} | $T_A = 25^\circ\text{C}$ | | $T_A = -40 \text{ to } +85^\circ\text{C}$ | | Unit |
|-----------|-----------------------------------|--|-----------|-----------|--------------------------|-------------------|---|---|------|
| | | | | | Typ | Guaranteed Limits | | | |
| V_{IHA} | Minimum HIGH Level Input Voltage | $V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$ | 5.5 | 3.3 | | 2.0 | 2.0 | V | |
| | | | 4.5 | 3.3 | | 2.0 | 2.0 | | |
| V_{IHB} | Input Voltage | An, \overline{OE} T/R | 5.0 | 3.6 | | 2.0 | 2.0 | V | |
| | | | 5.0 | 2.7 | | 2.0 | 2.0 | | |
| V_{ILA} | Maximum LOW Level Input Voltage | $V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$ | 5.5 | 3.3 | | 0.8 | 0.8 | V | |
| | | | 4.5 | 3.3 | | 0.8 | 0.8 | | |
| V_{ILB} | Input Voltage | An, \overline{OE} T/R | 5.0 | 2.7 | | 0.8 | 0.8 | V | |
| | | | 5.0 | 3.6 | | 0.8 | 0.8 | | |
| V_{OHA} | Minimum HIGH Level Output Voltage | $I_{OUT} = -100\mu A$ $I_{OH} = -24mA$ | 4.5 | 3.0 | 4.50 | 4.40 | 4.40 | V | |
| | | | 4.5 | 3.0 | 4.25 | 3.86 | 3.76 | | |
| V_{OHB} | Output Voltage | $I_{OUT} = -100\mu A$ $I_{OH} = -12mA$ $I_{OH} = -8mA$ | 4.5 | 3.0 | 2.99 | 2.9 | 2.9 | V | |
| | | | 4.5 | 3.0 | 2.80 | 2.4 | 2.4 | | |
| | | | 4.5 | 2.7 | 2.50 | 2.4 | 2.4 | | |
| V_{OLA} | Maximum LOW Level Output Voltage | $I_{OUT} = 100\mu A$ $I_{OL} = 24mA$ | 4.5 | 3.0 | 0.002 | 0.10 | 0.10 | V | |
| | | | 4.5 | 3.0 | 0.18 | 0.36 | 0.44 | | |
| V_{OLB} | Output Voltage | $I_{OUT} = 100\mu A$ $I_{OL} = 12mA$ $I_{OL} = 8mA$ | 4.5 | 3.0 | 0.002 | 0.10 | 0.10 | V | |
| | | | 4.5 | 3.0 | 0.1 | 0.31 | 0.40 | | |
| | | | 4.5 | 2.7 | 0.1 | 0.31 | 0.40 | | |

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DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Condition | V _{CCA} | V _{CCB} | T _A = 25°C | | T _A = -40 to +85°C | | Unit |
|--|---|--|--|------------------|-----------------------|-------------------|-------------------------------|-----|------|
| | | | | | Typ | Guaranteed Limits | | | |
| I _{IN} | Max Input Leakage Current | $\overline{OE}, T/\overline{R}$ V _I = V _{CCA} , GND | 5.5 | 3.6 | | ±0.1 | ±1.0 | | μA |
| I _{OZA} | Max 3-State Output Leakage | An V _I = V _{IH} , V _{IL} OE = V _{CCA} V _O = V _{CCA} , GND | 5.5 | 3.6 | | ±0.5 | ±5.0 | | μA |
| I _{OZB} | Max 3-State Output Leakage | Bn V _I = V _{IH} , V _{IL} OE = V _{CCA} V _O = V _{CCB} , GND | 5.5 | 3.6 | | ±0.5 | ±5.0 | | μA |
| ΔI _{CC} | Maximum I _{CC} T per Input | An, OE T/R | V _I =V _{CCA} -2.1V | 5.5 | 3.6 | 1.0 | 1.35 | 1.5 | mA |
| | | Bn | V _I =V _{CCB} -0.6V | 5.5 | 3.6 | | 0.35 | 0.5 | mA |
| I _{CCA} | Quiescent V _{CCA} Supply Current | An=V _{CCA} or GND Bn=V _{CCB} or GND OE=GND T/R=GND | 5.5 | 3.6 | | 8 | 80 | | μA |
| I _{CCB} | Quiescent V _{CCB} Supply Current | An=V _{CCA} or GND Bn=V _{CCB} or GND OE=GND T/R=V _{CCA} | 5.5 | 3.6 | | 5 | 50 | | μA |
| V _{OLPA} V _{OLPB} | Quiet Output Max Dynamic V _{OL} | Notes 1, 2 | 5.0 5.0 | 3.3 3.3 | | 1.5 1.2 | | | V |
| V _{OLVA} V _{OLVB} | Quiet Output Min Dynamic V _{OL} | Notes 1, 2 | 5.0 5.0 | 3.3 3.3 | | -1.2 -0.8 | | | V |
| V _{IHDA} V _{IHDB} | Min HIGH Level Dynamic Input Voltage | Notes 1, 3 | 5.0 5.0 | 3.3 3.3 | | 2.0 2.0 | | | V |
| V _{ILDA} V _{ILDB} | Max LOW Level Dynamic Input Voltage | Notes 1, 3 | 5.0 5.0 | 3.3 3.3 | | 0.8 0.8 | | | V |

1. Worst case package.
2. Max number of outputs defined as (n). Data inputs are driven 0V to V_{CC} level; one output at GND.
3. Max number of data inputs (n) switching. (n-1) inputs switching 0V to V_{CC} level. Input under test switching: V_{CC} level to threshold (V_{IHD}), 0V to threshold (V_{ILD}), f = 1MHz.

CAPACITIVE CHARACTERISTICS

| Symbol | Parameter | Condition | Typical | Unit |
|------------------|--|--|-------------------------|------|
| C _{IN} | Input Capacitance | V _{CCA} = 5.0V; V _{CCB} = 3.3V | 4.5 | pF |
| C _{I/O} | Input/Output Capacitance | V _{CCA} = 5.0V; V _{CCB} = 3.3V | 15 | pF |
| C _{PD} | Power Dissipation Capacitance (Measured at 10MHz) | B→A | V _{CCA} = 5.0V | 55 |
| | | A→B | V _{CCB} = 3.3V | 40 |

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AC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | $T_A = -40 \text{ to } +85^\circ\text{C}$ $C_L = 50\text{pF}$ | | | $T_A = -40 \text{ to } +85^\circ\text{C}$ $C_L = 50\text{pF}$ | | Unit |
|--------------------------|--|--|-----------------|--------------|--|--------------|------|
| | | $V_{CCA} = 5V \pm 0.5V$ $V_{CCB} = 3.3V \pm 0.3V$ | | | $V_{CCA} = 5V \pm 0.5V$ $V_{CCB} = 2.7V$ | | |
| | | Min | Typ (Note 4) | Max | Min | Max | |
| t_{PHL} t_{PLH} | Propagation Delay A to B | 1.0 1.0 | 5.1 5.3 | 9.0 9.0 | 1.0 1.0 | 10.0 10.0 | ns |
| t_{PHL} t_{PLH} | Propagation Delay B to A | 1.0 1.0 | 5.4 5.5 | 9.0 9.0 | 1.0 1.0 | 10.0 10.0 | ns |
| t_{PZL} t_{PZH} | Output Enable Time \overline{OE} to B | 1.0 1.0 | 6.5 6.7 | 10.5 10.5 | 1.0 1.0 | 11.5 11.5 | ns |
| t_{PZL} t_{PZH} | Output Enable Time \overline{OE} to A | 1.0 1.0 | 5.2 5.8 | 9.5 9.5 | 1.0 1.0 | 10.0 10.0 | ns |
| t_{PHZ} t_{PLZ} | Output Disable Time \overline{OE} to B | 1.0 1.0 | 6.0 3.3 | 10.0 7.0 | 1.0 1.0 | 10.0 7.5 | ns |
| t_{PHZ} t_{PLZ} | Output Disable Time \overline{OE} to A | 1.0 1.0 | 3.9 2.9 | 7.5 7.0 | 1.0 1.0 | 7.5 7.5 | ns |
| t_{OSHL} t_{OSLH} | Output to Output Skew, Data to Output (Note 5) | | 1.0 | 1.5 | | 1.5 | ns |

4. Typical values at $V_{CCA} = 5.0V$; $V_{CCB} = 3.3V$ at 25°C .

5. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

ORDERING INFORMATION

| Device | Package | Shipping† |
|------------------|----------------------|------------------|
| MC74LVX4245DWG | SOIC-24 | 30 Units / Rail |
| MC74LVX4245DWR2G | SOIC-24 (Pb-Free) | 1000 Tape & Reel |
| MC74LVX4245DTG | TSSOP-24* | 62 Units / Rail |
| MC74LVX4245DTR2G | TSSOP-24* | 2500 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

Dual Supply Octal Translating Transceiver

The 74LVX4245 is a dual-supply device well capable of bidirectional signal voltage translation. This level shifting ability provides an excellent interface between low voltage CPU local bus and a standard 5.0 V I/O bus. The device control inputs can be controlled by either the low voltage CPU and core logic or a bus arbitrator with 5.0 V I/O levels.

The LVX4245 is ideal for mixed voltage applications such as notebook computers using a 3.3 V CPU and 5.0 V peripheral devices.

Applications:

Mixed Mode Dual Supply Interface Solutions

The LVX4245 is designed to solve 3.0 V / 5.0 V interfaces when CMOS devices cannot tolerate I/O levels above their applied V_{CC} . If an I/O pin of a 3.0 V device is driven by a 5.0 V device, the P-Channel transistor in the 3.0 V device will conduct – causing current flow from the I/O bus to the 3.0 V power supply. The result may be destruction of the 3.0 V device through latchup effects. A current limiting resistor may be used to prevent destruction, but it causes speed degradation and needless power dissipation.

A better solution is provided in the LVX4245. It provides two different output levels that easily handle the dual voltage interface. The A port is a dedicated 5.0 V port; the B port is a dedicated 3.0 V port.

Since the LVX4245 is a '245 transceiver, the user may either use it for bidirectional or unidirectional applications. The center 20 pins are configured to match a '245 pinout. This enables the user to easily replace this level shifter with a 3.0 V '245 device without additional layout work or re-manufacture of the circuit board (when both buses are 3.0 V).

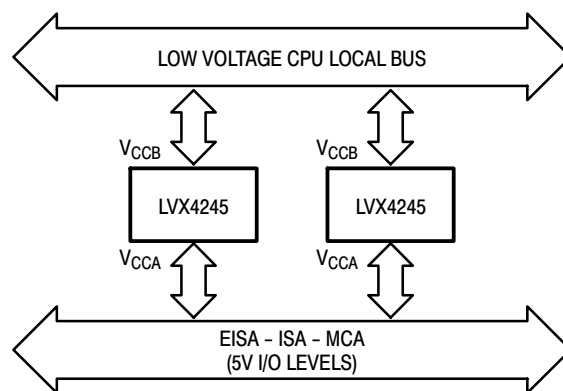


Figure 3. 3.3V/5V Interface Block Diagram

Powering Up the LVX4245

When powering up the LVX4245, please note that if the V_{CCB} pin is powered-up well in advance of the V_{CCA} pin, several milliamps of either I_{CCB} or I_{CC} current will result. If the V_{CCA} pin is powered-up in advance of the V_{CCB} pin then only nanoamps of I_{CC} current will result. In actuality the V_{CCB} can be powered “slightly” before the V_{CCA} without the current penalty, but this “setup time” is dependent on the power-up ramp rate of the V_{CC} pins. With a ramp rate of approximately 50 mV/ns (50V/ μ s) a 25 ns setup time was observed (V_{CCB} before V_{CCA}). With a 7.0 V/ μ s rate, the setup time was about 140ns. When all is said and done, the safest powerup strategy is to simply power V_{CCA} before V_{CCB} . One more note: if the V_{CCB} ramp rate is faster than the V_{CCA} ramp rate then power problems might still occur, even if the V_{CCA} powerup began prior to the V_{CCB} powerup.

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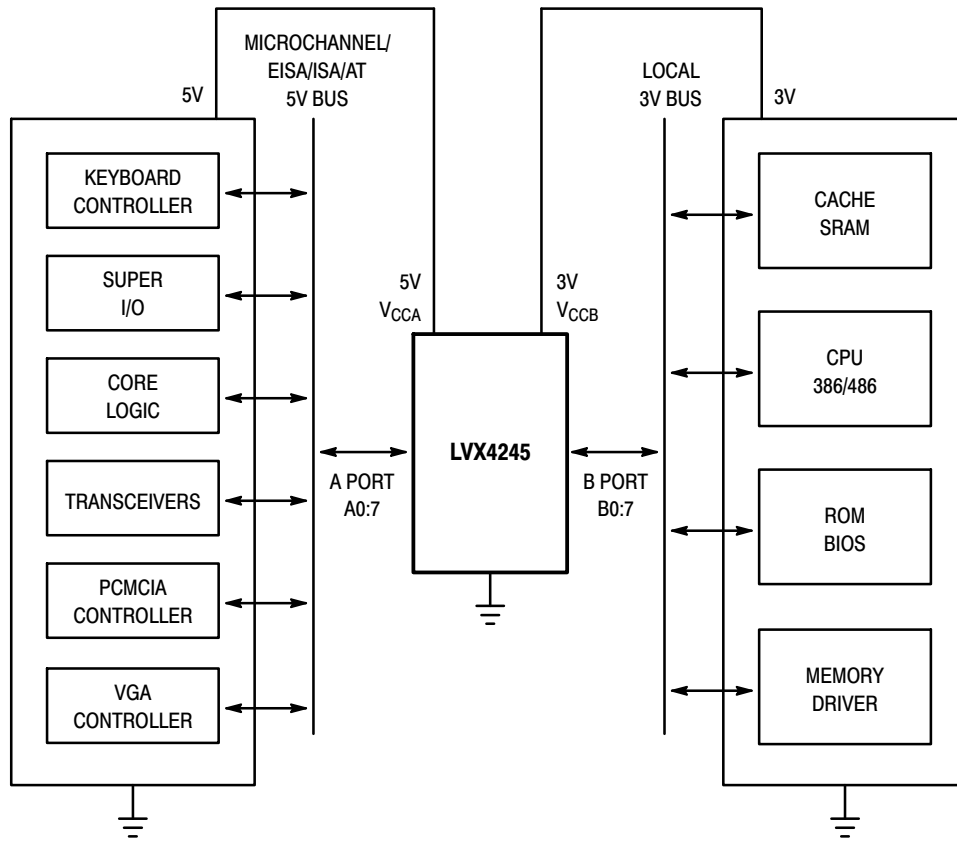


Figure 4. MC74LVX4245 Fits Into a System with 3V Subsystem and 5V Subsystem

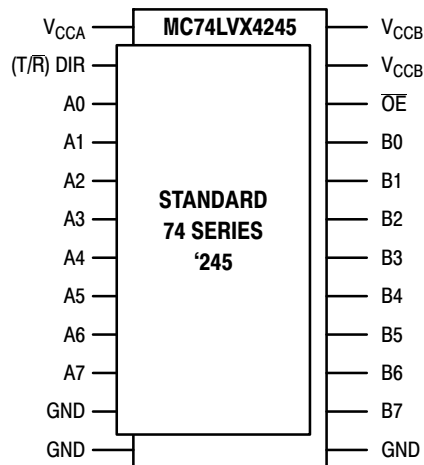
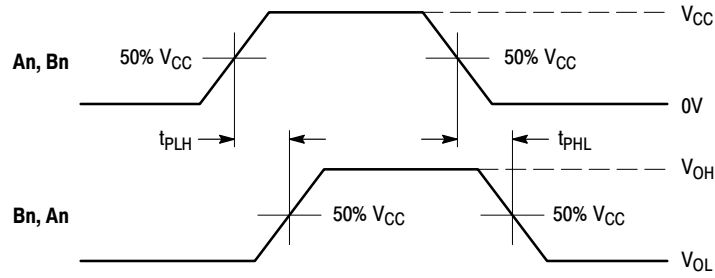
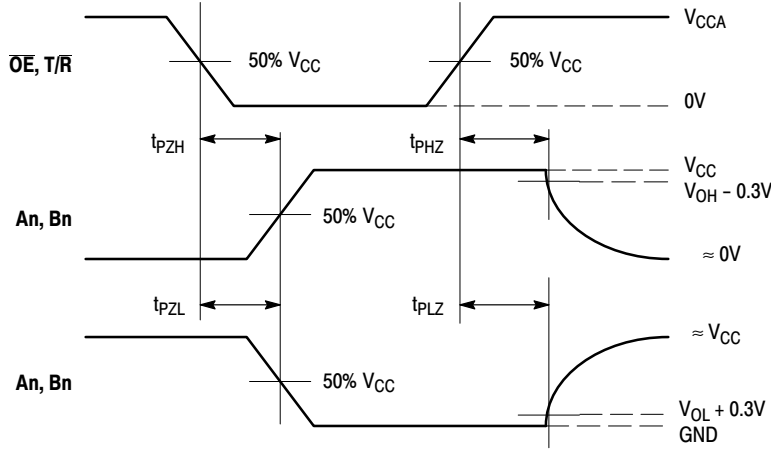


Figure 5. MC74LVX4245 Pin Arrangement Is Compatible to 20-Pin 74 Series '245s

MC74LVX4245

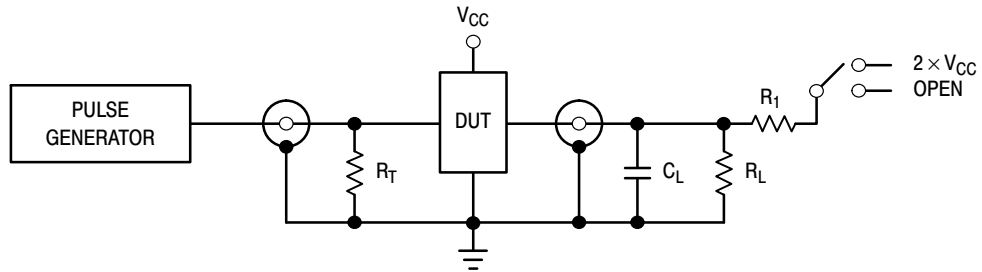


WAVEFORM 1 - PROPAGATION DELAYS
 $t_R = t_F = 2.5\text{ns}$, 10% to 90%; $f = 1\text{MHz}$; $t_W = 500\text{ns}$



WAVEFORM 2 - OUTPUT ENABLE AND DISABLE TIMES
 $t_R = t_F = 2.5\text{ns}$, 10% to 90%; $f = 1\text{MHz}$; $t_W = 500\text{ns}$

Figure 6. AC Waveforms



| TEST | SWITCH |
|---|-------------------|
| t_{PLH} , t_{PHL} , t_{PZH} , t_{PHZ} | Open |
| t_{PZL} , t_{PLZ} | $2 \times V_{CC}$ |

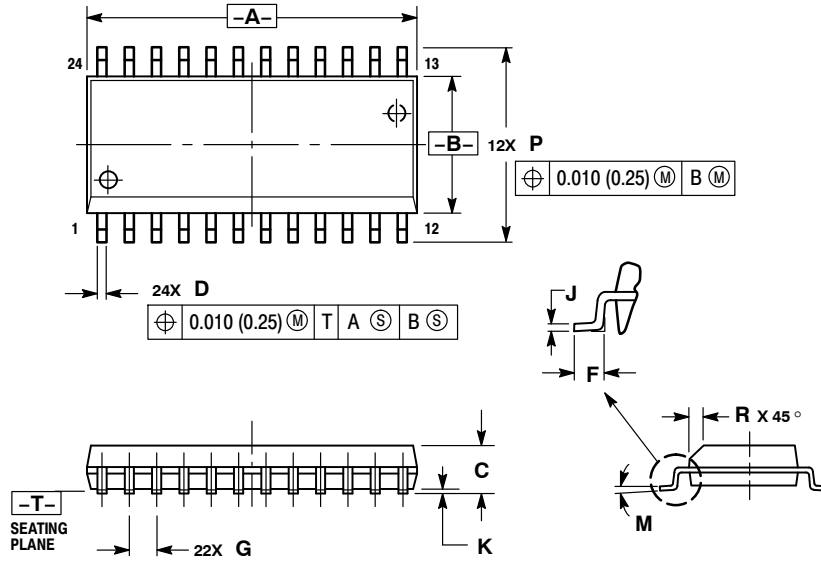
$C_L = 50\text{pF}$ or equivalent (Includes jig and probe capacitance)
 $R_L = R_1 = 500\Omega$ or equivalent
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 7. Test Circuit

MC74LVX4245

PACKAGE DIMENSIONS

SOIC-24
DW SUFFIX
CASE 751E-04
ISSUE E



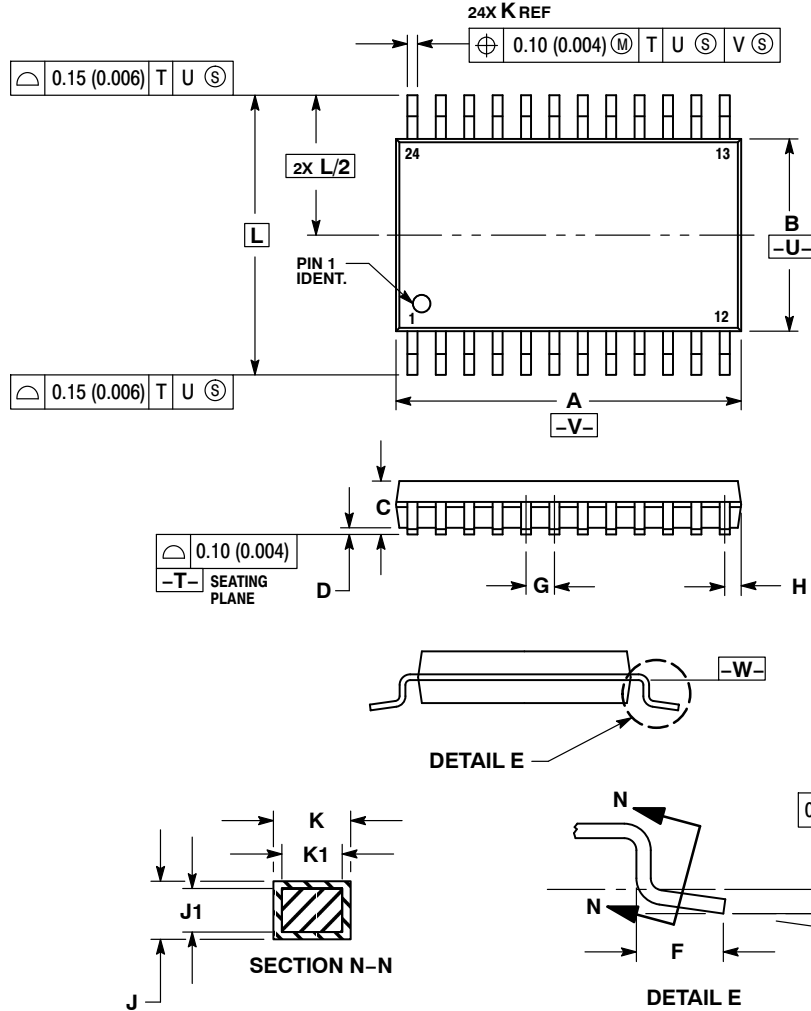
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 15.25 | 15.54 | 0.601 | 0.612 |
| B | 7.40 | 7.60 | 0.292 | 0.299 |
| C | 2.35 | 2.65 | 0.093 | 0.104 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.41 | 0.90 | 0.016 | 0.035 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.23 | 0.32 | 0.009 | 0.013 |
| K | 0.13 | 0.29 | 0.005 | 0.011 |
| M | 0° | 8° | 0° | 8° |
| P | 10.05 | 10.55 | 0.395 | 0.415 |
| R | 0.25 | 0.75 | 0.010 | 0.029 |

MC74LVX4245

PACKAGE DIMENSIONS

TSSOP-24
DT SUFFIX
CASE 948H-01
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 7.70 | 7.90 | 0.303 | 0.311 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

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Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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