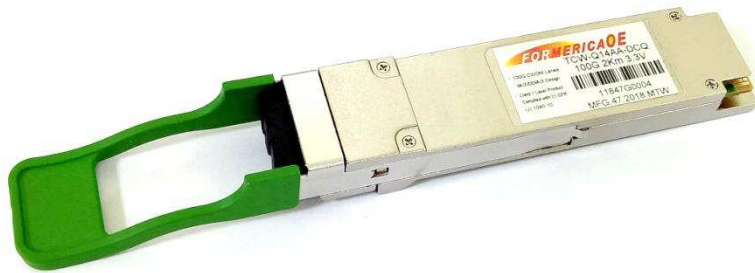


## Specification

### 100Gb/s QSFP28 Pluggable Optical Transceiver Module



## Ordering Information

**TCW-Q14AA-DCQ**

Model Name	Voltage	Category	Device type	Temperature	Distance
TCW-Q14AA-DCQ	3.3V	With DDMI	CWDM DFB	0°C ~ +70°C	2km

## Features

- QSFP28 MSA compliant
- 4 CWDM lanes MUX/DEMUX design
- Supports 103.1Gb/s aggregate bit rate
- 100G CWDM4 MSA Technical Spec
- Up to 2km transmission on single mode fiber (SMF).
- Operating case temperature : 0 ~ 70°C.
- 4x25G electrical interface (OIF CEI-28G-VSR)
- Maximum 3.5W operation power
- LC duplex connector.
- RoHS compliant.

## Applications

- Data Center Interconnect
- 100G Ethernet
- Infiniband QDR and DDR interconnects
- Enterprise networking

## General Description

This product is a transceiver module designed for 2km optical communication applications. The design is compliant to 100GBASE CWDM4 MSA standard. The module converts 4 inputs channels (ch) of 25Gb/s electrical data to 4 CWDM optical signals, and multiplexes them into a single channel for 100Gb/s optical transmission. Reversely, on the receiver side, the module optically de-multiplexes a 100Gb/s input into 4 CWDM channels signals, and converts them to 4 channel output electrical data.

The central wavelengths of the 4 CWDM channels are 1271, 1291, 1311 and 1331 nm as members of the CWDM wavelength grid defined in ITU-T G.694.2. It contains a duplex LC connector for the optical interface and a 38-pin connector for the electrical interface. To minimize the optical dispersion in the long-haul system, single-mode fiber (SMF) has to be applied in this module. Host FEC is required to support up to 2km fiber transmission.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP28 Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

## Functional Description

This product converts the 4-channel 100Gb/s electrical input data into CWDM optical signals (light), by a driven 4-wavelength Distributed Feedback Laser (DFB) array. The light is combined by the MUX parts as a 100Gb/s data, propagating out of the transmitter module from the SMF. The receiver module accepts the 100Gb/s CWDM optical signals input, and de-multiplexes it into 4 individual 25Gb/s channels with different wavelength. Each wavelength light is collected by a discrete photo diode, and then outputted as electric data after amplified by a TIA and a post amplifier. Figure 1 shows the functional block diagram of this product.

A single +3.3V power supply is required to power up this product. Both power supply pins VccTx and VccRx are internally connected and should be applied concurrently. As per MSA specifications the module offers 7 low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, LPMode, ModPrsL and IntL.

Module Select (ModSelL) is an input pin. When held low by the host, this product responds to 2-wire serial communication commands. The ModSelL allows the use of this product on a single 2-wire interface bus – individual ModSelL lines must be used.

Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the QSFP+ memory map.

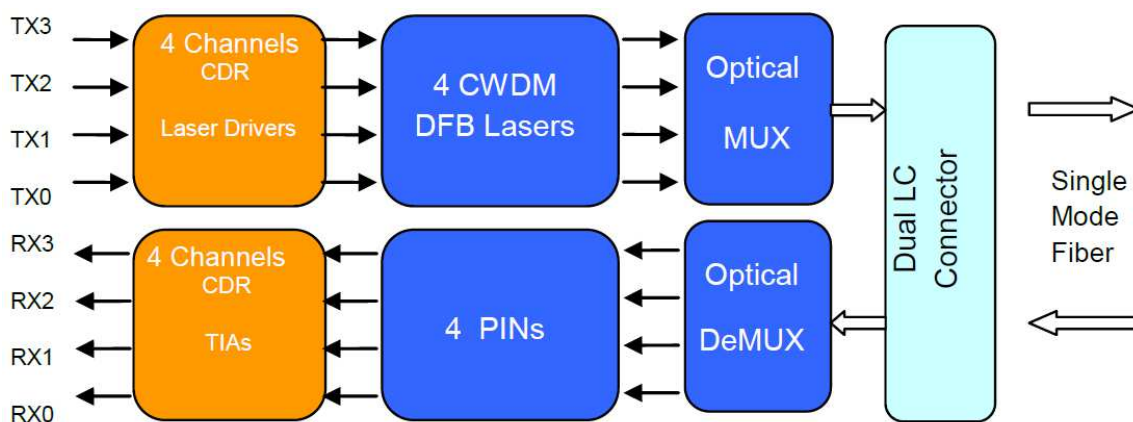
The ResetL pin enables a complete reset, returning the settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until it indicates a completion of the reset interrupt. The product indicates this by posting an IntL (Interrupt) signal with the Data\_Not\_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

Low Power Mode (LPMode) pin is used to set the maximum power consumption for the product in order to protect hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted.

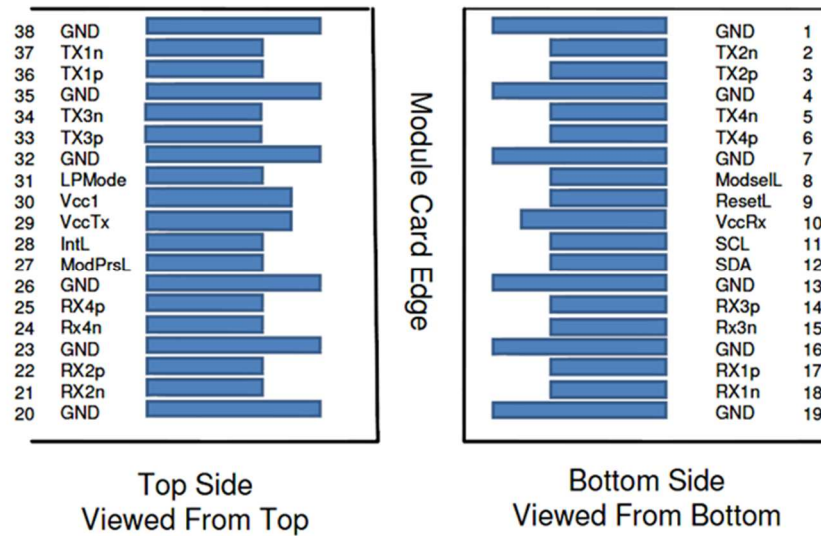
Module Present (ModPrsL) is a signal local to the host board which, in the absence of a product, is normally pulled up to the host Vcc. When the product is inserted into the connector, it completes the path to ground through a resistor on the host board and asserts the signal. ModPrsL then indicates its present by setting ModPrsL to a “Low” state.

Interrupt (IntL) is an output pin. “Low” indicates a possible operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to the Host Vcc voltage on the Host board.

### Transceiver Block Diagram



## Pin Assignment and Pin Description



## Pin Definitions

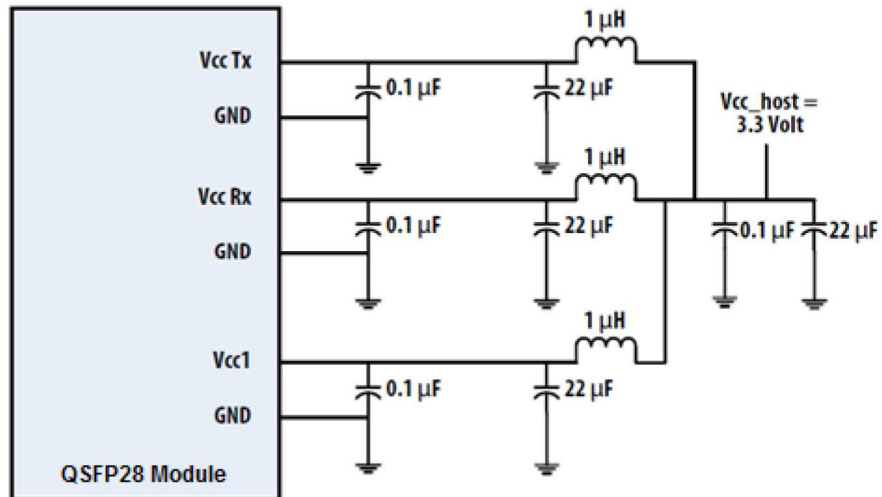
PIN	Logic	Symbol	Name/Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	
7		GND	Ground	1
8	LVTLL-I	ModSelL	Module Select	
9	LVTLL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVC MOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVC MOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1

20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	1
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3 V Power Supply transmitter	2
30		Vcc1	+3.3 V Power Supply	2
31	LVTTL-I	LPMMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Output	
38		GND	Ground	1

**Notes:**

1. **GND is the symbol for signal and supply (power) common for the QSFP28 module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common groundplane.**
2. **VccRx, Vcc1 and VccTx are the receiving and transmission power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown in Figure 1 below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the module in any combination. The connector pins are each rated for a maximum current of 1000mA.**

### Recommended Power Supply Filter



### Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Max	Unit	Notes
Storage Temperature	T <sub>s</sub>	-40	85	°C	
Operating Case Temperature	T <sub>OP</sub>	0	70		
Power Supply Voltage	V <sub>CC</sub>	-0.5	3.6	V	
Relative Humidity (non-condensation)	RH	0	85	%	

### Recommended Operating Conditions

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Operating Case Temperature	T <sub>OP</sub>	0		70	°C	
Power Supply Voltage	V <sub>CC</sub>	3.135	3.30	3.465	V	
Data Rate, each Lane			25.78125		Gb/s	
Data Rate Accuracy		-100		100	ppm	
Control Input Voltage High		2		V <sub>CC</sub>	V	
Control Input Voltage Low		0		0.8	V	
Link Distance with G.652	D	0.002		2	Km	

## Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Parameter	Test Point	Min	Typ.	Max	Unit	Note
TRx Power Consumption				3.5	W	
Supply Current	I <sub>cc</sub>			1.06	A	
<b>Transmitter (each Lane)</b>						
Overload Differential Voltage pk-pk	TP1a	900			mV	
Common Mode Voltage (V <sub>cm</sub> )	TP1	-350		2850	mV	1
Differential Termination Resistance Mismatch	TP1			10	%	At 1MHZ
Differential Return Loss (SDD11)	TP1	See CEI-28G-VSR Equation 13-19			dB	
Common Mode to Differential conversion and Differential to Common Mode conversion (SDC11, SCD11)	TP1	See CEI-28G-VSR Equation 13-20			dB	
Stressed Input Test	TP1a	See CEI-28G-VSR Section 13.3.11.2.1				
<b>Receiver (each Lane)</b>						
Differential Voltage, pk-pk	TP4			900	mV	
Common Mode Voltage (V <sub>cm</sub> )	TP4	-350		2850	mV	
Common Mode Noise, RMS	TP4			17.5	mV	
Differential Termination Resistance Mismatch	TP4			10	%	At 1MHZ
Differential Return Loss (SDD22)	TP4	See CEI-28G-VSR Equation 13-19			dB	
Common Mode to Differential conversion and Differential to Common Mode conversion (SDC22, SCD22)	TP4	See CEI-28G-VSR Equation 13-21			dB	
Common Mode Return Loss (SCC22)	TP4			-2	dB	2



Transition Time, 20 to 80%	TP4	9.5			Ps	
Vertical Eye Closure (VEC)	TP4			5.5	dB	
Eye Width at $10^{-15}$ probability (EW15)	TP4	0.57			UI	
Eye Height at $10^{-15}$ probability (EH15)	TP4	228			mV	

**Notes:**

1. Vcm is generated by the host. Specification includes effects of ground offset voltage.
2. From 250MHz to 30GHz.

## Optical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Lane Center Wavelengths (Range)	L0	1264.5	1271	1277.5	nm	
	L1	1284.5	1291	1297.5	nm	
	L2	1304.5	1311	1317.5	nm	
	L3	1324.5	1331	1337.5	nm	
<b>Transmitter</b>						
Side-Mode Suppression Ratio	SMSR	30			dB	
Total Average Launch Power	$P_T$			8.5	dBm	
Output Optical Power: Average	$P_{O_{AVE}}$	-6.5		2.5	dBm	
Optical Modulation Amplitude (OMA), each Lane	POMA	-4.0		2.5	dBm	1
Launch Power in OMA minus Transmitter and Dispersion Penalty (TDP), each Lane		-5.0			dBm	
TDP, each Lane				3.0	dB	
Extinction Ratio	ER	3.5			dB	
Optical Return Loss Tolerance	TOL			20	dB	
Transmitter Reflectance	$R_T$			-12	dB	
Average Launch Power OFF Transmitter, each Lane	$P_{off}$			-30	dBm	
Transmitter Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}		{0.31, 0.4, 0.45, 0.34, 0.38, 0.4}				2

Receiver						
Damage Threshold, each Lane	DT	3.5			dBm	3
Average receive power, Each Lane		-11.5		2.5	dBm	
Receive Power (OMA), each Lane				2.5	dBm	
Receiver Sensitivity (OMA), each Lane				-10	dBm	for BER =5x10 <sup>-5</sup>
Stressed Receiver Sensitivity (OMA), each Lane				-7.3	dBm	4
Receiver Reflectance	R <sub>R</sub>			-26	dB	
LOS Assert	LOSA	-30			dBm	
LOS Deassert	LOSD			-15	dBm	
LOS Hysteresis	LOSH	0.5			dB	
Receiver Electrical 3 dB upper Cutoff Frequency, each Lane				31	GHz	
Conditions of Stress Receiver Sensitivity Test (Note 5)						
Vertical Eye Closure Penalty, each Lane			1.9		dB	
Stressed Eye J2 Jitter, each Lane			0.33		UI	
Stressed Eye J4 Jitter, each Lane			0.48		UI	
SRS eye mask definition { X1, X2, X3, Y1, Y2, Y3 }		{0.39, 0.5, 0.5, 0.39, 0.39, 0.4}				

**Notes:**

1. Even if the TDP < 1.0 dB, the OMA min must exceed the minimum value specified here.
2. Hit ratio 5x10<sup>-5</sup>.
3. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
4. Measured with conformance test signal for BER = 5x10<sup>-5</sup>.
5. Vertical eye closure penalty, stressed eye J2 jitter, stressed eye J4 jitter, and SRS eye mask definition are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

## Digital Diagnostic Functions

The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

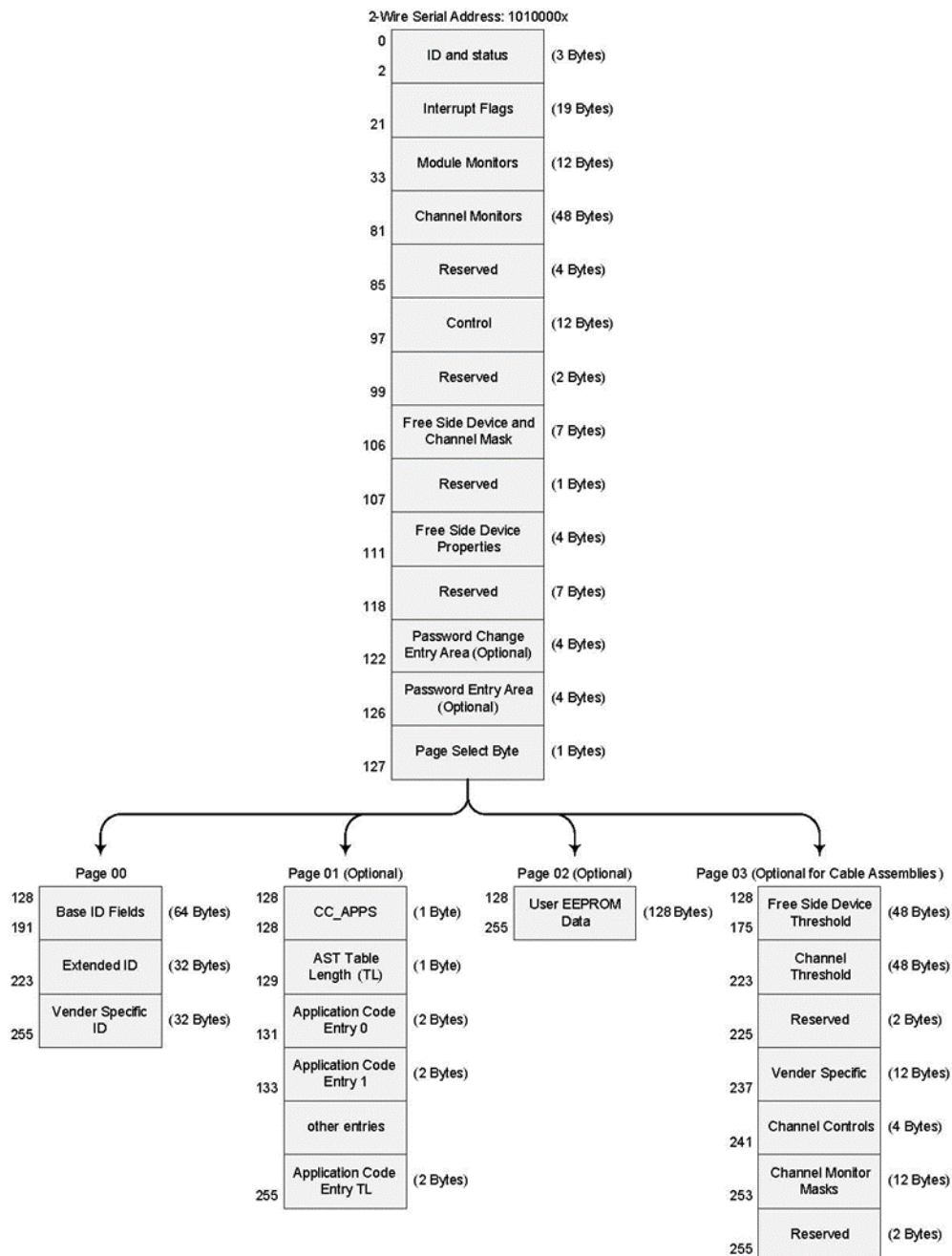
Parameter	Symbol	Min	Max	Unit	Note
Temperature monitor absolute error	DMI_Temp	-3	3	degC	Over temperature
Supply voltage monitor absolute error	DMI_VCC	-0.1	0.1	V	Over range
Channel RX power monitor absolute error	DMI_RX_Ch	-2	2	dB	1
Channel Bias current monitor	DMI_Ibias_Ch	-10%	-10%	mA	
Channel TX power monitor absolute error	DMI_TX_Ch	-2	2	dB	1

**Notes:**

Due to measurement accuracy of different single mode fibers, there could be an additional +/- 1 dB fluctuation, or a +/- 3 dB total accuracy.

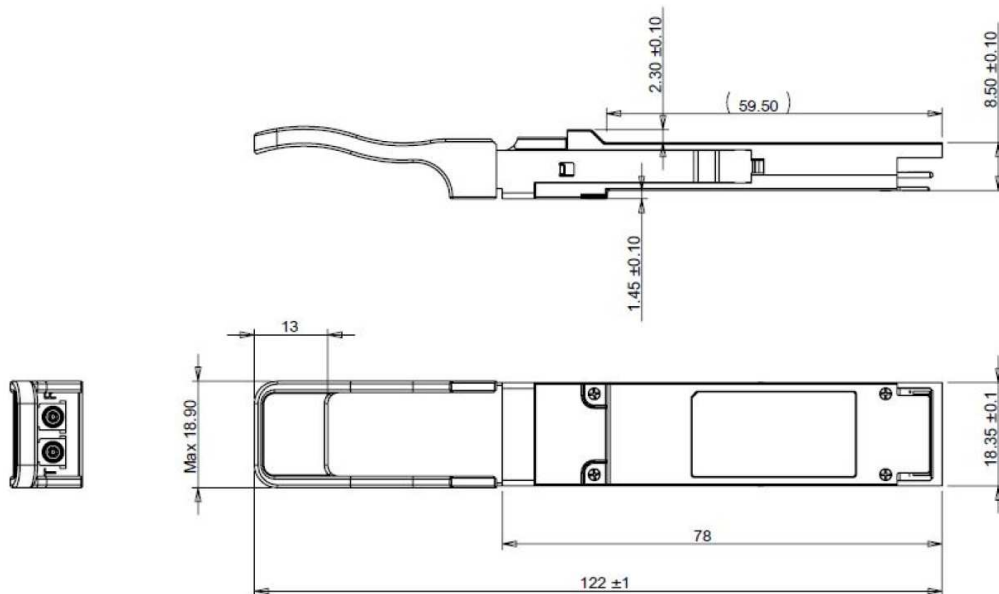
## Memory Map

The memory map is structured as a single address and multiple page approaches, according to the QSFP28 SFF-8636 MSA specification as shown in the below. For more detailed description of this memory map or lower pages, please see our Memory Map document with flexible customization settings.



## Mechanical Design Diagram

Unit: mm



## ESD

Normal ESD precautions are required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

## Laser Safety

This is a Class 1 Laser Product according to IEC / EN 60825-1: 2014 (Third Edition). This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

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