

# MAX97003

## High-Efficiency, Low-Noise Audio Subsystem

### General Description

The MAX97003 audio subsystem combines a mono speaker amplifier with a stereo headphone amplifier. The headphone and speaker amplifiers have independent volume and on/off controls. The four inputs are configurable as two differential or four single-ended inputs.

To minimize output noise, both the headphone and speaker outputs utilize a downward expander/noise gate to attenuate noise when no desired input signal is present.

The speaker output incorporates an adjustable dynamic range compressor (DRC) and distortion limiter to protect the speaker and maximize loudness. This allows high gain for low-level signals without compromising the quality of large signals.

All controls are performed using the two-wire I<sup>2</sup>C interface. The IC operates in the extended -40°C to +85°C temperature range, and is available in the 2.0mm x 2.4mm, 20-bump WLP package (0.4mm pitch).

### Applications

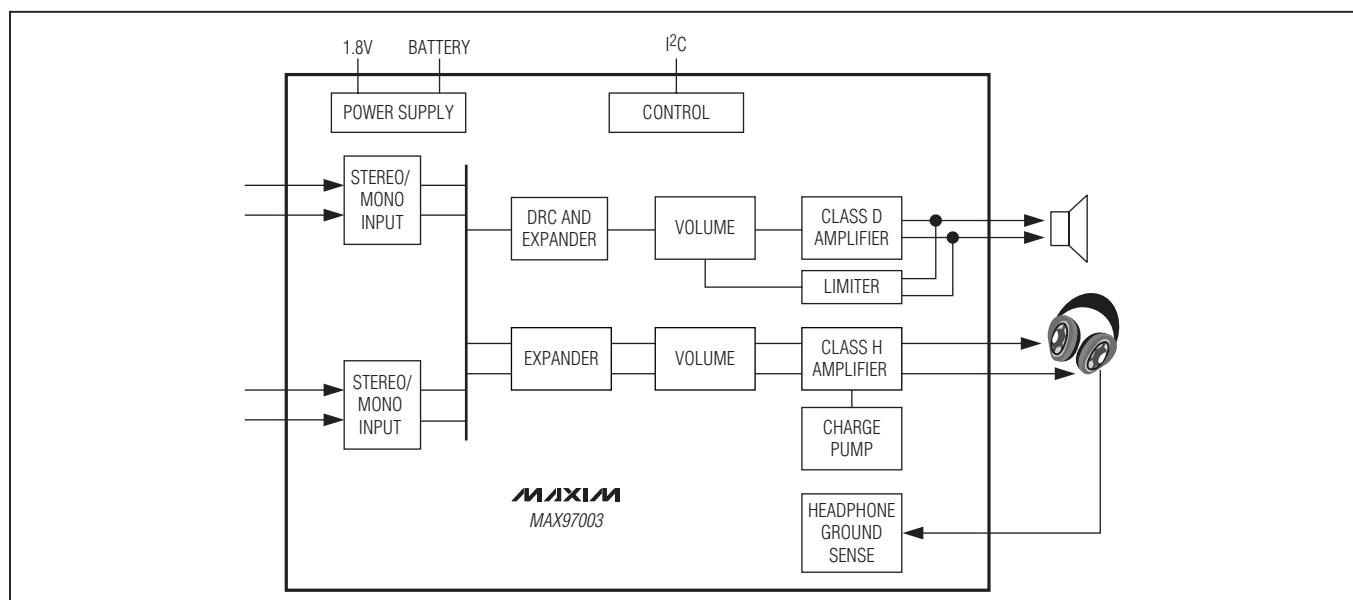
Cell Phones  
Portable Media Players

Ordering Information appears at end of data sheet.

### Features

- ◆ 2.7V to 5.5V Speaker Supply Voltage
- ◆ 1.8V Headphone Supply Voltage
- ◆ 1.0W Speaker Output ( $V_{PVDD} = 4.2V$ ,  $Z_{SPK} = 8\Omega + 68\mu H$ , 1% THD+N)
- ◆ 32mW/Channel Headphone Output ( $R_{HP} = 32\Omega$ )
- ◆ Active Emissions Limiting for Enhanced EMI Reduction
- ◆ Efficient Class H Headphone Amplifier
- ◆ Ground-Referenced Headphone Outputs
- ◆ Headphone Ground Sense
- ◆ 2 Stereo Single-Ended/Mono Differential Inputs
- ◆ Integrated Expander/Noise Gate for Low Output Noise
- ◆ Integrated DRC (Speaker Outputs)
- ◆ Integrated Distortion Limiter (Speaker Outputs)
- ◆ Extensive Click-and-Pop Reduction Circuitry
- ◆ TDMA Noise Free
- ◆ 2.0mm x 2.4mm, 20-Bump WLP Package (0.4mm Pitch)

### Simplified Block Diagram



For related parts and recommended products to use with this part, refer to: [www.maxim-ic.com/MAX97003.related](http://www.maxim-ic.com/MAX97003.related).

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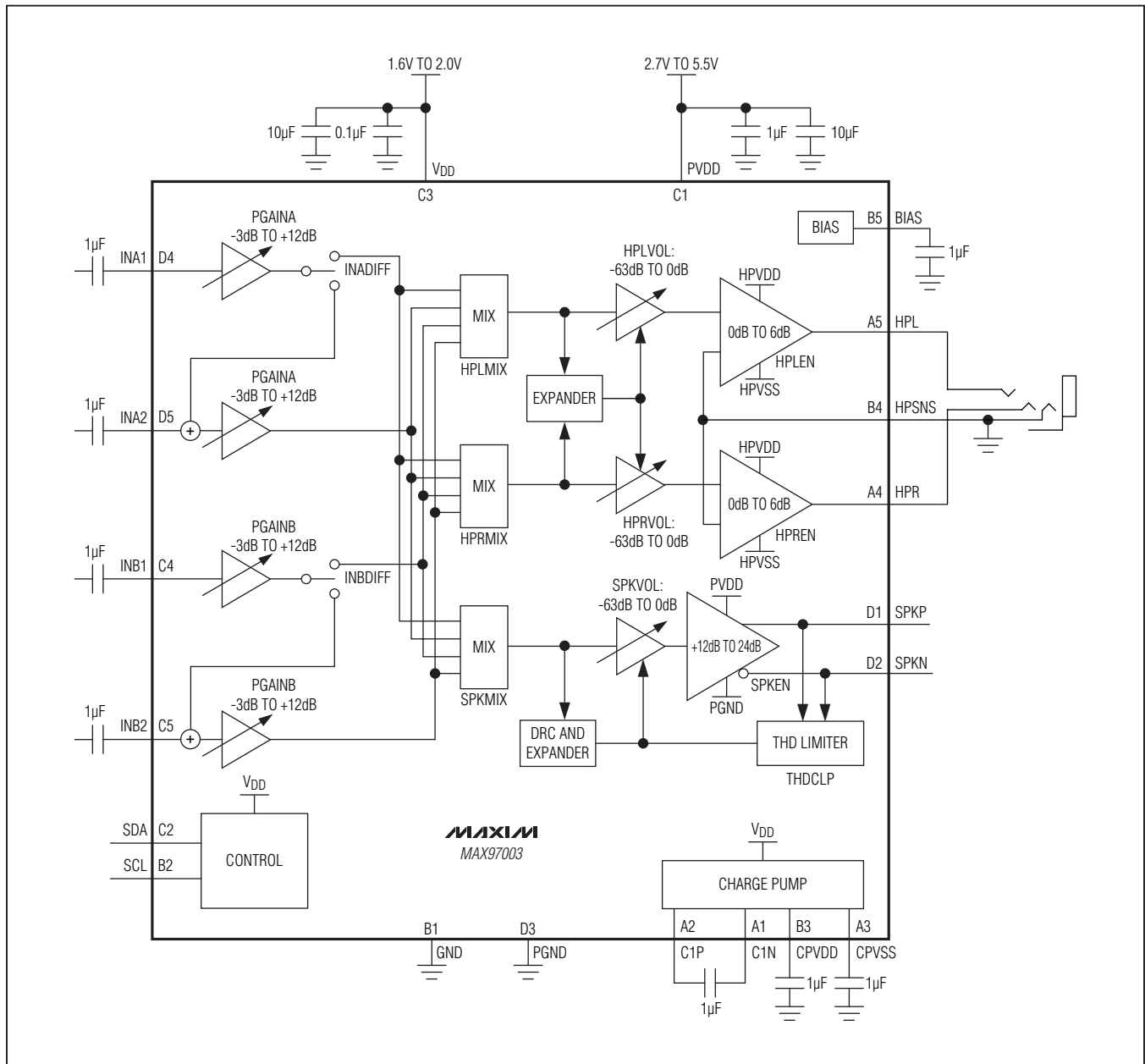
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## High-Efficiency, Low-Noise Audio Subsystem

### Functional Diagram/Typical Application Circuit



# High-Efficiency, Low-Noise Audio Subsystem

## ABSOLUTE MAXIMUM RATINGS

(Voltages with respect to GND.)

|                         |                                                            |
|-------------------------|------------------------------------------------------------|
| V <sub>DD</sub> , CPVDD | -0.3V to +2.2V                                             |
| BIAS                    | -0.3V to (V <sub>DD</sub> + 0.3V)                          |
| PVDD                    | -0.3V to +6.0V                                             |
| PGND                    | -0.1V to +0.1V                                             |
| CPVSS                   | -2.2V to +0.3V                                             |
| C1N                     | (V <sub>CPVSS</sub> - 0.3V) to (V <sub>CPVDD</sub> + 0.3V) |
| C1P                     | -0.3V to (V <sub>CPVDD</sub> + 0.3V)                       |
| HPL, HPR                | (V <sub>CPVSS</sub> - 0.3V) to (V <sub>CPVDD</sub> + 0.3V) |
| INA1, INA2, INB1, INB2  | -0.3V to +6.0V                                             |
| SDA, SCL                | -0.3V to +6.0V                                             |
| SPKP, SPKN              | -0.3V to (V <sub>PVDD</sub> + 0.3V)                        |
| HPSNS                   | -0.3V to +0.3V                                             |

|                                                         |                 |
|---------------------------------------------------------|-----------------|
| Continuous Current In/Out of PVDD, PGND, SPK_           | ±800mA          |
| Continuous Current In/Out of HPR, HPL, V <sub>DD</sub>  | ±140mA          |
| Continuous Input Current (all other pins)               | ±20mA           |
| Duration of SPK_ Short Circuit to GND or PVDD           | Continuous      |
| Duration of Short Circuit Between SPKP and SPKN         | Continuous      |
| Duration of HP_ Short Circuit to GND or V <sub>DD</sub> | Continuous      |
| Continuous Power Dissipation (T <sub>A</sub> = +70°C)   |                 |
| WLP Multilayer Board                                    |                 |
| (derate 21.7mW/°C above +70°C)                          | 1.74W           |
| Junction Temperature                                    | +150°C          |
| Operating Temperature Range                             | -40°C to +85°C  |
| Storage Temperature Range                               | -65°C to +150°C |
| Soldering Temperature (reflow)                          | +260°C          |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>DD</sub> = 1.8V, V<sub>PVDD</sub> = 4.2V, V<sub>GND</sub> = V<sub>PGND</sub> = 0V. Headphone path: PGAIN<sub>-</sub> = -1.5dB, HP\_VOL = 0dB, HPGAIN = +2dB, input signal configured single-ended. Speaker path: PGAIN<sub>-</sub> = 0dB, SPKVOL = 0dB, SPKGAIN = +12dB, input signal configured differential. Speaker loads (Z<sub>SPK</sub>) connected between SPKP and SPKN. Headphone loads (R<sub>HP</sub>) connected from HPL or HPR to GND. SDA and SCL pullup voltage = 1.8V. Z<sub>SPK</sub> = ∞, R<sub>HP</sub> = ∞. C<sub>C1P-C1N</sub> = C<sub>CPVDD</sub> = C<sub>CPVSS</sub> = C<sub>BIAS</sub> = 1μF. T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Note 1)

| PARAMETER                                | SYMBOL          | CONDITIONS                                                                                                                                    | MIN               | TYP  | MAX  | UNITS |
|------------------------------------------|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------|-------------------|------|------|-------|
| Speaker Amplifier Supply Voltage Range   | PVDD            | Guaranteed by PSRR test                                                                                                                       | 2.7               |      | 5.5  | V     |
| Headphone Amplifier Supply Voltage Range | V <sub>DD</sub> | Guaranteed by PSRR test                                                                                                                       | 1.6               |      | 2    | V     |
| Quiescent Current                        | I <sub>DD</sub> | HP mode, T <sub>A</sub> = +25°C, stereo SE input on INA routed to HP output, HP expander disabled                                             | I <sub>VDD</sub>  | 1.21 | 1.6  | mA    |
|                                          |                 |                                                                                                                                               | I <sub>PVDD</sub> | 1.07 | 1.3  |       |
|                                          |                 | HP mode, T <sub>A</sub> = +25°C, stereo SE input on INA routed to HP output, HP expander enabled                                              | I <sub>VDD</sub>  | 2.46 | 2.95 |       |
|                                          |                 |                                                                                                                                               | I <sub>PVDD</sub> | 1.34 | 1.6  |       |
|                                          |                 | SPK mode, T <sub>A</sub> = +25°C mono differential input on INA routed to SPK output; SPK expander, DRC, and limiter all disabled             | I <sub>VDD</sub>  | 0.1  | 0.15 |       |
|                                          |                 |                                                                                                                                               | I <sub>PVDD</sub> | 2.25 | 2.6  |       |
|                                          |                 | SPK mode, T <sub>A</sub> = +25°C mono differential input on INA routed to SPK output; SPK expander, DRC, and limiter all enabled              | I <sub>VDD</sub>  | 1.35 | 1.65 |       |
|                                          |                 |                                                                                                                                               | I <sub>PVDD</sub> | 2.6  | 2.95 |       |
|                                          |                 | SPK + HP mode, T <sub>A</sub> = +25°C stereo SE input on INA routed to HP and SPK output; SPK and HP expanders, DRC, and limiter all disabled | I <sub>VDD</sub>  | 1.21 | 1.6  |       |
|                                          |                 |                                                                                                                                               | I <sub>PVDD</sub> | 2.74 | 3.2  |       |

# High-Efficiency, Low-Noise Audio Subsystem

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = 1.8V$ ,  $V_{PVDD} = 4.2V$ ,  $V_{GND} = V_{PGND} = 0V$ . Headphone path:  $PGAIN_- = -1.5dB$ ,  $HP\_VOL = 0dB$ ,  $HPGAIN = +2dB$ , input signal configured single-ended. Speaker path:  $PGAIN_- = 0dB$ ,  $SPKVOL = 0dB$ ,  $SPKGAIN = +12dB$ , input signal configured differential. Speaker loads ( $Z_{SPK}$ ) connected between  $SPKP$  and  $SPKN$ . Headphone loads ( $R_{HP}$ ) connected from  $HPL$  or  $HPR$  to  $GND$ . SDA and SCL pullup voltage =  $1.8V$ .  $Z_{SPK} = \infty$ ,  $R_{HP} = \infty$ .  $C_{C1P-C1N} = C_{CPVDD} = C_{CPVSS} = C_{BIAS} = 1\mu F$ .  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .) (Note 1)

| PARAMETER                   | SYMBOL            | CONDITIONS                                                                                                    |                  | MIN   | TYP   | MAX   | UNITS            |
|-----------------------------|-------------------|---------------------------------------------------------------------------------------------------------------|------------------|-------|-------|-------|------------------|
| Shutdown Current            | I <sub>SHDN</sub> | I <sub>VDD</sub> , T <sub>A</sub> = +25°C                                                                     |                  |       | 0.08  | 2.5   | μA               |
|                             |                   | I <sub>PVDD</sub> , T <sub>A</sub> = +25°C                                                                    |                  |       | 0.05  | 1     |                  |
| Turn On-Time                | t <sub>ON</sub>   | Time from power-on to full operation                                                                          | SLEW = 0         |       | 17    |       | ms               |
|                             |                   |                                                                                                               | SLEW = 1         |       | 10    |       |                  |
| PREAMPLIFIERS               |                   |                                                                                                               |                  |       |       |       |                  |
| Input Resistance            | R <sub>IN</sub>   | T <sub>A</sub> = +25°C                                                                                        | -3dB to +9dB     | 15    | 20.4  | 28.5  | kΩ               |
|                             |                   |                                                                                                               | +10.5dB to +12dB | 5.2   | 6.96  | 9.5   |                  |
| Gain                        |                   | PGAIN_ = 0x0                                                                                                  |                  | -3.2  | -2.98 | -2.79 | dB               |
|                             |                   | PGAIN_ = 0x1                                                                                                  |                  |       | -1.49 |       |                  |
|                             |                   | PGAIN_ = 0x2                                                                                                  |                  | -0.22 | -0.02 | +0.21 |                  |
|                             |                   | PGAIN_ = 0x3                                                                                                  |                  |       | 1.57  |       |                  |
|                             |                   | PGAIN_ = 0x4                                                                                                  |                  |       | 3.04  |       |                  |
|                             |                   | PGAIN_ = 0x5                                                                                                  |                  |       | 4.52  |       |                  |
|                             |                   | PGAIN_ = 0x6                                                                                                  |                  |       | 6.06  |       |                  |
|                             |                   | PGAIN_ = 0x7                                                                                                  |                  |       | 7.51  |       |                  |
|                             |                   | PGAIN_ = 0x8                                                                                                  |                  |       | 9.01  |       |                  |
|                             |                   | PGAIN_ = 0x9                                                                                                  |                  |       | 10.59 |       |                  |
|                             |                   | PGAIN_ = 0xA                                                                                                  |                  | 11.82 | 12    | 12.36 |                  |
| Maximum Input Signal Swing  |                   | Preamp = 0dB                                                                                                  |                  |       | 2.4   |       | V <sub>P-P</sub> |
| Common-Mode Rejection Ratio | CMRR              | f = 1kHz (differential input mode), 0dB                                                                       |                  |       | 63    |       | dB               |
| Input DC Voltage            |                   | IN__ inputs                                                                                                   |                  | 1.2   | 1.23  | 1.275 | V                |
| Bias Voltage                | V <sub>BIAS</sub> |                                                                                                               |                  | 1.2   | 1.23  | 1.275 | V                |
| SPEAKER AMPLIFIER           |                   |                                                                                                               |                  |       |       |       |                  |
| Output Offset Voltage       | V <sub>OS</sub>   | T <sub>A</sub> = +25°C (volume at mute, SPKGAIN = 00)                                                         |                  |       | ±0.5  | ±2.5  | mV               |
|                             |                   | T <sub>A</sub> = +25°C (volume at 0dB, SPKGAIN = 00)                                                          |                  |       | ±1.0  |       |                  |
| Click-and-Pop Level         | K <sub>CP</sub>   | Peak voltage, T <sub>A</sub> = +25°C, A-weighted, 32 samples per second, volume at 0dB, SPKGAIN = 00 (Note 2) | Into shutdown    |       | -72   |       | dBV              |
|                             |                   |                                                                                                               | Out of shutdown  |       | -65   |       |                  |

# High-Efficiency, Low-Noise Audio Subsystem

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = 1.8V$ ,  $V_{PVDD} = 4.2V$ ,  $V_{GND} = V_{PGND} = 0V$ . Headphone path:  $PGAIN_- = -1.5dB$ ,  $HP\_VOL = 0dB$ ,  $HPGAIN = +2dB$ , input signal configured single-ended. Speaker path:  $PGAIN_- = 0dB$ ,  $SPKVOL = 0dB$ ,  $SPKGAIN = +12dB$ , input signal configured differential. Speaker loads ( $Z_{SPK}$ ) connected between SPKP and SPKN. Headphone loads ( $R_{HP}$ ) connected from HPL or HPR to GND. SDA and SCL pullup voltage = 1.8V.  $Z_{SPK} = \infty$ ,  $R_{HP} = \infty$ .  $C_{C1P-C1N} = C_{CPVDD} = C_{CPVSS} = C_{BIAS} = 1\mu F$ .  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .) (Note 1)

| PARAMETER                                | SYMBOL    | CONDITIONS                                                                              |                                                      | MIN    | TYP      | MAX    | UNITS         |
|------------------------------------------|-----------|-----------------------------------------------------------------------------------------|------------------------------------------------------|--------|----------|--------|---------------|
| Power-Supply Rejection Ratio<br>(Note 2) | PSRR      | $T_A = +25^\circ C$                                                                     | $V_{PVDD} = 2.7V$ to $5.5V$                          | 65     | 90.4     |        | dB            |
|                                          |           |                                                                                         | $f = 217Hz$ ,<br>$V_{RIPPLE} = 200mV_{P-P}$          |        | 80       |        |               |
|                                          |           |                                                                                         | $f = 1kHz$ ,<br>$V_{RIPPLE} = 200mV_{P-P}$           |        | 78       |        |               |
|                                          |           |                                                                                         | $f = 10kHz$ ,<br>$V_{RIPPLE} = 200mV_{P-P}$          |        | 72       |        |               |
| Output Power (Note 3)                    | $P_{OUT}$ | THD+N = 1%                                                                              | $Z_{SPK} = 8\Omega + 68\mu H$ ,<br>$V_{PVDD} = 4.2V$ |        | 1007     |        | mW            |
|                                          |           |                                                                                         | $Z_{SPK} = 8\Omega + 68\mu H$ ,<br>$V_{PVDD} = 3.6V$ |        | 735      |        |               |
|                                          |           |                                                                                         | $Z_{SPK} = 4\Omega + 33\mu H$ ,<br>$V_{PVDD} = 5.0V$ |        | 2585     |        |               |
| Total Harmonic Distortion Plus Noise     | THD+N     | $f = 1kHz$ , $P_{OUT} = 700mW$ , $T_A = +25^\circ C$ ,<br>$Z_{SPK} = 8\Omega + 68\mu H$ |                                                      |        | 0.06     |        | %             |
|                                          |           | $f = 1kHz$ , $P_{OUT} = 350mW$ , $T_A = +25^\circ C$ ,<br>$Z_{SPK} = 8\Omega + 68\mu H$ |                                                      |        | 0.029    | 0.048  |               |
| Output Noise                             |           | A-weighted                                                                              | Noise gate disabled                                  |        | 40       |        | $\mu V_{RMS}$ |
|                                          |           |                                                                                         | Noise gate enabled                                   |        | 25       |        |               |
| Signal-to-Noise Ratio                    | SNR       | A-weighted,<br>$P_{OUT} = 700mW$                                                        | Noise gate disabled                                  |        | 93       |        | dB            |
|                                          |           |                                                                                         | Noise gate enabled                                   |        | 98       |        |               |
| Output Frequency                         | $f_{OSC}$ | Spread spectrum                                                                         |                                                      |        | 298.9    |        | kHz           |
| Spread-Spectrum Bandwidth                |           |                                                                                         |                                                      |        | $\pm 10$ |        | kHz           |
| Gain                                     |           | SPKGAIN = 00                                                                            |                                                      |        | 11.69    |        | dB            |
|                                          |           | SPKGAIN = 01                                                                            |                                                      | 15.4   | 15.65    | 15.92  |               |
|                                          |           | SPKGAIN = 10                                                                            |                                                      |        | 19.64    |        |               |
|                                          |           | SPKGAIN = 11                                                                            |                                                      |        | 23.7     |        |               |
| Current Limit                            |           |                                                                                         |                                                      |        | 2        |        | A             |
| Efficiency                               | $\eta$    | $P_{OUT} = 1W$ , $f = 1kHz$ , $Z_{SPK} = 8\Omega + 68\mu H$                             |                                                      |        | 92       |        | %             |
| Volume Control                           |           | SPKVOL = 0x00                                                                           |                                                      | -63.35 | -62.87   | -62.36 | dB            |
|                                          |           | SPKVOL = 0x3F                                                                           |                                                      | -0.044 | 0        | 0.13   |               |
| Volume Control Step Size                 |           |                                                                                         |                                                      |        | 1        |        | dB            |
| Mute Attenuation                         |           | $f = 1kHz$                                                                              |                                                      |        | 118      |        | dB            |

# High-Efficiency, Low-Noise Audio Subsystem

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = 1.8V$ ,  $V_{PVDD} = 4.2V$ ,  $V_{GND} = V_{PGND} = 0V$ . Headphone path:  $PGAIN_- = -1.5dB$ ,  $HP\_VOL = 0dB$ ,  $HPGAIN = +2dB$ , input signal configured single-ended. Speaker path:  $PGAIN_- = 0dB$ ,  $SPKVOL = 0dB$ ,  $SPKGAIN = +12dB$ , input signal configured differential. Speaker loads ( $Z_{SPK}$ ) connected between  $SPKP$  and  $SPKN$ . Headphone loads ( $R_{HP}$ ) connected from  $HPL$  or  $HPR$  to  $GND$ . SDA and SCL pullup voltage =  $1.8V$ .  $Z_{SPK} = \infty$ ,  $R_{HP} = \infty$ .  $C_{C1P-C1N} = C_{CPVDD} = C_{CPVSS} = C_{BIAS} = 1\mu F$ .  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .) (Note 1)

| PARAMETER                             | SYMBOL             | CONDITIONS                                                                                      |                                                       | MIN                         | TYP                        | MAX                         | UNITS |
|---------------------------------------|--------------------|-------------------------------------------------------------------------------------------------|-------------------------------------------------------|-----------------------------|----------------------------|-----------------------------|-------|
| CHARGE PUMP                           |                    |                                                                                                 |                                                       |                             |                            |                             |       |
| Charge-Pump Frequency                 |                    | V <sub>HPL</sub> = V <sub>HPR</sub> = 0V                                                        |                                                       | 80                          | 83.3                       | 86                          | kHz   |
|                                       |                    | V <sub>HPL</sub> = V <sub>HPR</sub> = 0.2V                                                      |                                                       | 665                         |                            |                             |       |
|                                       |                    | V <sub>HPL</sub> = V <sub>HPR</sub> = 0.5V                                                      |                                                       | 500                         |                            |                             |       |
| Positive Output Voltage               | V <sub>CPVDD</sub> | V <sub>OUT</sub> > V <sub>TH</sub>                                                              |                                                       | V <sub>DD</sub>             |                            |                             | V     |
|                                       |                    | V <sub>OUT</sub> < V <sub>TH</sub>                                                              |                                                       | V <sub>DD</sub> /2          |                            |                             |       |
| Negative Output Voltage               | V <sub>CPVSS</sub> | V <sub>OUT</sub> > V <sub>TH</sub>                                                              |                                                       | -V <sub>DD</sub>            |                            |                             | V     |
|                                       |                    | V <sub>OUT</sub> < V <sub>TH</sub>                                                              |                                                       | -V <sub>DD</sub> /2         |                            |                             |       |
| Output Voltage Threshold              | V <sub>TH</sub>    | Output voltage at which the charge pump switches modes, V <sub>OUT</sub> rising or falling      |                                                       | ±V <sub>DD</sub><br>x 0.216 | ±V <sub>DD</sub><br>x 0.25 | ±V <sub>DD</sub><br>x 0.278 | V     |
| Mode Transition Timeouts              |                    | Time it takes for the charge pump to transition from invert to split mode                       |                                                       | 30                          |                            |                             | ms    |
|                                       |                    | Time it takes for the charge pump to transition from split to invert mode                       |                                                       | 20                          |                            |                             | µs    |
| HEADPHONE AMPLIFIERS                  |                    |                                                                                                 |                                                       |                             |                            |                             |       |
| Output Offset Voltage                 | VOS                | T <sub>A</sub> = +25°C                                                                          |                                                       | ±0.15                       |                            | ±0.5                        | mV    |
| Click-and-Pop Level                   | K <sub>CP</sub>    | Peak voltage, T <sub>A</sub> = +25°C, A-weighted, 32 samples per second, volume at 0dB (Note 2) | Into shutdown                                         | -73                         |                            |                             | dBV   |
|                                       |                    |                                                                                                 | Out of shutdown                                       | -73                         |                            |                             |       |
| Power-Supply Rejection Ratio (Note 2) | PSRR               | T <sub>A</sub> = +25°C                                                                          | V <sub>DD</sub> = 1.6V to 2.0V                        | 65                          | 99.9                       |                             | dB    |
|                                       |                    |                                                                                                 | f = 217Hz, V <sub>RIPPLE</sub> = 200mV <sub>P-P</sub> | 93                          |                            |                             |       |
|                                       |                    |                                                                                                 | f = 1kHz, V <sub>RIPPLE</sub> = 200mV <sub>P-P</sub>  | 88                          |                            |                             |       |
|                                       |                    |                                                                                                 | f = 20kHz, V <sub>RIPPLE</sub> = 200mV <sub>P-P</sub> | 65                          |                            |                             |       |

# High-Efficiency, Low-Noise Audio Subsystem

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = 1.8V$ ,  $V_{PVDD} = 4.2V$ ,  $V_{GND} = V_{PGND} = 0V$ . Headphone path:  $PGAIN_- = -1.5dB$ ,  $HP\_VOL = 0dB$ ,  $HPGAIN = +2dB$ , input signal configured single-ended. Speaker path:  $PGAIN_- = 0dB$ ,  $SPKVOL = 0dB$ ,  $SPKGAIN = +12dB$ , input signal configured differential. Speaker loads ( $Z_{SPK}$ ) connected between SPKP and SPKN. Headphone loads ( $R_{HP}$ ) connected from HPL or HPR to GND. SDA and SCL pullup voltage = 1.8V.  $Z_{SPK} = \infty$ ,  $R_{HP} = \infty$ ,  $C_{C1P-C1N} = C_{CPVDD} = C_{CPVSS} = C_{BIAS} = 1\mu F$ .  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .) (Note 1)

| PARAMETER                            | SYMBOL           | CONDITIONS                                                             |                       | MIN    | TYP   | MAX               | UNITS |
|--------------------------------------|------------------|------------------------------------------------------------------------|-----------------------|--------|-------|-------------------|-------|
| Output Power                         | P <sub>OUT</sub> | THD+N = 1%,<br>PGAINA = -1.5dB,<br>HPGAIN = +2dB                       | R <sub>HP</sub> = 16Ω | 42     |       | mW                |       |
|                                      |                  |                                                                        | R <sub>HP</sub> = 32Ω | 32     |       |                   |       |
|                                      |                  | THD+N = 0.1%,<br>PGAINA = -1.5dB,<br>HPGAIN = +2dB                     | R <sub>HP</sub> = 32Ω | 27     |       |                   |       |
| Channel-to-Channel Gain Tracking     |                  | HPL to HPR, volume at 0dB, HPLMIX = 0x1, HPRMIX = 0x2, IN_DIFF = 0     |                       | 0.25   | 1.5   | %                 |       |
| Total Harmonic Distortion Plus Noise | THD+N            | R <sub>HP</sub> = 32Ω, P <sub>OUT</sub> = 10mW, f = 1kHz               |                       | 0.005  |       | %                 |       |
|                                      |                  | R <sub>HP</sub> = 16Ω, P <sub>OUT</sub> = 10mW, f = 1kHz               |                       | 0.006  |       |                   |       |
| Output Noise                         |                  | A-weighted                                                             | Noise gate disabled   | 10     |       | μV <sub>RMS</sub> |       |
|                                      |                  |                                                                        | Noise gate enabled    | 5.9    |       |                   |       |
| Signal-to-Noise Ratio                | SNR              | A-weighted,<br>P <sub>OUT</sub> = 10mW                                 | Noise gate disabled   | 94.2   |       | dB                |       |
|                                      |                  |                                                                        | Noise gate enabled    | 96.4   |       |                   |       |
| Capacitive Drive                     | C <sub>L</sub>   |                                                                        |                       | 1000   |       | pF                |       |
| Crosstalk                            |                  | HPL to HPR, HPR to HPL, R <sub>HP</sub> = 32Ω, P <sub>OUT</sub> = 10mW | f = 20Hz to 10kHz     | -78    |       | dB                |       |
|                                      |                  |                                                                        | f = 1kHz              | -83    |       |                   |       |
| Gain                                 |                  | HPGAIN = 00                                                            |                       | -0.53  | -0.25 | +0.09             | dB    |
|                                      |                  | HPGAIN = 01                                                            |                       | 1.72   |       |                   |       |
|                                      |                  | HPGAIN = 10                                                            |                       | 3.72   |       |                   |       |
|                                      |                  | HPGAIN = 11                                                            |                       | 5.85   |       |                   |       |
| Volume Control                       |                  | HP_VOL = 0x00                                                          |                       | -63.74 | -63.3 | -62.9             | dB    |
|                                      |                  | HP_VOL = 0x3F                                                          |                       | -0.50  | -0.27 | +0.09             |       |
| Volume Control Step Size             |                  |                                                                        |                       | 1      |       | dB                |       |
| Mute Attenuation                     |                  | f = 1kHz                                                               |                       | 100    |       | dB                |       |
| SPEAKER DRC                          |                  |                                                                        |                       |        |       |                   |       |
| Release Time                         |                  | DRCRLS = 000                                                           |                       | 800    |       | ms/step           |       |
|                                      |                  | DRCRLS = 101                                                           |                       | 25     |       |                   |       |
| Attack Time                          |                  | DRCATK = 000                                                           |                       | 0.5    |       | ms                |       |
|                                      |                  | DRCATK = 111                                                           |                       | 50     |       |                   |       |
| Compression Ratio                    |                  | DRCEN = 001                                                            |                       | 1.34:1 |       | ratio             |       |
|                                      |                  | DRCEN = 101                                                            |                       | ∞:1    |       |                   |       |

# High-Efficiency, Low-Noise Audio Subsystem

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = 1.8V$ ,  $V_{PVDD} = 4.2V$ ,  $V_{GND} = V_{PGND} = 0V$ . Headphone path:  $PGAIN_- = -1.5dB$ ,  $HP\_VOL = 0dB$ ,  $HPGAIN = +2dB$ , input signal configured single-ended. Speaker path:  $PGAIN_- = 0dB$ ,  $SPKVOL = 0dB$ ,  $SPKGAIN = +12dB$ , input signal configured differential. Speaker loads ( $Z_{SPK}$ ) connected between  $SPKP$  and  $SPKN$ . Headphone loads ( $R_{HP}$ ) connected from  $HPL$  or  $HPR$  to  $GND$ . SDA and SCL pullup voltage =  $1.8V$ .  $Z_{SPK} = \infty$ ,  $R_{HP} = \infty$ .  $C_{C1P-C1N} = C_{CPVDD} = C_{CPVSS} = C_{BIAS} = 1\mu F$ .  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .) (Note 1)

| PARAMETER                      | SYMBOL | CONDITIONS                           |               | MIN   | TYP | MAX              | UNITS |
|--------------------------------|--------|--------------------------------------|---------------|-------|-----|------------------|-------|
| Compression Threshold          |        | DRCTH = 0x01                         |               | 0.839 |     | V <sub>RMS</sub> |       |
|                                |        | DRCTH = 0x1F                         |               | 0.199 |     |                  |       |
| SPEAKER AND HEADPHONE EXPANDER |        |                                      |               |       |     |                  |       |
| Attack Time                    |        | High signal to low signal transition | EXP_ATK = 000 | 500   |     | ms/step          |       |
|                                |        |                                      | EXP_ATK = 101 | 25    |     |                  |       |
|                                |        |                                      | EXP_ATK = 110 | 15    |     |                  |       |
| Release Time                   |        | Low-signal to high-signal transition |               | 0.2   |     | ms/step          |       |
| Expander Threshold             |        | EXP_TH = 0x1                         |               | 32    |     | mV <sub>P</sub>  |       |
|                                |        | EXP_TH = 0xF                         |               | 1     |     |                  |       |
| SPEAKER DISTORTION LIMITER     |        |                                      |               |       |     |                  |       |
| Distortion Threshold           |        | THDCLP = 0x1                         |               | < 1   |     | %                |       |
|                                |        | THDCLP = 0xF                         |               | 24    |     |                  |       |
| Attack Time                    |        |                                      |               | 0.5   |     | ms               |       |
| Release Time                   |        | THDRLS = 000                         |               | 0.076 |     | s                |       |
|                                |        | THDRLS = 111                         |               | 6.2   |     |                  |       |

## DIGITAL I/O CHARACTERISTICS

( $V_{DD} = 1.8V$ ,  $V_{PVDD} = 4.2V$ ,  $V_{GND} = V_{PGND} = 0V$ .  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .) (Note 1)

| PARAMETER                               | SYMBOL    | CONDITIONS                          | MIN            | TYP | MAX            | UNITS   |
|-----------------------------------------|-----------|-------------------------------------|----------------|-----|----------------|---------|
| <b>DIGITAL INPUTS (SDA and SCL)</b>     |           |                                     |                |     |                |         |
| Input Voltage High                      | $V_{IH}$  |                                     | 0.7 x $V_{DD}$ |     |                | V       |
| Input Voltage Low                       | $V_{IL}$  |                                     |                |     | 0.4 x $V_{DD}$ | V       |
| Input Hysteresis                        | $V_{HYS}$ |                                     |                | 200 |                | mV      |
| Input Capacitance                       | $C_{IN}$  |                                     |                | 10  |                | pF      |
| Input Leakage Current                   | $I_{IN}$  | $T_A = +25^\circ C$                 |                |     | $\pm 1.0$      | $\mu A$ |
| Input Leakage Current                   | $I_{IN}$  | $V_{DD} = 0V$ , $T_A = +25^\circ C$ |                |     | $\pm 1.0$      | $\mu A$ |
| <b>DIGITAL OUTPUTS (SDA Open Drain)</b> |           |                                     |                |     |                |         |
| Output Low Voltage SDA                  | $V_{OL}$  | $I_{SINK} = 3mA$                    |                |     | 0.4            | V       |

## High-Efficiency, Low-Noise Audio Subsystem

### I<sup>2</sup>C TIMING CHARACTERISTICS

(V<sub>DD</sub> = 1.8V, V<sub>PVDD</sub> = 4.2V, V<sub>GND</sub> = V<sub>PGND</sub> = 0V. T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Note 1)

| PARAMETER                                       | SYMBOL              | CONDITIONS | MIN                    | TYP | MAX | UNITS |
|-------------------------------------------------|---------------------|------------|------------------------|-----|-----|-------|
| Serial-Clock Frequency                          | f <sub>SCL</sub>    |            | 0                      |     | 400 | kHz   |
| Bus Free Time Between STOP and START Conditions | t <sub>BUF</sub>    |            | 1.3                    |     |     | μs    |
| Hold Time (Repeated) START Condition            | t <sub>HD,STA</sub> |            | 0.6                    |     |     | μs    |
| SCL Pulse-Width Low                             | t <sub>LOW</sub>    |            | 1.3                    |     |     | μs    |
| SCL Pulse-Width High                            | t <sub>HIGH</sub>   |            | 0.6                    |     |     | μs    |
| Setup Time for a Repeated START Condition       | t <sub>SU,STA</sub> |            | 0.6                    |     |     | μs    |
| Data Hold Time                                  | t <sub>HD,DAT</sub> |            | 0                      |     | 900 | ns    |
| Data Setup Time                                 | t <sub>SU,DAT</sub> |            | 100                    |     |     | ns    |
| SDA and SCL Receiving Rise Time                 | t <sub>R</sub>      | (Note 4)   | 20 + 0.1C <sub>B</sub> |     |     | ns    |
| SDA and SCL Receiving Fall Time                 | t <sub>F</sub>      | (Note 4)   | 20 + 0.1C <sub>B</sub> |     | 300 | ns    |
| SDA Transmitting Fall Time                      | t <sub>F</sub>      | (Note 4)   | 20 + 0.1C <sub>B</sub> |     | 250 | ns    |
| Setup Time for STOP Condition                   | t <sub>SU,STO</sub> |            | 0.6                    |     |     | μs    |
| Bus Capacitance                                 | C <sub>B</sub>      |            |                        |     | 400 | pF    |
| Pulse Width of Suppressed Spike                 | t <sub>SP</sub>     |            | 0                      |     | 50  | ns    |

**Note 1:** 100% production tested at T<sub>A</sub> = +25°C. Specifications over temperature limits are guaranteed by design.

**Note 2:** Amplifier inputs are AC-coupled to GND.

**Note 3:** Class D amplifier testing performed with a resistive load in series with an inductor to simulate an actual speaker load.

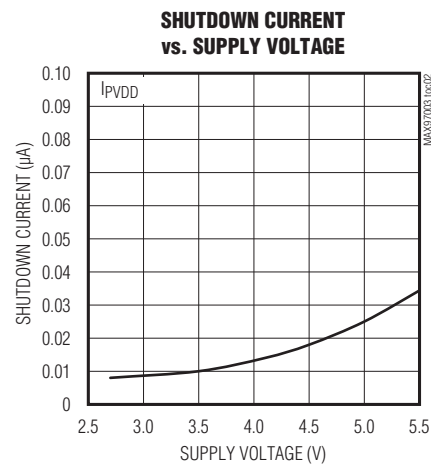
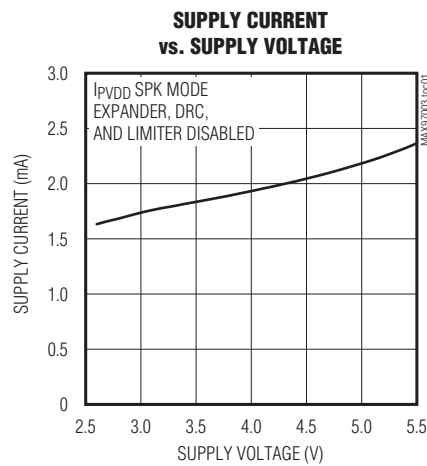
**Note 4:** C<sub>B</sub> is in pF.

## High-Efficiency, Low-Noise Audio Subsystem

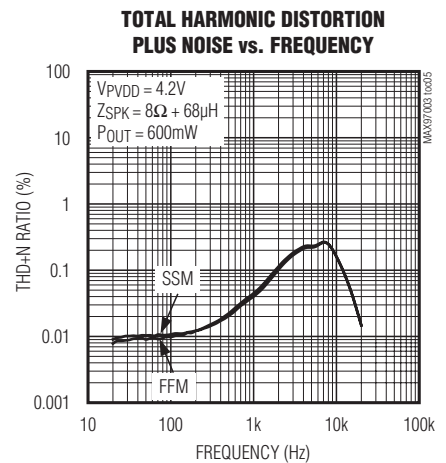
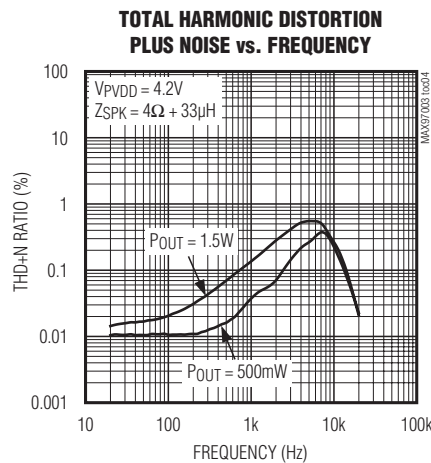
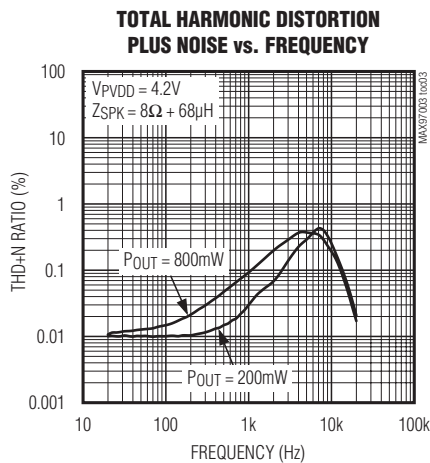
### Typical Operating Characteristics

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### GENERAL



### SPEAKER AMPLIFIER

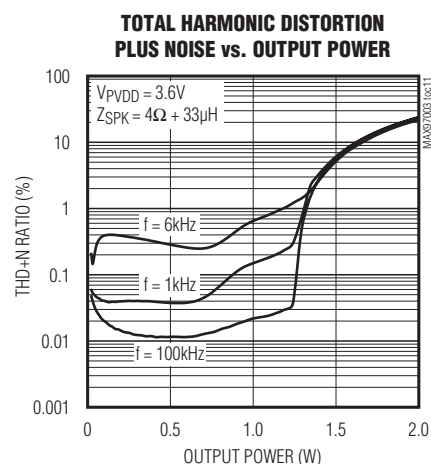
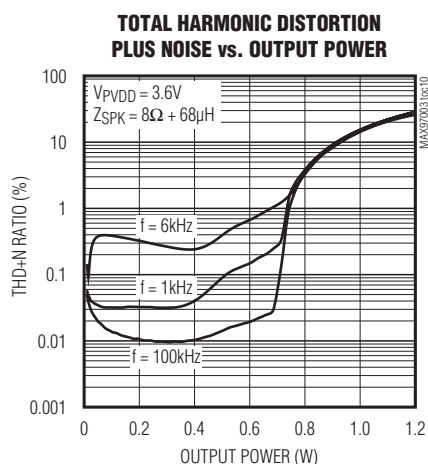
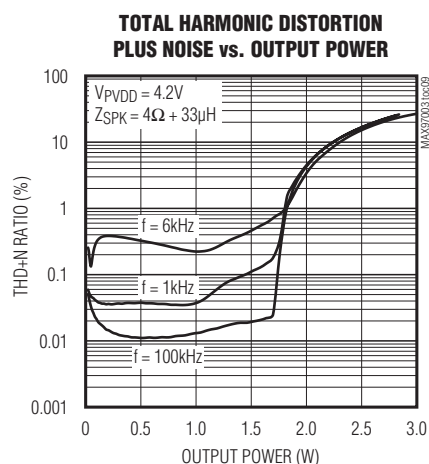
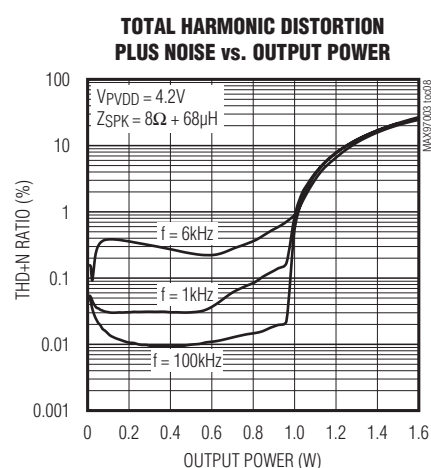
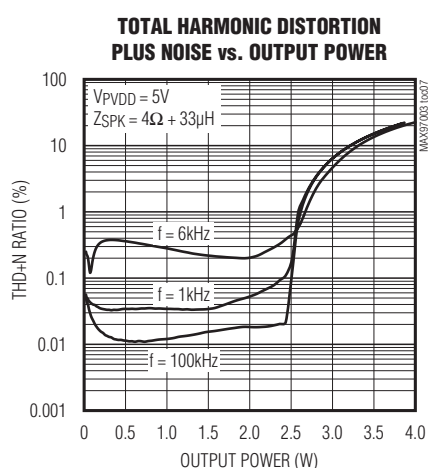
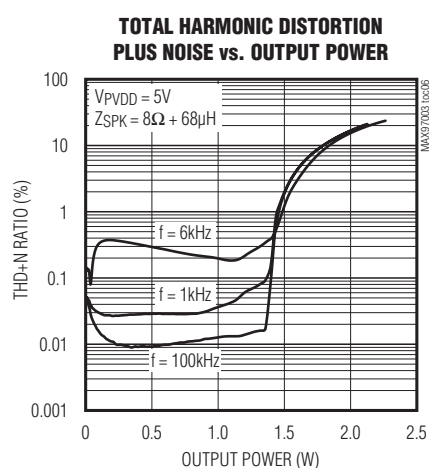


## High-Efficiency, Low-Noise Audio Subsystem

### Typical Operating Characteristics (continued)

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### SPEAKER AMPLIFIER

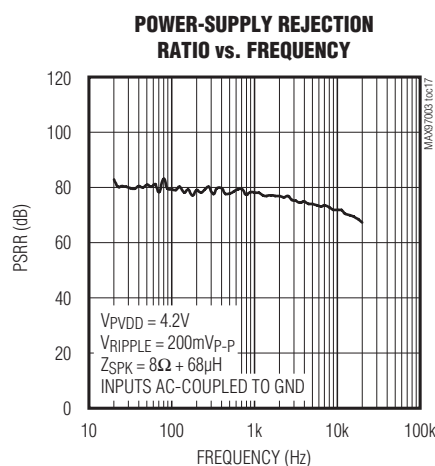
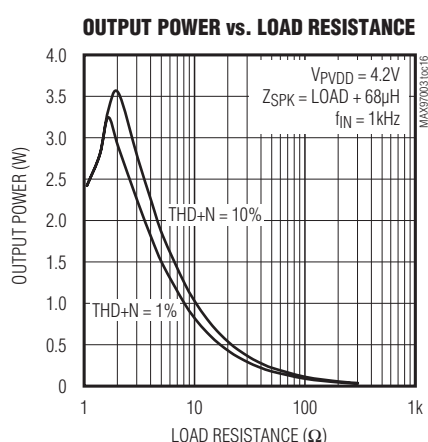
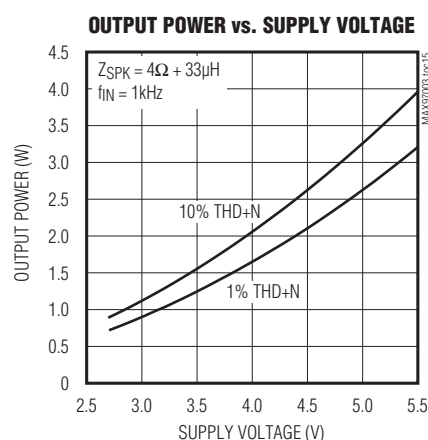
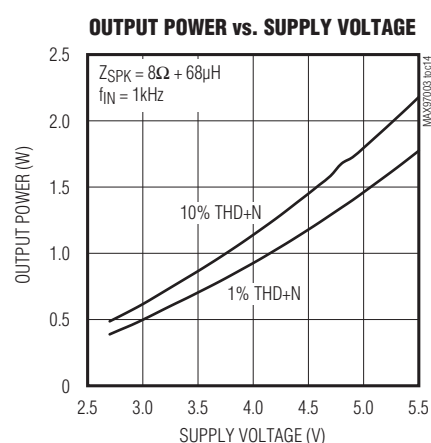
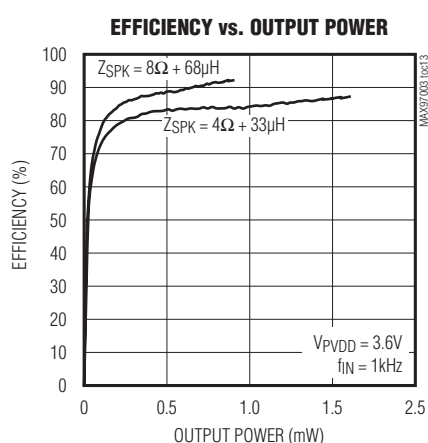
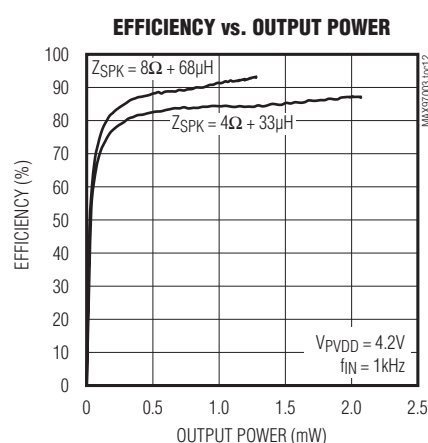


## High-Efficiency, Low-Noise Audio Subsystem

### Typical Operating Characteristics (continued)

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### SPEAKER AMPLIFIER

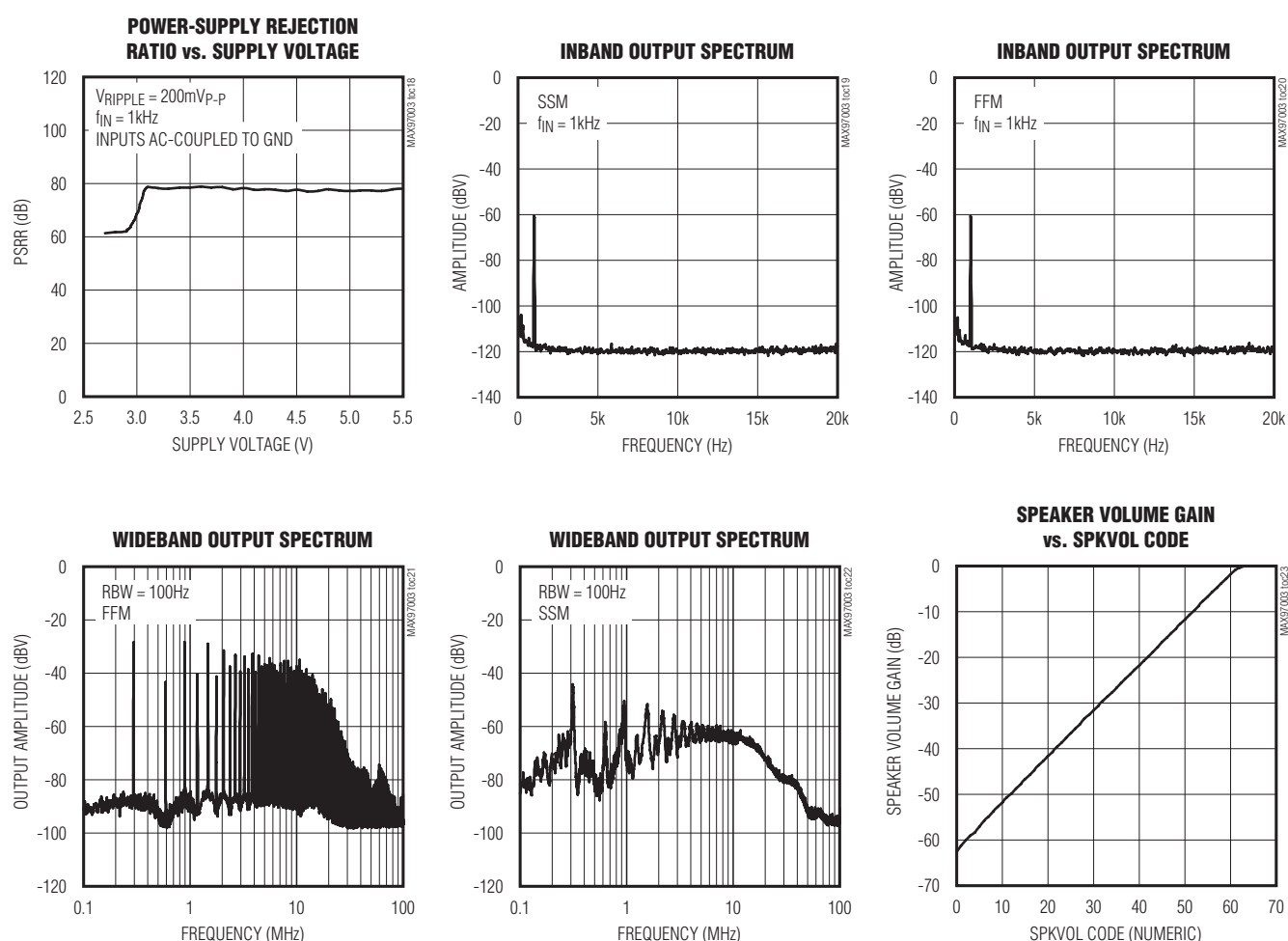


## High-Efficiency, Low-Noise Audio Subsystem

### Typical Operating Characteristics (continued)

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### SPEAKER AMPLIFIER

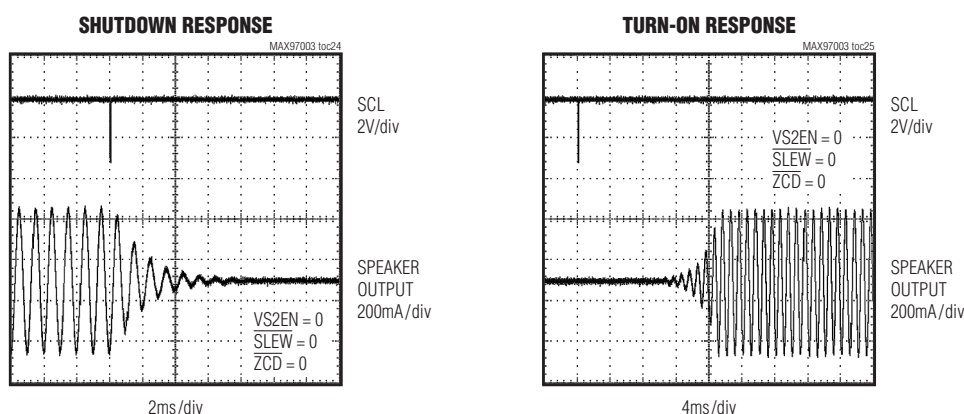


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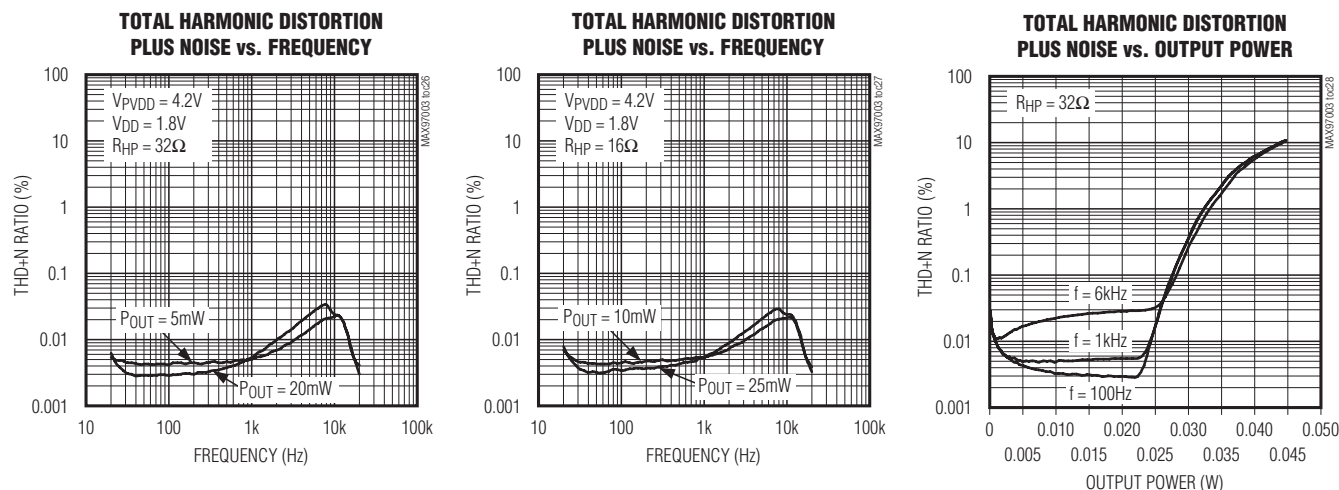
### Typical Operating Characteristics (continued)

( $V_{DD} = 1.8V$ ,  $V_{PVDD} = 4.2V$ ,  $V_{GND} = V_{PGND} = 0V$ . Headphone path:  $PGAIN_- = -1.5dB$ ,  $HP\_VOL = 0dB$ ,  $HPGAIN = +2dB$ , input signal configured single-ended. Speaker path:  $PGAIN_- = 0dB$ ,  $SPKVOL = 0dB$ ,  $SPKGAIN = +12dB$ , input signal configured differential. Speaker loads ( $Z_{SPK}$ ) connected between  $SPKP$  and  $SPKN$ . Headphone loads ( $R_{HP}$ ) connected from  $HPL$  or  $HPR$  to  $GND$ . SDA and SCL pullup voltage =  $1.8V$ .  $Z_{SPK} = \infty$ ,  $R_{HP} = \infty$ .  $C_{C1P-C1N} = C_{CPVDD} = C_{CPVSS} = C_{BIAS} = 1\mu F$ .)

### SPEAKER AMPLIFIER



### HEADPHONE AMPLIFIER

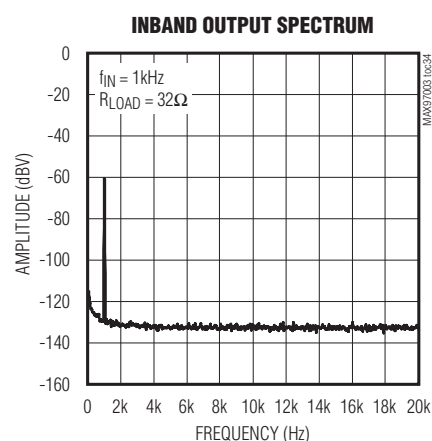
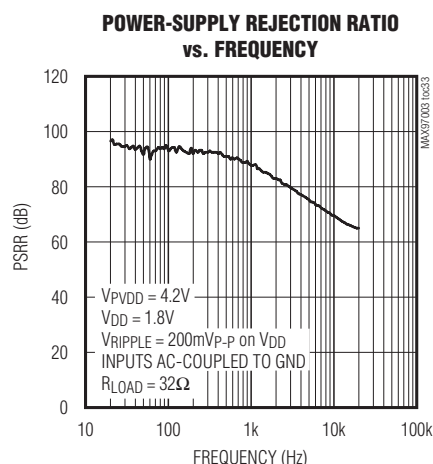
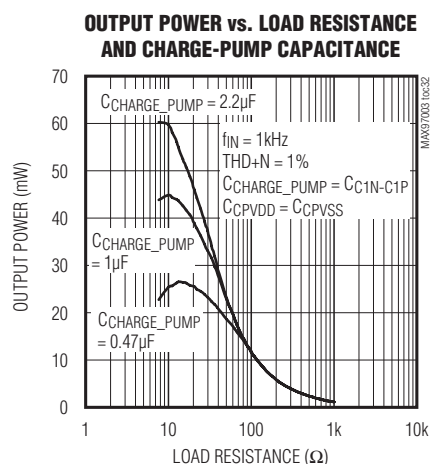
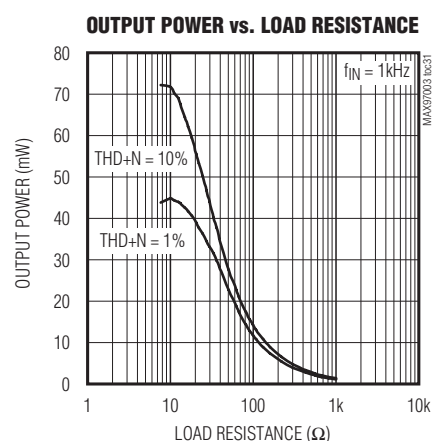
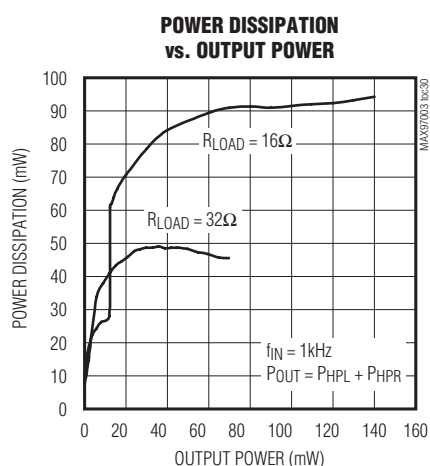
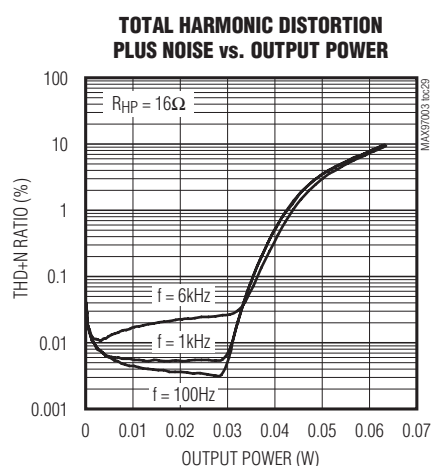


## High-Efficiency, Low-Noise Audio Subsystem

### Typical Operating Characteristics (continued)

( $V_{DD} = 1.8V$ ,  $V_{PVDD} = 4.2V$ ,  $V_{GND} = V_{PGND} = 0V$ . Headphone path:  $PGAIN_- = -1.5dB$ ,  $HP\_VOL = 0dB$ ,  $HPGAIN = +2dB$ , input signal configured singled-ended. Speaker path:  $PGAIN_- = 0dB$ ,  $SPKVOL = 0dB$ ,  $SPKGAIN = +12dB$ , input signal configured differential. Speaker loads ( $Z_{SPK}$ ) connected between SPKP and SPKN. Headphone loads ( $R_{HP}$ ) connected from HPL or HPR to GND. SDA and SCL pullup voltage = 1.8V.  $Z_{SPK} = \infty$ ,  $R_{HP} = \infty$ .  $C_{C1P-C1N} = C_{CPVDD} = C_{CPVSS} = C_{BIAS} = 1\mu F$ .)

### HEADPHONE AMPLIFIER

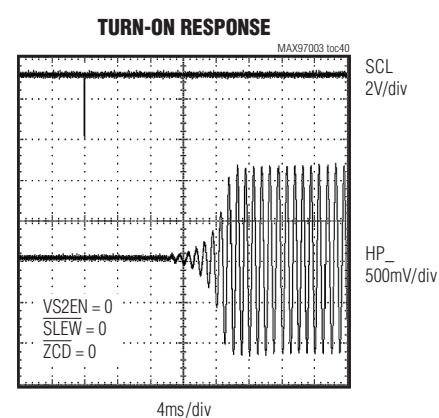
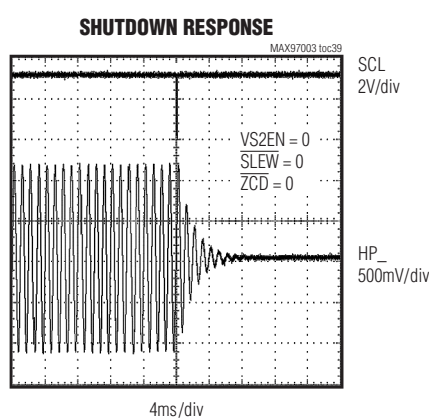
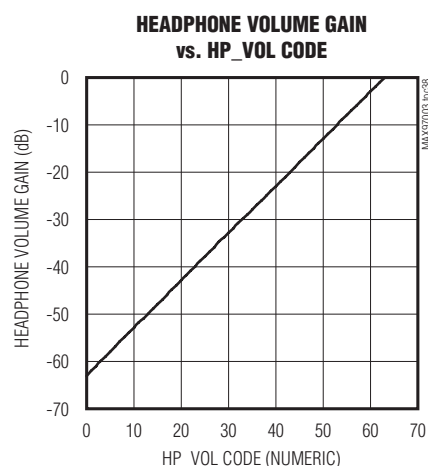
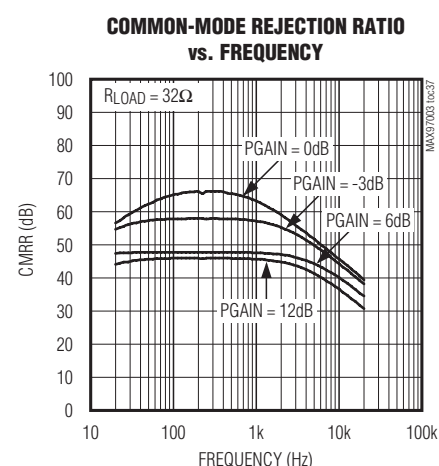
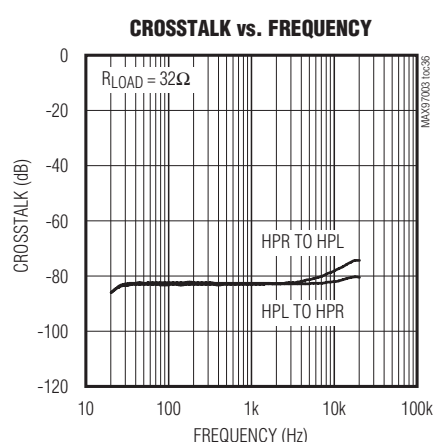
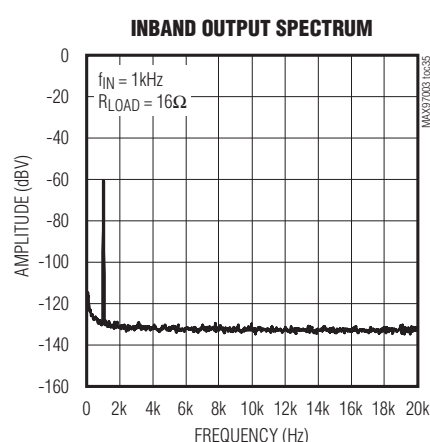


## High-Efficiency, Low-Noise Audio Subsystem

### Typical Operating Characteristics (continued)

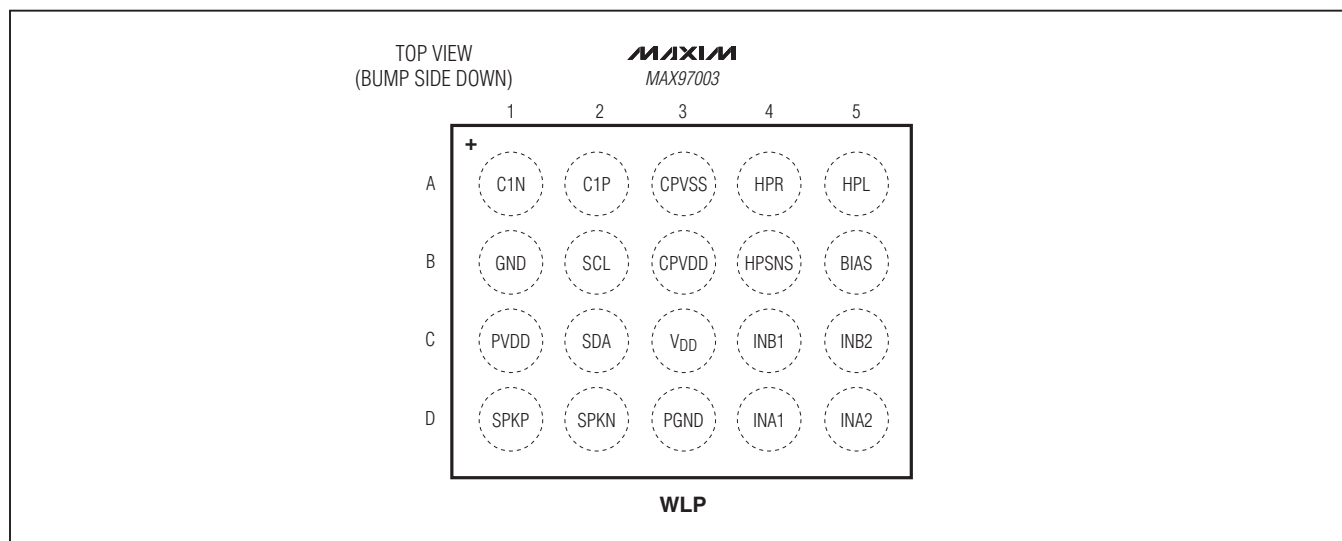
( $V_{DD} = 1.8V$ ,  $V_{PVDD} = 4.2V$ ,  $V_{GND} = V_{PGND} = 0V$ . Headphone path:  $PGAIN_- = -1.5dB$ ,  $HP\_VOL = 0dB$ ,  $HPGAIN = +2dB$ , input signal configured singled-ended. Speaker path:  $PGAIN_- = 0dB$ ,  $SPKVOL = 0dB$ ,  $SPKGAIN = +12dB$ , input signal configured differential. Speaker loads ( $Z_{SPK}$ ) connected between  $SPKP$  and  $SPKN$ . Headphone loads ( $R_{HP}$ ) connected from  $HPL$  or  $HPR$  to  $GND$ . SDA and SCL pullup voltage =  $1.8V$ .  $Z_{SPK} = \infty$ ,  $R_{HP} = \infty$ .  $C_{C1P-C1N} = C_{CPVDD} = C_{CPVSS} = C_{BIAS} = 1\mu F$ .)

### HEADPHONE AMPLIFIER



## High-Efficiency, Low-Noise Audio Subsystem

### Bump Configuration



### Bump Description

| BUMP | NAME  | FUNCTION                                                                                         |
|------|-------|--------------------------------------------------------------------------------------------------|
| A1   | C1N   | Charge-Pump Flying Capacitor Negative Terminal. Connect a 1μF capacitor between C1P and C1N.     |
| A2   | C1P   | Charge-Pump Flying Capacitor Positive Terminal. Connect a 1μF capacitor between C1P and C1N.     |
| A3   | CPVSS | Headphone Amplifier Negative Power Supply. Bypass with a 1μF capacitor to PGND.                  |
| A4   | HPR   | Headphone Amplifier Right Output                                                                 |
| A5   | HPL   | Headphone Amplifier Left Output                                                                  |
| B1   | GND   | Analog Ground                                                                                    |
| B2   | SCL   | Serial Clock Input. Connect a pullup resistor from SCL to the I <sup>2</sup> C bus supply.       |
| B3   | CPVDD | Headphone Amplifier Positive Power Supply. Bypass with a 1μF capacitor to PGND.                  |
| B4   | HPSNS | Headphone Ground Sense. Connect to the headset jack's ground terminal.                           |
| B5   | BIAS  | Common-Mode Bias. Bypass to GND with a 1μF capacitor.                                            |
| C1   | PVDD  | Speaker Amplifier Power Supply. Bypass with a 0.1μF and a 10μF capacitor to PGND.                |
| C2   | SDA   | Serial-Data Input/Output. Connect a pullup resistor from SDA to the I <sup>2</sup> C bus supply. |
| C3   | VDD   | Headphone Amplifier Supply. Bypass with a 0.1μF and a 10μF capacitor to GND.                     |
| C4   | INB1  | Input B1. Left or negative input.                                                                |
| C5   | INB2  | Input B2. Right or positive input.                                                               |
| D1   | SPKP  | Positive Speaker Output                                                                          |
| D2   | SPKN  | Negative Speaker Output                                                                          |
| D3   | PGND  | Speaker Amplifier Ground and Charge-Pump Ground                                                  |
| D4   | INA1  | Input A1. Left or negative input.                                                                |
| D5   | INA2  | Input A2. Right or positive input.                                                               |

## High-Efficiency, Low-Noise Audio Subsystem

### Detailed Description

The MAX97003 audio subsystem combines a mono speaker amplifier with a stereo headphone amplifier. The high-efficiency 1W class D speaker amplifier operates directly from a lithium-ion battery and consumes no more than 0.05μA when in shutdown mode. The headphone amplifier utilizes a dual-mode charge pump and a Class H output stage to maximize efficiency while outputting a ground-referenced signal that does not require output coupling capacitors. The headphone and speaker amplifiers have independent volume and on/off control. The four inputs are configurable as two differential inputs or four single-ended inputs. All control is performed using the two-wire I<sup>2</sup>C interface.

The speaker amplifier incorporates a distortion limiter to automatically reduce the volume level when excessive clipping occurs. This allows high gain for low-level signals without compromising the quality of large signals. The speaker amplifier also features an adjustable DRC that provides programmable compression or limiting of the audio signal. Both the headphone and speaker

amplifiers feature a downward expander/noise gate to attenuate noise when no input signal is present. The headphone amplifier features a ground-sense pin to eliminate ground loop noise when the headphone jack is in use.

### Signal Path

The signal path consists of flexible inputs, signal mixing, volume control, and output amplifiers (Figure 1). The inputs can be configured for single-ended or differential signals (Figure 2). The internal preamplifiers feature programmable gain settings using internal resistors. Following preamplification, the input signals are mixed, volume adjusted, and routed to the headphone and speaker amplifiers based on the desired configuration.

### Class D Speaker Amplifier

The Class D speaker amplifier utilizes active emissions-limiting and spread-spectrum modulation to minimize the EMI radiated by the amplifier.

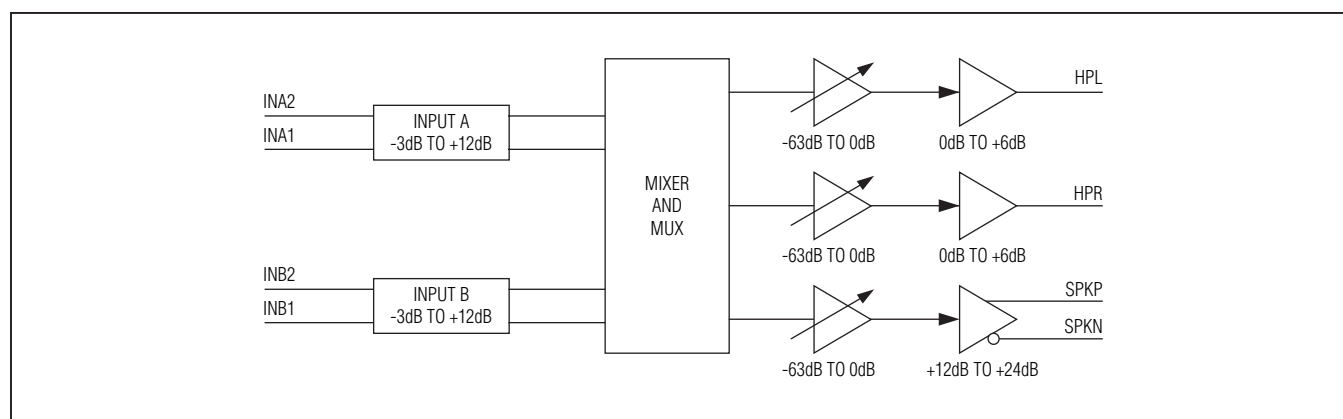


Figure 1. Signal Path

## High-Efficiency, Low-Noise Audio Subsystem

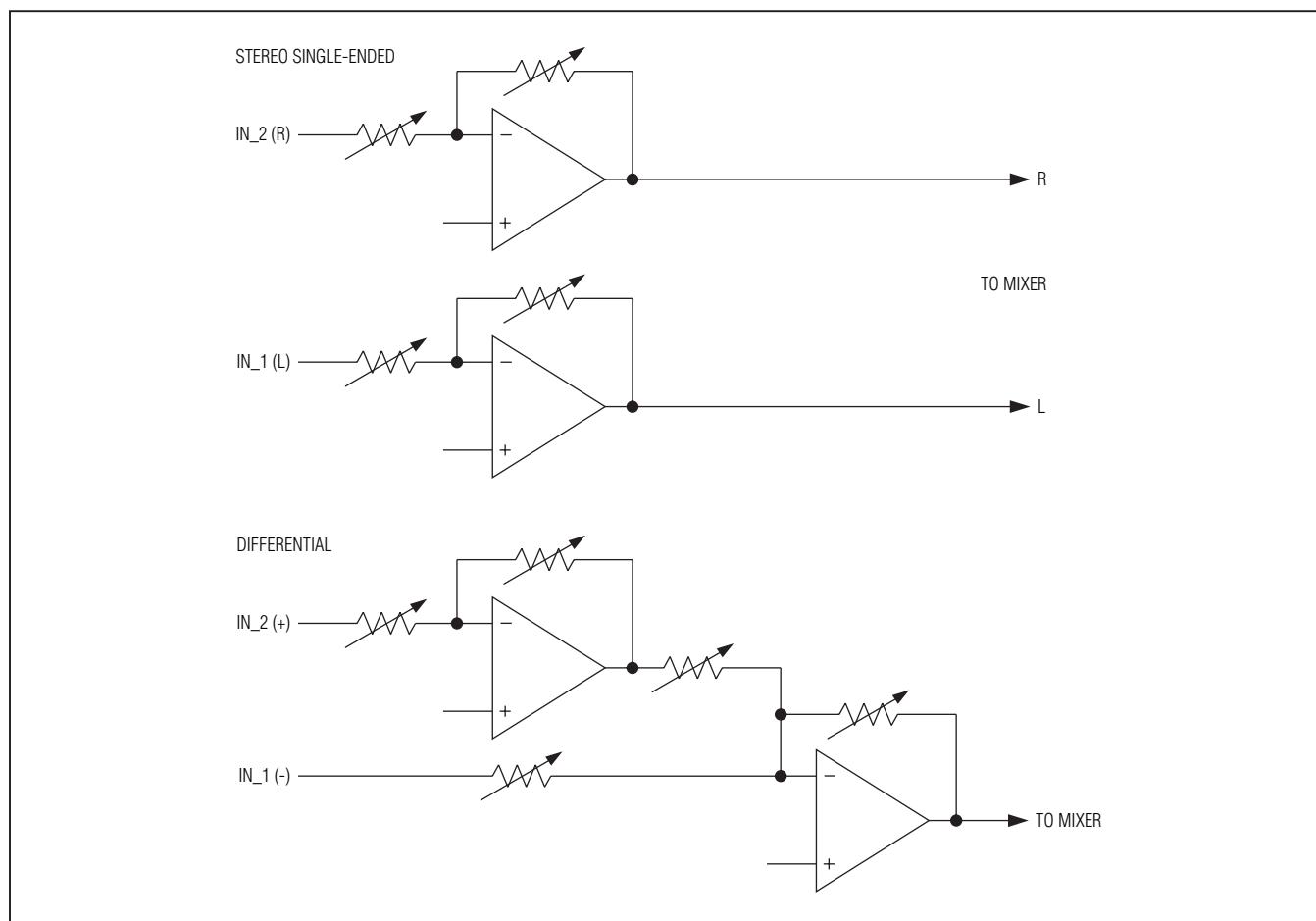


Figure 2. Stereo Single-Ended and Differential Input Configurations

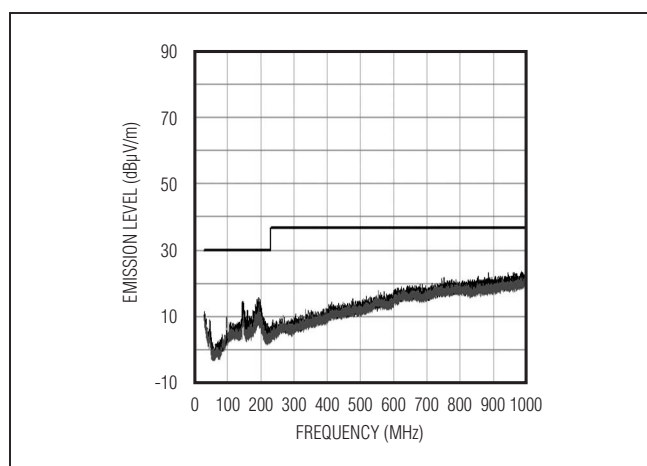


Figure 3. EMI with 12in of Speaker Cable

### Ultra-Low EMI Filterless Output Stage

Traditional Class D amplifiers require the use of external LC filters or shielding to meet EN55022B electromagnetic-interference (EMI) regulation standards. Maxim's patented active emissions limiting edge-rate control circuitry and spread-spectrum modulation reduces EMI emissions, while maintaining up to 93% efficiency. Maxim's spread-spectrum modulation mode flattens wideband spectral components, while proprietary techniques ensure that the cycle-to-cycle variation of the switching period does not degrade audio reproduction or efficiency. The IC's spread-spectrum modulator randomly varies the switching frequency by  $\pm 10\text{kHz}$  around the center frequency (300kHz). Above 10MHz, the wideband spectrum looks like noise for EMI purposes. See [Figure 3](#).

## High-Efficiency, Low-Noise Audio Subsystem

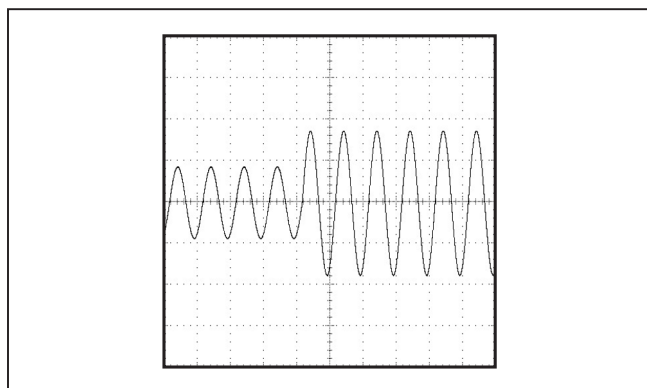


Figure 4. Low-Signal to High-Signal Transition, No Clipping, DRC Disabled

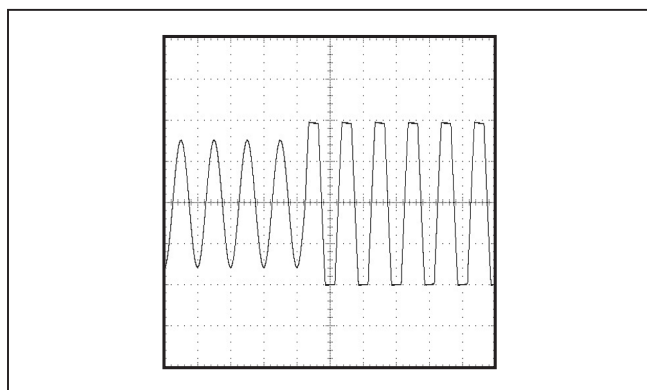


Figure 5. Low-Signal to High-Signal Transition, Increased Gain, DRC Disabled

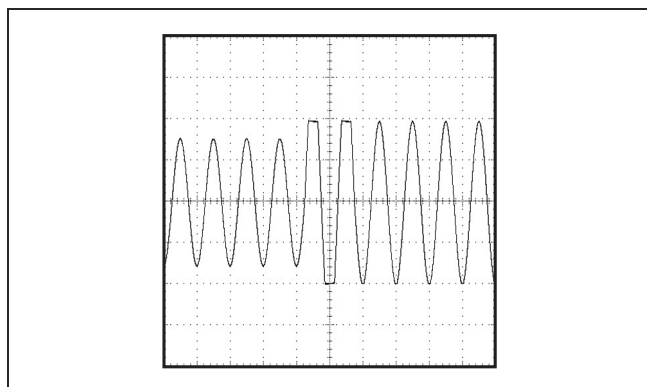


Figure 6. Low-Signal to High-Signal Transition, Increased Gain, DRC Enabled

### Dynamic Range Compressor (DRC)

The speaker amplifier features a dynamic range compressor (DRC) that attenuates high-amplitude signals and allows for a higher gain setting to be selected without clipping the output signal. This increases the perceived loudness of the audio signal and maintains a stable output amplitude despite changes in input amplitude. [Figure 4](#), [Figure 5](#), and [Figure 6](#) demonstrate the benefits of using the DRC. Each of these figures uses the same input signal.

To operate the DRC, select a threshold level, compression ratio, attack time constant, and release time through registers 0x0A and 0x0B. When enabled, RMS signal levels that cross above the selected DRC threshold level are attenuated based on the selected compression ratio ([Figure 7](#)). Attenuation is achieved by automatically modifying the speaker volume to a lower gain setting. The user-selected gain setting is automatically restored when the RMS signal level falls below the DRC threshold. The attack time constant determines the time constant used when the DRC engages. The release time determines the time-per-step used when the DRC disengages.

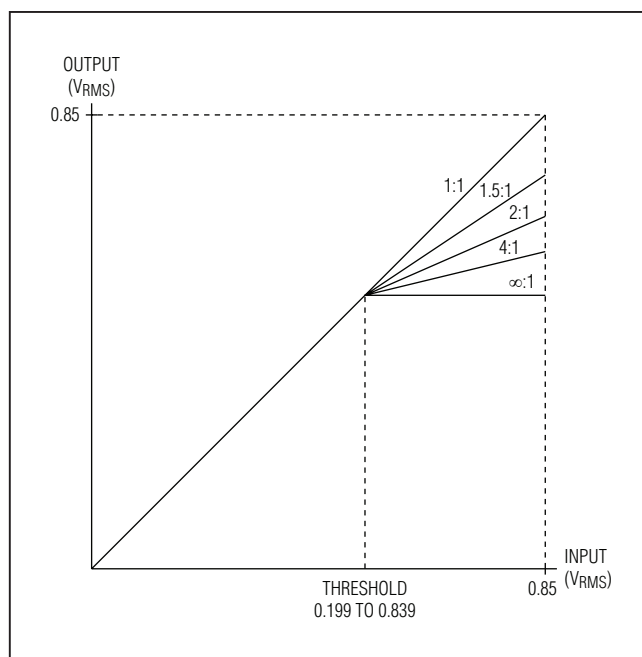


Figure 7. DRC Gain Curve

# High-Efficiency, Low-Noise Audio Subsystem

## Expander

The IC's speaker and headphone amplifier signal paths include an expander. The expander reduces the noise floor when there is no desired input signal by attenuating peak signals that are below the selected expander threshold (Figure 8). Attenuation is achieved by automatically modifying the speaker or headphone volume to a lower gain setting. Expansion ratio and attack time settings are configured by registers 0x0C for the headphone path and 0x0D for the speaker path. The expansion ratio determines the input:output relationship used when the input signal is below the selected threshold. The expansion attack time determines the time-per-step used when the expander engages. Figure 9 and Figure 10 show the benefits of the expander by comparing the output with the expander disabled against the output with the expander enabled.

The expander acts as a noise gate when the expansion ratio is set to an input:output relationship of infinity:1. In this case, all signals below the selected threshold are muted.

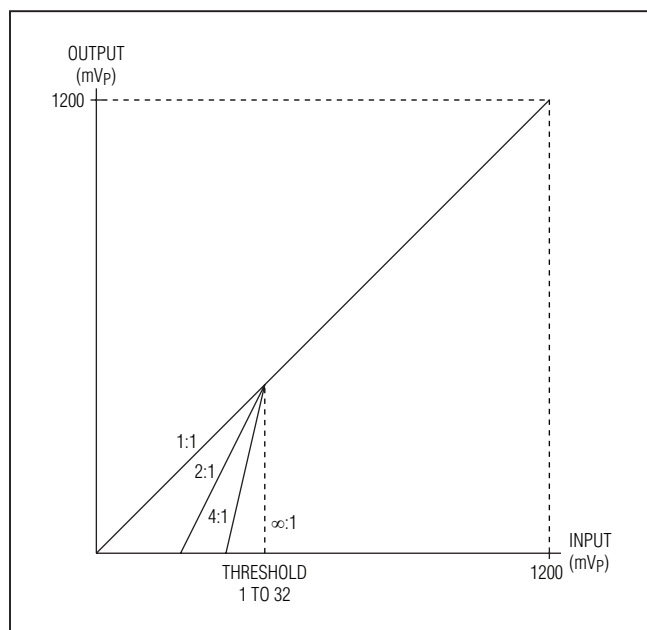


Figure 8. Expander Gain Curve

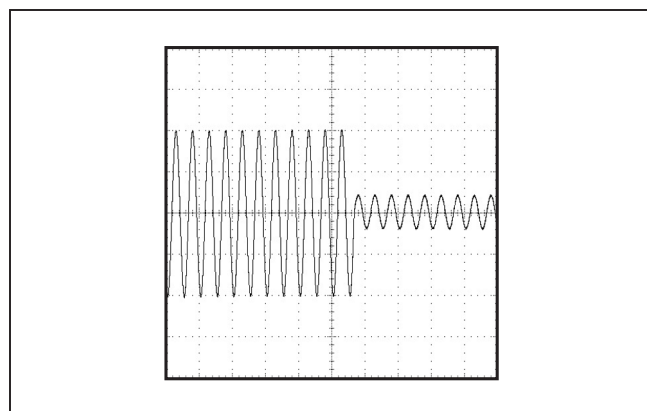


Figure 9. High-Signal to Low-Signal Transition, Expander Disabled

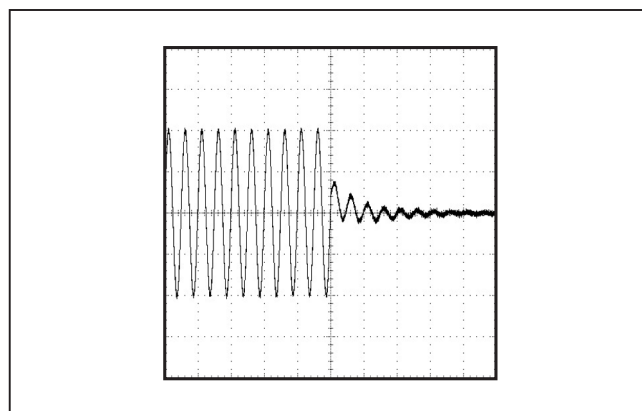


Figure 10. High-Signal to Low-Signal Transition, Expander Enabled

## High-Efficiency, Low-Noise Audio Subsystem

### Speaker Low-Power Mode

The IC's speaker path expander includes a low-power mode that increases power efficiency when there is no desired input signal. Set the programmable threshold in register 0x0F to determine when low-power mode is activated. When low-power mode is enabled, the Class D switching output is active only if the speaker volume setting selected by the expander is above the selected low-power mode threshold. For example, if the speaker low-power mode threshold is set to -30dB and the input

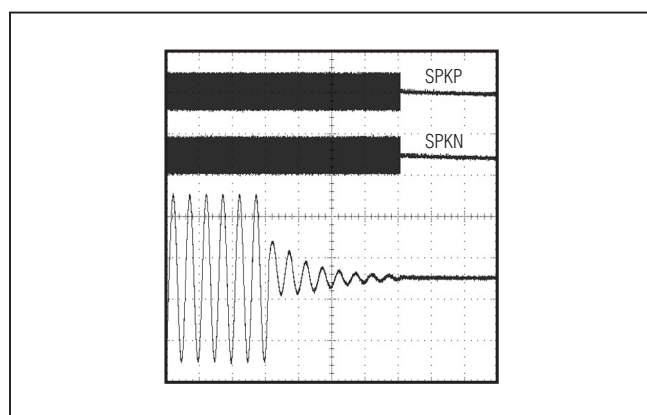


Figure 11. High-Signal to Low-Signal Transition, Speaker Expander with Speaker Low-Power Mode

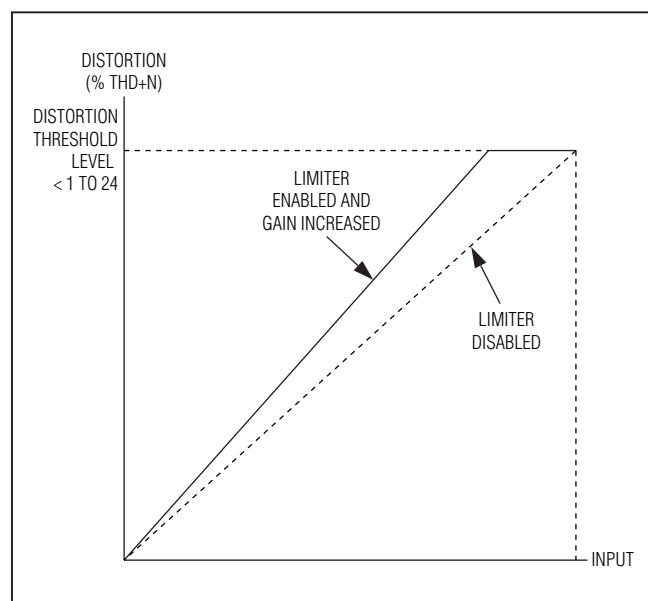


Figure 12. Limiter Gain Curve

signal is such that the speaker expander attenuates the output volume setting to at least -30dB, the Class D amplifier is turned off (Figure 11). Low-power mode is only available when the speaker expander is enabled.

### Distortion Limiter

The speaker amplifier integrates a limiter to provide speaker protection and ensures high-quality audio. When enabled, the limiter monitors the audio signal at the output of the Class D speaker amplifier and decreases the gain if the distortion exceeds the predefined threshold. Attenuation is achieved by automatically modifying the speaker volume as appropriate. The limiter automatically tracks the battery voltage to reduce the gain as the battery voltage drops.

Figure 12 shows the typical output vs. input curves with and without the distortion limiter. The dotted line shows the maximum gain for a given distortion limit without the distortion limiter. The solid line shows how, with the distortion limiter enabled, the gain can be increased without exceeding the set distortion limit. When the limiter is enabled, selecting a high gain level results in peak signals being attenuated while low signals are left unchanged. This increases the perceived loudness without the harshness of a clipped waveform.

To operate the distortion limiter, select a distortion threshold and release time constant through the 0x0E register.  $\overline{\text{ZCD}}$  must be set to 0 in register 0x11 for the distortion limiter to operate properly.

### Headphone Amplifier

#### DirectDrive

Traditional single-supply headphone amplifiers have outputs biased at a nominal DC voltage (typically half the supply). Large coupling capacitors are needed to block this DC bias from the headphone. Without these capacitors, a significant amount of DC current flows to the headphone, resulting in unnecessary power dissipation and possible damage to both headphone and headphone amplifier.

Maxim's patented DirectDrive® architecture uses a charge pump to create an internal negative supply voltage. This allows the headphone outputs of the IC to be biased at GND while operating from a single supply (Figure 13). Without a DC component, there is no need for the large DC-blocking capacitors. Instead of two large (220μF, typ) capacitors, the IC's charge pump requires

*DirectDrive is a registered trademark of Maxim Integrated Products, Inc.*

## High-Efficiency, Low-Noise Audio Subsystem

two small ceramic capacitors, conserving board space, reducing cost, and improving the frequency response of the headphone amplifier. See the Output Power vs. Charge-Pump Capacitance and Load Resistance graph in the [Typical Operating Characteristics](#) section for details of the possible capacitor sizes. There is a low DC voltage on the amplifier outputs due to amplifier offset. However, the offset of the IC is typically  $\pm 0.15\text{mV}$ , which, when combined with a  $32\Omega$  load, results in less than  $5\mu\text{A}$  of DC current flow to the headphones.

In addition to the cost and size disadvantages of the DC-blocking capacitors required by conventional headphone amplifiers, these capacitors limit the amplifier's low-frequency response and can distort the audio signal. Previous attempts at eliminating the

output-coupling capacitors involved biasing the headphone return (sleeve) to the DC bias voltage of the headphone amplifiers. This method raises a few issues:

- The sleeve is typically grounded to the chassis. Using the midrail biasing approach, the sleeve must be isolated from system ground, complicating product design.
- During an ESD strike, the amplifier's ESD structures are the only path to system ground. Thus, the amplifier must be able to withstand the full energy from an ESD strike.
- When using the headphone jack as a line out to other equipment, the bias voltage on the sleeve can conflict with the ground potential from other equipment, resulting in possible damage to the amplifiers.

### Charge Pump

The IC's dual-mode charge pump generates both the positive and negative power supply for the headphone amplifier. To maximize efficiency, both the charge pump's switching frequency and output voltage change based on signal level.

When the input signal level is less than 10% of  $V_{DD}$ , the switching frequency is reduced to a low rate. This minimizes switching-losses in the charge pump. When the input signal exceeds 10% of  $V_{DD}$ , the switching frequency increases to support the load current.

For input signals below 25% of  $V_{DD}$ , the charge pump generates  $\pm(V_{DD}/2)$  to minimize the voltage drop across the amplifier's power stage and thus improves efficiency. Input signals that exceed 25% of  $V_{DD}$  cause the charge pump to output  $\pm V_{DD}$ . The higher output voltage allows for full output power from the headphone amplifier.

To prevent audible glitches when transitioning from the  $\pm(V_{DD}/2)$  output mode to the  $\pm V_{DD}$  output mode, the charge pump transitions very quickly. This quick change draws significant current from  $V_{DD}$  for the duration of the transition. The bypass capacitor on  $V_{DD}$  supplies the required current and prevent droop on  $V_{DD}$ .

The charge pump's dynamic switching mode can be turned off through the I<sup>2</sup>C interface. The charge pump can then be forced to output either  $\pm(V_{DD}/2)$  or  $\pm V_{DD}$  regardless of input signal level.

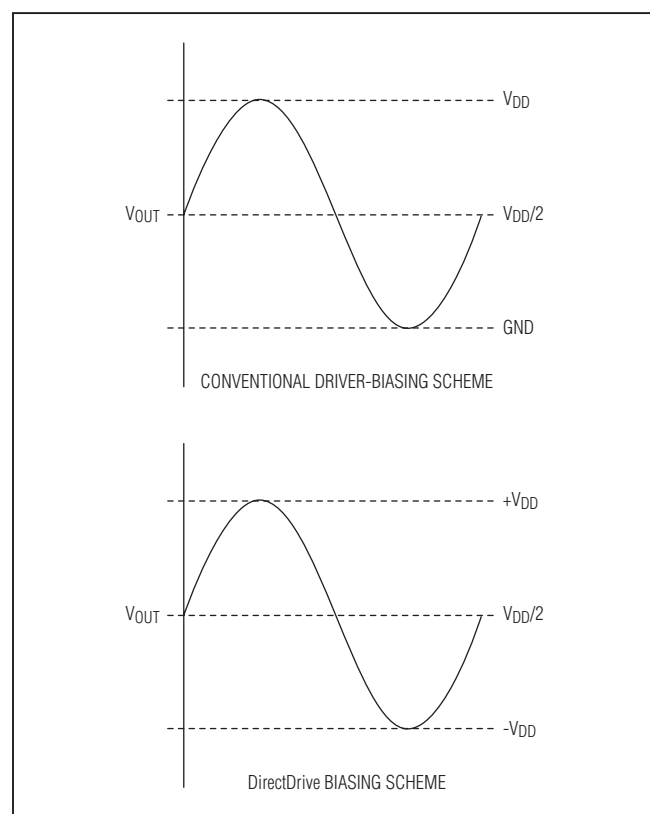


Figure 13. Traditional Amplifier Output vs. MAX97003 DirectDrive Output

## High-Efficiency, Low-Noise Audio Subsystem

### Class H Operation

A Class H amplifier uses a Class AB output stage with power supplies that are modulated by the output signal. In the case of the IC, two nominal power-supply differentials of 1.8V (+0.9V to -0.9V) and 3.6V (+1.8V to -1.8V) are available from the charge pump. [Figure 14](#) shows the operation of the output voltage dependent power supply.

### Ground Sense

The headphone amplifier features output ground sensing that is used to reduce ground loop noise when the headphone output jack is connected to a different ground than the amplifier ground. An example of this is when the headphone jack is used as a lineout and connected to an external power amplifier. In addition, the ground sense reduces noise that can be caused by voltage drops between the amplifier ground and the headphone jack ground pin during normal headphone use. HPSNS must be connected to the ground pin on the headphone jack.

### Volume-Change Features

The IC includes several features that enhance performance during volume changes. Zero-crossing detection, volume slewing, and enhanced volume smoothing are used to improve click-and-pop performance during volume changes. Volume readback is used to report the actual volume setting after the DRC, expander, or distortion limiter applies an automatic volume change.

### Zero-Crossing Detection

The IC features zero-crossing detection to reduce clicks and pops during volume changes. When zero-crossing detection is enabled, all volume changes are delayed until a zero-crossing has been detected. If no zero-crossing is detected within 100ms, then the zero-crossing detector times out and volume changes are executed.

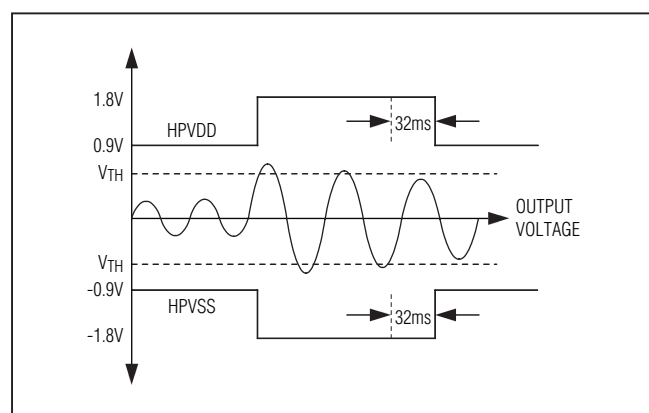


Figure 14. Class H Operation

Disabling zero-crossing detection allows volume changes to occur immediately.

### Volume Slewing

The IC offers volume slewing for all volume changes to further reduce clicks and pops. When enabled, the IC ramps through intermediate volume settings when a change to the volume is made. If zero-crossing detection is disabled, slewing occurs at a rate of 0.2ms per step. If zero-crossing detection is enabled, slew time depends on the input signal. If the duration between zero-crossings is less than 0.2ms, the slew time is limited at 0.2ms per volume change. If the duration between zero-crossings is longer than 0.2ms, volume changes occur at each zero-crossing. Volume slewing also provides a soft-start at power-on and soft-stop at power-off.

### Enhanced Volume Smoothing

Enhanced volume smoothing can be used when the volume slewing feature is enabled. When enhanced volume smoothing is enabled and a volume change occurs, the IC waits for each step in the ramp to be applied before executing the next step. When zero-crossing detection is enabled, enhanced volume smoothing prevents large steps in the output volume when no zero-crossings are detected.

### Volume Readback

The IC features three volume readback registers that report the actual volume settings of the speaker, left headphone, and right headphone volume registers. The DRC, expander, and distortion limiter are capable of automatically adjusting these volume registers according to their respective settings.

### I<sup>2</sup>C Slave Address

The IC's audio subsystem uses a slave address of 0x9A or 1001101 R/W. The address is defined as the 7 most significant bits (MSBs) followed by the read/write bit. Set the read/write bit to 1 to configure the audio subsystem to read mode. Set the read/write bit to 0 to configure the IC to write mode. The address is the first byte of information sent to the IC after the START condition.

### Registers Map

19 internal registers program the audio subsystem. [Table 1](#) lists all of the registers, their addresses, and power-on-reset states. Register 0xFF indicates the device revision. Write zeros to all unused bits in the register table when updating the register, unless otherwise noted.

# High-Efficiency, Low-Noise Audio Subsystem

**Table 1. Register Map**

| REGISTER                        | B7     | B6   | B5       | B4      | B3     | B2     | B1      | B0    | ADDRESS | DEFAULT | R/W |
|---------------------------------|--------|------|----------|---------|--------|--------|---------|-------|---------|---------|-----|
| STATUS                          |        |      |          |         |        |        |         |       |         |         |     |
| Left Headphone Volume Readback  | 0      | 0    | HPLVOLRB |         |        |        |         |       | 0x00    | —       | R   |
| Right Headphone Volume Readback | 0      | 0    | HPRVOLRB |         |        |        |         |       | 0x01    | —       | R   |
| Speaker Volume Readback         | 0      | 0    | SPKVOLRB |         |        |        |         |       | 0x02    | —       | R   |
| Input A Configuration           | 0      | 0    | 0        | INADIFF | PGAINA |        |         |       | 0x03    | 0x00    | R/W |
| Input B Configuration           | 0      | 0    | 0        | INBDIFF | PGAINB |        |         |       | 0x04    | 0x00    | R/W |
| Headphone Mixer                 | HPLMIX |      |          |         | HPRMIX |        |         |       | 0x05    | 0x00    | R/W |
| Speaker Mixer                   | 0      | 0    | 0        | 0       | SPKMIX |        |         |       | 0x06    | 0x00    | R/W |
| Left Headphone Volume           | HPLM   | 0    | HPLVOL   |         |        |        |         |       | 0x07    | 0x00    | R/W |
| Right Headphone Volume          | HPRM   | 0    | HPRVOL   |         |        |        |         |       | 0x08    | 0x00    | R/W |
| Speaker Volume                  | SPKM   | 0    | SPKVOL   |         |        |        |         |       | 0x09    | 0x00    | R/W |
| Dynamic Range Control           | DRCEN  |      |          | DRCATK  |        | DRCRLS |         |       | 0x0A    | 0x00    | R/W |
| Dynamic Range Control           | 0      | 0    | 0        | DRCTH   |        |        |         |       | 0x0B    | 0x00    | R/W |
| Headphone Expander              | EXPHEN |      | EXPHATK  |         |        | EXPHTH |         |       | 0x0C    | 0x00    | R/W |
| Speaker Expander                | EXPSEN |      | EXPSATK  |         |        | EXPSTH |         |       | 0x0D    | 0x00    | R/W |
| Distortion Limiter              | THDCLP |      |          |         | 0      | THDRLS |         |       | 0x0E    | 0x00    | R/W |
| Speaker Low-Power Mode          | SLPEN  | 0    | SLPTH    |         |        |        |         |       | 0x0F    | 0x00    | R/W |
| Output Gain                     | 0      | 0    | 0        | 0       | HPGAIN |        | SPKGAIN |       | 0x10    | 0x00    | R/W |
| Advanced Configuration          | VS2EN  | SLEW | ZCD      | 0       | FFM    | 0      | CPSEL   | FIXED | 0x11    | 0x00    | R/W |
| Power Management                | SHDN   | 0    | 0        | 0       | 0      | SPKEN  | HPLEN   | HPREN | 0x12    | 0x00    | R/W |
| REVISION ID                     |        |      |          |         |        |        |         |       |         |         |     |
| Rev ID                          | REV    |      |          |         |        |        |         |       | 0xFF    | 0x40    | R   |

## High-Efficiency, Low-Noise Audio Subsystem

### Volume Readback

The Volume Readback registers report the actual volume setting of each output volume control when the DRC, expander, or distortion limiter is active.

**Table 2. Volume Readback Registers**

| REGISTER           | BIT  | NAME                               | DESCRIPTION   |              |       |              |       |              |       |              |    |
|--------------------|------|------------------------------------|---------------|--------------|-------|--------------|-------|--------------|-------|--------------|----|
| 0x00/0x01/<br>0x02 | 5    | HPLVOLRB/<br>HPRVOLRB/<br>SPKVOLRB | Output Volume |              |       |              |       |              |       |              |    |
|                    |      |                                    | VALUE         | GAIN<br>(dB) | VALUE | GAIN<br>(dB) | VALUE | GAIN<br>(dB) | VALUE | GAIN<br>(dB) |    |
|                    |      |                                    | 0x00          | -63          | 0x10  | -47          | 0x20  | -31          | 0x30  | -15          |    |
|                    | 4    |                                    | 0x01          | -62          | 0x11  | -46          | 0x21  | -30          | 0x31  | -14          |    |
|                    |      |                                    | 0x02          | -61          | 0x12  | -45          | 0x22  | -29          | 0x32  | -13          |    |
|                    |      |                                    | 0x03          | -60          | 0x13  | -44          | 0x23  | -28          | 0x33  | -12          |    |
|                    |      |                                    | 0x04          | -59          | 0x14  | -43          | 0x24  | -27          | 0x34  | -11          |    |
|                    | 3    |                                    | 0x05          | -58          | 0x15  | -42          | 0x25  | -26          | 0x35  | -10          |    |
|                    |      |                                    | 0x06          | -57          | 0x16  | -41          | 0x26  | -25          | 0x36  | -9           |    |
|                    |      |                                    | 0x07          | -56          | 0x17  | -40          | 0x27  | -24          | 0x37  | -8           |    |
|                    |      |                                    | 2             | 0x08         | -55   | 0x18         | -39   | 0x28         | -23   | 0x38         | -7 |
|                    | 0x09 |                                    |               | -54          | 0x19  | -38          | 0x29  | -22          | 0x39  | -6           |    |
|                    | 1    |                                    |               | 0x0A         | -53   | 0x1A         | -37   | 0x2A         | -21   | 0x3A         | -5 |
|                    |      |                                    |               | 0x0B         | -52   | 0x1B         | -36   | 0x2B         | -20   | 0x3B         | -4 |
|                    |      |                                    | 0x0C          | -51          | 0x1C  | -35          | 0x2C  | -19          | 0x3C  | -3           |    |
|                    |      |                                    | 0             | 0x0D         | -50   | 0x1D         | -34   | 0x2D         | -18   | 0x3D         | -2 |
|                    | 0x0E |                                    |               | -49          | 0x1E  | -33          | 0x2E  | -17          | 0x3E  | -1           |    |
|                    | 0x0F |                                    |               | -48          | 0x1F  | -32          | 0x2F  | -16          | 0x3F  | 0            |    |

## High-Efficiency, Low-Noise Audio Subsystem

### Input Configuration

The input configuration registers allow the selection of single-ended or differential modes as well as preamp gain settings for INA and INB.

**Table 3. Input Configuration Registers**

| REGISTER  | BIT | NAME                | DESCRIPTION                                                                                                                                                                                                                                   |            |         |            |
|-----------|-----|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|---------|------------|
| 0x03/0x04 | 4   | INADIFF/<br>INBDIFF | <b>Input A/B Differential Mode.</b> Configures the input as either a mono differential signal ( $IN_+ = IN_2 - IN_1$ ) or as a stereo signal ( $IN_1 = \text{left}$ , $IN_2 = \text{right}$ ).<br>0 = Stereo single-ended<br>1 = Differential |            |         |            |
|           | 3   | PGAINA/<br>PGAINB   | <b>Input A/B Preamp Gain.</b> Set the input gain to maximize output signal level for a given input signal range to improve the SNR of the system.                                                                                             |            |         |            |
|           |     |                     | VALUE                                                                                                                                                                                                                                         | LEVEL (dB) | VALUE   | LEVEL (dB) |
|           | 2   |                     | 0x0                                                                                                                                                                                                                                           | -3         | 0x6     | +6         |
|           |     |                     | 0x1                                                                                                                                                                                                                                           | -1.5       | 0x7     | +7.5       |
|           | 1   |                     | 0x2                                                                                                                                                                                                                                           | -0         | 0x8     | +9         |
|           |     |                     | 0x3                                                                                                                                                                                                                                           | +1.5       | 0x9     | +10.5      |
|           |     |                     | 0x4                                                                                                                                                                                                                                           | +3         | 0xA-0xF | +12        |
|           | 0   |                     | 0x5                                                                                                                                                                                                                                           | +4.5       | —       | —          |

## High-Efficiency, Low-Noise Audio Subsystem

### Mixers

The IC features independent mixers for the left headphone, right headphone, and speaker paths. Each output can select any combination of any inputs. This allows for mixing two audio signals together and routing independent signals to the headphone and speaker amplifiers. If one of the inputs is not selected by either mixer, it is automatically powered down to reduce current consumption.

**Table 4. Mixer Registers**

| REGISTER | BIT | NAME   | DESCRIPTION                                                                                             |                                  |
|----------|-----|--------|---------------------------------------------------------------------------------------------------------|----------------------------------|
| 0x05     | 7   | HPLMIX | <b>Left Headphone Mixer.</b> Selects which of the four inputs is routed to the left headphone output.   |                                  |
|          | 6   |        | 0000                                                                                                    | No input                         |
|          | 5   |        | xxx1                                                                                                    | INA1 (Disabled when INADIFF = 1) |
|          | 4   |        | xx1x                                                                                                    | INA2 (Select when INADIFF = 1)   |
|          |     |        | x1xx                                                                                                    | INB1 (Disabled when INBDIFF = 1) |
|          |     |        | 1xxx                                                                                                    | INB2 (Select when INBDIFF = 1)   |
|          | 3   | HPRMIX | <b>Right Headphone Mixer.</b> Selects which of the four inputs is routed to the right headphone output. |                                  |
|          | 2   |        | 0000                                                                                                    | No input                         |
|          | 1   |        | xxx1                                                                                                    | INA1 (Disabled when INADIFF = 1) |
|          | 0   |        | xx1x                                                                                                    | INA2 (Select when INADIFF = 1)   |
| 0x06     |     |        | x1xx                                                                                                    | INB1 (Disabled when INBDIFF = 1) |
|          |     |        | 1xxx                                                                                                    | INB2 (Select when INBDIFF = 1)   |
|          | 3   | SPKMIX | <b>Speaker Mixer.</b> Selects which of the four inputs is routed to the speaker output.                 |                                  |
|          | 2   |        | 0000                                                                                                    | No input                         |
|          | 1   |        | xxx1                                                                                                    | INA1 (Disabled when INADIFF = 1) |
|          | 0   |        | xx1x                                                                                                    | INA2 (Select when INADIFF = 1)   |

## High-Efficiency, Low-Noise Audio Subsystem

### Volume Control

The speaker, left headphone, and right headphone have independent volume control registers that allow a gain to be selected from -63dB to 0dB.

**Table 5. Headphone Volume Control Registers**

| REGISTER           | BIT | NAME                         | DESCRIPTION                                    |           |       |           |       |           |       |           |  |  |
|--------------------|-----|------------------------------|------------------------------------------------|-----------|-------|-----------|-------|-----------|-------|-----------|--|--|
| 0x07/0x08/<br>0x09 | 7   | HPLM/<br>HPRM/<br>SPKM       | <b>Output Mute</b><br>0 = Unmuted<br>1 = Muted |           |       |           |       |           |       |           |  |  |
|                    | 5   | HPLVOL/<br>HPRVOL/<br>SPKVOL | <b>Output Volume</b>                           |           |       |           |       |           |       |           |  |  |
|                    |     |                              | VALUE                                          | GAIN (dB) | VALUE | GAIN (dB) | VALUE | GAIN (dB) | VALUE | GAIN (dB) |  |  |
|                    |     |                              | 0x00                                           | -63       | 0x10  | -47       | 0x20  | -31       | 0x30  | -15       |  |  |
|                    |     |                              | 0x01                                           | -62       | 0x11  | -46       | 0x21  | -30       | 0x31  | -14       |  |  |
|                    | 4   |                              | 0x02                                           | -61       | 0x12  | -45       | 0x22  | -29       | 0x32  | -13       |  |  |
|                    |     |                              | 0x03                                           | -60       | 0x13  | -44       | 0x23  | -28       | 0x33  | -12       |  |  |
|                    |     |                              | 0x04                                           | -59       | 0x14  | -43       | 0x24  | -27       | 0x34  | -11       |  |  |
|                    |     |                              | 0x05                                           | -58       | 0x15  | -42       | 0x25  | -26       | 0x35  | -10       |  |  |
|                    |     |                              | 0x06                                           | -57       | 0x16  | -41       | 0x26  | -25       | 0x36  | -9        |  |  |
|                    | 3   |                              | 0x07                                           | -56       | 0x17  | -40       | 0x27  | -24       | 0x37  | -8        |  |  |
|                    |     |                              | 0x08                                           | -55       | 0x18  | -39       | 0x28  | -23       | 0x38  | -7        |  |  |
|                    |     |                              | 0x09                                           | -54       | 0x19  | -38       | 0x29  | -22       | 0x39  | -6        |  |  |
|                    |     |                              | 0x0A                                           | -53       | 0x1A  | -37       | 0x2A  | -21       | 0x3A  | -5        |  |  |
|                    |     |                              | 0x0B                                           | -52       | 0x1B  | -36       | 0x2B  | -20       | 0x3B  | -4        |  |  |
|                    |     |                              | 0x0C                                           | -51       | 0x1C  | -35       | 0x2C  | -19       | 0x3C  | -3        |  |  |
|                    |     |                              | 0x0D                                           | -50       | 0x1D  | -34       | 0x2D  | -18       | 0x3D  | -2        |  |  |
|                    |     |                              | 0x0E                                           | -49       | 0x1E  | -33       | 0x2E  | -17       | 0x3E  | -1        |  |  |
|                    | 0   |                              | 0x0F                                           | -48       | 0x1F  | -32       | 0x2F  | -16       | 0x3F  | 0         |  |  |

## High-Efficiency, Low-Noise Audio Subsystem

### Dynamic Range Control

The DRC attenuates high-level signals without affecting low-level signals. Attenuation is achieved by automatically modifying the speaker volume as appropriate. When the DRC is enabled, the overall volume can be increased without clipping the high-level signals. To operate the DRC, select a compression threshold, compression ratio, attack time constant, and release time.

**Table 6. Dynamic Range Control Registers**

| REGISTER | BIT  | NAME   | DESCRIPTION                                                                                                                                            |                           |           |                           |
|----------|------|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------|-----------|---------------------------|
| 0x0A     | 7    | DRCEN  | <b>DRC Enable and Compression Ratio</b><br>000 = 1:1 (disabled)<br>001 = 1.34:1<br>010 = 2:1<br>011 = 4:1<br>100 – 111 = ∞:1                           |                           |           |                           |
|          | 6    |        |                                                                                                                                                        |                           |           |                           |
|          | 5    |        |                                                                                                                                                        |                           |           |                           |
|          | 4    | DRCATK | <b>DRC Attack Time Constant.</b> Defines the time constant used during attack.<br>00 = 500μs<br>01 = 1ms<br>10 = 10ms<br>11 = 50ms                     |                           |           |                           |
|          | 3    |        |                                                                                                                                                        |                           |           |                           |
|          | 2    | DRCRLS | <b>DRC Release Time.</b> Defines the release rate per step.<br>000 = 800ms<br>001 = 400ms<br>010 = 150ms<br>011 = 75ms<br>100 = 50ms<br>101–111 = 25ms |                           |           |                           |
|          | 1    |        |                                                                                                                                                        |                           |           |                           |
|          | 0    |        |                                                                                                                                                        |                           |           |                           |
| 0x0B     | 4    | DRCTH  | <b>Compression Threshold Level.</b> Specifies the minimum input signal level for which compression is applied.                                         |                           |           |                           |
|          | 3    |        | VALUE                                                                                                                                                  | LEVEL (V <sub>RMS</sub> ) | VALUE     | LEVEL (V <sub>RMS</sub> ) |
|          |      |        | 0x00                                                                                                                                                   | Reserved                  | 0x10      | 0.354                     |
|          |      |        | 0x01                                                                                                                                                   | 0.839                     | 0x11      | 0.334                     |
|          |      |        | 0x02                                                                                                                                                   | 0.792                     | 0x12      | 0.315                     |
|          |      |        | 0x03                                                                                                                                                   | 0.748                     | 0x13      | 0.298                     |
|          | 2    |        | 0x04                                                                                                                                                   | 0.706                     | 0x14      | 0.281                     |
|          |      |        | 0x05                                                                                                                                                   | 0.667                     | 0x15      | 0.265                     |
|          |      |        | 0x06                                                                                                                                                   | 0.629                     | 0x16      | 0.251                     |
|          |      |        | 0x07                                                                                                                                                   | 0.594                     | 0x17      | 0.237                     |
|          |      |        | 0x08                                                                                                                                                   | 0.561                     | 0x18      | 0.223                     |
|          | 1    |        | 0x09                                                                                                                                                   | 0.529                     | 0x19      | 0.211                     |
|          |      |        | 0x0A                                                                                                                                                   | 0.500                     | 0x1A–0x1F | 0.199                     |
|          |      |        | 0                                                                                                                                                      | 0x0B                      | 0.472     |                           |
|          | 0x0C |        |                                                                                                                                                        | 0.445                     |           |                           |
|          | 0x0D |        |                                                                                                                                                        | 0.421                     |           |                           |
|          | 0x0E |        |                                                                                                                                                        | 0.397                     |           |                           |
|          | 0x0F | 0.375  |                                                                                                                                                        |                           |           |                           |

## High-Efficiency, Low-Noise Audio Subsystem

### Expander (Noise Gate)

The expander/noise gate eliminates noise when no desired signal is present by attenuating peak signals that are below the selected threshold. Attenuation is achieved by automatically modifying the headphone or speaker volume as appropriate. To operate the headphone or speaker expander, select an expansion threshold, expansion ratio, and attack time in the appropriate headphone or speaker expander registers.

**Table 7. Expander Registers**

| REGISTER  | BIT | NAME                | DESCRIPTION                                                                                                                                                          |                              |
|-----------|-----|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------|
| 0x0C/0x0D | 7   | EXPHEN/<br>EXPSEN   | <b>Headphone/Speaker Expansion Ratio</b><br>00 = 1:1 (disabled)<br>01 = 2:1<br>10 = 4:1<br>11 = ∞:1 (noise gate)                                                     |                              |
|           | 6   |                     |                                                                                                                                                                      |                              |
|           | 5   | EXPHATK/<br>EXPSATK | <b>Headphone/Speaker Expander Attack Time.</b> Decreases volume after the signal drops below the selected expander threshold.                                        |                              |
|           | 4   |                     | VALUE                                                                                                                                                                | ATTACK TIME (ms/step)        |
|           |     |                     | 000                                                                                                                                                                  | 500                          |
|           |     |                     | 001                                                                                                                                                                  | 350                          |
|           |     |                     | 010                                                                                                                                                                  | 250                          |
|           |     |                     | 011                                                                                                                                                                  | 100                          |
|           | 3   |                     | 100                                                                                                                                                                  | 50                           |
|           |     |                     | 101                                                                                                                                                                  | 25                           |
|           |     | 110–111             | 15                                                                                                                                                                   |                              |
|           | 2   | EXPHTH/<br>EXPSTH   | <b>Headphone/Speaker Noise Gate Threshold.</b> The expander attenuates or mutes the output below this threshold. Thresholds are based on the PGA input signal level. |                              |
|           | 1   |                     | VALUE                                                                                                                                                                | THRESHOLD (mV <sub>p</sub> ) |
|           |     |                     | 0x0                                                                                                                                                                  | Reserved                     |
| 0x1       |     |                     | 32                                                                                                                                                                   |                              |
| 0x2       |     |                     | 20                                                                                                                                                                   |                              |
| 0x3       |     |                     | 10                                                                                                                                                                   |                              |
| 0         | 0x4 |                     | 8                                                                                                                                                                    |                              |
|           | 0x5 |                     | 4                                                                                                                                                                    |                              |
|           | 0x6 |                     | 2                                                                                                                                                                    |                              |
|           | 0x7 |                     | 1                                                                                                                                                                    |                              |

## High-Efficiency, Low-Noise Audio Subsystem

### Distortion Limiter

The distortion limiter monitors the audio signal at the output of the Class D speaker amplifier and decreases the gain if the distortion exceeds the selected threshold. Attenuation is achieved by automatically modifying the speaker volume as appropriate. To operate the distortion limiter, select a distortion limit (% THD+N) and a release time constant.

**Table 8. Distortion Limiter Register**

| REGISTER | BIT | NAME   | DESCRIPTION                                                                                                                                                                                                                                                  |                      |       |                      |
|----------|-----|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|-------|----------------------|
| 0x0E     | 7   | THDCLP | <b>Distortion Limit.</b> Measured in % THD+N. $\overline{ZCD}$ must be set to 0 for the distortion limiter to function.                                                                                                                                      |                      |       |                      |
|          | 6   |        | VALUE                                                                                                                                                                                                                                                        | DISTORTION LIMIT (%) | VALUE | DISTORTION LIMIT (%) |
|          |     |        | 0x0                                                                                                                                                                                                                                                          | Limiter disabled     | 0x8   | 12                   |
|          |     |        | 0x1                                                                                                                                                                                                                                                          | < 1                  | 0x9   | 14                   |
|          |     |        | 0x2                                                                                                                                                                                                                                                          | 1                    | 0xA   | 16                   |
|          |     |        | 0x3                                                                                                                                                                                                                                                          | 2                    | 0xB   | 18                   |
|          |     |        | 0x4                                                                                                                                                                                                                                                          | 4                    | 0xC   | 20                   |
|          |     |        | 0x5                                                                                                                                                                                                                                                          | 6                    | 0xD   | 21                   |
|          |     |        | 0x6                                                                                                                                                                                                                                                          | 8                    | 0xE   | 22                   |
|          | 0x7 |        | 10                                                                                                                                                                                                                                                           | 0xF                  | 24    |                      |
|          | 2   | THDRLS | <b>Limiter Release Time Constant.</b> Time constant used while increasing the gain after distortion is no longer detected at the output.<br>000 = 6.2s<br>001 = 3.1s<br>010 = 1.6s<br>011 = 815ms<br>100 = 419ms<br>101 = 223ms<br>110 = 116ms<br>111 = 76ms |                      |       |                      |
|          | 1   |        |                                                                                                                                                                                                                                                              |                      |       |                      |
|          |     |        |                                                                                                                                                                                                                                                              |                      |       |                      |
|          | 0   |        |                                                                                                                                                                                                                                                              |                      |       |                      |
|          |     |        |                                                                                                                                                                                                                                                              |                      |       |                      |

## High-Efficiency, Low-Noise Audio Subsystem

### Speaker Low-Power Mode

The speaker expander includes a low-power mode that increases power efficiency when a desired audio signal is not present. When this feature is enabled, the Class D switching output is active only if the speaker volume setting selected by the expander is above the selected low-power mode threshold. Low-power mode is only available when the speaker expander is enabled.

**Table 9. Speaker Low-Power Mode Register**

| REGISTER | BIT | NAME  | DESCRIPTION                                                                                                                                                                                                                            |           |       |           |       |           |       |           |  |  |
|----------|-----|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|-----------|-------|-----------|-------|-----------|--|--|
| 0x0F     | 7   | SLPEN | <b>Speaker Low-Power Mode.</b> Only functions if EXPSEN ≠ 0.<br>0 = Class D output is active continuously.<br>1 = Class D output is active if the speaker volume setting selected by the expander is above SLPTH.                      |           |       |           |       |           |       |           |  |  |
|          | 5   | SLPTH | <b>Speaker Low-Power Mode Volume Threshold.</b> Threshold used to determine if speaker amplifier should be enabled or disabled. If the volume selected by the expander is less than this threshold, the speaker amplifier is disabled. |           |       |           |       |           |       |           |  |  |
|          | 4   |       | VALUE                                                                                                                                                                                                                                  | GAIN (dB) | VALUE | GAIN (dB) | VALUE | GAIN (dB) | VALUE | GAIN (dB) |  |  |
|          | 3   |       | 0x00                                                                                                                                                                                                                                   | -63       | 0x10  | -47       | 0x20  | -31       | 0x30  | -15       |  |  |
|          |     |       | 0x01                                                                                                                                                                                                                                   | -62       | 0x11  | -46       | 0x21  | -30       | 0x31  | -14       |  |  |
|          |     |       | 0x02                                                                                                                                                                                                                                   | -61       | 0x12  | -45       | 0x22  | -29       | 0x32  | -13       |  |  |
|          |     |       | 0x03                                                                                                                                                                                                                                   | -60       | 0x13  | -44       | 0x23  | -28       | 0x33  | -12       |  |  |
|          | 2   |       | 0x04                                                                                                                                                                                                                                   | -59       | 0x14  | -43       | 0x24  | -27       | 0x34  | -11       |  |  |
|          |     |       | 0x05                                                                                                                                                                                                                                   | -58       | 0x15  | -42       | 0x25  | -26       | 0x35  | -10       |  |  |
|          |     |       | 0x06                                                                                                                                                                                                                                   | -57       | 0x16  | -41       | 0x26  | -25       | 0x36  | -9        |  |  |
|          |     |       | 0x07                                                                                                                                                                                                                                   | -56       | 0x17  | -40       | 0x27  | -24       | 0x37  | -8        |  |  |
|          | 1   |       | 0x08                                                                                                                                                                                                                                   | -55       | 0x18  | -39       | 0x28  | -23       | 0x38  | -7        |  |  |
|          |     |       | 0x09                                                                                                                                                                                                                                   | -54       | 0x19  | -38       | 0x29  | -22       | 0x39  | -6        |  |  |
|          |     |       | 0x0A                                                                                                                                                                                                                                   | -53       | 0x1A  | -37       | 0x2A  | -21       | 0x3A  | -5        |  |  |
|          |     |       | 0x0B                                                                                                                                                                                                                                   | -52       | 0x1B  | -36       | 0x2B  | -20       | 0x3B  | -4        |  |  |
|          | 0   |       | 0x0C                                                                                                                                                                                                                                   | -51       | 0x1C  | -35       | 0x2C  | -19       | 0x3C  | -3        |  |  |
|          |     |       | 0x0D                                                                                                                                                                                                                                   | -50       | 0x1D  | -34       | 0x2D  | -18       | 0x3D  | -2        |  |  |
|          |     |       | 0x0E                                                                                                                                                                                                                                   | -49       | 0x1E  | -33       | 0x2E  | -17       | 0x3E  | -1        |  |  |
|          |     |       | 0x0F                                                                                                                                                                                                                                   | -48       | 0x1F  | -32       | 0x2F  | -16       | 0x3F  | 0         |  |  |

## High-Efficiency, Low-Noise Audio Subsystem

### Output Gain

The output stage of the headphone and speaker amplifiers can be configured to provide additional gain. The headphone amplifier allows a range of 0dB to +6dB. The speaker amplifier allows range of +12dB to +24dB.

**Table 10. Output Gain Register**

| REGISTER | BIT | NAME    | DESCRIPTION                                                                        |
|----------|-----|---------|------------------------------------------------------------------------------------|
| 0x10     | 3   | HPGAIN  | <b>Headphone Output Gain</b><br>00 = 0dB<br>01 = +2dB<br>10 = +4dB<br>11 = +6dB    |
|          | 2   |         |                                                                                    |
|          | 1   | SPKGAIN | <b>Speaker Output Gain</b><br>00 = +12dB<br>01 = +16dB<br>10 = +20dB<br>11 = +24dB |
|          | 0   |         |                                                                                    |

## High-Efficiency, Low-Noise Audio Subsystem

### Advanced Configuration

The IC includes several advanced configurations related to automatic volume changes initiated by the DRC, expander, and distortion limiter. In addition, settings for the Class D speaker modulation scheme and headphone charge pump are configured in register 0x11.

**Table 11. Advanced Configuration Register**

| REGISTER | BIT | NAME                     | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|----------|-----|--------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x11     | 7   | VS2EN                    | <b>Enhanced Volume Smoothing.</b> During volume slewing, the controller waits for each step in the ramp to be applied before executing the next step. When zero-crossing detection is enabled, this prevents large steps in the output volume when no zero-crossings are detected.<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                  |
|          | 6   | $\overline{\text{SLEW}}$ | <b>Volume Slewing.</b> Determines whether volume slewing is used on all volume control changes to reduce clicks and pops. When enabled, volume changes cause the IC to ramp through intermediate volume settings whenever a change to the volume is made. If $\overline{\text{ZCD}} = 1$ , slewing occurs at a rate of 0.2ms per step. If $\overline{\text{ZCD}} = 0$ , slew time depends on the input signal frequency. This bit also activates soft-start at power-on and soft-stop at power-off.<br>0 = Enabled<br>1 = Disabled |
|          | 5   | $\overline{\text{ZCD}}$  | <b>Zero-Crossing Detection.</b> Determines whether zero-crossing detection is used on all volume control changes to reduce clicks and pops. Disabling zero-crossing detection allows volume changes to occur immediately. Zero-crossing detection times out at 100ms.<br>0 = Enabled<br>1 = Disabled                                                                                                                                                                                                                               |
|          | 3   | FFM                      | <b>Fixed Class D Frequency Enable</b><br>0 = Spread-spectrum modulation<br>1 = Fixed-frequency modulation                                                                                                                                                                                                                                                                                                                                                                                                                          |
|          | 1   | CPSEL                    | <b>Charge-Pump Output Select.</b> Works with FIXED to set $\pm V_{DD}$ or $\pm V_{DD}/2$ outputs on CPVDD and CPVSS. Ignored when FIXED = 0.<br>0 = $\pm V_{DD}$ on CPVDD/CPVSS<br>1 = $\pm V_{DD}/2$ on CPVDD/CPVSS                                                                                                                                                                                                                                                                                                               |
|          | 0   | FIXED                    | <b>Class H Mode.</b> When enabled, this bit forces the charge pump to generate static power rails for CPVDD and CPVSS, instead of dynamically adjusting them based on output signal level.<br>0 = Class H mode<br>1 = Fixed supply mode                                                                                                                                                                                                                                                                                            |

## High-Efficiency, Low-Noise Audio Subsystem

### Power Management

The power management register allows the speaker, left headphone, and right headphone signal paths to be enabled. It also enables the IC device.

**Table 12. Power Management Register**

| REGISTER | BIT | NAME                     | DESCRIPTION                                                            |
|----------|-----|--------------------------|------------------------------------------------------------------------|
| 0x12     | 7   | $\overline{\text{SHDN}}$ | <b>Software Shutdown</b><br>0 = Device disabled<br>1 = Device enabled  |
|          | 2   | SPKEN                    | <b>Speaker Amplifier Enable</b><br>0 = Disabled<br>1 = Enabled         |
|          | 1   | HPLEN                    | <b>Left Headphone Amplifier Enable</b><br>0 = Disabled<br>1 = Enabled  |
|          | 0   | HPREN                    | <b>Right Headphone Amplifier Enable</b><br>0 = Disabled<br>1 = Enabled |

### I<sup>2</sup>C Serial Interface

The IC features an I<sup>2</sup>C/SMBus-compatible, two-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication between the IC and the master at clock rates up to 400kHz. [Figure 1](#) shows the two-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. The master device writes data to the IC by transmitting the proper slave address followed by the register address and then the data word. Each transmit

sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted to the IC is 8 bits long and is followed by an acknowledge clock pulse. A master reading data from the IC transmits the proper slave address followed by a series of nine SCL pulses. The IC transmits data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START (S) or REPEATED START (Sr) condition, a not acknowledge, and a STOP

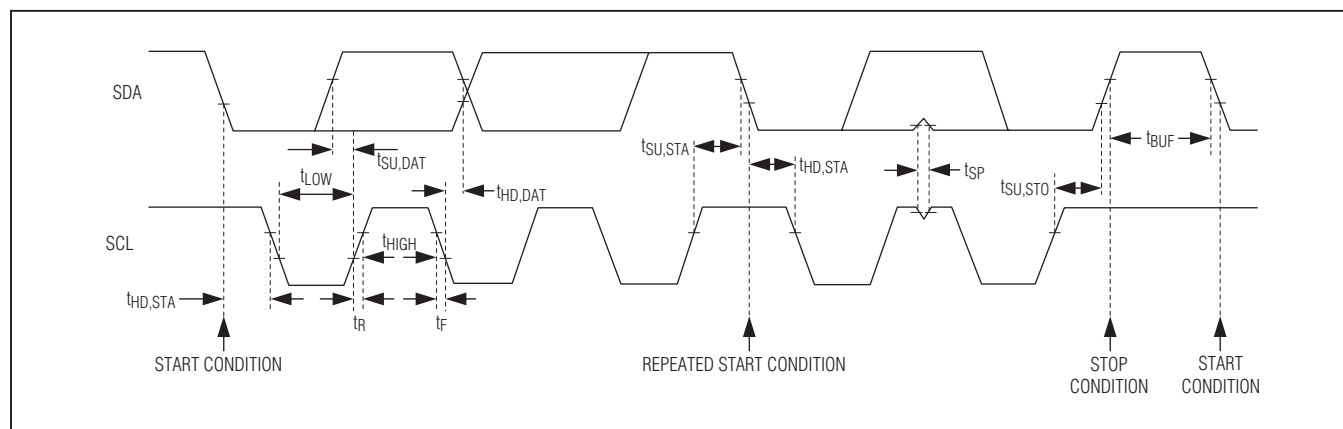


Figure 15. I<sup>2</sup>C Serial Interface Timing Diagram

## High-Efficiency, Low-Noise Audio Subsystem

(P) condition. SDA operates as both an input and an open-drain output. A pullup resistor, typically greater than  $500\Omega$ , is required on SDA. SCL operates only as an input. A pullup resistor, typically greater than  $500\Omega$ , is required on SCL if there are multiple masters on the bus, or if the single master has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the IC from high voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

### Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals. See the [START and STOP Conditions](#) section.

### START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 16). A START condition from the master signals the beginning of a transmission to the IC. The master terminates transmission, and frees

the bus, by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition.

### Early STOP Conditions

The IC recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

### Slave Address

The slave address is defined as the seven most significant bits (MSBs) followed by the read/write bit. For the IC, the seven most significant bits are 1001101. Setting the read/write bit to 1 (slave address = 0x9B) configures the IC for read mode. Setting the read/write bit to 0 (slave address = 0x9A) configures the IC for write mode. The address is the first byte of information sent to the IC after the START condition.

### Acknowledge

The acknowledge bit (ACK) is a clocked ninth bit that the IC uses to handshake receipt each byte of data when in write mode (Figure 17). The IC pulls down SDA during the entire master-generated ninth clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master retries communication. The master pulls down SDA during the ninth clock cycle to acknowledge receipt of data when the IC is in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not-acknowledge is sent when the master reads the final byte of data from the IC, followed by a STOP condition.

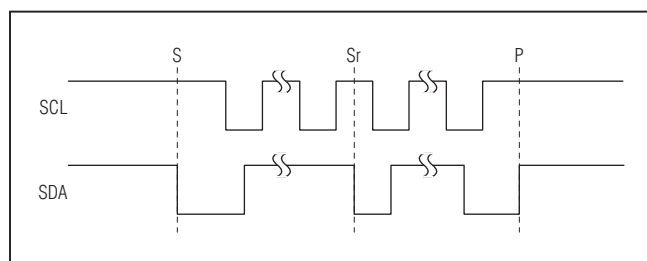


Figure 16. START, STOP, and REPEATED START Conditions

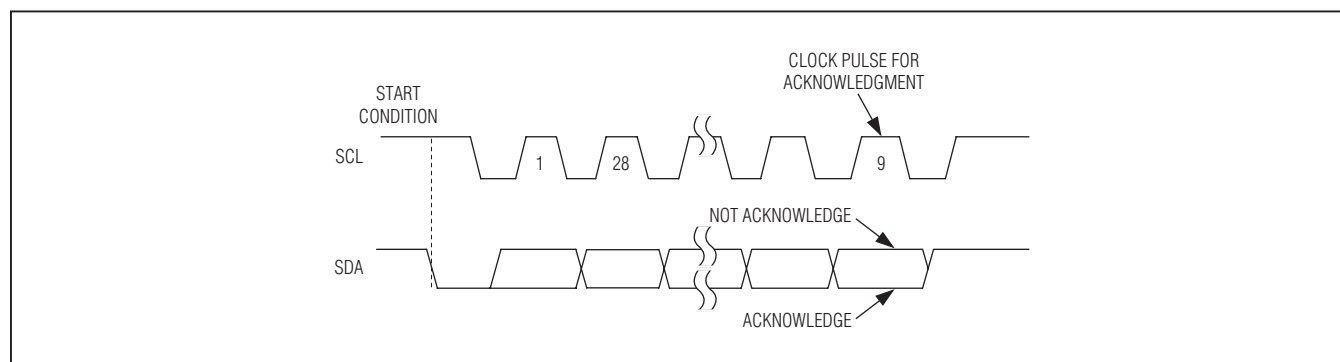


Figure 17. Acknowledge

## High-Efficiency, Low-Noise Audio Subsystem

### Write Data Format

A write to the IC includes transmission of a START condition, the slave address with the R/W bit set to 0, one byte of data to configure the internal register address pointer, one or more bytes of data, and a STOP condition. [Figure 18](#) illustrates the proper frame format for writing one byte of data to the IC. [Figure 19](#) illustrates the frame format for writing n-bytes of data to the IC.

The slave address with the R/W bit set to 0 indicates that the master intends to write data to the IC. The IC acknowledges receipt of the address byte during the master-generated ninth SCL pulse.

The second byte transmitted from the master configures the IC's internal register address pointer. The pointer tells

the IC where to write the next byte of data. An acknowledge pulse is sent by the IC upon receipt of the address pointer data.

The third byte sent to the IC contains the data that are written to the chosen register. An acknowledge pulse from the IC signals receipt of the data byte. The address pointer autoincrements to the next register address after each received data byte. This autoincrement feature allows a master to write to sequential registers within one continuous frame. The master signals the end of transmission by issuing a STOP condition. Register addresses greater than 0x12 are reserved. Do not write to these addresses.

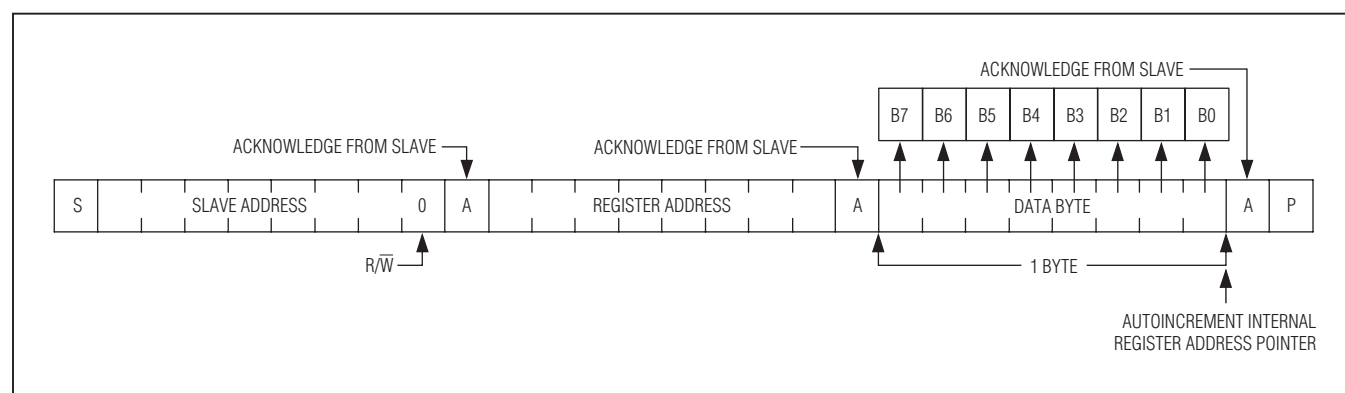


Figure 18. Writing 1 Byte of Data to the IC

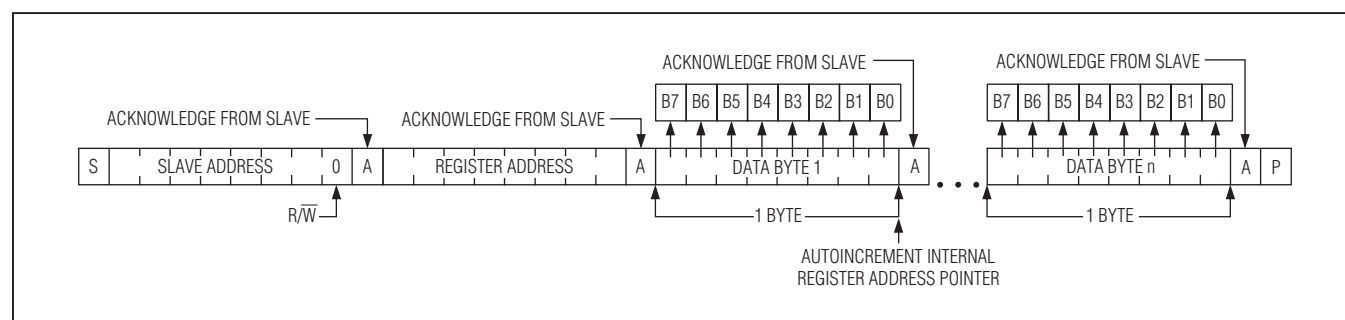


Figure 19. Writing n-Bytes of Data to the IC

## High-Efficiency, Low-Noise Audio Subsystem

### Read Data Format

Send the slave address with the R/W bit set to 1 to initiate a read operation. The IC acknowledges receipt of its slave address by pulling SDA low during the ninth SCL clock pulse. A START command followed by a read command resets the address pointer to register 0x00.

The first byte transmitted from the IC is the contents of register 0x00. Transmitted data is valid on the rising edge of SCL. The address pointer autoincrements after each read data byte. This autoincrement feature allows all registers to be read sequentially within one continuous frame. A STOP condition can be issued after any number of read data bytes. If a STOP condition is issued followed by another read operation, the first data byte to be read are from register 0x00.

The address pointer can be preset to a specific register before a read command is issued. The master pre-sets the address pointer by first sending the IC's slave address with the R/W bit set to 0 followed by the register address. A REPEATED START condition is then sent followed by the slave address with the R/W bit set to 1. The IC then transmits the contents of the specified register. The address pointer autoincrements after transmitting the first byte.

The master acknowledges receipt of each read byte during the acknowledge clock pulse. The master must acknowledge all correctly received bytes except the last byte. The final byte must be followed by a not acknowledge from the master and then a STOP condition. [Figure 20](#) illustrates the frame format for reading one byte from the IC. [Figure 21](#) illustrates the frame format for reading multiple bytes from the IC.

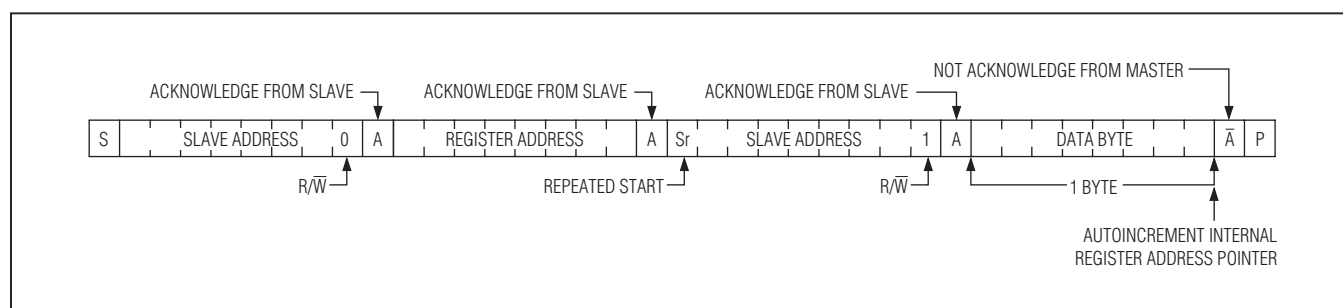


Figure 20. Reading One Byte of Data from the IC

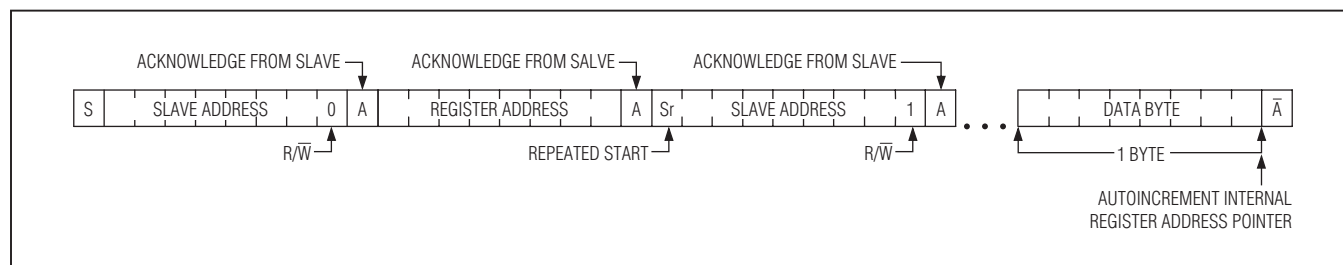


Figure 21. Reading n-Bytes of Data from the IC

# High-Efficiency, Low-Noise Audio Subsystem

## Applications Information

### Filterless Class D Operation

Traditional Class D amplifiers require an output filter to recover the audio signal from the amplifier's output. The filters add cost, increase the solution size of the amplifier, and can decrease efficiency and THD+N performance. The traditional PWM scheme uses large differential output swings ( $2 \times V_{PDD}$  peak-to-peak) and causes large ripple currents. Any parasitic resistance in the filter components results in a loss of power, lowering the efficiency.

The IC does not require an output filter. The device relies on the inherent inductance of the speaker coil and the natural filtering of both the speaker and the human ear to recover the audio component of the square-wave output. Eliminating the output filter results in a smaller, less costly, more efficient solution.

Because the frequency of the IC output is well beyond the bandwidth of most speakers, voice coil movement due to the square-wave frequency is very small. Although this movement is small, a speaker not designed to handle the additional power can be damaged. For optimum results, use a speaker with a series inductance  $> 10\mu\text{H}$ . Typical  $8\Omega$  speakers exhibit series inductances in the  $20\mu\text{H}$  to  $100\mu\text{H}$  range.

### RF Susceptibility

GSM radios transmit using time-division multiple access (TDMA) with 217Hz intervals. The result is an RF signal with strong amplitude modulation at 217Hz and its harmonics that is easily demodulated by audio amplifiers. The IC is designed specifically to reject RF signals. PCB layout, however, has a large impact on the susceptibility of the end product.

In RF applications, improvements to both layout and component selection decreases the IC's susceptibility to RF noise and prevent RF signals from being demodulated into audible noise. Trace lengths should be kept below 1/4 of the wavelength of the RF frequency of interest. Minimizing the trace lengths prevents them from functioning as antennas and coupling RF signals into the IC. The wavelength ( $\lambda$ ) in meters is given by:  $\lambda = c/f$  where  $c = 3 \times 10^8$  m/s, and  $f$  = the RF frequency of interest.

Route audio signals on middle layers of the PCB to allow ground planes above and below to shield them from RF interference. Ideally, the top and bottom layers of the PCB should primarily be ground planes to create effective shielding.

Additional RF immunity can also be obtained by relying on the self-resonant frequency of capacitors as it exhibits the frequency response similar to a notch filter. Depending on the manufacturer, 10pF to 20pF capacitors typically exhibit self resonance at RF frequencies. These capacitors when placed at the input pins can effectively shunt the RF noise at the inputs of the IC. For these capacitors to be effective, they must have a low-impedance, low-inductance path to the ground plane. Avoid using microvias to connect to the ground plane whenever possible as these vias do not conduct well at RF frequencies.

### Startup/Shutdown Sequencing

To ensure proper device initialization and minimal click-and-pop, program the IC's control registers in the correct order. [Table 13](#) lists the correct startup sequence for the device. To shutdown the IC, simply set SHDN = 0.

**Table 13. Startup Sequence**

| SEQUENCE | DESCRIPTION                | REGISTERS        |
|----------|----------------------------|------------------|
| 1        | Ensure SHDN = 0            | 0x12             |
| 2        | Configure inputs           | 0x03, 0x04       |
| 3        | Configure mixers           | 0x05, 0x06       |
| 4        | Configure volume           | 0x07, 0x08, 0x09 |
| 5        | Configure output gain      | 0x10             |
| 6        | Enable amplifiers          | 0x12             |
| 7        | Configure expander and DRC | 0x0A–0x0F        |
| 10       | Set SHDN = 1               | 0x12             |

## High-Efficiency, Low-Noise Audio Subsystem

### Component Selection

#### Optional Ferrite Bead Filter

For applications in which speaker leads exceed 20mm, additional EMI suppression can be achieved by using a filter constructed from a ferrite bead and a capacitor to ground (Figure 22). Use a ferrite bead with low DC resistance, high frequency (> 600MHz) impedance between 100Ω and 600Ω, and rated for at least 1A. The capacitor value varies based on the ferrite bead chosen and the actual speaker lead length. Select a capacitor less than 1nF based on EMI performance.

#### Input Capacitor

An input capacitor,  $C_{IN}$ , in conjunction with the input impedance of the IC line inputs forms a highpass filter that removes the DC bias from an incoming analog signal. The AC-coupling capacitor allows the amplifier to automatically bias the signal to an optimum DC level. Assuming zero source impedance, the -3dB point of the highpass filter is given by:

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}}$$

$R_{IN}$  is defined in the [Electrical Characteristics](#) table under the Input Resistance section. Choose  $C_{IN}$  so that  $f_{-3dB}$  is well below the lowest frequency of interest. For best audio quality, use capacitors whose dielectrics have low-voltage coefficients, such as tantalum or aluminum electrolytic. Capacitors with high-voltage coefficients, such as ceramics, can result in increased distortion at low frequencies.

#### Charge-Pump Capacitor Selection

Use capacitors with an ESR less than 100mΩ for optimum performance. Low-ESR ceramic capacitors minimize the output resistance of the charge pump. Most surface-mount ceramic capacitors satisfy the ESR requirement. For best performance over the extended temperature range, select capacitors with an X7R dielectric.

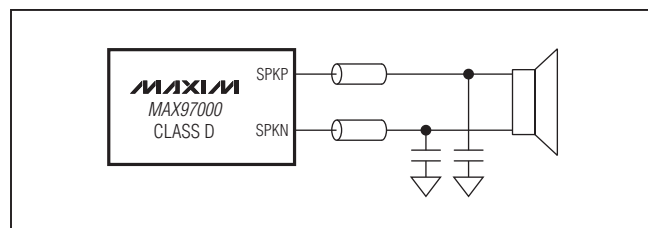


Figure 22. Optional Class D Ferrite Bead Filter

#### Charge-Pump Flying Capacitor

The value of the flying capacitor (connected between C1N and C1P) affects the output resistance of the charge pump. A value that is too small degrades the device's ability to provide sufficient current drive, which leads to a loss of output voltage. Increasing the value of the flying capacitor reduces the charge-pump output resistance to an extent. Above 1μF, the on-resistance of the internal switches and the ESR of external charge-pump capacitors dominate.

#### Charge-Pump Holding Capacitor

The holding capacitor (bypassing CPVSS) value and ESR directly affect the ripple at CPVSS. Increasing the capacitor's value reduces output ripple. Likewise, decreasing the ESR reduces both ripple and output resistance. Lower capacitance values can be used in systems with low maximum output power levels. See the Output Power vs. Load Resistance graph in the [Typical Operating Characteristics](#) section for more information.

#### Supply Bypassing, Layout, and Grounding

Proper layout and grounding are essential for optimum performance. Use a large continuous ground plane on a dedicated layer of the PCB to minimize loop areas. Connect GND and PGND directly to the ground plane using the shortest trace length possible. Proper grounding improves audio performance, minimizes crosstalk between channels, and prevents digital noise from coupling into the analog signals.

Place the capacitor between C1P and C1N as close as possible to the IC to minimize trace length from C1P to C1N. Inductance and resistance added to C1P and C1N reduce the output power of the headphone amplifier. Bypass CPVDD and CPVSS with capacitors located close to the pins with a short trace length to PGND. Close decoupling of CPVDD and CPVSS minimizes supply ripple and maximizes output power from the headphone amplifier.

Bypass PVDD to PGND with as little trace length as possible. Connect SPKP and SPKN to the speaker using the shortest and widest traces possible. Reducing trace length minimizes radiated EMI. Route SPKP/SPKN as a differential pair on the PCB to minimize the loop area and thereby the inductance of the circuit. If filter components are used on the speaker outputs, be sure to locate them as close as possible to the IC to ensure maximum effectiveness. Minimize the trace length from any ground tied passive components to PGND to further minimize radiated EMI.

## High-Efficiency, Low-Noise Audio Subsystem

An evaluation kit (EV kit) is available to provide an example layout for the IC. The EV kit allows quick setup of the IC and includes easy-to-use software allowing all internal registers to be controlled.

### WLP Applications Information

For the latest application details on WLP construction, dimensions, tape carrier information, PCB techniques,

bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to the Application Note 1891: *Wafer-Level Packaging (WLP) and its Applications* on Maxim's website. [Figure 23](#) shows the dimensions of the WLP balls used on the IC.

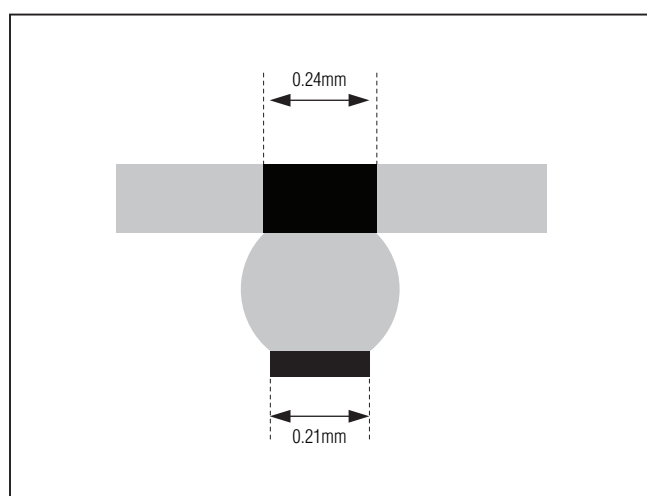


Figure 23. WLP Ball Dimensions

### Ordering Information

| PART         | TEMP RANGE     | PIN-PACKAGE |
|--------------|----------------|-------------|
| MAX97003EWP+ | -40°C to +85°C | 20 WLP      |

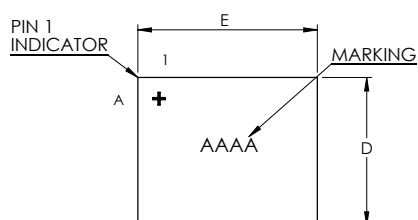
+Denotes a lead(Pb)-free/RoHS-compliant package.

## High-Efficiency, Low-Noise Audio Subsystem

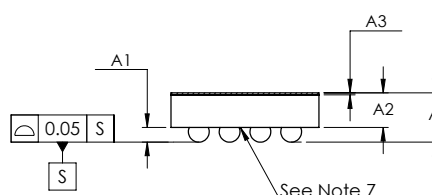
### Package Information

For the latest package outline information and land patterns (footprints), go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO.             | LAND PATTERN NO.                               |
|--------------|--------------|-------------------------|------------------------------------------------|
| 20 WLP       | W201A2+1     | <a href="#">21-0544</a> | Refer to <a href="#">Application Note 1891</a> |

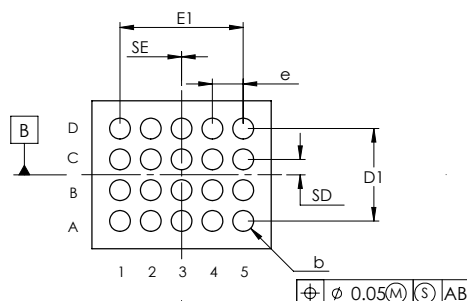


TOP VIEW



SIDE VIEW

| COMMON DIMENSIONS |        |       |
|-------------------|--------|-------|
| A                 | 0.64   | ±0.05 |
| A1                | 0.19   | ±0.03 |
| A2                | 0.45   | REF   |
| A3                | 0.025  | BASIC |
| b                 | Ø 0.27 | ±0.03 |
| D1                | 1.20   | BASIC |
| E1                | 1.60   | BASIC |
| e                 | 0.40   | BASIC |
| SD                | 0.20   | BASIC |
| SE                | 0.00   | BASIC |



BOTTOM VIEW

| PKG. CODE | E    |      | D    |      | DEPOPULATED BUMPS |
|-----------|------|------|------|------|-------------------|
|           | MIN  | MAX  | MIN  | MAX  |                   |
| W201A2+1  | 2.33 | 2.36 | 1.92 | 1.95 | NONE              |
| W201B2+1  | 2.16 | 2.19 | 1.60 | 1.63 | NONE              |
| W201C2+1  | 2.01 | 2.04 | 1.61 | 1.64 | NONE              |
| W201D2+1  | 2.08 | 2.11 | 1.71 | 1.74 | NONE              |

#### NOTES:

1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeter.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02 unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front - side finish can be either Black or Clear.

-DRAWING NOT TO SCALE-

|                                                         |                      |      |     |
|---------------------------------------------------------|----------------------|------|-----|
| <b>MAXIM</b>                                            |                      |      |     |
| TITLE PACKAGE OUTLINE<br>20 BUMPS, WLP PKG. 0.4mm PITCH |                      |      |     |
| APPROVAL                                                | DOCUMENT CONTROL NO. | REV. | 1/1 |
|                                                         | 21-0544              | B    |     |

**High-Efficiency, Low-Noise Audio Subsystem*****Revision History***

| REVISION<br>NUMBER | REVISION<br>DATE | DESCRIPTION     | PAGES<br>CHANGED |
|--------------------|------------------|-----------------|------------------|
| 0                  | 9/11             | Initial release | —                |

*Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time. The parametric values (min and max limits) shown in the Electrical Characteristics table are guaranteed. Other parametric values quoted in this data sheet are provided for guidance.*

**Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600 \_\_\_\_\_ 48**

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Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

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