

TC74LCX541F, TC74LCX541FT, TC74LCX541FK

Low-Voltage Octal Bus Buffer with 5-V Tolerant Inputs and Outputs

The TC74LCX541 is a high-performance CMOS octal bus buffer. Designed for use in 3.3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

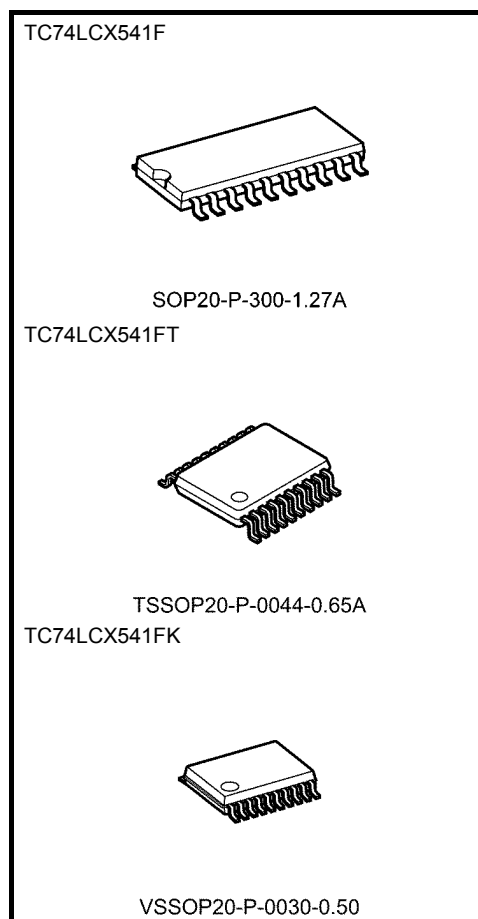
The device is designed for low-voltage (3.3 V) VCC applications, but it could be used to interface to 5 V supply environment for both inputs and outputs.

The TC74LCX541 is a non-inverting 3-state buffer having two active-low output enables. When either $\overline{OE1}$ or $\overline{OE2}$ are high, the terminal outputs are in the high-impedance state. This device is designed to be used with 3-state memory address drivers, etc.

All inputs are equipped with protection circuits against static discharge.

Features

- Low-voltage operation: $V_{CC} = 1.65$ to 3.6 V
- High-speed operation: $t_{pd} = 6.5$ ns (max) ($V_{CC} = 3.0$ to 3.6 V)
- Output current: $|I_{OH}|/I_{OL} = 24$ mA (min) ($V_{CC} = 3.0$ V)
- Latch-up performance: $\geq \pm 500$ mA
- Available in JEITA SOP, TSSOP and VSSOP (US)
- Power-down protection provided on all inputs and outputs
- Pin and function compatible with the 74 series (74AC/VHC/HC/F/ALS/LS etc.) 541 type



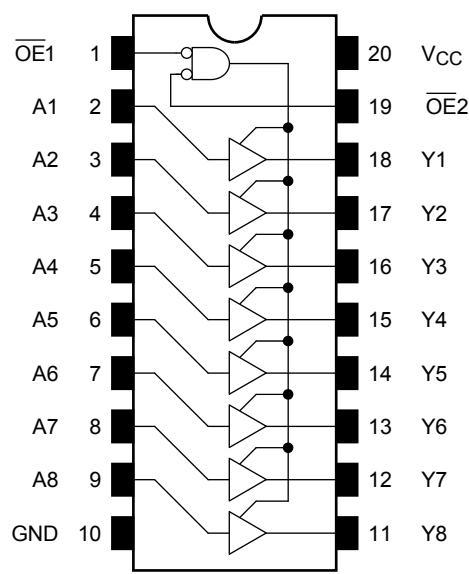
Weight:

| | |
|----------------------|-----------------|
| SOP20-P-300-1.27A | : 0.22 g (typ.) |
| TSSOP20-P-0044-0.65A | : 0.08 g (typ.) |
| VSSOP20-P-0030-0.50 | : 0.03 g (typ.) |

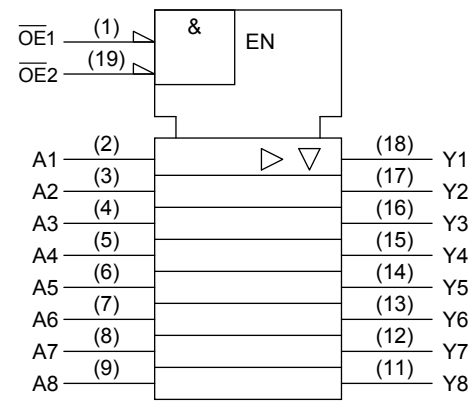
Note: The Electrical Characteristics of $V_{CC}=1.8\pm0.15$ V is only applicable for products which manufactured from January 2009 onward.

Start of commercial production
1995-02

Pin Assignment (top view)



IEC Logic Symbol



Truth Table

| Inputs | | | Outputs |
|--------|-----|----|---------|
| OE1 | OE2 | An | |
| H | X | X | Z |
| X | H | X | Z |
| L | L | H | H |
| L | L | L | L |

X: Don't care

Z: High impedance

Absolute Maximum Ratings (Note 1)

| Characteristics | Symbol | Rating | Unit |
|-----------------------------|------------------|---------------------------------|------|
| Power supply voltage | V_{CC} | -0.5 to 7.0 | V |
| DC input voltage | V_{IN} | -0.5 to 7.0 | V |
| DC output voltage | V_{OUT} | -0.5 to 7.0 (Note 2) | V |
| | | -0.5 to $V_{CC} + 0.5$ (Note 3) | |
| Input diode current | I_{IK} | -50 | mA |
| Output diode current | I_{OK} | ± 50 (Note 4) | mA |
| DC output current | I_{OUT} | ± 50 | mA |
| Power dissipation | P_D | 180 | mW |
| DC V_{CC} /ground current | I_{CC}/I_{GND} | ± 100 | mA |
| Storage temperature | T_{stg} | -65 to 150 | °C |

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: Output in OFF state

Note 3: High or low state. I_{OUT} absolute maximum rating must be observed.

Note 4: $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

Operating Ranges (Note 1)

| Characteristics | Symbol | Rating | Unit |
|--------------------------|-----------------|------------------------|------|
| Power supply voltage | V_{CC} | 1.65 to 3.6 | V |
| | | 1.5 to 3.6 (Note 2) | |
| Input voltage | V_{IN} | 0 to 5.5 | V |
| Output voltage | V_{OUT} | 0 to 5.5 (Note 3) | V |
| | | 0 to V_{CC} (Note 4) | |
| Output current | I_{OH}/I_{OL} | ± 24 (Note 5) | mA |
| | | ± 12 (Note 6) | |
| Operating temperature | T_{opr} | -40 to 85 | °C |
| Input rise and fall time | dt/dv | 0 to 10 (Note 7) | ns/V |

Note 1: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Note 2: Data retention only

Note 3: Output in OFF state

Note 4: High or low state

Note 5: $V_{CC} = 3.0$ to 3.6 V

Note 6: $V_{CC} = 2.7$ to 3.0 V

Note 7: $V_{IN} = 0.8$ to 2.0 V, $V_{CC} = 3.0$ V

Electrical Characteristics
DC Characteristics (Ta = -40 to 85°C)

| Characteristics | | Symbol | Test Condition | | | Min | Max | Unit |
|---------------------------------------|---------|------------------|---|---------------------------|---------------------|----------------------|----------------------|------|
| | | | | | V _{CC} (V) | | | |
| Input voltage | H-level | V _{IH} | — | | 1.65 to 2.3 | V _{CC} ×0.9 | — | V |
| | | | | | 2.3 to 2.7 | 1.7 | — | |
| | | | | | 2.7 to 3.6 | 2.0 | — | |
| | L-level | V _{IL} | — | | 1.65 to 2.3 | — | V _{CC} ×0.1 | |
| | | | | | 2.3 to 2.7 | — | 0.7 | |
| | | | | | 2.7 to 3.6 | — | 0.8 | |
| Output voltage | H-level | V _{OH} | V _{IN} = V _{IH} or V _{IL} | I _{OH} = −100 μA | 1.65 to 3.6 | V _{CC} −0.2 | — | V |
| | | | | I _{OH} = −4 mA | 1.65 | 1.05 | — | |
| | | | | I _{OH} = −8 mA | 2.3 | 1.7 | — | |
| | | | | I _{OH} = −12 mA | 2.7 | 2.2 | — | |
| | | | | I _{OH} = −18 mA | 3.0 | 2.4 | — | |
| | | | | I _{OH} = −24 mA | 3.0 | 2.2 | — | |
| | L-level | V _{OL} | V _{IN} = V _{IH} or V _{IL} | I _{OL} = 100 μA | 1.65 to 3.6 | — | 0.2 | |
| | | | | I _{OL} = 4 mA | 1.65 | — | 0.45 | |
| | | | | I _{OL} = 8 mA | 2.3 | — | 0.7 | |
| | | | | I _{OL} = 12 mA | 2.7 | — | 0.4 | |
| | | | | I _{OL} = 16 mA | 3.0 | — | 0.4 | |
| | | | | I _{OL} = 24 mA | 3.0 | — | 0.55 | |
| Input leakage current | | I _{IN} | V _{IN} = 0 to 5.5 V | 1.65 to 3.6 | — | ±5.0 | μA | |
| 3-state output off-state current | | I _{OZ} | V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0 to 5.5 V | 1.65 to 3.6 | — | ±5.0 | μA | |
| Power off leakage current | | I _{OFF} | V _{IN} /V _{OUT} = 5.5 V | 0 | — | 10.0 | μA | |
| Quiescent supply current | | I _{CC} | V _{IN} = V _{CC} or GND | 1.65 to 3.6 | — | 10.0 | μA | |
| | | | V _{IN} /V _{OUT} = 3.6 to 5.5 V | 1.65 to 3.6 | — | ±10.0 | | |
| Increase in I _{CC} per input | | ΔI _{CC} | V _{IH} = V _{CC} − 0.6 V | 2.7 to 3.6 | — | 500 | | |

AC Characteristics (Ta = -40 to 85°C)

| Characteristics | Symbol | Test Condition | V _{CC} (V) | Min | Max | Unit |
|------------------------|--|--------------------|---------------------|-----|------|------|
| | | | | | | |
| Propagation delay time | t _{pLH} t _{pHL} | Figure 1, Figure 2 | 1.8 ± 0.15 | — | 25.0 | ns |
| | | | 2.5 ± 0.2 | — | 8.5 | |
| | | | 2.7 | — | 7.5 | |
| | | | 3.3 ± 0.3 | 1.5 | 6.5 | |
| Output enable time | t _{pZL} t _{pZH} | Figure 1, Figure 3 | 1.8 ± 0.15 | — | 34.0 | ns |
| | | | 2.5 ± 0.2 | — | 17.0 | |
| | | | 2.7 | — | 9.5 | |
| | | | 3.3 ± 0.3 | 1.5 | 8.5 | |
| Output disable time | t _{pLZ} t _{pHZ} | Figure 1, Figure 3 | 1.8 ± 0.15 | — | 32.0 | ns |
| | | | 2.5 ± 0.2 | — | 16.0 | |
| | | | 2.7 | — | 8.5 | |
| | | | 3.3 ± 0.3 | 1.5 | 7.5 | |
| Output to output skew | t _{osLH} t _{osHL} | (Note) | 2.7 | — | — | ns |
| | | | 3.3 ± 0.3 | — | 1.0 | |

Note: Parameter guaranteed by design.

(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)

Dynamic Switching Characteristics (Ta = 25°C, input: t_r = t_f = 2.5 ns, C_L = 50 pF, R_L = 500 Ω)

| Characteristics | Symbol | Test Condition | V _{CC} (V) | Typ. | Unit | |
|------------------------------|-----------------|------------------|--|------|------|---|
| | | | | | | |
| Quiet output maximum dynamic | V _{OL} | V _{OLP} | V _{IH} = 3.3 V, V _{IL} = 0 V | 3.3 | 0.8 | V |
| Quiet output minimum dynamic | V _{OL} | V _{OLV} | V _{IH} = 3.3 V, V _{IL} = 0 V | 3.3 | 0.8 | V |

Capacitive Characteristics (Ta = 25°C)

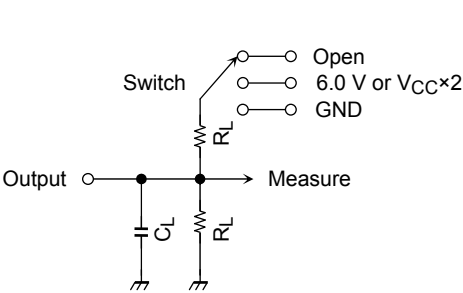
| Characteristics | Symbol | Test Condition | | Typ. | Unit | |
|-------------------------------|------------------|--------------------------|---------------------|------|------|----|
| | | | V _{CC} (V) | | | |
| Input capacitance | C _{IN} | — | 3.3 | 7 | pF | |
| Output capacitance | C _{OUT} | — | 3.3 | 8 | pF | |
| Power dissipation capacitance | C _{PD} | f _{IN} = 10 MHz | (Note) | 3.3 | 40 | pF |

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

AC Test Circuit



| Parameter | Switch |
|--------------------|---|
| t_{pLH}, t_{pHL} | Open |
| t_{pLZ}, t_{pZL} | 6.0 V @ $V_{CC} = 3.3 \pm 0.3V$ @ $V_{CC} = 2.7V$ |
| | $V_{CC} \times 2$ @ $V_{CC} = 2.5 \pm 0.2V$ @ $V_{CC} = 1.8 \pm 0.15V$ |
| t_{pHZ}, t_{pZH} | GND |

Figure 1

The diagram illustrates the timing characteristics of a CMOS inverter. The input signal (Input A) is a square wave with a rise time $t_r = 2.5 \text{ ns}$ and a fall time $t_f = 2.5 \text{ ns}$. The input voltage levels are V_{IH} (high) and V_{IM} (midpoint), with the signal falling to 10% of V_{IH} during the fall time. The output signal (Output Y) is a square wave with a low-to-high propagation delay t_{pLH} and a high-to-low propagation delay t_{pHL} . The output voltage levels are V_{OH} (high) and V_{OL} (low), with the signal falling to V_{OM} (midpoint) during the fall time.

The diagram illustrates the timing characteristics of the 74VHC125 during enable and disable transitions. The **Output Enable (\overline{OE})** signal transitions from high to low (enabling) and from low to high (disabling). The output signals **Output (Y) Low to Off to Low** and **Output (Y) High to Off to High** show the output voltage levels during these transitions.

Timing Parameters:

- t_r : Enable rise time (from low to high).
- t_f : Enable fall time (from high to low).
- t_{pLZ} : Low-to-Z propagation delay (from \overline{OE} falling edge to output reaching V_X).
- t_{pZL} : Z-to-L propagation delay (from \overline{OE} rising edge to output reaching V_{IM}).
- t_{pHZ} : High-to-Z propagation delay (from \overline{OE} falling edge to output reaching V_Y).
- t_{pZH} : Z-to-H propagation delay (from \overline{OE} rising edge to output reaching V_{OM}).

Voltage Levels:

- V_{IH} : Input high voltage.
- V_{IM} : Input medium voltage (90% of V_{IH}).
- V_{OL} : Output low voltage.
- V_{OM} : Output medium voltage (10% of V_{OH}).
- V_{OH} : Output high voltage.
- V_X : Output voltage at the end of t_{pLZ} .
- V_Y : Output voltage at the end of t_{pHZ} .

Output States:

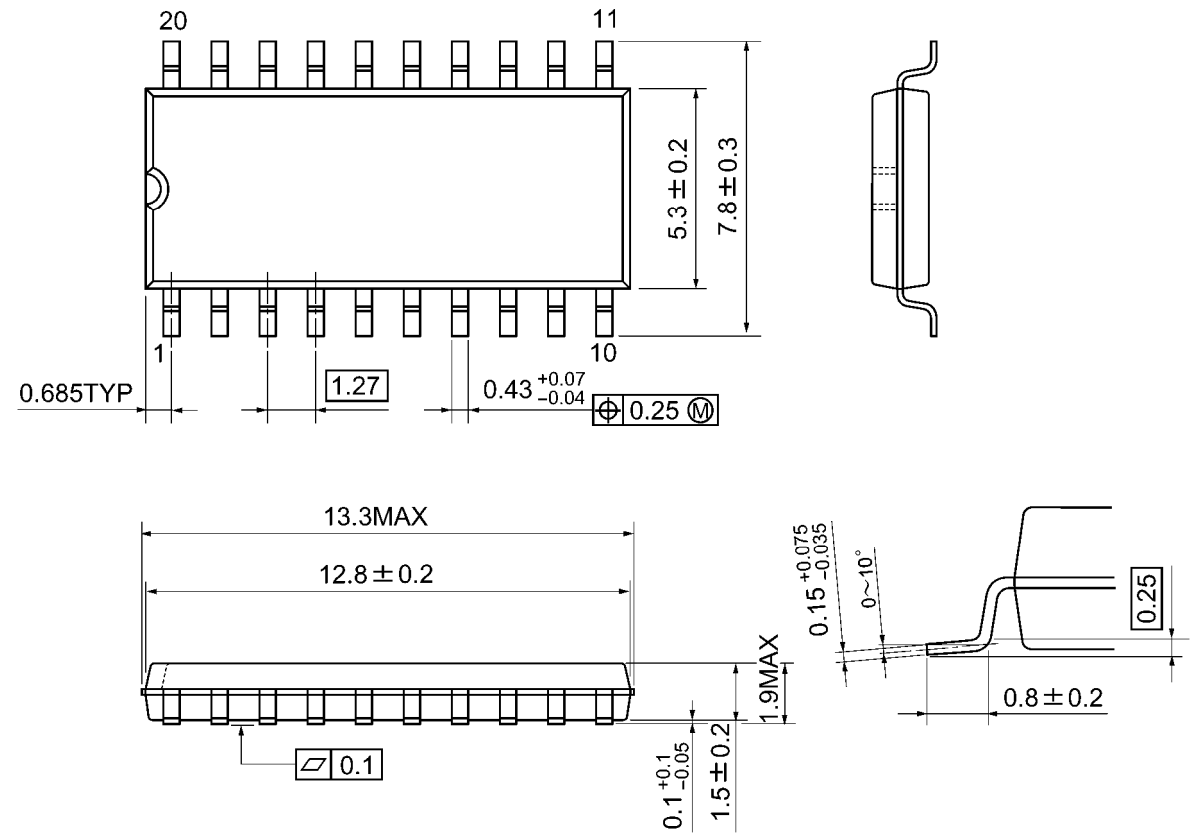
- Outputs enabled:** When \overline{OE} is low.
- Outputs disabled:** When \overline{OE} is high.
- Outputs enabled:** When \overline{OE} transitions from high to low.

| | Symbol | V _{CC} | | |
|--------|-----------------|-----------------------|------------------------|------------------------|
| | | 3.3 ± 0.3 V 2.7V | 2.5 ± 0.2 V | 1.8 ± 0.15 V |
| Input | V _{IH} | 2.7V | V _{CC} | V _{CC} |
| | V _{IM} | 1.5V | V _{CC} /2 | V _{CC} /2 |
| | tr,tf | 2.5ns | 2.0ns | 2.0ns |
| Output | V _{OM} | 1.5V | V _{OH} /2 | V _{OH} /2 |
| | V _X | V _{OL} +0.3V | V _{OL} +0.15V | V _{OL} +0.15V |
| | V _Y | V _{OH} -0.3V | V _{OH} -0.15V | V _{OH} -0.15V |
| Load | C _L | 50pF | 30pF | 30pF |
| | R _L | 500Ω | 500Ω | 1kΩ |

Package Dimensions

SOP20-P-300-1.27A

Unit: mm

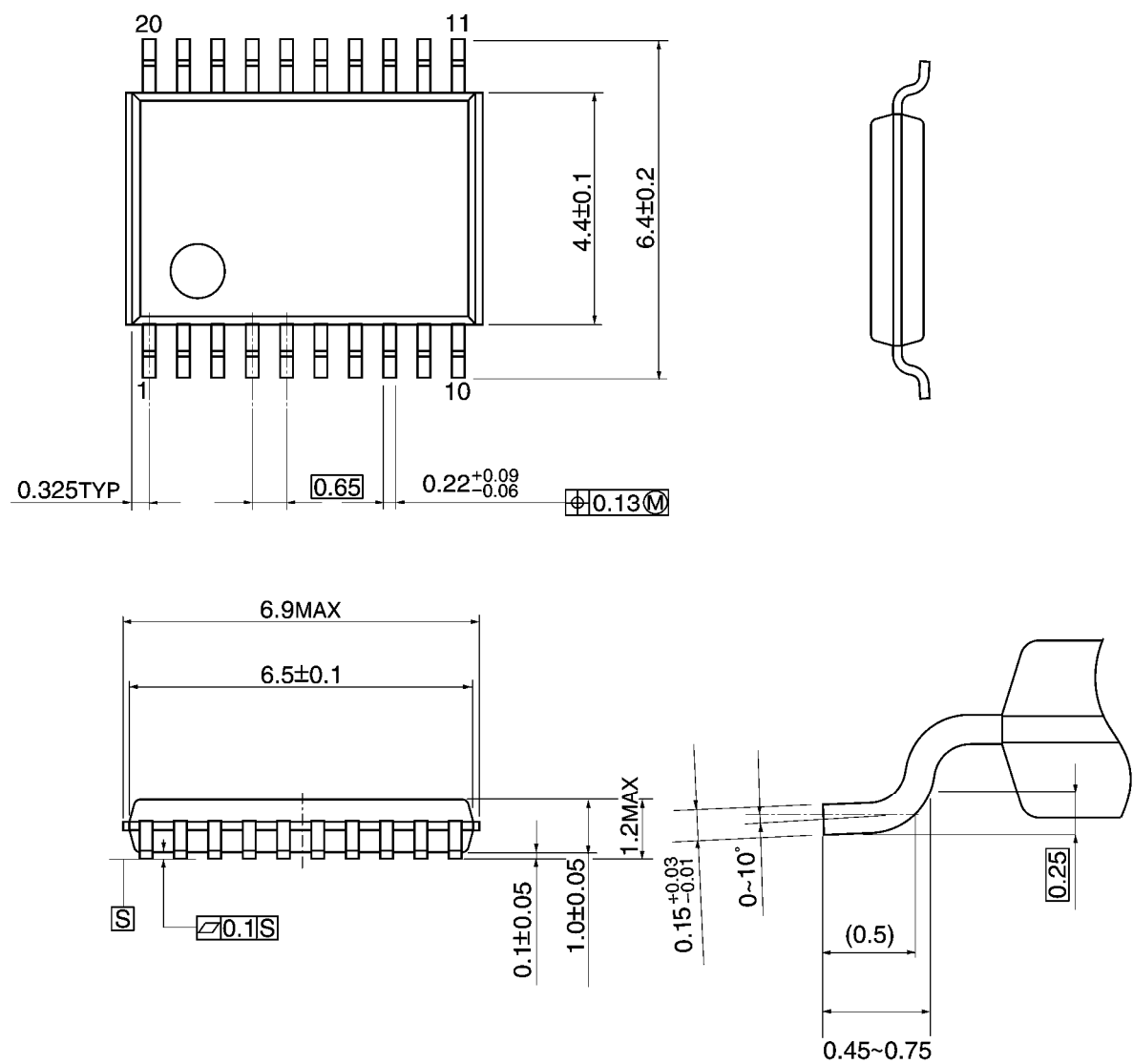


Weight: 0.22 g (typ.)

Package Dimensions

TSSOP20-P-0044-0.65A

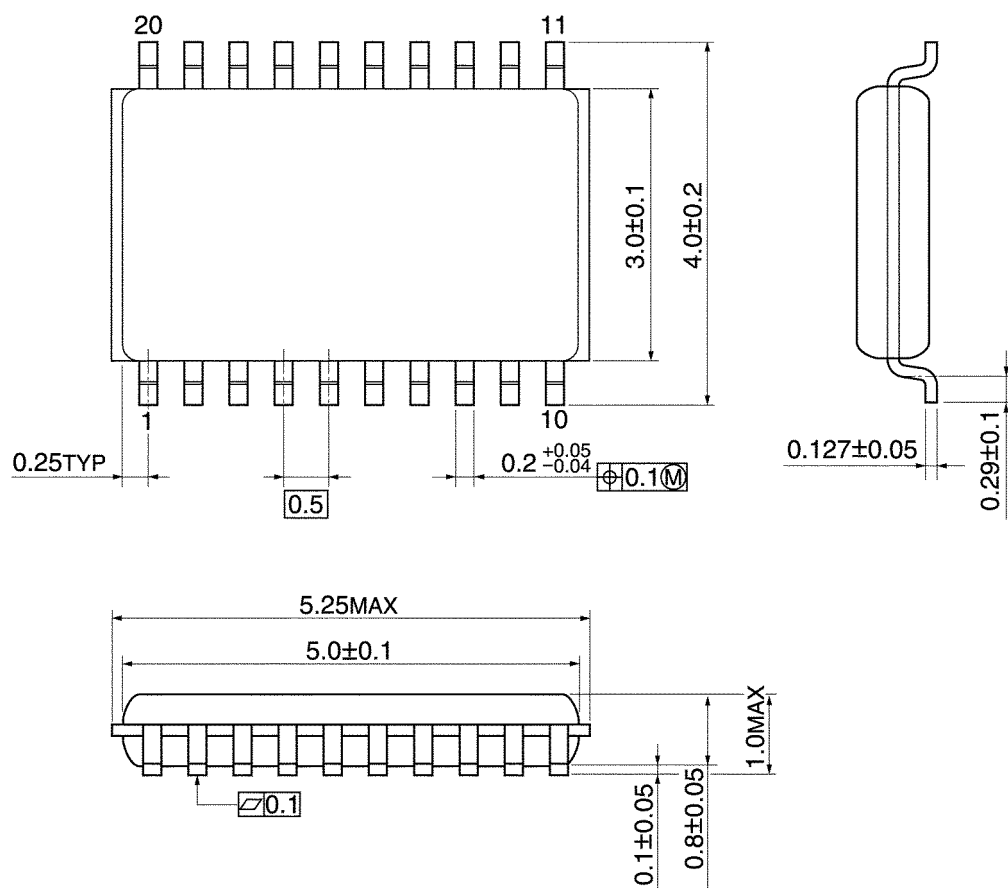
Unit: mm



Weight: 0.08 g (typ.)

VSSOP20-P-0030-0.50

Unit: mm



Weight: 0.03 g (typ.)

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