LTC4233/LTC4234
10A/20A Guaranteed SOA Hot Swap Controller

DESCRIPTION

Demonstration circuit 2116A features the LTC4233/ LTC®4234 10A/20A Guaranteed SOA Hot Swap™ Controllers. The LTC4233 and LTC4234 are ideally suited for compact power distribution control in 2.9V to 15V applications for hot board insertion protection, high side power switching, and electronic circuit breaker functions. They provide a rich set of features to support Hot Swap applications including:

- 2.5% Accurate Undervoltage and Overvoltage Protection

- Overtemperature Protection

- Adjustable Inrush Current Control

- Adjustable, 11% Accurate Current Limit

- Adjustable Output Voltage Ramp Rate

- Configurable for Auto Retry or Latch Off for Overcurrent Faults

- Power Good and Fault Outputs

Available in 38-pin 5mm × 9mm QFN packages, the LTC4234 is showcased on DC2116A-A while the LTC4233 is showcased on DC2116A-B, both configured for a 12V application. By changing a few passive components, 2.9V to 15V applications can easily be evaluated.

Design files for this circuit board are available at http://www.linear.com/demo/DC2116A

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PERFORMANCE SUMMARY Specifications are at T_A = 25°C

PARAMETER	CONDITIONS	VALUE
Input Supply Voltage Range		2.9V to 15V
Nominal Operating Voltage		12.0V
Overvoltage Lockout	Nominal	15.2V
Undervoltage Lockout (Voltage Falling)	Nominal	9.2V
Undervoltage Lockout (Voltage Rising)	Nominal	9.9V
Output Current Limit	Nominal (LTC4233)	11.2A
	Nominal (LTC4234)	22.5A
Maximum Load Capacitance	Nominal	8200µF
Timer Expiration Period	Nominal	1.2ms or 2.0ms

QUICK START PROCEDURE

Table 1. Power Input and Output Connections

NOMENCLATURE	CONNECTOR	DESCRIPTION
VDD	E13	12V In
GND	E14	12V In Return
VOUT	E6	12V Out
GND	E7	12V Out Return

Table 2. Test Points

NOMENCLATURE	TURRET	DESCRIPTION
INTVCC	E1	$INTV_{CC}$ monitor
TIMER	E2	TIMER pin monitor
PG	E3	PG pin monitor
ISET	E4	I_{SET} pin monitor
IMON	E5	I_{MON} pin monitor
GND	E8	V_{OUT} return monitor
VOUT	E9	V_{OUT} monitor
UV	E10	UV pin monitor
OV	E11	OV pin monitor
VDD	E12	V_{DD} monitor
GND	E15	V_{DD} return monitor
SENSE	E16	SENSE pin monitor
$\overline{FLT}$	E17	$\overline{FLT}$ pin monitor
GATE	E18	GATE pin monitor
GND	E19, E20, E21	Ground

Table 3. LED Indicators

NOMENCLATURE	PART DESIGNATOR	DESCRIPTION
FAULT	D1 (Red)	Indicates Overcurrent Fault
POWER BAD	D2 (Red)	V_{OUT} Not Up to Full Voltage
INPUT POWER	D3 (Green)	Input Voltage Present
OUTPUT POWER	D4 (Green)	Output Voltage Present

Table 4. Jumpers

NOMENCLATURE	PART DESIGNATOR	DESCRIPTION
AUTORETRY	JP1	ON Position for Autoretry
TIMER DURATION	JP2	1.2ms or 2.0ms Timer Duration

DC2116A-A QUICK START PROCEDURE

DC2116A-A is easy to set up to evaluate the performance of the LTC4234. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below.

DC2116A has two user configurable jumper options:

- JP1 AUTORETRY – Set to ON for auto retry or OFF for latch off on over-current faults. (Default position: OFF)

- JP2 TIMER DURATION – Set to 2ms for the internal 2ms timer or 1.2ms determined by C2, C2 may be replaced for other timer durations. (Default position: 1.2ms)

LEDs indicate the state of input power (D2), output power (D4), FAULT (D3) and PG (D1). Load current can be monitored on the IMON turret, which has a value of 0.1V/A determined by RMON (20k.)

Set an adjustable power supply, capable of supplying 30 amps, at 16V. Turn off power and connect the supply to the VDD and GND banana jacks.

Connect a suitable load to the VOUT and GND banana jacks. This load can be an electronic load or power resistors capable of dissipating 300W.

NOTE: Because the LTC4234 incorporates foldback current limiting, the nominal startup current supplied to the load is approximately 5.7A, and may be as low as 4A. This current limit increases linearly until the FB pin exceeds 0.6V ($V_{OUT} > 5.1V$). An electronic constant current load set to $\leq$ 20 amps will not permit the circuit to turn on unless it is gated on by the PG signal (as would be the case with a DC/DC converter controlled by the PG signal). Resistive loading will not have this problem.
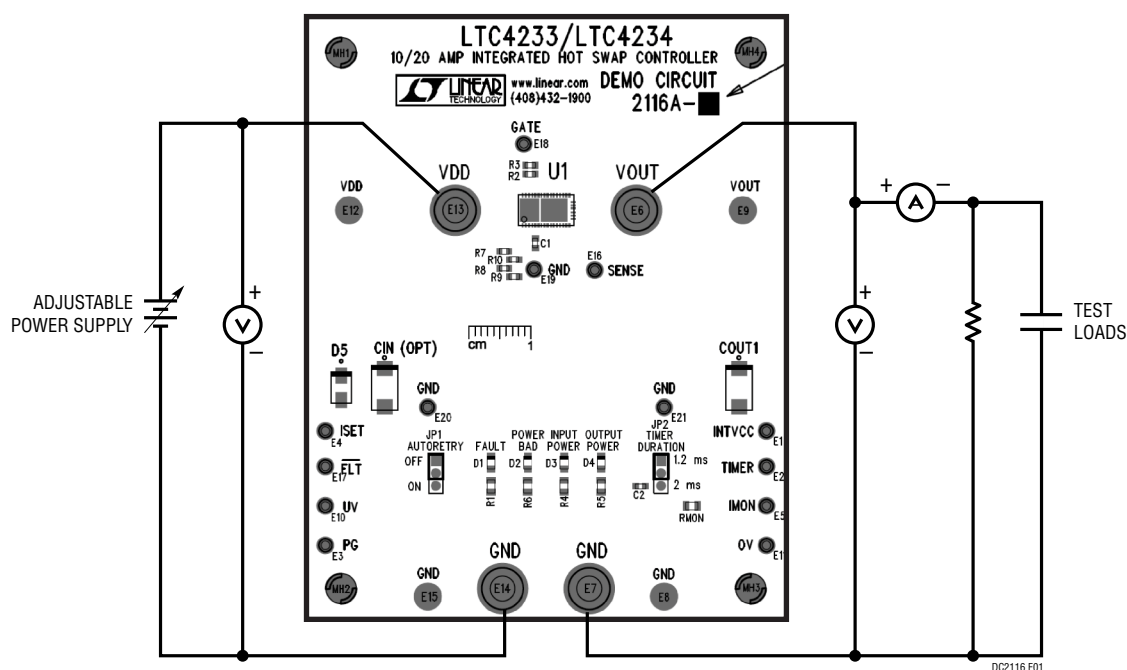

Figure 1. Proper Measurement Equipment Setup

DC2116A-A QUICK START PROCEDURE

Turn on the power supply; verify the input voltage is 12V. Verify the output voltage and the load current; D3 and D4 should both be illuminated (input voltage and output voltage, respectively) and both D1 (FLT) and D2 (PG) should be off. On power-up, observe the slope of V_{OUT}. This should be in the range of 0.15 to 0.55V/ms, corresponding to a ramp-up time of 22ms to 80ms to 12V. With the circuit functioning, additional evaluations can now be performed.

OV/UV/PG thresholds – Set the input supply to zero and ramp the voltage slowly, observing the following events. Above 10.0V, the circuit will be out of UV lockout and the output should ramp up, lighting D4. Above 10.9V the FB pin will be past its threshold, asserting the PG pin high and extinguishing D2. Increasing the supply past 15.2V will engage OV lockout; D4 will extinguish and D2 will light. Note that the voltages indicated in this step are maximums, taking into consideration the tolerances of the resistors and the LTC4234 thresholds.

Current Limit Thresholds – With the input supply set to 12V, load the output with a 0.59Ω power resistor capable of dissipating 300W. Power should remain on, as the current

will be below the 20A minimum current limit threshold. Next, load the output with a 0.48Ω power resistor. Power should be interrupted, as the current will be above the 25A maximum current limit threshold.

Inrush into capacitive load – One of the main functions of a Hot Swap circuit is to provide controlled ramp-up into a capacitive load to avoid disturbing the input power supply. For the following tests, ensure that the AUTORETRY jumper is set to OFF and the TIMER DURATION jumper is set to 2.0ms. To guarantee that current limit is never reached during ramp-up into a capacitor, the current must be less than the minimum current limit threshold of 4A when the gate ramp rate is at its maximum value of 0.6V/ms. (Note that the minimum current limit threshold occurs when the FB pin is at 0V.)
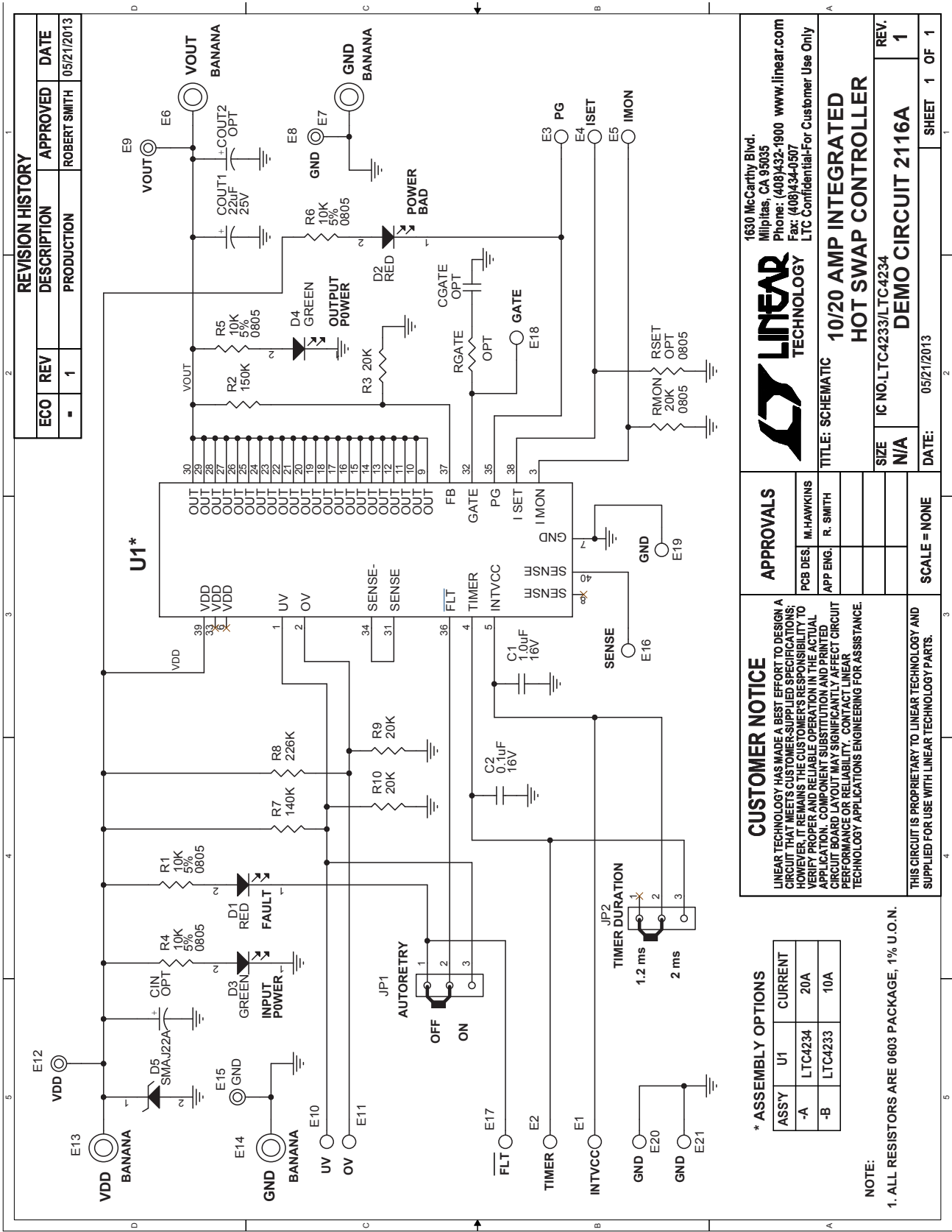
$$C = i/(dV/dt) = 4A/(0.6V/ms) = 6667\mu F$$

Thus the circuit will always power up successfully with a 6000µF capacitor at V_{OUT}, and observation of the TIMER turret post will show that it never begins to ramp.

DC2116A-B QUICK START PROCEDURE

The LTC4233, on the DC2116A-B, should be tested as above with actual values scaled to values shown in the data sheet.

dc2116afa

SCHEMATIC DIAGRAM

REVISION HISTORY

ECO	REV	DESCRIPTION	APPROVED	DATE
-	1	PRODUCTION	ROBERT SMITH	05/21/2013

U1*

OUT (30, 29, 28, 27, 26, 25, 24, 23, 22, 21, 20, 19, 18, 17, 16, 15, 14, 13, 12, 11, 10, 9)

VDD (39, 33, 6)
FB 37
GATE 32
PG 35
I SET 38
I MON 3
GND 7
UV 1
OV 2
SENSE- 34
SENSE 31
SENSE 40
SENSE 8
FLT 36
TIMER 4
INTVCC 5

VOUT BANANA — E6, E9, VOUT
GND BANANA — E7, E8, GND
VDD BANANA — E12, E13, VDD
GND BANANA — E14, E15, GND

PG E3
ISET E4
IMON E5
GATE E18
SENSE E16
GND E19

COUT2 OPT
COUT1 22µF 25V
R6 10K 5% 0805
D2 RED POWER BAD
CGATE OPT
RGATE OPT
RSET OPT 0805
RMON 20K 0805
R5 10K 5% 0805
D4 GREEN OUTPUT POWER
R2 150K
R3 20K

R8 226K
R9 20K
R7 140K
R10 20K
R1 10K 5% 0805
D1 RED FAULT
R4 10K 5% 0805
D3 GREEN INPUT POWER
CIN OPT
D5 SMAJ22A
C1 1.0µF 16V
C2 0.1µF 16V

JP1 AUTORETRY (OFF, ON) 1 2 3
JP2 TIMER DURATION (1.2 ms, 2 ms) 1 2 3

UV E10
OV E11
FLT E17
TIMER E2
INTVCC E1
GND E20
GND E21

VDD

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TITLE: SCHEMATIC

10/20 AMP INTEGRATED HOT SWAP CONTROLLER

IC NO.LTC4233/LTC4234

DEMO CIRCUIT 2116A

REV. 1

APPROVALS

PCB DES.	M.HAWKINS
APP ENG.	R. SMITH

SIZE N/A

DATE: 05/21/2013

SCALE = NONE

SHEET 1 OF 1

* **ASSEMBLY OPTIONS**

ASS'Y	U1	CURRENT
-A	LTC4234	20A
-B	LTC4233	10A

NOTE:
1. ALL RESISTORS ARE 0603 PACKAGE, 1% U.O.N.

dc2116afa

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