



3.3V, 3.2Gbps DUAL, DIFFERENTIAL 2:1 LVDS MULTIPLEXER with INTERNAL TERMINATION

Precision Edge®
SY89543L

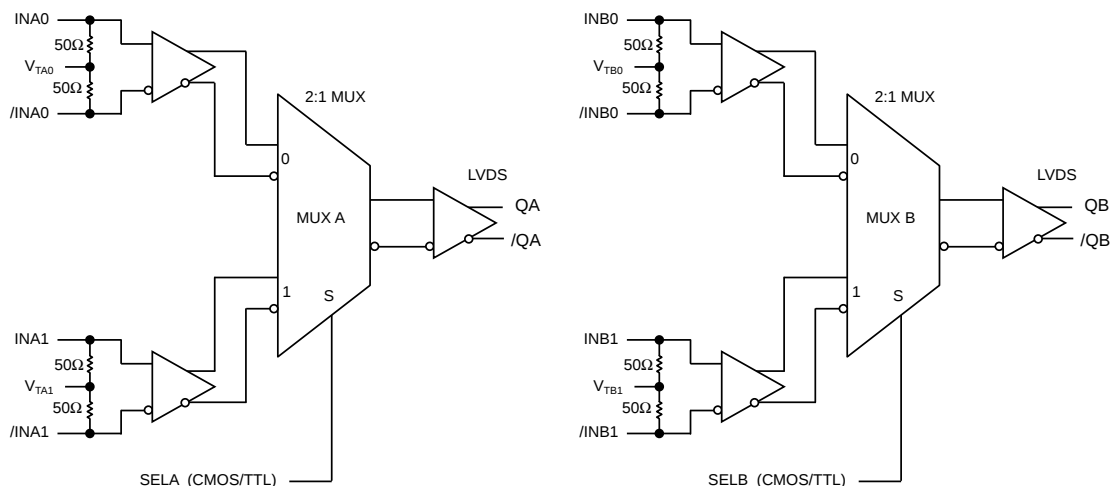
FEATURES

- Dual 2:1 multiplexer
- Guaranteed AC performance over temp and voltage:
 - DC-to > 3.2Gbps data rate throughput
 - < 510ps In-to-Out t_{pd}
 - < 150ps t_r/t_f
- Ultra-low jitter design:
 - < 1ps_{RMS} random jitter
 - < 10ps_{PP} deterministic jitter
 - < 10ps_{PP} total jitter (clock)
 - < 0.7ps_{RMS} crosstalk-induced jitter
- Unique input isolation design minimizes crosstalk
- Internal input termination
- Unique input termination and V_T pin accepts DC-coupled and AC-coupled inputs (LVDS, LVPECL, CML)
- 350mV LVDS output swing
- CMOS/TTL compatible MUX select
- Power supply 3.3V +10%
- -40 to +85°C temperature range
- Available in 32-pin (5mm x 5mm) MLF® package

APPLICATIONS

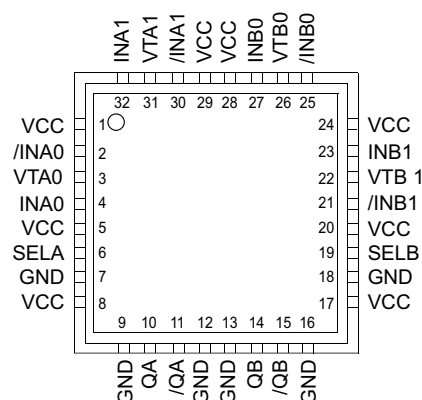
- Redundant clock/data switchover
- SONET/SDH multi-channel select applications
- Fiber Channel applications
- GigE applications

FUNCTIONAL BLOCK DIAGRAM



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MicroLeadFrame and MLF are registered trademarks of Amkor Technology, Inc.

PACKAGE/ORDERING INFORMATION



32-Pin MLF®

Ordering Information⁽¹⁾

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89543LMI	MLF-32	Industrial	SY89543L	Sn-Pb
SY89543LMITR ⁽²⁾	MLF-32	Industrial	SY89543L	Sn-Pb
SY89543LMG ⁽³⁾	MLF-32	Industrial	SY89543L with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY89543LMGTR ^(2, 3)	MLF-32	Industrial	SY89543L with Pb-Free bar-line indicator	Pb-Free NiPdAu

Notes:

1. Contact factory for die availability. Dice are guaranteed at $T_A = 25^\circ\text{C}$, DC electricals only.
2. Tape and Reel.
3. Recommended for new designs.

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
4, 2, 32, 30, 27, 25, 23, 21	INA0, /INA0, INA1, /INA1, INB0, /INB0, INB1, /INB1	Differential Inputs: These input pairs are the differential signal inputs to the device. Inputs accept AC- or DC-coupled signals as small as 100mV. Each pin of a pair internally terminates to a V_T pin through 50Ω. Note that these inputs will default to an indeterminate state if left open. Unused differential input pairs can be terminated by connecting one input to V_{CC} and the complementary input to GND through a 1kΩ resistor. The V_T pin is to be left open in this configuration. Please refer to the "Input Interface Applications" section for more details.
3, 31, 26, 22	VTA0, VTA1, VTB0, VTB1	Input Termination Center-Tap: Each side of the differential input pair, terminates to a V_T pin. The V_{TA0} , V_{TA1} , V_{TB0} , V_{TB1} pins provide a center-tap to a termination network for maximum interface flexibility. See "Input Interface Applications" section for more details.
6, 19	SELA, SELB	These single-ended TTL/CMOS compatible inputs select the inputs to the multiplexers. Note that these inputs are internally connected to a 25kΩ pull-up resistor and will default to logic HIGH state if left open.
1, 5, 8, 17, 20, 24, 28, 29	VCC	Positive Power Supply: Bypass with 0.1μF 0.01μF low ESR capacitors. The 0.01μF capacitor should be as close to V_{CC} pin as possible.
10, 11, 14, 15	QA, /QA, QB, /QB	Differential Outputs: This differential LVDS output pair provides a copy of the selected input. It is a logic function of the INA0, INA1, INB0, INB1 and SELA and SELB inputs. Please refer to the "Truth Table" for details. Unused output pairs must be terminated with 100Ω across the differential pair.
7, 9, 12, 13, 16, 18	GND, Exposed pad	Ground: Ground pin and exposed pad must be connected to the same ground plane.

Absolute Maximum Ratings⁽¹⁾

Supply Voltage (V_{CC})	 -0.5V to +4.0V
Input Voltage (V_{IN})	 -0.5V to V_{CC}
Termination Current ⁽³⁾	
Source or sink current on V_T	 ± 100 mA
Input Current	
Source or sink current on IN, /IN	 ± 50 mA
Lead Temperature (soldering, 20 sec.)	 +260°C
Storage Temperature (T_S)	 -65°C to +150°C

Operating Ratings⁽²⁾

Supply Voltage (V_{CC})	 3.0V to 3.6V
Ambient Temperature (T_A)	 -40°C to +85°C
Package Thermal Resistance ⁽⁴⁾	
MLF® (θ_{JA})	
Still-Air	 35°C/W
500lfpm	 28°C/W
MLF® (Ψ_{JB})	
Junction-to-Board	 20°C/W

DC ELECTRICAL CHARACTERISTICS⁽⁵⁾

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$; Unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply		3.0	3.3	3.6	V
I_{CC}	Power Supply Current	No Load, Max. V_{CC} ⁽⁶⁾		66	88	mA
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		80	100	120	Ω
R_{IN}	Input Resistance (IN-to- V_T , /IN-to- V_T)		40	50	60	Ω
V_{IH}	Input High Voltage (IN, /IN)		1.2		V_{CC}	V
V_{IL}	Input Low Voltage (IN, /IN)		0		$V_{IH}-0.1$	V
V_{IN}	Input Voltage Swing (IN, /IN)	Notes 7	0.1		V_{CC}	V
V_{DIFF_IN}	Differential Input Voltage Swing IN - /IN	Notes 7	0.2			V
IN-to- V_T	Voltage from Input to V_T				1.8	V

Notes:

1. Permanent device damage may occur if "Absolute Maximum Ratings" are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to "Absolute Maximum Ratings" conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Due to the limited drive capability use for input of the same package only.
4. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. Ψ_{JB} uses 4-layer θ_{JA} in still air unless otherwise stated.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
6. Includes current through internal 50 Ω pull-ups.
7. See "Operating Characteristics" section for V_{IN} and V_{DIFF_IN} definition.

LVDS OUTPUTS DC ELECTRICAL CHARACTERISTICS⁽⁹⁾

$V_{CC} = 3.3V \pm 10\%$; $T_A = -40^\circ C$ to $+85^\circ C$; $R_L = 100\Omega$ across Q and /Q, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage (Q, /Q)	See Figure 5a			1.475	V
V_{OL}	Output LOW Voltage (Q, /Q)	See Figure 5a	0.925			V
V_{OUT}	Output Voltage Swing (Q, /Q)	See Figures 1a, 5a	250	350		mV
$V_{DIFF-OUT}$	Differential Output Voltage Swing Q - /Q	See Figure 1b	500	700		mV
V_{OCM}	Output Common Mode Voltage (Q, /Q)	See Figure 5b	1.125		1.275	V
ΔV_{OCM}	Change in Common Mode Voltage (Q, /Q)	See Figure 5b	-50		+50	mV

LVTTTL/CMOS DC ELECTRICAL CHARACTERISTICS⁽⁹⁾

$V_{CC} = 3.3V \pm 10\%$; $T_A = -40^\circ C$ to $+85^\circ C$; unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0		V_{CC}	V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current				40	μA
I_{IL}	Input LOW Current				-300	μA

Note:

9. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC ELECTRICAL CHARACTERISTICS⁽¹⁰⁾

$V_{CC} = 3.3V \pm 10\%$; $T_A = -40^\circ C$ to $+85^\circ C$; $R_L = 100\Omega$ across Q and /Q, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency	NRZ Data	3.2			Gbps
		$V_{OUT} > 200mV$ Clock		3		GHz
t_{PD}	Differential Propagation Delay	IN-to-Q	310	410	510	ps
		SEL-to-Q	250	450	650	ps
t_{SKEW}	Input-to-Input Skew	Note 11			25	ps
	Channel-to-Channel Skew	Note 12		10	30	ps
	Part-to-Part Skew	Note 13			200	ps
t_{JITTER}	Data Random Jitter (RJ)	Note 14			1	ps _{RMS}
	Deterministic Jitter (DJ)	Note 15			10	ps _{PP}
	Clock Total Jitter (TJ)	Note 16			10	ps _{PP}
	Cycle-to-Cycle Jitter	Note 17			1	ps _{RMS}
	Crosstalk-Induced Jitter	Note 18			0.7	ps _{RMS}
t_R, t_F	Output Rise / Fall Time (20% to 80%)	At full output swing	40	80	150	ps

Notes:

10. Measured with 100mV input swing. See "Timing Diagrams" section for definition of parameters. High-frequency AC-parameters are guaranteed by design and characterization.
11. Input-to-input skew is the difference in time from an input-to-output in comparison to any other input-to-output. In addition, the input-to-input skew does not include the output skew.
12. Channel-to-channel skew is measured between two different outputs under identical conditions.
13. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs. Total skew is calculated as the RMS (Root Mean Square) of the input skew and output skew.
14. RJ is measured with a K28.7 comma detect character pattern, measured at 1.25Gbps and 3.2Gbps.
15. DJ is measured at 1.25Gbps and 3.2Gbps, with both K28.5 and 2²³-1 PRBS pattern.
16. Total jitter definition: with an ideal clock input of frequency $\leq f_{MAX}$, no more than one output edge in 10¹² output edges will deviate by more than the specified peak-to-peak jitter value.
17. Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, $T_n - T_{n-1}$ where T is the time between rising edges of the output signal.
18. Crosstalk is measured at the output while applying two similar frequencies to adjacent inputs that are asynchronous with respect to each other at the inputs.

SINGLE-ENDED AND DIFFERENTIAL SWINGS

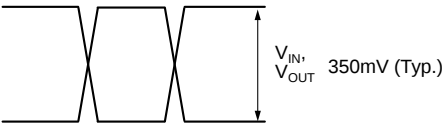


Figure 1a. Single-Ended Voltage Swing

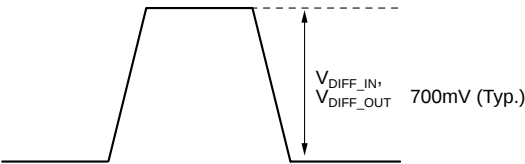


Figure 1b. Differential Voltage Swing

TIMING DIAGRAM

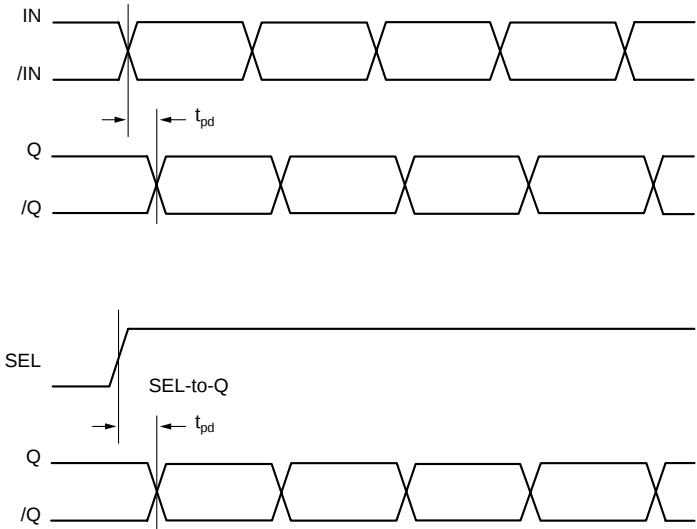


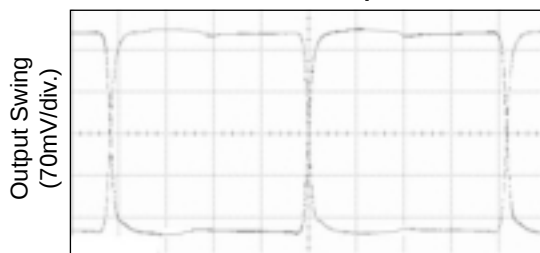
Figure 2. Timing Diagram

TRUTH TABLE

IN0	IN1	SEL	Q	/Q
0	X	0	0	1
1	X	0	1	0
X	0	1	0	1
X	1	1	1	0

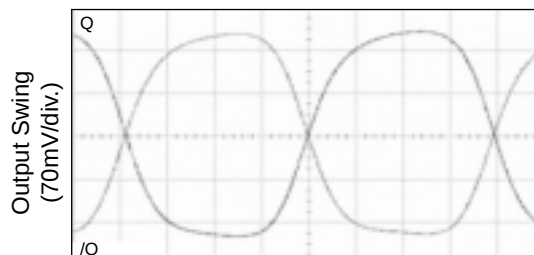
FUNCTIONAL CHARACTERISTICS

200MHz Output



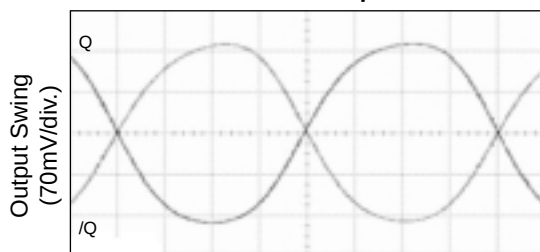
TIME (600ps/div.)

1.6GHz Output



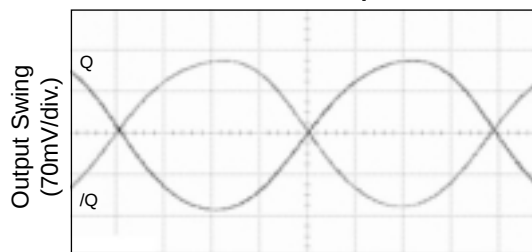
TIME (80ps/div.)

2.5GHz Output

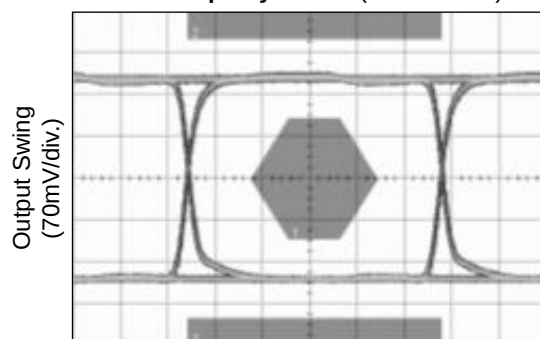


TIME (50ps/div.)

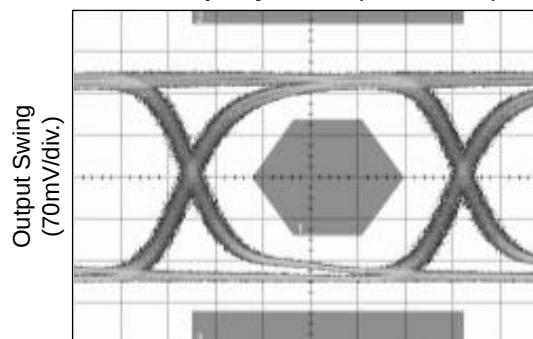
3.2GHz Output



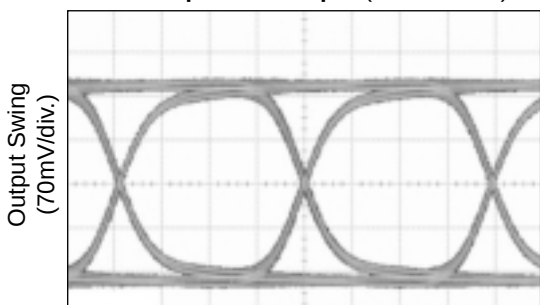
TIME (40ps/div.)

622Mbps Eye Mask ($2^{23}-1$ PRBS)

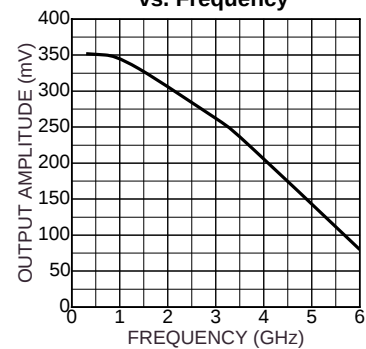
TIME (300ps/div.)

2.5Gbps Eye Mask ($2^{23}-1$ PRBS)

TIME (70ps/div.)

3.2Gbps Data Output ($2^{23}-1$ PRBS)

TIME (80ps/div.)

Output Amplitude
vs. Frequency

INPUT AND OUTPUT STAGE INTERNAL TERMINATION

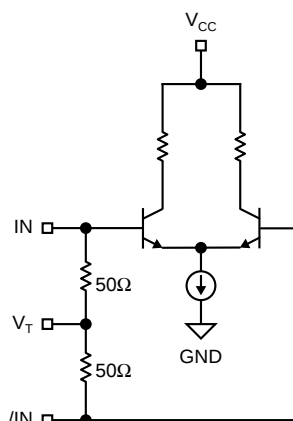


Figure 3. Simplified Differential Input Stage

INPUT INTERFACE APPLICATIONS

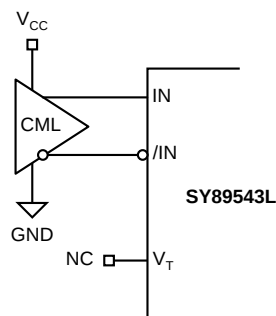


Figure 4a. CML Interface (DC-Coupled)

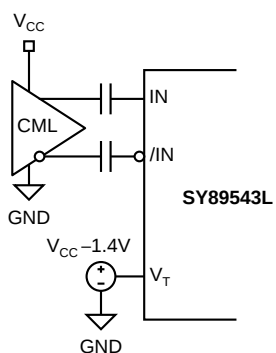


Figure 4b. CML Interface (AC-Coupled)

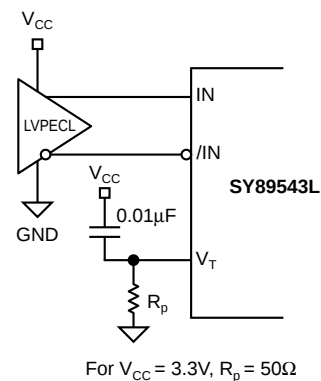


Figure 4c. LVPECL Interface (DC-Coupled)

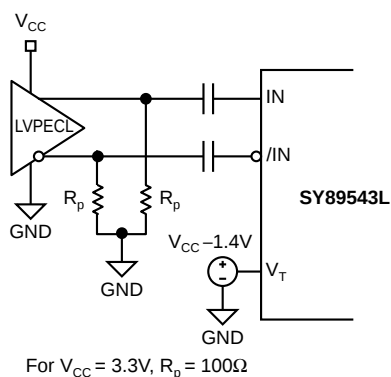


Figure 4d. LVPECL Interface (AC-Coupled)

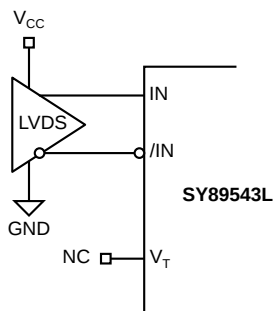


Figure 4e. LVDS Interface

OUTPUT INTERFACE APPLICATIONS

LVDS specifies a small swing of 350mV typical, on a nominal 1.25V common mode above ground. The common mode voltage has tight limits to permit large variations in

ground between an LVDS driver and receiver. Also, change in common mode voltage, as a function of data input, is kept to a minimum, to keep EMI low.

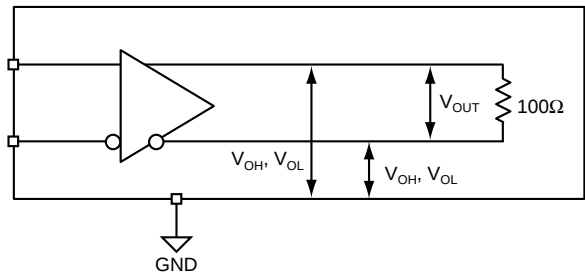


Figure 5a. LVDS Differential Measurement

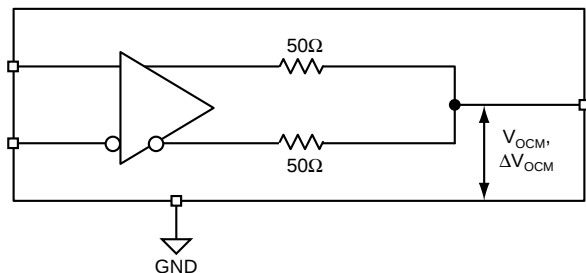


Figure 5b. LVDS Common Mode Measurement

RELATED MICREL PRODUCTS AND SUPPORT DOCUMENTATION

Part Number	Function	Data Sheet Link
SY89542U	2.5V, 3.2Gbps Dual, Differential 2:1 LVDS Multiplexer with Internal Input Termination	http://www.micrel.com/_PDF/HBW/sy89542u.pdf
SY89544U	2.5V, 3.2Gbps 4:1 LVDS Multiplexer with Internal Input Termination	http://www.micrel.com/_PDF/HBW/sy89544u.pdf
SY89545L	3.3V, 3.2Gbps, Differential 4:1 LVDS Multiplexer with Internal Input Termination	http://www.micrel.com/_PDF/HBW/sy89545l.pdf
SY89546U	2.5V, 3.2Gbps, Differential 4:1 LVDS Multiplexer with 1:2 Fanout and Internal Input Termination	http://www.micrel.com/_PDF/HBW/sy89546u.pdf
SY89547L	3.3V, 3.2Gbps, Differential 4:1 LVDS Multiplexer with 1:2 Fanout and Internal Input Termination	http://www.micrel.com/_PDF/HBW/sy89547l.pdf
	MLF® Application Note	www.amkor.com/products/notes_papers/LF_AppNote_0902.pdf
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

Technical drawing of a square microstrip antenna. The drawing shows a square patch with a central square hole. Dimensions and labels include:

- Top edge: 0.25 ± 0.05 32X (width of the top microstrip feed line)
- Top edge: 0.50 BSC (width of the top microstrip feed line)
- Top edge: 32 (width of the top microstrip feed line)
- Left edge: 0.20 MIN. (width of the left microstrip feed line)
- Left edge: 3.10 ± 0.10 (height of the left microstrip feed line)
- Right edge: 1 (width of the right microstrip feed line)
- Right edge: 2 (width of the right microstrip feed line)
- Bottom edge: 0.40 ± 0.05 4X (width of the bottom microstrip feed line)
- Bottom edge: 3.10 ± 0.10 (height of the bottom microstrip feed line)
- Pin #1 ID R0.20 (radius of the top-right corner)

The diagram illustrates a cross-section of a power module assembly. At the top, a **Package** is shown with a central **Die** and an **EP- Exposed Pad**. Below the package is a **CompSide Island** containing several circular features. The assembly is mounted on a **Heavy Copper Plane**, which is connected to V_{EE} . Arrows indicate **Heat Dissipation** from the package and the compside island into the heavy copper plane.

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

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