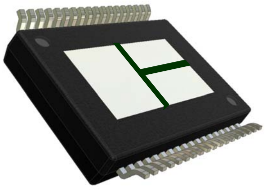
# VNH5050A-E

## Automotive fully integrated H-bridge motor driver

## Features

| Type | $R_{DS(on)}$ | $I_{out}$ | $V_{ccmax}$ |
|---|---|---|---|
| VNH5050A-E | 50 mΩ max<br>(per leg) | 30 A | 41 V |

- Output current: 30 A
- 3 V CMOS compatible inputs
- Undervoltage and overvoltage shutdown
- Overvoltage clamp
- Thermal shutdown
- Cross-conduction protection
- Current and power limitation
- Very low standby power consumption
- PWM operation up to 20 KHz
- Protection against loss of ground and loss of $V_{CC}$
- Current sense output proportional to motor current
- Output protected against short to ground and short to $V_{CC}$
- Package: ECOPACK®



PowerSSO-36 TP

## Description

The VNH5050A-E is a full bridge motor driver intended for a wide range of automotive applications. The device incorporates a dual monolithic high-side driver and two low-side switches. All switches are designed using STMicroelectronics® well known and proven proprietary VIPower® M0 technology that allows to efficiently integrate on the same die a true Power MOSFET with an intelligent signal/protection circuitry. The three dies are assembled in a PowerSSO-36 TP package on electrically isolated lead frames. This package, specifically designed for the harsh automotive environment offers improved thermal performance thanks to exposed die pads. Moreover, its fully symmetrical mechanical design allows superior manufacturability at board level. The input signals $IN_A$ and $IN_B$ can directly interface to the microcontroller to select the motor direction and the brake condition. The $DIAG_A/EN_A$ or $DIAG_B/EN_B$, when connected to an external pull-up resistor, enables one leg of the bridge. Each $DIAG_A/EN_A$ provides a digital diagnostic feedback signal as well. The normal operating condition is explained in the truth table. The CS pin allows monitoring the motor current by delivering a current proportional to its value when CS_DIS pin is driven low or left open. When CS_DIS is driven high, CS pin is in high impedance condition. The PWM, up to 20 KHz, allows to control the speed of the motor in all possible conditions. In all cases, a low level state on the PWM pin turns off both the $LS_A$ and $LS_B$ switches.

**Table 1. Device summary**

| Package | Order codes | |
|---|---|---|
| | Tube | Tape and reel |
| PowerSSO-36 TP | VNH5050A-E | VNH5050ATR-E |

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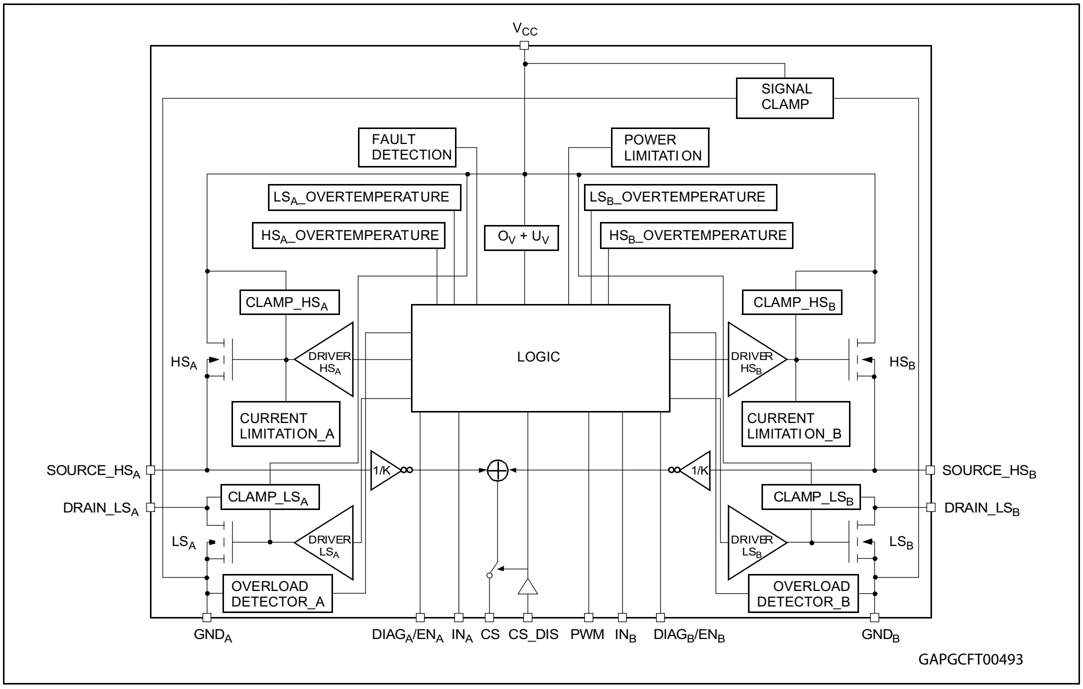
# 1 Block diagram and pin description

## Figure 1. Block diagram



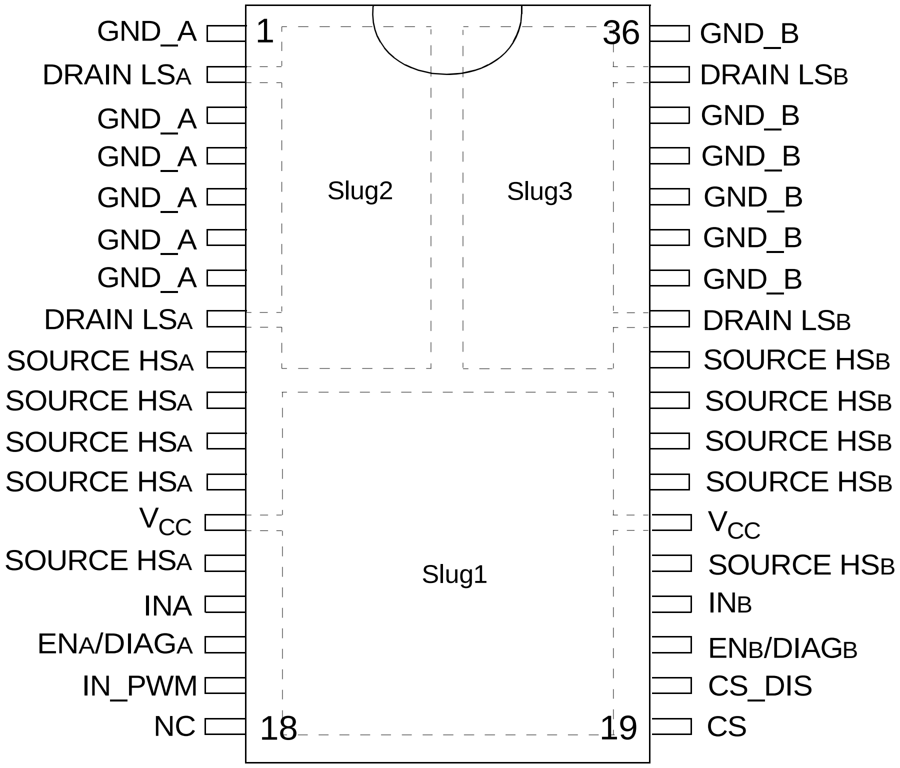
## Table 2. Block description

| Name | Description |
|---|---|
| Logic control | Allows the turn-on and the turn-off of the high-side and the low-side switches according to the truth table. |
| Undervoltage/overvoltage | Shuts down the device for battery voltage outside the range (4,5...24V). |
| High-side and low-side clamp voltage | Protect the high-side and the low-side switches from high voltage on the battery line. |
| High-side and low-side driver | Drive the gate of the concerned switch to allow a proper $R_{DS(on)}$ for the leg of the bridge. |
| Current limitation | Limits the motor current in case of short circuit. |
| High-side and low-side overtemperature protection | In case of short-circuit with the increase of the junction temperature, it shuts down the concerned driver to prevent degradation and to protect the die. |
| Low-side overload detector | Detects when low-side current exceeds shutdown current and latches off the concerned low-side. |
| Fault detection | Signalizes an abnormal condition of the switch (output shorted to ground or output shorted to battery) by pulling down the concerned ENx/DIAGx pin. |
| Power limitation | Limits the power dissipation of the high-side driver inside safe range in case of short to ground condition. |

### Table 3. Suggested connections for unused and not connected pins

| Connection / pin | Current sense | N.C. | SOURCE_HSx | DRAIN_LSx | INPUTx, PWM DIAGx/ENx CS_DIS |
|---|---|---|---|---|---|
| Floating | Not allowed | X | X | X | X |
| To ground | Through 1 kΩ resistor | X | Not allowed | X | Through 10 kΩ resistor |

### Figure 2. Configuration diagram (top view)



### Table 4. Pin definitions and functions

| Pin N° | Symbol | Function |
|---|---|---|
| 13, 24 | $V_{CC}$, Heat slug1 | Drain of high-side switches and power supply voltage. |
| 18 | NC | Not connected. |
| 15 | INA | Clockwise input. |
| 16 | ENA/DIAGA | Status of high-side and low-side switches A;<br>Open drain output. |
| 17 | IN_PWM | PWM input. |
| 19 | CS | Output of current sense. |

**Table 4. Pin definitions and functions (continued)**

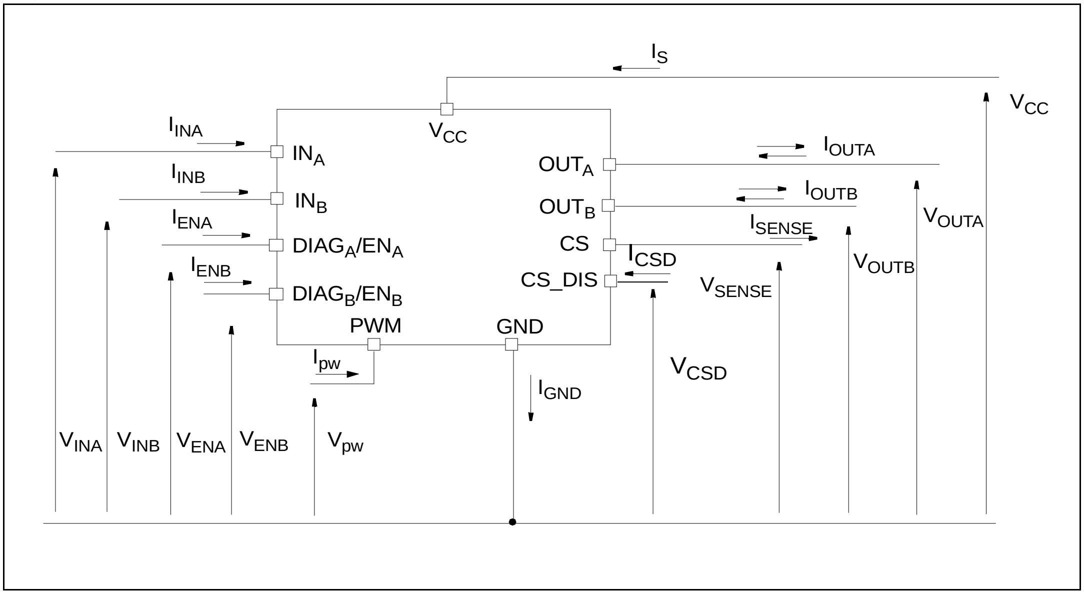
| Pin N° | Symbol | Function |
|---|---|---|
| 20 | CS_DIS | Active high CMOS compatible pin to disable current sense pin. |
| 21 | ENB/DIAGB | Status of high-side and low-side switches B;<br>Open drain output. |
| 22 | INB | Counter clockwise input. |
| 23, 25, 26, 27, 28, 29, 35 | OUTB, Heat Slug3 | Source of high-side switch B / drain of low-side switch B. |
| 30, 31, 32, 33, 34,36 | GND_B | Source of low-side switch B. |
| 2, 8, 9, 10, 11, 12, 14 | OUT$_A$, Heat Slug2 | Source of high-side switch A / drain of low-side switch A. |
| 1, 3, 4, 5, 6, 7 | GND_A | Source of low-side switch A. |

**Table 5. Pin functions description**

| Name | Description |
|---|---|
| V$_{CC}$ | Battery connection. |
| GND | Power ground. |
| OUT$_A$<br>OUT$_B$ | Power connections to the motor. |
| IN$_A$<br>IN$_B$ | Voltage controlled input pins with hysteresis, CMOS compatible. These two pins control the state of the bridge in normal operation according to the truth table (brake to V$_{CC}$, Brake to GND, clockwise and counterclockwise). |
| PWM | Voltage controlled input pin with hysteresis, CMOS compatible.Gates of low-side FETS get modulated by the PWM signal during their on phase allowing speed control of the motor. |
| EN$_A$/DIAG$_A$<br>EN$_B$/DIAG$_B$ | Open drain bidirectional logic pins.These pins must be connected to an external pull up resistor. When externally pulled low, they disable half-bridge A or B. In case of fault detection (thermal shutdown of a high-side FET or excessive on-state voltage drop across a low-side FET), these pins are pulled low by the device (see truth table in fault condition). |
| CS | Analog current sense output. This output delivers a current proportional to the motor current if CS_DIS is low or left open. The information can be read back as an analog voltage across an external resistor. |
| CS_DIS | Active high CMOS compatible pin to disable the current sense pin. |

# 2 Electrical specifications

Figure 3. Current and voltage conventions



## 2.1 Absolute maximum ratings

Table 6. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | + 41 | V |
| $I_{max}$ | DC output current | Internally limited | A |
| $I_R$ | Reverse output current (continuous)(1) | 25 | A |
| $I_{IN}$ | Input current ($IN_A$ and $IN_B$ pins) | +/- 10 | mA |
| $I_{EN}$ | Enable input current ($DIAG_A/EN_A$ and $DIAG_B/EN_B$ pins) | +/- 10 | mA |
| $I_{pw}$ | PWM Input current | +/- 10 | mA |
| $I_{CS\_DIS}$ | CS_DIS input current | +/- 10 | mA |
| $V_{CS}$ | Current sense maximum voltage | $V_{CC}$-41/+$V_{CC}$ | V |
| $V_{ESD}$ | Electrostatic discharge<br>(Human body model: R = 1.5 kΩ, C = 100 pF) | 2 | kV |
| $T_c$ | Junction operating temperature | -40 to 150 | °C |
| $T_{STG}$ | Storage temperature | -55 to 150 | °C |
| $I_{GND}$ | DC reverse ground pin current | 200 | mA |

1. Based on the internal wires capability.

## 2.2 Thermal data

Table 7. Thermal data

| Symbol | Parameter | | Max. value | Unit |
|---|---|---|---|---|
| $R_{thj\text{-}case}$ | Thermal resistance junction-case (per leg) | HSD | 3.7 | °C/W |
| | | LSD | 3.9 | °C/W |
| $R_{thj\text{-}amb}$ | Thermal resistance junction-ambient | | See *Figure 17* | °C/W |

## 2.3 Electrical characteristics

$V_{CC}$ = 9 V up to 18 V; -40 °C < $T_j$ < 150 °C, unless otherwise specified.

**Table 8. Power section**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Operating supply voltage | | 5.5 | | 18 | V |
| $I_S$ | Supply current | Off-state with all fault cleared and ENx = 0 (standby)<br>$IN_A$ = $IN_B$ = PWM = 0;<br>$T_j$ = 25 °C; $V_{CC}$ = 13 V | | 3 | 6 | µA |
| | | Off-state with all fault cleared and ENx = 0 (standby)<br>$V_{CC}$ = 13 V;<br>$IN_A$ = $IN_B$ = PWM = 0;<br>$T_j$ = -40 °C to 150 °C | | | 10 | µA |
| | | Off-state (no standby)<br>$IN_A$ = $IN_B$ = PWM = 0;<br>ENx = 5 V;<br>$T_j$ = -40 °C to 150 °C | | | 5 | mA |
| | | On-state:<br>$IN_A$ or $IN_B$ = 5V; no PWM | | 3 | 6 | mA |
| | | On-state:<br>$IN_A$ or $IN_B$ = 5 V;<br>PWM = 20 kHz | | | 8 | mA |
| $R_{ONHS}$ | Static high-side resistance | $I_{OUT}$ = 8.5 A; $T_j$ = -40 °C | | 17 | | mΩ |
| | | $_{OUT}$ = 8.5 A; $T_j$ = 25 °C | | 26 | | mΩ |
| | | $I_{OUT}$ = 8.5 A; $T_j$ = 150 °C | | 52 | | mΩ |
| | | $I_{OUT}$ = 8.5 A;<br>$T_j$ = - 40 °C to 150 °C | | | 60 | mΩ |
| $R_{ONLS}$ | Static low-side resistance | $I_{OUT}$ = 8.5 A; $T_j$ = 25 °C | | 20 | | mΩ |
| | | $I_{OUT}$ = 8.5 A;<br>$T_j$ = - 40 °C to 150 °C | | | 40 | mΩ |
| $V_f$ | High-side free-wheeling diode forward voltage | $I_{OUT}$ = -8.5 A; $T_j$ = 150 °C | | 0.7 | 0.9 | V |
| $I_{L(off)}$ | High-side off-state output current (per channel) | $T_j$ = 25 °C; $V_{CC}$ = 13V;<br>$V_{OUTX}$ = $EN_X$ = 0 V | 0 | | 3 | µA |
| | | $T_j$ = 125°C; $V_{CC}$ = 13V;<br>$V_{OUTX}$ = $EN_X$ = 0 V | 0 | | 5 | µA |
| $I_{RM}$ | Dynamic cross-conduction current | $I_{OUT}$ = 8.5 A (see *Figure 7*) | | 1 | | A |

**Table 9. Logic inputs ($IN_A$, $IN_B$, $EN_A$, $EN_B$, PWM, CS_DIS)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input low level voltage | Normal operation ($DIAG_X/EN_X$ pin acts as an input pin) | | | 0.9 | V |
| $V_{IH}$ | Input high level voltage | Normal operation ($DIAG_X/EN_X$ pin acts as an input pin) | 2.1 | | | V |
| $V_{IHYST}$ | Input hysteresis voltage | Normal operation ($DIAG_X/EN_X$ pin acts as an input pin) | 0.15 | | | V |
| $V_{ICL}$ | Input clamp voltage | $I_{IN}$ = 1 mA | 5.5 | 6.3 | 7.5 | V |
| | | $I_{IN}$ = -1 mA | -1.0 | -0.7 | -0.3 | V |
| $I_{INL}$ | Input current | $V_{IN}$ = 0.9 V | 1 | | | µA |
| $I_{INH}$ | Input current | $V_{IN}$ = 2.1 V | | | 10 | µA |
| $V_{DIAG}$ | Enable output low level voltage | Fault operation ($DIAG_X/EN_X$ pin acts as an output pin); $I_{EN}$ = 1 mA | | | 0.4 | V |

**Table 10. Switching ($V_{CC}$ = 13 V, $R_{LOAD}$ = 1.5 Ω)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| f | PWM frequency | | 0 | | 20 | kHz |
| $t_{d(on)}$ | Turn-on delay time | Input rise time < 1µs<br>(see *Figure 6*) | | | 250 | µs |
| $t_{d(off)}$ | Turn-off delay time | Input rise time < 1µs<br>(see *Figure 6*) | | | 250 | µs |
| $t_r$ | Rise time | See *Figure 5* | | 1 | 2 | µs |
| $t_f$ | Fall time | See *Figure 5* | | 1 | 2 | µs |
| $t_{DEL}$ | Delay time during change of operating mode | See *Figure 4* | 200 | 400 | 1600 | µs |
| $t_{rr}$ | High-side free wheeling diode reverse recovery time | See *Figure 7* | | 100 | | ns |

**Table 11. Protections and diagnostics**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{USD}$ | Undervoltage shutdown | | | 3 | 5 | V |
| $V_{USDhyst}$ | Undervoltage shutdown hysteresis | | | 0.5 | | V |
| $V_{OV}$ | $V_{CC}$ overvoltage shutdown | | 24 | 27 | 30 | V |
| $I_{LIM\_H}$ | High-side current limitation | | 30 | 42 | 60 | A |

**Table 11. Protections and diagnostics (continued)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD\_LS}$ | Shutdown LS current | | 30 | 50 | 70 | A |
| $V_{CLP}$ | Total clamp voltage ($V_{CC}$ to GND) | $I_{OUT}$ = 8.5 A | 41 | 46 | 52 | V |
| $V_{CLPH}$ | High-side clamp voltage ($V_{CC}$ to $OUT_A$ =0 or $OUT_B$ =0) | $I_{OUT}$ = 8.5 A | 41 | 46 | 52 | V |
| $T_{SD\_LS}$ | Time to shutdown for the low-side | | | 10 | | µs |
| $V_{CLPLS}$ | Low-side clamp voltage ($OUT_A$ = $V_{CC}$ or $OUT_B$ = $V_{CC}$ to GND) | $I_{OUT}$ = 8.5 A | 25 | 28 | 31 | V |
| $T_{TSD}$(1) | Thermal shutdown temperature | $V_{IN}$ = 2.1 V | 150 | 175 | 200 | °C |
| $T_{TR}$(2) | Thermal reset temperature | | 135 | | | °C |
| $T_{HYST}$(2) | Thermal hysteresis ($T_{SD}$-$T_R$) | | | 16 | | °C |
| $T_{TSD\_LS}$ | Low-side thermal shutdown temperature | $V_{IN}$ = 0 V | 150 | 175 | 200 | °C |

1. $T_{TSD}$ is the minimum threshold temperature between HS and LS
2. Valid for both HSD and LSD.

**Table 12. Current sense (9 V < $V_{CC}$ < 18 V)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $K_1$ | $I_{OUT}/I_{SENSE}$ | $I_{OUT}$ = 5 A; $V_{SENSE}$ = 0.8 V; $V_{CSD}$ = 0 V; $T_j$ = - 40 °C to 150 °C | 4350 | 5100 | 6270 | |
| $K_2$ | $I_{OUT}/I_{SENSE}$ | $I_{OUT}$ = 10 A; $V_{SENSE}$ = 1.6 V; $V_{CSD}$ = 0 V; $T_j$ = - 40 °C to 150 °C | 4350 | 5030 | 5870 | |
| $K_3$ | $I_{OUT}/I_{SENSE}$ | $I_{OUT}$ = 25 A; $V_{SENSE}$ = 4 V; $V_{CSD}$ = 0 V; $T_j$ = - 40 °C to 150 °C | 4100 | 4930 | 5490 | |
| $dK_1/K_1$(1) | Analog sense current drift | $I_{OUT}$ = 5 A; $V_{SENSE}$ = 0.8 V; $V_{CSD}$ = 0 V; $T_j$ = - 40 °C to 150°C | -14 | | 14 | % |
| $dK_2/K_2$(1) | Analog sense current drift | $I_{OUT}$ = 10 A; $V_{SENSE}$ = 1.6 V; $V_{CSD}$ = 0 V; $T_j$ = - 40 °C to 150°C | -13 | | 13 | % |
| $dK_3/K_3$(1) | Analog sense current drift | $I_{OUT}$ = 25 A; $V_{SENSE}$ = 4 V; $V_{CSD}$ = 0 V; $T_j$ = - 40 °C to 150 °C | -13 | | 13 | % |

### Table 12. Current sense (9 V < $V_{CC}$ < 18 V) (continued)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{SENSE}$ | Max analog sense output voltage | $I_{OUT}$ = 10 A; $V_{CSD}$ = 0 V;<br>$R_{SENSE}$ = 800 Ω | 5 | | | V |
| $I_{SENSETYP\_500}$ | Typical analog sense | $I_{OUT}$ = 500 mA; $V_{CC}$ = 13 V;<br>$T_j$ = - 40 °C | | 87 | | µA |
| | | $I_{OUT}$ = 500 mA; $V_{CC}$ = 13 V;<br>$T_j$ = 25 °C | | 91 | | µA |
| | | $I_{OUT}$ = 500 mA; $V_{CC}$ = 13 V;<br>$T_j$ = 150 °C | | 100 | | µA |
| $I_{SENSE0}$ | Analog sense leakage current | $I_{OUT}$ = 0 A; $V_{SENSE}$ = 0 V;<br>$V_{CSD}$ = 5 V; $V_{IN}$ = 0 V;<br>$T_j$ = - 40 °C to 150°C | 0 | | 5 | µA |
| | | $V_{CSD}$ = 0 V; $V_{IN}$ = 5 V;<br>$T_j$ = - 40 °C to 150 °C | 0 | | 180 | µA |
| | | $V_{CSD}$ = 5 V; $V_{IN}$ = 5 V;<br>$I_{OUT}$ = 8.5 A | 0 | | 5 | µA |
| $t_{DSENSEH}$ | Delay response time from falling edge of CS_DIS pin | $V_{IN}$ = 5 V; $V_{SENSE}$ < 4 V,<br>$I_{OUT}$ = 8.5 A;<br>$I_{SENSE}$ = 90 % of $I_{SENSEmax}$<br>(see *Figure 8*) | | | 50 | µs |
| $t_{DSENSEL}$ | Delay response time from rising edge of CS_DIS pin | $V_{IN}$ = 5 V; $V_{SENSE}$ < 4 V;<br>$I_{OUT}$ = 8.5 A;<br>$I_{SENSE}$ = 10 % of $I_{SENSEmax}$<br>(see *Figure 8*) | | | 20 | µs |

1. Analog sense current drift is deviation of factor K for a given device over (-40°C to 150°C and 9 V < $V_{CC}$ < 18 V) with respect to its value measured at $T_j$ = 25 °C, $V_{CC}$ = 13 V.

**Figure 4. Definition of the delay times measurement**

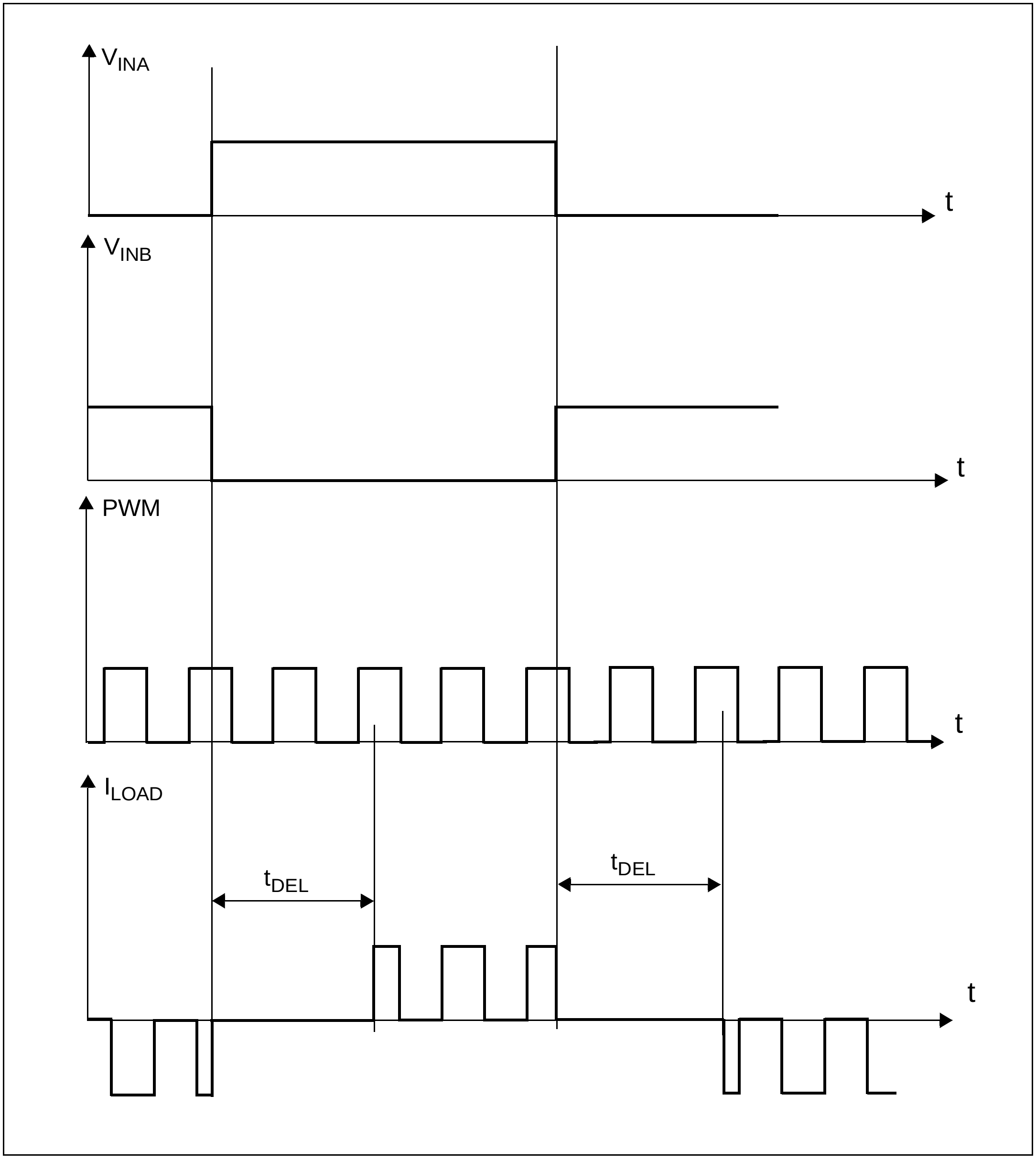


Figure 5. Definition of the low-side switching times

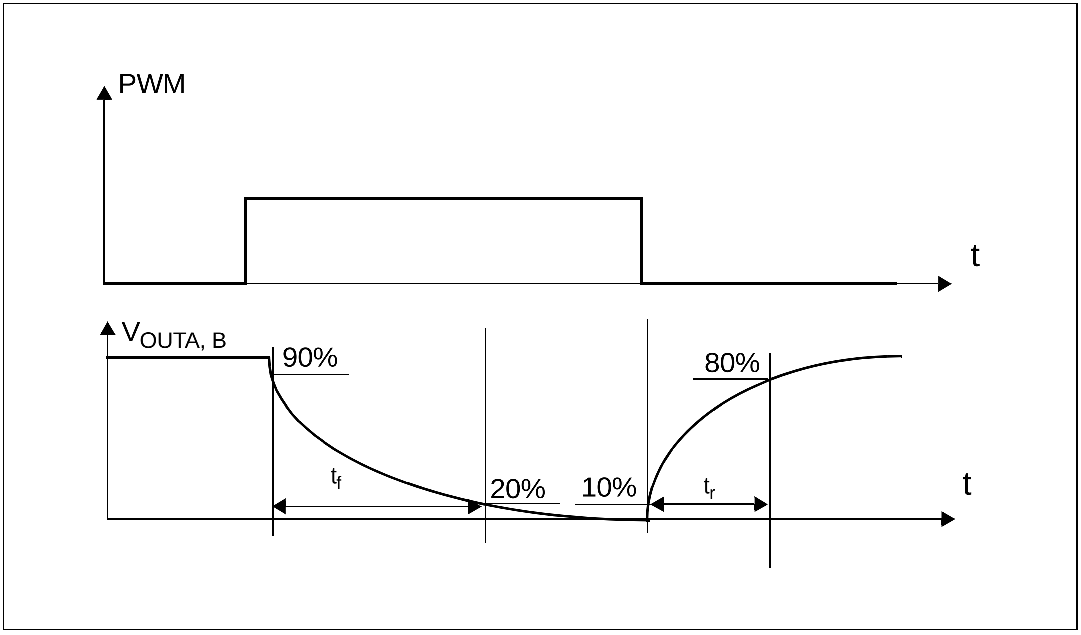


Figure 6. Definition of the high-side switching times

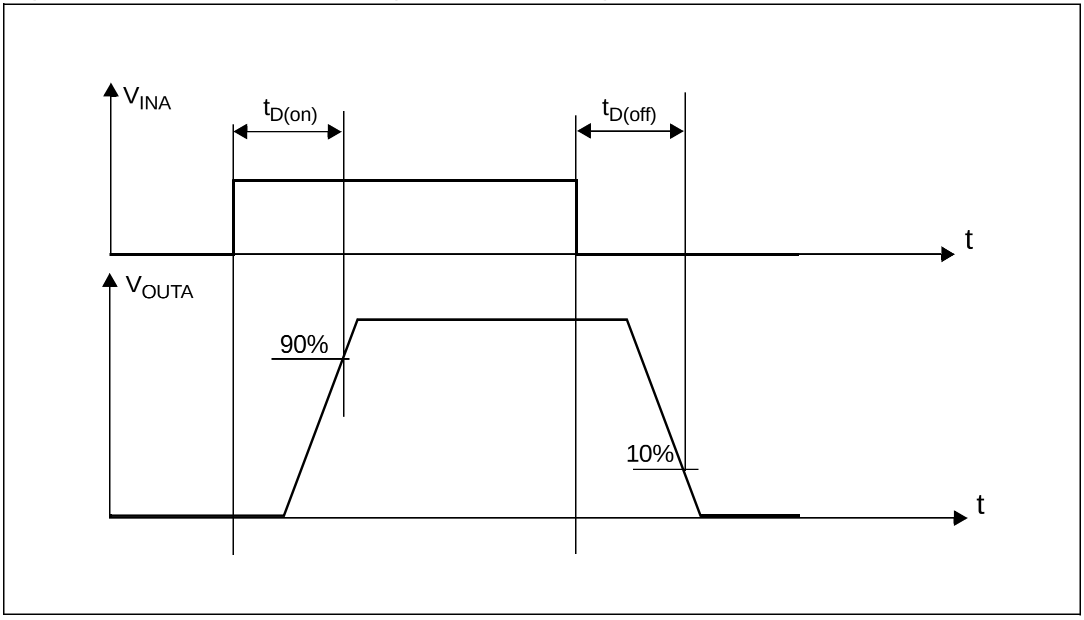


Figure 7. Definition of dynamic cross conduction current during a PWM operation

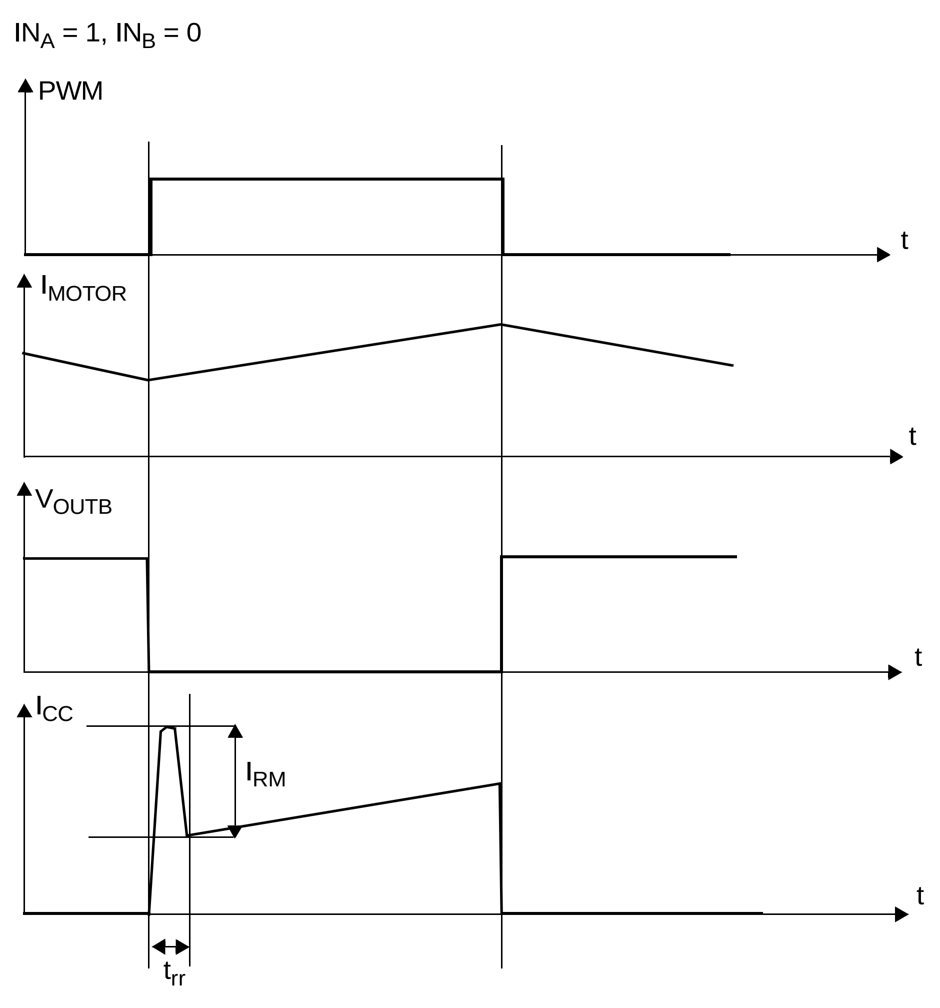


Figure 8. Definition of delay response time of sense current

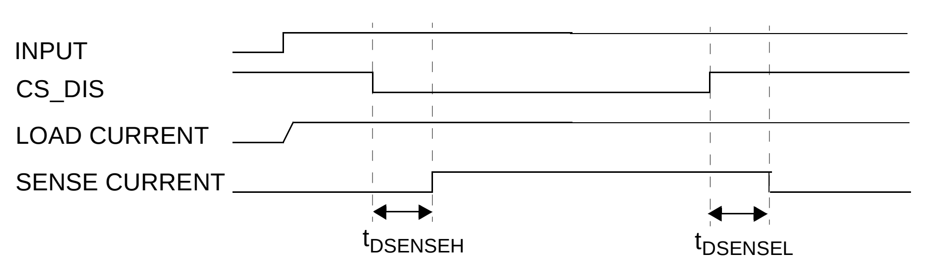


**Table 13. Truth table in normal operating conditions**

| $IN_A$ | $IN_B$ | $DIAG_A/EN_A$ | $DIAG_B/EN_B$ | $OUT_A$ | $OUT_B$ | CS | Operating mode |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | H | H | High Imp. | Brake to $V_{CC}$ |
| | 0 | | | | L | $I_{SENSE} = I_{OUT}/K$ | Clockwise (CW) |
| 0 | 1 | | | L | H | | Counterclockwise (CCW) |
| | 0 | | | | L | High Imp. | Brake to GND |

**Table 14. Truth table in fault conditions (detected on $OUT_A$)**

| $IN_A$ | $IN_B$ | $DIAG_A/EN_A$ | $DIAG_B/EN_B$ | $OUT_A$ | $OUT_B$ | CS ($V_{CSD}$=0V) |
|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 1 | OPEN | H | High impedance |
| | 0 | | | | L | |
| 0 | 1 | | | | H | $I_{OUTB}/K$ |
| | 0 | | | | L | High impedance |
| X | X | | 0 | | OPEN | |
| | | Fault Information | | Protection Action | | |

*Note:* *In normal operating conditions the $DIAG_X/EN_X$ pin is considered as an input pin by the device. This pin must be externally pulled high.*

### Table 15. Electrical transient requirements (part 1/3)

| ISO 7637-2: 2004(E) Test pulse | Test levels(1) | | Number of pulses or test times | Burst cycle/pulse repetition time | | Delays and Impedance |
|---|---|---|---|---|---|---|
| | III | IV | | Min. | Max. | |
| 1 | -75V | -100V | 5000 pulses | 0.5s | 5s | 2 ms, 10Ω |
| 2a | +37V | +50V | 5000 pulses | 0.2s | 5s | 50µs, 2Ω |
| 3a | -100V | -150V | 1h | 90ms | 100ms | 0.1µs, 50Ω |
| 3b | +75V | +100V | 1h | 90ms | 100ms | 0.1µs, 50Ω |
| 4 | -6V | -7V | 1 pulse | | | 100ms, 0.01Ω |
| 5b(2) | +65V | +87V | 1 pulse | | | 400ms, 2Ω |

1. The above test levels must be considered referred to $V_{CC}$ = 13.5V except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground.

### Table 16. Electrical transient requirements (part 2/3)

| ISO 7637-2: 2004E Test pulse | Test level results | |
|---|---|---|
| | III | VI |
| 1 | C | C |
| 2a | C | C |
| 3a | C | C |
| 3b | C | C |
| 4 | C | C |
| 5b(1) | C | C |

1. Valid in case of external load dump clamp: 40V maximum referred to ground.

### Table 17. Electrical transient requirements (part 3/3)

| Class | Contents |
|---|---|
| C | All functions of the device performed as designed after exposure to disturbance. |
| E | One or more functions of the device did not perform as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device. |

## 2.4 Waveforms

Figure 9. Waveforms in full-bridge operation

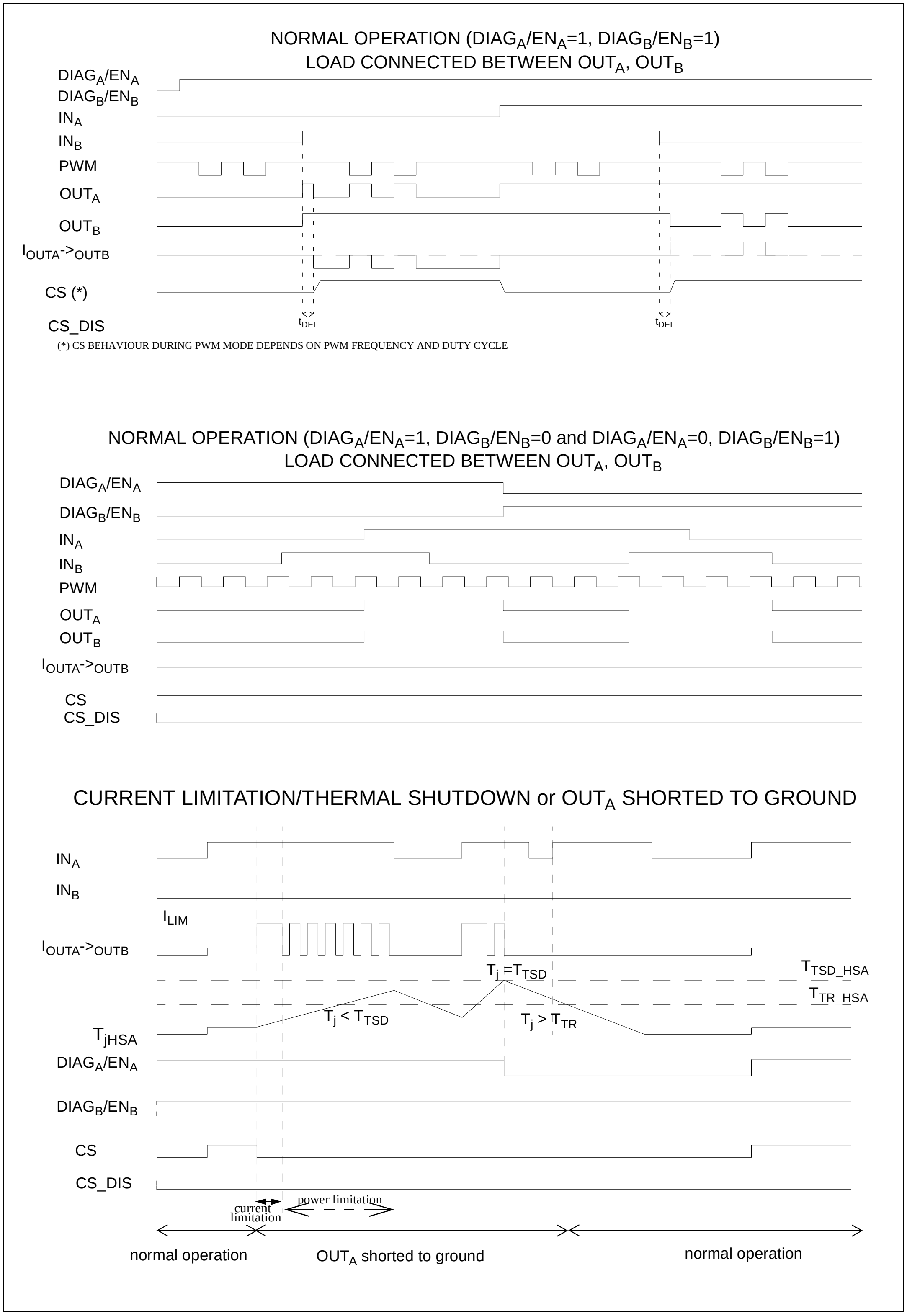
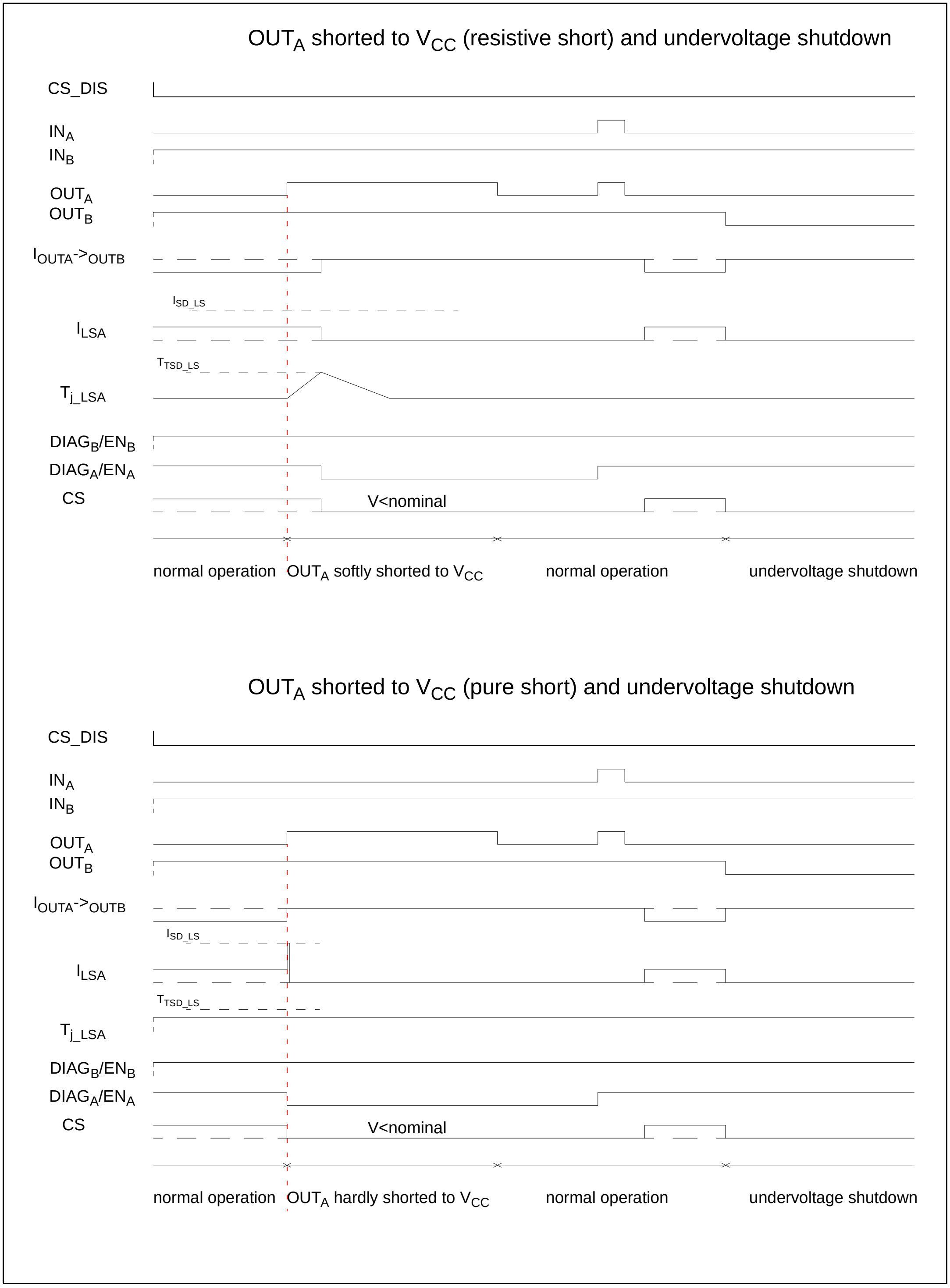


**Figure 10. Waveforms in full-bridge operation (continued)**



$OUT_A$ shorted to $V_{CC}$ (resistive short) and undervoltage shutdown

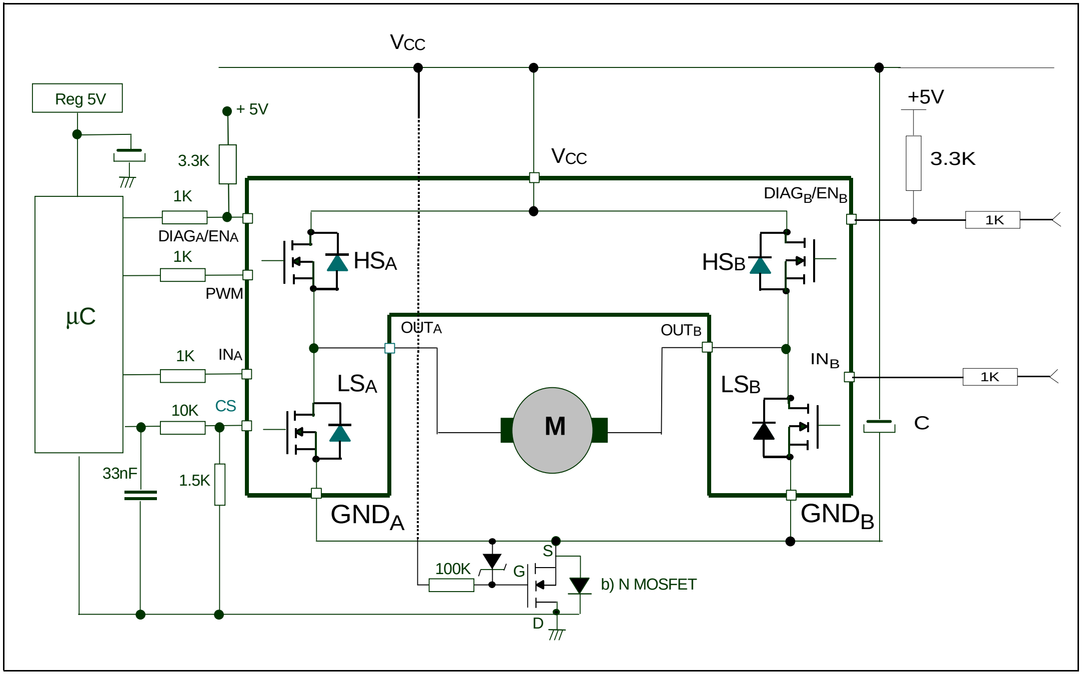
$OUT_A$ shorted to $V_{CC}$ (pure short) and undervoltage shutdown

# 3 Application information

In normal operating conditions the $DIAG_X/EN_X$ pin is considered as an input pin by the device. This pin must be externally pulled high.

PWM pin usage: In all cases, a “0” on the PWM pin turns off both $LS_A$ and $LS_B$ switches. When PWM rises back to “1”, $LS_A$ or $LS_B$ turn on again depending on the input pin state.

**Figure 11. Typical application circuit for DC to 20 kHz PWM operation short circuit protection**



*Note: The value of the blocking capacitor (C) depends on the application conditions and defines voltage and current ripple on supply line at PWM operation. Stored energy of the motor inductance may fly back into the blocking capacitor, if the bridge driver goes into 3-state. This causes a hazardous overvoltage if the capacitor is not big enough. As basic orientation, 500µF per 10A load current is recommended.*

In case of a fault condition the $DIAG_X/EN_X$ pin is considered as an output pin by the device.

The fault conditions are:

- Overtemperature on one or both high-sides
- Short to battery condition on the output (over current detection on the low-side Power MOSFET)

Possible origins of fault conditions may be:

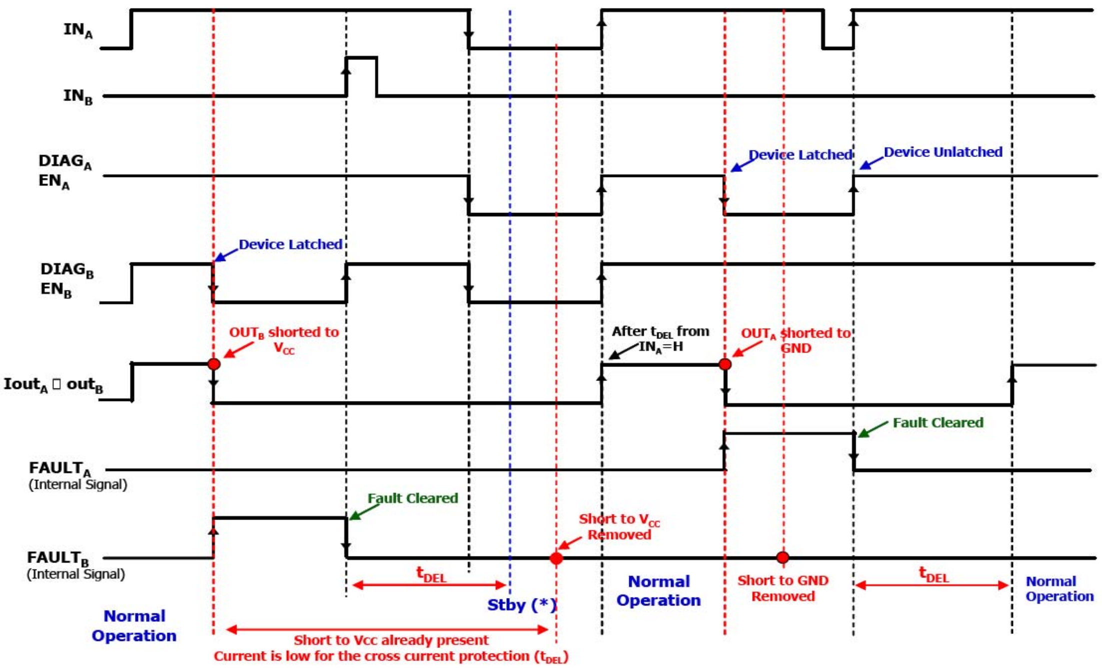
$OUT_A$ is shorted to ground → overtemperature detection on high-side A

$OUT_A$ is shorted to $V_{CC}$ → low-side Power MOSFET over current detection

When a fault condition is detected, the user can identify which power element is in fault by monitoring the $IN_A$, $IN_B$, $DIAG_A/EN_A$ and $DIAG_B/EN_B$ pins.

In any case, when a fault is detected, the faulty leg of the bridge is latched off. To turn on the respective output ($OUT_X$) again, the input signal must rise from low to high level.

**Figure 12. Behavior in fault condition (how a fault can be cleared)**



*Note:* *In case of the fault condition is not removed, the procedure for unlatching and sending the device in Stby mode is:*

*- Clear the fault in the device (toggle: $IN_A$ if $EN_A = 0$ or $IN_B$ if $EN_B = 0$)*

*- Pull low all inputs, PWM and Diag/EN pins within $t_{DEL}$.*

*If the Diag/En pins are already low, PWM = 0, the fault can be cleared simply toggling the input. The device enters in stby mode as soon as the fault is cleared.*

## 3.1 Reverse battery protection

Three possible solutions can be considered:

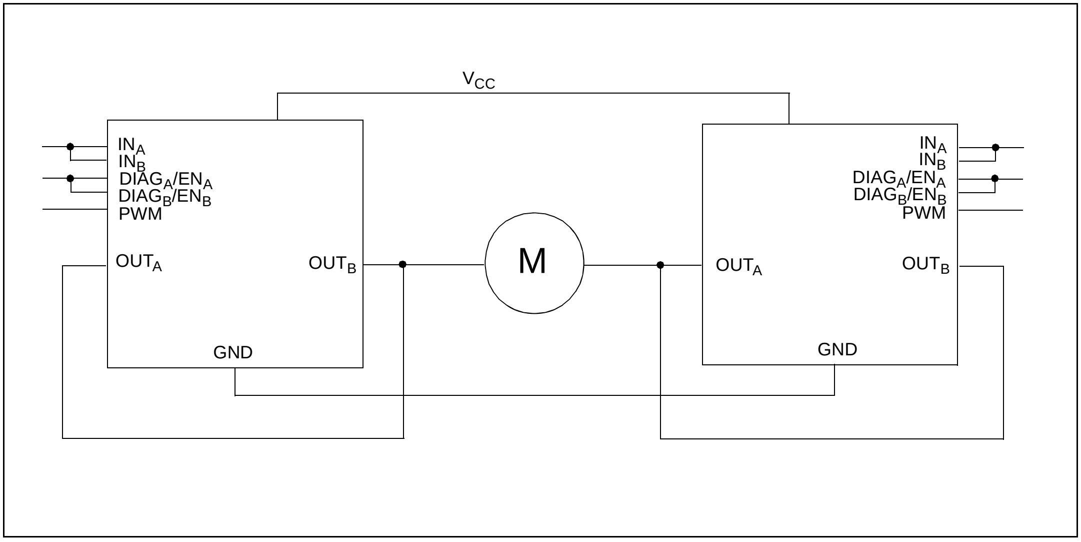
- A Schottky diode D connected to $V_{CC}$ pin
- An N-channel MOSFET connected to the GND pin (see *Figure 11*)
- A P-channel MOSFET connected to the $V_{CC}$ pin

The device sustains no more than -25 A in reverse battery conditions because of the two body diodes of the Power MOSFETs. Additionally, in reverse battery condition the I/Os of VNH5050A-E is pulled down to the $V_{CC}$ line (approximately -1.5 V).

Series resistor must be inserted to limit the current sunk from the microcontroller I/Os. If $I_{Rmax}$ is the maximum target reverse current through µC I/Os, series resistor is:

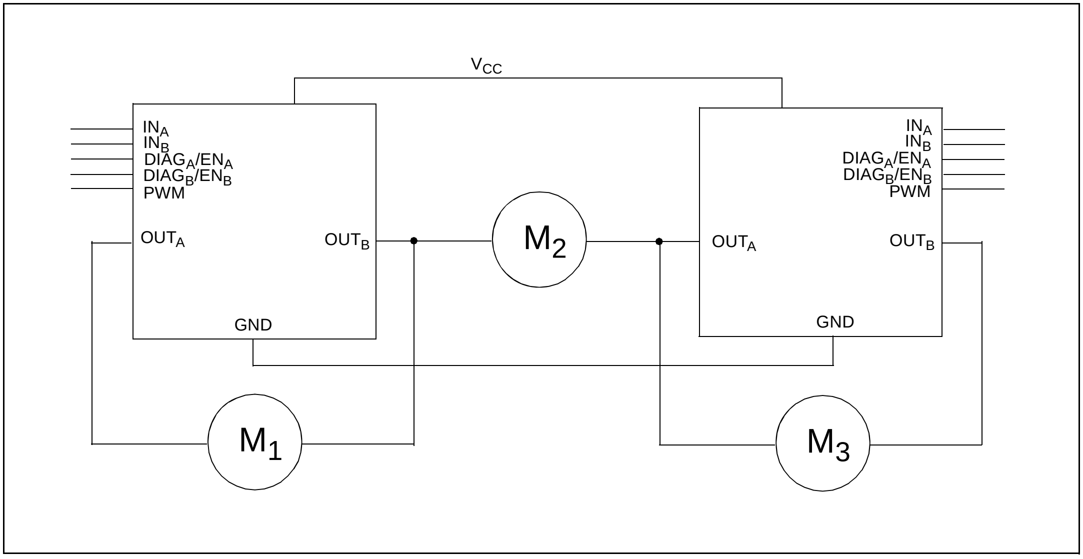
$$R = \frac{V_{IOs} - V_{CC}}{I_{Rmax}}$$

**Figure 13. Half-bridge configuration**



*Note: The VNH5050A-E can be used as a high power half-bridge driver.*

**Figure 14. Multi-motors configuration**

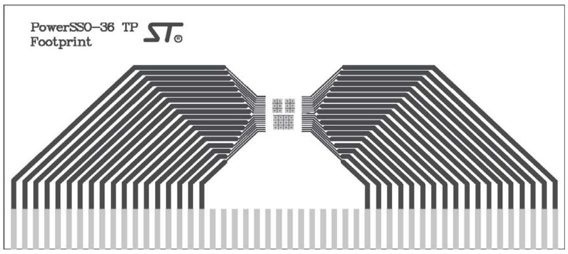


*Note: The VNH5050A-E can easily be designed in multi-motors driving applications such as seat positioning systems where only one motor has to be driven at a time.* $DIAG_X/EN_X$ *pins allow to put unused half-bridges in high impedance.*

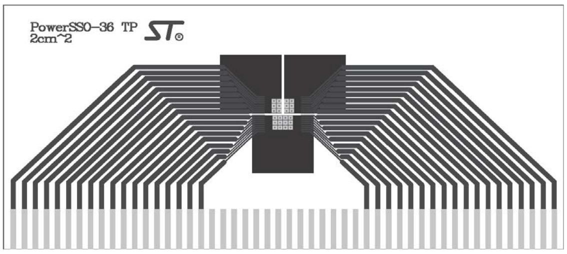
# 4 Package and PCB thermal data

## 4.1 PowerSSO-36 thermal data

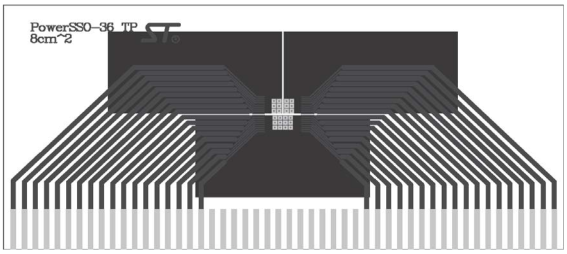
**Figure 15. PowerSSO-36™ PC board**



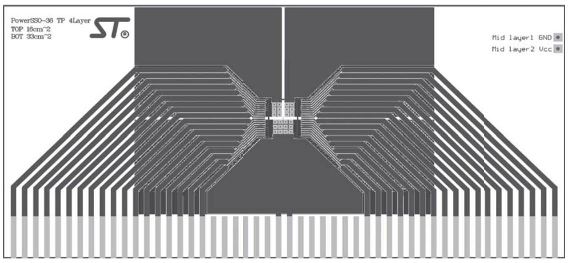
Double layers: footprint



Double layers: 2cm$^2$ of Cu



Double layers: 8cm$^2$ of Cu



Four layers: Cu on top layer: 16 cm$^2$; Cu on bottom layer: 32 cm$^2$; Cu on middle layer: total coverage

*Note:* *Board finish thickness 1.6 mm +/- 10%, Board double layers and four layers, Board dimension 129x60, Board Material FR4, Cu thickness 0.070mm (front and back side), Thermal vias spaced on a 1.2 mm x 1.2 mm grid, Vias pad clearance thickness 0.2 mm, Thermal via diameter 0.3 mm +/- 0.08 mm, Cu thickness on vias 0.025 mm, Footprint dimension 4.1 mm x 6.5 mm.*

**Figure 16. Chipset configuration**

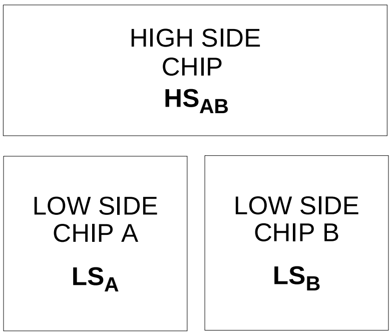
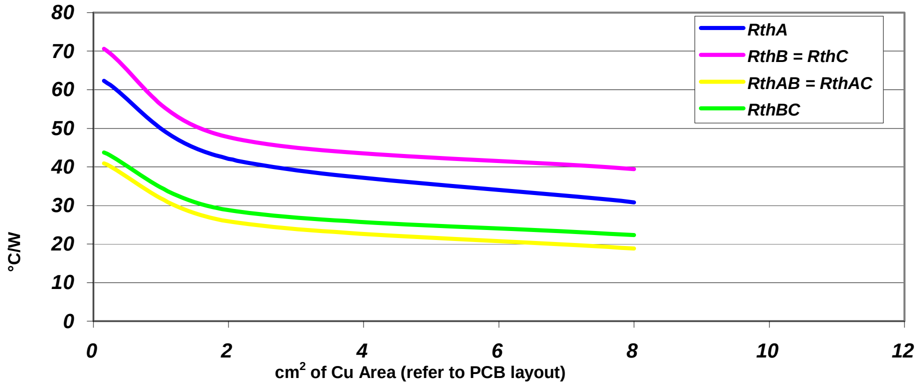


**Figure 17. Auto and mutual $R_{thj-amb}$ vs PCB copper area in open box free air condition**



### 4.1.1 Thermal calculation in clockwise and anti-clockwise operation in steady-state mode

**Table 18. Thermal calculation in clockwise and anti-clockwise operation in steady-state mode**

| $HS_A$ | $HS_B$ | $LS_A$ | $LS_B$ | $T_{jHSAB}$ | $T_{jLSA}$ | $T_{jLSB}$ |
|---|---|---|---|---|---|---|
| ON | OFF | OFF | ON | $P_{dHSA} \times R_{thHS} + P_{dLSB} \times R_{thHSLS} + T_{amb}$ | $P_{dHSA} \times R_{thHSLS} + P_{dLSB} \times R_{thLSLS} + T_{amb}$ | $P_{dHSA} \times R_{thHSLS} + P_{dLSB} \times R_{thLS} + T_{amb}$ |
| OFF | ON | ON | OFF | $P_{dHSB} \times R_{thHS} + P_{dLSA} \times R_{thHSLS} + T_{amb}$ | $P_{dHSB} \times R_{thHSLS} + P_{dLSA} \times R_{thLS} + T_{amb}$ | $P_{dHSB} \times R_{thHSLS} + P_{dLSA} \times R_{thLSLS} + T_{amb}$ |

### 4.1.2 Thermal resistances definition (values according to the PCB heatsink area)

$\mathbf{R_{thHS}}$ = $R_{thHSA}$ = $R_{thHSB}$ = High Side Chip Thermal Resistance Junction to Ambient ($HS_A$ or $HS_B$ in ON state)

$\mathbf{R_{thLS}}$ = $R_{thLSA}$ = $R_{thLSB}$ = Low Side Chip Thermal Resistance Junction to Ambient

$R_{\mathbf{thHSLS}}$ = $R_{thHSALSB}$ = $R_{thHSBLSA}$ = Mutual Thermal Resistance Junction to Ambient between High Side and Low Side Chips

$R_{\mathbf{thLSLS}}$ = $R_{thLSALSB}$ = Mutual Thermal Resistance Junction to Ambient between Low Side Chips

### 4.1.3 Thermal calculation in transient mode[a]

$T_{\mathbf{jHSAB}} = Z_{thHS} \times P_{dHSAB} + Z_{thHSLS} \times (P_{dLSA} + P_{dLSB}) + T_{amb}$

$T_{\mathbf{jLSA}} = Z_{thHSLS} \times P_{dHSAB} + Z_{thLS} \times P_{dLSA} + Z_{thLSLS} \times P_{dLSB} + T_{amb}$

$T_{\mathbf{jLSB}} = Z_{thHSLS} \times P_{dHSAB} + Z_{thLSLS} \times P_{dLSA} + Z_{thLS} \times P_{dLSB} + T_{amb}$

Single pulse thermal impedance definition (values according to the PCB heatsink area).

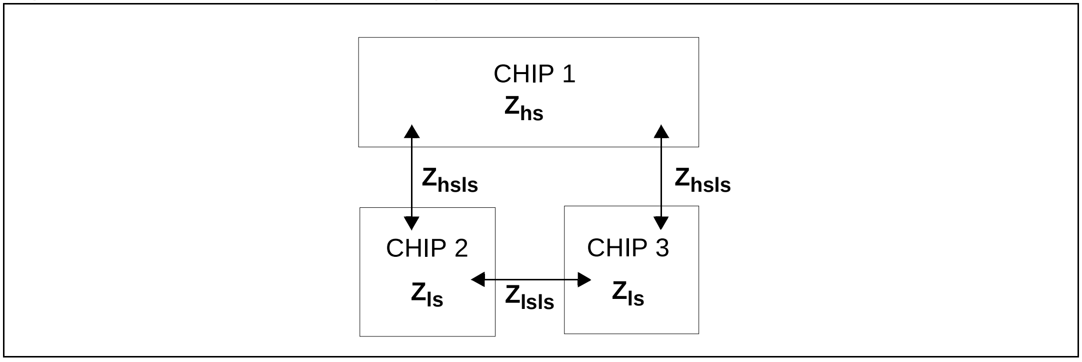
$Z_{\mathbf{thHS}}$ = High Side Chip Thermal Impedance Junction to Ambient

$Z_{\mathbf{thLS}}$ = $Z_{thLSA}$ = $Z_{thLSB}$ = Low Side Chip Thermal Impedance Junction to Ambient

$Z_{\mathbf{thHSLS}}$ = $Z_{thHSABLSA}$ = $Z_{thHSABLSB}$ = Mutual Thermal Impedance Junction to Ambient between High Side and Low Side Chips

$Z_{\mathbf{thLSLS}}$ = $Z_{thLSALSB}$ = Mutual Thermal Impedance Junction to Ambient between Low Side Chips

**Figure 18. Detailed chipset configuration**



**Equation 1: pulse calculation formula**

$$Z_{TH\delta} = R_{TH} \bullet (\delta + Z_{THtp}(1 - \delta))$$

$$\text{where } \delta = t_p / T$$

---

[a] Calculation is valid in any dynamic operating condition. $P_d$ values set by user.

Figure 19. PowerSSO-36 HSD thermal impedance junction ambient single pulse

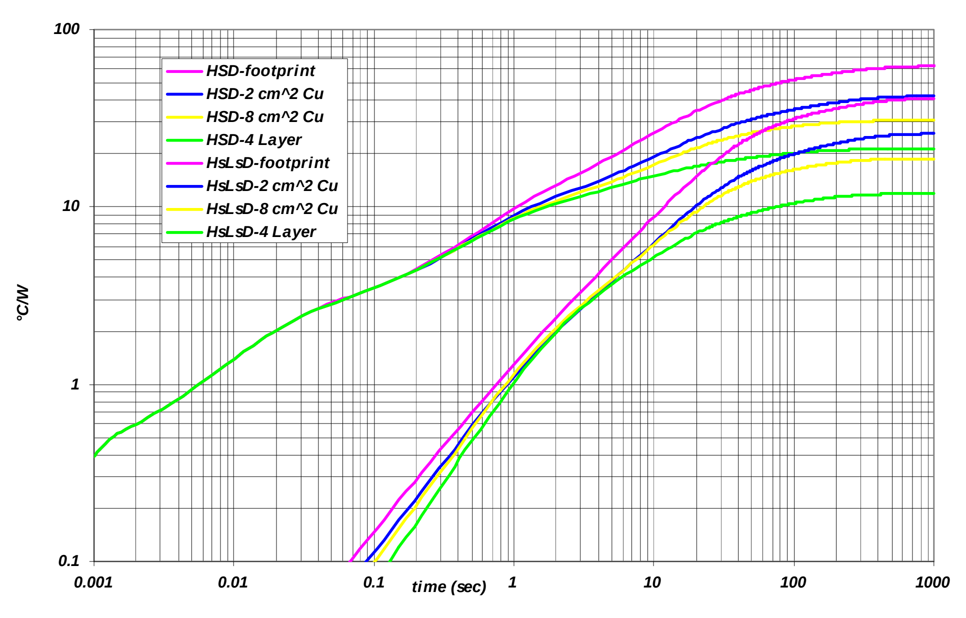
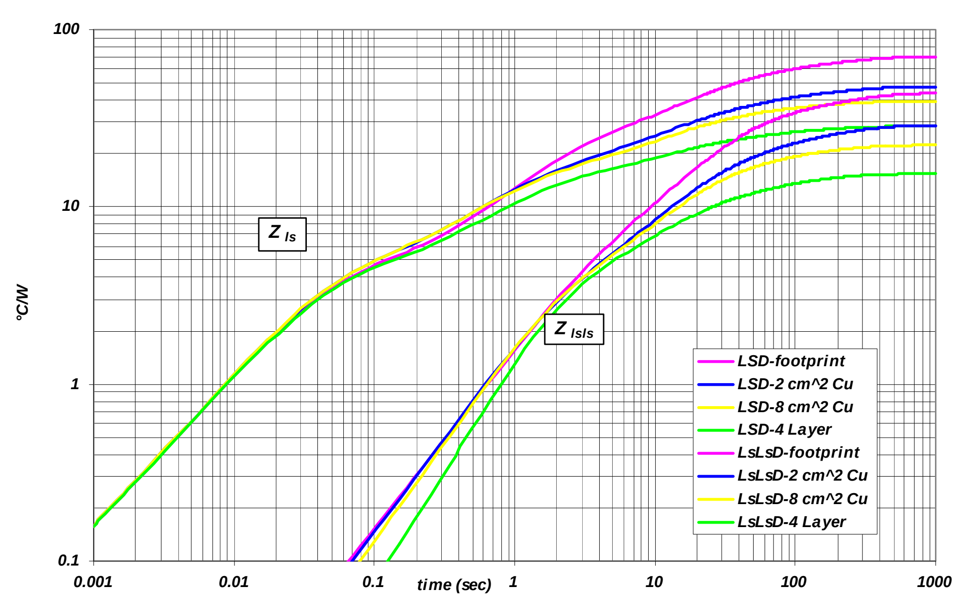
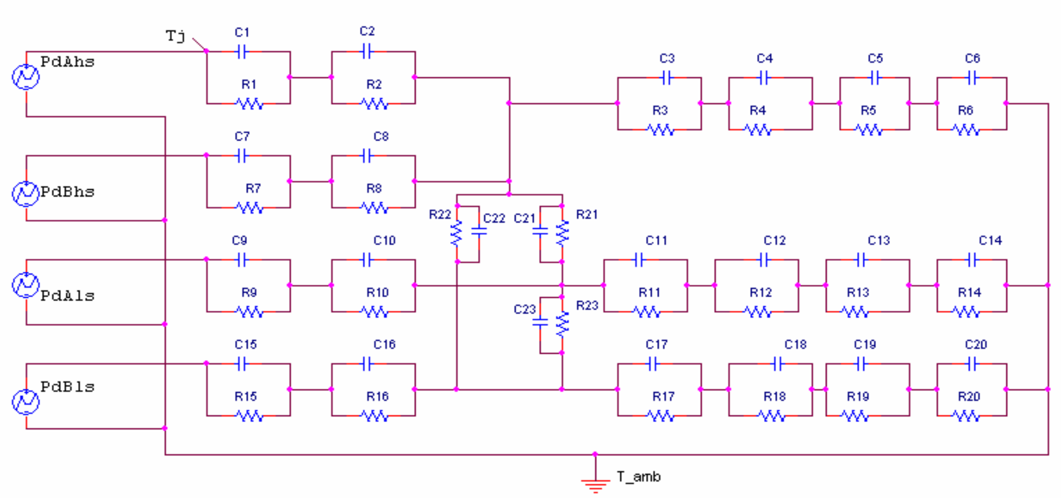


Figure 20. PowerSSO-36 LSD thermal impedance junction ambient single pulse



### Figure 21. Thermal fitting model of an H-bridge in PowerSSO-36



### Table 19. Thermal parameters[1]

| Area/island ($cm^2$) | Footprint | 2 | 8 | 4L |
|---|---|---|---|---|
| R1 = R7 (°C/W) | 0.4 | | | |
| R2 = R8 (°C/W) | 2 | | | |
| R3 (°C/W) | 8 | | | |
| R4 (°C/W) | 30 | 16 | 16 | 10 |
| R5 (°C/W) | 40 | 22 | 12 | 5 |
| R6 (°C/W) | 36 | 28 | 10 | 6 |
| R9 = R15 (°C/W) | 0.1 | | | |
| R10 = R16 (°C/W) | 3.6 | | | |
| R11 = R17 (°C/W) | 22 | 14 | 14 | 14 |
| R12 = R18 (°C/W) | 49 | 30 | 30 | 20 |
| R13 = R19 (°C/W) | 52 | 36 | 28 | 16 |
| R14 = R20 (°C/W) | 50 | 32 | 26 | 18 |
| R21 = R22 (°C/W) | 80 | 60 | 50 | 40 |
| R23 (°C/W) | 80 | 50 | 45 | 30 |
| C1 = C7 = C9 = C15 (W.s/°C) | 0.0005 | | | |
| C2 = C8 (W.s/°C) | 0.008 | | | |
| C3 (W.s/°C) | 0.09 | | | |
| C4 (W.s/°C) | 0.5 | 0.8 | 0.8 | 0.8 |
| C5 (W.s/°C) | 0.8 | 1.4 | 2 | 3 |
| C6 (W.s/°C) | 5 | 6 | 8 | 10 |
| C10 = C16 (W.s/°C) | 0.009 | | | |
| C11 = C17 (W.s/°C) | 0.07 | | | |
| C12 = C18 (W.s/°C) | 0.45 | 0.45 | 0.45 | 0.6 |
| C13 = C19 (W.s/°C) | 0.8 | 1 | 1.2 | 2.5 |
| C14 = C20 (W.s/°C) | 4 | 5 | 6 | 8 |
| C21 = C22 = C23 (W.s/°C) | 0.01 | 0.006 | 0.005 | 0.005 |

1. The blank space means that the value is the same as the previous one.

# 5 Package and packing information

## 5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

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## 5.2 PowerSSO-36 TP package information

**Figure 22. PowerSSO-36 TP package dimensions**

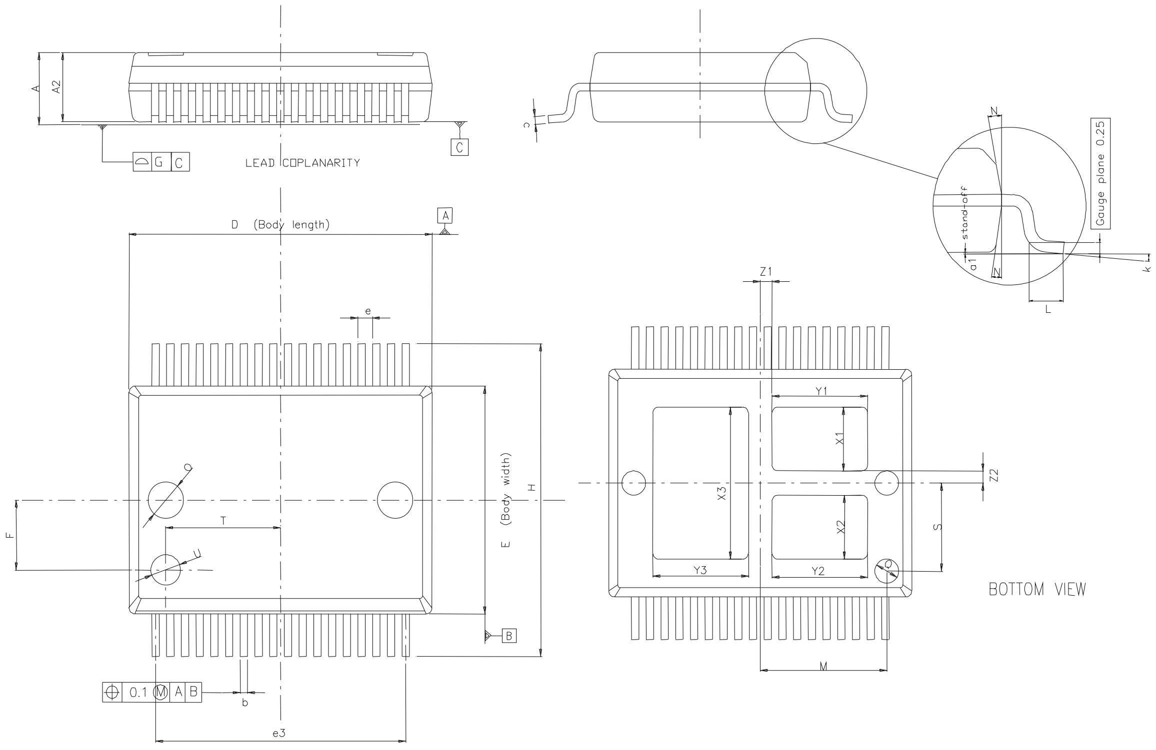
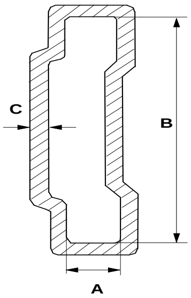


**Table 20. PowerSSO-36 TP mechanical data**

| Symbol | Millimeters | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 2.15 | - | 2.47 |
| A2 | 2.15 | - | 2.40 |
| a1 | 0 | - | 0.1 |
| b | 0.18 | - | 0.36 |
| c | 0.23 | - | 0.32 |
| D | 10.10 | - | 10.50 |
| E | 7.4 | - | 7.6 |
| e | - | 0.5 | - |
| e3 | - | 8.5 | - |
| F | | 2.3 | |
| G | - | - | 0.1 |
| H | 10.1 | - | 10.5 |
| h | - | - | 0.4 |
| k | 0 deg | | 8 deg |
| L | 0.6 | - | 1 |
| M | | 4.3 | |
| N | - | - | 10 deg |
| O | | 1.2 | |
| Q | | 0.8 | |
| S | | 2.9 | |
| T | | 3.65 | |
| U | | 1.0 | |
| X1 | 1.85 | | 2.35 |
| Y1 | 3 | | 3.5 |
| X2 | 1.85 | | 2.35 |
| Y2 | 3 | | 3.5 |
| X3 | 4.7 | - | 5.2 |
| Y3 | 3 | - | 3.5 |
| Z1 | | 0.4 | |
| Z2 | | 0.4 | |

## 5.3 PowerSSO-36 TP packing information

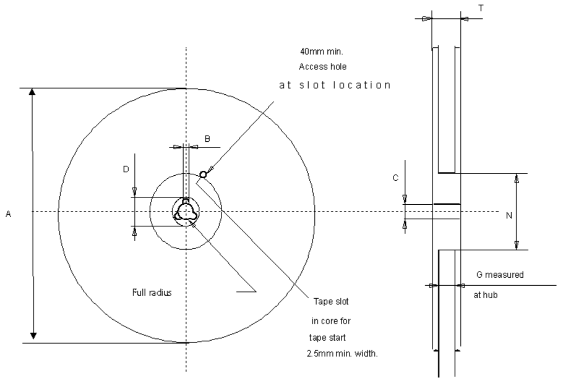
Figure 23. PowerSSO-36 TP tube shipment (no suffix)



| | |
|---|---|
| **Base Qty** | 49 |
| **Bulk Qty** | 1225 |
| **Tube length (±0.5)** | 532 |
| **A** | 3.5 |
| **B** | 13.8 |
| **C (±0.1)** | 0.6 |

All dimensions are in mm.

Figure 24. PowerSSO-36 TP tape and reel shipment (suffix “TR”)



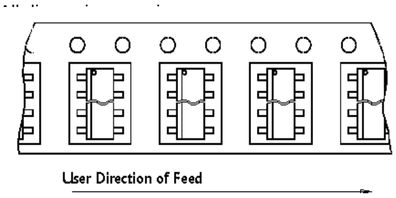
**Reel dimensions**

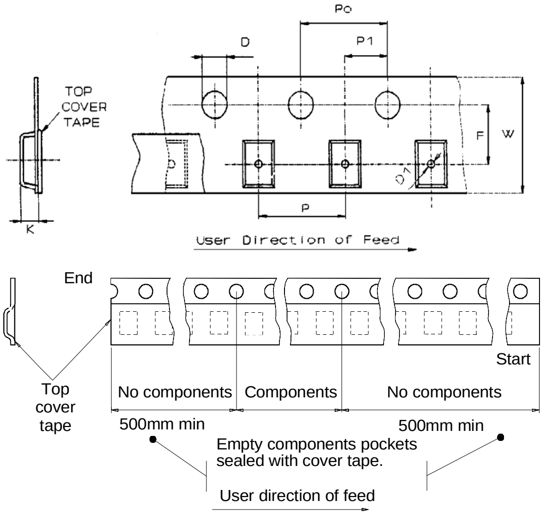
| | |
|---|---|
| **Base Qty** | 1000 |
| **Bulk Qty** | 1000 |
| **A (max)** | 330 |
| **B (min)** | 1.5 |
| **C (±0.2)** | 13 |
| **F** | 20.2 |
| **G (+2 / -0)** | 24.4 |
| **N (min)** | 100 |
| **T (max)** | 30.4 |

**Tape dimensions**

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

| | | |
|---|---|---|
| **Tape width** | **W** | 24 |
| **Tape Hole Spacing** | **P0 (±0.1)** | 4 |
| **Component Spacing** | **P** | 12 |
| **Hole Diameter** | **D (±0.05)** | 1.55 |
| **Hole Diameter** | **D1 (min)** | 1.5 |
| **Hole Position** | **F (±0.1)** | 11.5 |
| **Compartment Depth** | **K (max)** | 2.85 |
| **Hole Spacing** | **P1 (±0.1)** | 2 |





# 6 Revision history

Table 21. Document revision history

| Date | Revision | Description of changes |
|---|---|---|
| 06-Jul-2009 | 1 | Initial release. |
| 15-Sep-2009 | 2 | Updated *Figure 1: Block diagram*.<br>Updated following tables:<br>– *Table 2: Block description*<br>– *Table 6: Absolute maximum ratings*<br>– *Table 8: Power section*<br>– *Table 11: Protections and diagnostics*<br>– *Table 12: Current sense* $(9\ V < V_{CC} < 18\ V)$<br>– *Table 14: Truth table in fault conditions (detected on OUTA)*<br>Updated *Chapter 3: Application information*.<br>Modified *Table 12: Current sense* $(9\ V < V_{CC} < 18\ V)$. |
| 02-Dec-2009 | 3 | Updated following tables:<br>– *Table 8: Power section*<br>– *Table 10: Switching* $(V_{CC} = 13\ V, R_{LOAD} = 1.5\ \Omega)$<br>– *Table 11: Protections and diagnostics*<br>– *Table 12: Current sense* $(9\ V < V_{CC} < 18\ V)$<br>Added *Chapter 4: Package and PCB thermal data* |
| 16-Dec-2009 | 4 | Updated *Table 4: Pin definitions and functions* |
| 02-Mar-2010 | 5 | Updated *Table 14: Truth table in fault conditions (detected on OUTA)*. |
| 30-Apr-2010 | 6 | Updated following tables:<br>– *Table 10: Switching* $(V_{CC} = 13\ V, R_{LOAD} = 1.5\ \Omega)$<br>– *Table 11: Protections and diagnostics* |
| 30-Jun-2010 | 7 | Updated following tables:<br>– *Table 7: Thermal data*<br>– *Table 8: Power section*<br>– *Table 12: Current sense* $(9\ V < V_{CC} < 18\ V)$ |
| 05-Jul-2010 | 8 | Updated *Table 19: Thermal parameters*. |
| 19-Oct-2010 | 9 | Updated *Table 12: Current sense* $(9\ V < V_{CC} < 18\ V)$<br>Updated *Section 4.1.3: Thermal calculation in transient mode*<br>Added *Figure 18: Detailed chipset configuration* |
| 22-Dec-2011 | 10 | Updated *Figure 1: Block diagram*<br>Added *Table 3: Suggested connections for unused and not connected pins*<br>*Table 11: Protections and diagnostics*:<br>– $T_{TSD}$, $T_{TR}$, $T_{HYST}$: added note<br>Updated *Figure 9: Waveforms in full-bridge operation* and *Figure 10: Waveforms in full-bridge operation (continued)* |
| 19-Sep-2013 | 11 | Updated Disclaimer. |

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