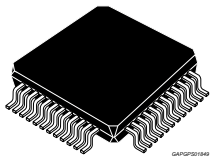
L9654

Quad squib driver and dual sensor interface ASIC for safety application

Datasheet - production data



LQFP48

Features

- 4 deployment drivers sized to deliver 1.2 A (min) for 2 ms (min) and 1.75 A (min) for 1ms (min).
- Independently controlled high-side and low-side MOS for diagnosis
- Analog output available for resistance
- Squib short to ground, short to battery and MOS diagnostic available on SPI register
- Capability to deploy the squib with 1.2 A (min.) or 1.75 A under 35 V load-dump condition and the low-side MOS is shorted to ground
- Capability to deploy the squib with 1.2 A (min.) at 6.9 V V_{RES} and 1.75 A at 12 V V_{RES}.
- Interface with 2 satellite sensors
- Programmable independent current trip points for each satellite channel
- Support Manchester protocol for satellite sensors
- Supports for variable bit rate detection
- Independent current limit and fault timer shutdown protection for each satellite output
- Short to ground and short to battery detection and reporting for each satellite channel
- 5.5 MHz SPI interface
- Satellite message error detection
- Low voltage internal reset
- 2 kV ESD capability on all pins
- Package: 48 lead LQFP
- Technology: ST Proprietary BCD5s (0.57 µm)

Description

L9654 is intended to deploy up to 4 squibs and to interface up to 2 satellites.

Squib drivers are sized to deploy 1.2 A (min.) for 2 ms (min.) during load dump and 1.75 A (min.) for 1 ms (min.) during load dump.

Diagnostic of squib driver and squib resistance measurement is controlled by micro controllers.

Satellite interfaces support Manchester decoder with variable bit rates.

Table 1. Device summary

Order code	Package	Packing
L9654	LQFP48	Tray
L9654TR	LQFP48	Tape and reel

Contents

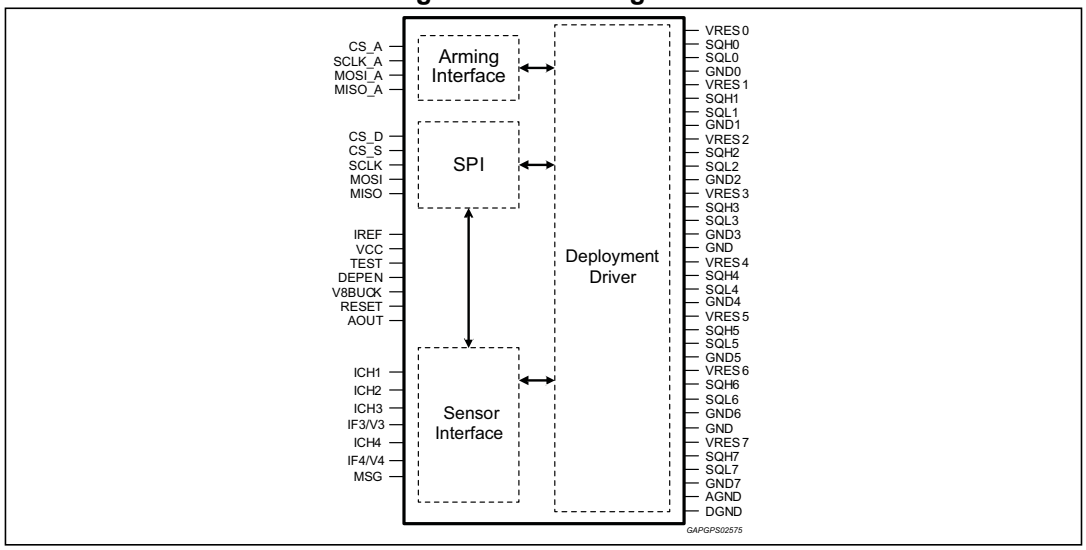
List of tables

List of figures

1 Block diagram and application schematic

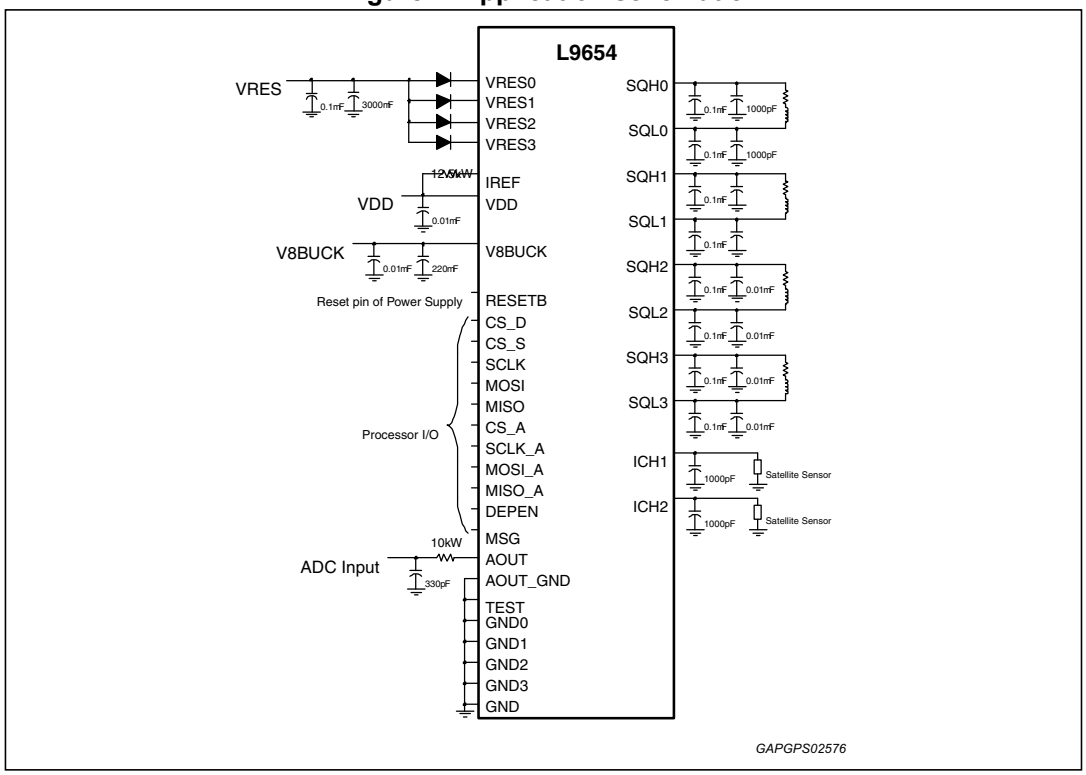
1.1 Block diagram

Figure 1. Block diagram



1.2 Application schematic

Figure 2. Application schematic



2 Pin description

Table 2. Pin function

Pin #	Pin name	Description	I/O type	Reset state
1	MISO_A	Arming SPI data out	Output	Hi-Z
2	NC	No connect	-	-
3	RESETB	Reset pin	Input	Pullup
4	GND	Signal ground (analog & digital)	-	-
5	VDD	VDD supply voltage	Input	-
6	NC	No connect	-	-
7	CS_A	SPI chip select for arming interface	Input	Pulldown
8	CS_S	SPI chip select for satellite interface	Input	Pulldown
9	CS_D	SPI Chip select for deployment driver	Input	Pulldown
10	DEPEN	Deployment enable	Input	Pulldown
11	MOSI	SPI data in	Input	Hi-Z
12,13	NC	No connect	-	-
14	MOSI_A	Arming SPI data in	Input	Hi-Z
15	SCLK_A	Arming SPI clock	Input	Hi-Z
16	SCLK	SPI clock	Input	Hi-Z
17	GND2	Power ground for loop channel 2	-	-
18	SQL2	Low-side driver output for channel 2	Output	Pulldown
19	SQH2	High-side driver output for channel 2	Output	Hi-Z
20	VRES2	Reserve voltage for loop channel 2	Input	-
21	VRES3	Reserve voltage for loop channel 3	Input	-
22	SQH3	High-side driver output for channel 3	Output	Hi-Z
23	SQL3	Low-side driver output for channel 3	Output	Pulldown
24	GND3	Power ground for loop channel 3	-	-
25	TEST	Test pin	Input	Pulldown
26	NC	No connect	-	-
27	V8BUCK	Supply Voltage for Satellite Interface and Resistance Measurement	Input	-
28	NC	No connect	-	-
29	ICH2	Current sense output for channel 2	Output	Hi-Z
30	NC	No connect	-	-
31	ICH1	Current sense output for channel 1	Output	Hi-Z
32	NC	No connect	-	-
33	IREF	External current reference resistor	Output	-

Table 2. Pin function (continued)

Pin #	Pin name	Description	I/O type	Reset state
34	AOUT_GND	Ground reference for AOUT	-	-
35	AOUT	Analog output for loop diagnostics	Output	Hi-Z
36	NC	No connect	-	-
37	GND1	Power ground for loop channel 1	-	-
38	SQL1	Low-side driver output for channel 1	Output	Pulldown
39	SQH1	High-side driver output for channel 1	Output	Hi-Z
40	VRES1	Reserve voltage for loop channel 1	Input	-
41	VRES0	Reserve voltage for loop channel 0	Input	-
42	SQH0	High-side driver output for channel 0	Output	Hi-Z
43	SQL0	Low-side driver output for channel 0	Output	Pulldown
44	GND0	Power ground for loop channel 0	-	-
45	NC	No connect	-	-
46	MSG	Message waiting	Output	Pulldown
47	MISO	SPI data out	Output	Hi-Z
48	NC	No connect	-	-

2.1 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value.	Unit
$R_{th\ j\text{-}amb}$	Thermal resistance junction-to-ambient	68	°C/W

3 Electrical specification

3.1 Maximum ratings

The device may not operate properly if maximum operating condition is exceeded.

Table 4. Maximum operating conditions

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	4.9 to 5.1	V
V_{8BUCK}	V8BUCK voltage	7 to 8.5	V
V_{RES}	VRES voltage (VRES0, VRES1, VRES2, VRES3)	35	V
V_I	Discrete input voltage (RESETB, DEPEN, CS_A, CS_D, CS_S, SCLK, SCLK_A, MOSI, MOSI_A, MISO, MISO_A)	0.3 to (V_{DD} +0.3)	V
T_j	Junction temperature	-40 to 150	°C

3.2 Absolute maximum ratings

Maximum ratings are absolute ratings; exceeding any one of these values may cause permanent damage to the integrated circuit.

Table 5. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	-0.3 to 5.5	V
V_{8BUCK}	V8BUCK voltage	0.3 to 40	V
V_{RES}	VRES voltage (VRES0, VRES1, VRES2, VRES3)	0.3 to 40	V
SQ_{L-H}	Squib high and low-side drivers (SQH0, SQH1, SQH2, SQH3, SQL0, SQL1, SQL2, SQL3)	0.3 to 40	V
V_I	Discrete input voltage (RESETB, DEPEN, CS_A, CS_D, CS_S, SCLK, SCLK_A, MOSI, MOSI_A, MISO, MISO_A)	-0.3 to 5.5	V
ICHx	Satellite input voltage (ICH1, ICH2, ICH3, ICH4)	-3 to 40	V
-	Analog/digital outputs voltage (AOUT, IREF, MSG, IF3V3, IF4V4)	-0.3 to 5.5	V
T_j	Maximum steady-state junction temperature	150	°C
T_{amb}	Ambient temperature	-40 to 95	°C
T_{stg}	Storage temperature	-65 to 150	°C

3.3 Electrical characteristics

3.3.1 DC characteristics

V_{RES} = 6.5 to 35 V, V_{DD} = 4.9 to 5.1 V, V_{8BUCK} = 7.0 V to 8.5 V, T_{amb} = -40°C to +95°C.

Table 6. DC specification general

Symbol	Parameter	Test condition	Min.	Typ	Max.	Unit
V_{RST}(1)	Internal voltage reset V_{DD}	V_{DD} drops until deployment drivers are disabled	4.0	-	4.5	V
V_{RST_L}(2)			2.1	-	3.0	
I_{DD}	Input current V_{DD}	Normal operation; I_{CH1-2} = 0 A	4.5	-	7.0	mA
		Short to –0.3V on SQH; I_{CH1-2} = 0 A	4.2	-	7.9	
		Short to –0.3V on SQL; I_{CH1-2} = 0A	4.2	-	7.9	
		Deployment; I_{CH1-2} = 0A	4.2	-	7.9	
R_{IREF_H}	Resistance threshold I_{REF}	-	20.0	-	60.0	kΩ
R_{IREF_L}		-	2.0	-	9.0	kΩ
V_{IH_RESETB}	Input voltage threshold RESETB	-	-	-	2.0	V
V_{IL_RESETB}		-	0.8	-		V
V_{HYS}		-	100	-	400	mV
V_{IH_DEPEN}	Input voltage threshold DEPEN	-	-	-	2.0	V
V_{IL_DEPEN}		-	0.8	-	-	V
I_{PD}	Input pull-down current DEPEN	V_{IN} = V_{IL} to V_{DD}	10	-	50	µA
V_{IH_TEST}	Input voltage threshold TEST	-	-	-	3.6	V
V_{IL_TEST}		-	0.8	-	-	V
I_{TEST}	Input pull-down current TEST	TEST = 5 V	1.0	-	2.5	mA
I_{PU}	Input pull-up current RESETB	RESETB = V_{IH} to GND	10	-	60	µA
I_{V8BUCK}	Current consumption V8BUCK	-	25	-	40	µA
V_{IH}	Input voltage threshold MOSI, MOSI_A, SCLK, SCLK_A, CS_S, CS_D, CS_A	Input Logic = 1	-	-	2.0	V
V_{IL}		Input Logic = 0	0.8	-	-	V
V_{HYS}		-	100	-	400	mV
I_{LKG}	Input leakage current MOSI, MOSI_A, SCLK, SCLK_A	V_{IN} = V_{DD}		-	1	µA
		V_{IN} = 0 to V_{IH}	-1	-	-	µA
I_{PD}	Input pulldown current CS_S, CS_D, CS_A	V_{IN} = V_{IL} to V_{DD}	10	-	50	µA
V_{OH}	Output voltage MISO, MISO_A, MSG	I_{OH} = -800 µA	V_{DD}–0.8	-	-	V
V_{OL}		I_{OL} = 1.6 mA	-	-	0.4	V
I_{HI_Z}	Tri-state current MISO, MISO_A,	MISO = VDD	-	-	1	µA
		MISO = 0 V	-1	-	-	µA

1. V_{RST} shall have a POR de-glitch timer.
2. $V_{RST\ L}$ shall have no timer.

V_{RES} = 6.5 to 40 V, V_{DD} = 4.9 to 5.1 V, V_{8BUCK} = 7.0 V to 8.5 V, T_{amb} = -40 °C to +95 °C.

Table 7. DC specification: deployment drivers

Symbol	Parameter	Test conditions	Min.	Typ	Max.	Units
V_{OH}	Output voltage AOUT	High Saturation Voltage; I_{AOUT} = -500µA	V_{DD}-04	-	-	V
V_{OL}		Low Saturation Voltage; I_{AOUT} = +500µA	-	-	0.3	V
I_Z	Tri-state current AOUT	AOUT = V_{DD}	-	-	1	µA
		AOUT = 0V	-1	-	-	µA
I_{LKG}	Leakage current SQH	V8BUCK = V_{DD} = 0, V_{RES} = 36 V, V_{SQH} = 0 V	-	-	50	µA
I_{STG}		V8BUCK = 18V; V_{DD} = 5V; V_{SQH} = -0.3V	-5	-	-	mA
I_{LKG}	Bias current VRES(1)	V8BUCK = 18 V; V_{DD} = 5 V; V_{RES} = 36V; SQH shorted to SQL	-	-	10	µA
I_{LKG}	Leakage current SQL	V8BUCK = V_{DD} = 0, V_{SQL} = 18 V	-10	-	10	µA
I_{STG}		V8BUCK = 18 V; V_{DD} = 5V; V_{SQL} = -0.3 V	-5	-	-	mA
I_{STB}		V8BUCK = 18 V; V_{DD} = 5 V; V_{SQL} = 18 V	-	-	5	mA
I_{PD}	Pull-down current SQL	V_{SQL} = 1.8 V to V_{DD}	900	-	1300	µA
I_{PD_SQH}	Pull-down current SQH	V_{SQH} = SBTH to V_{RES}	900	-	1300	µA
V_{BIAS}	Diagnostics bias voltage	I_{SQH} = -1.5 mA (nominal: 2.0 V)	1.80	-	2.20	V
I_{BIAS}	Diagnostics bias current	V_{SQH} = 0V	-7	-	-	I_{PD}
V_{STB}	Short to battery threshold	(Nominal 3.0 V)	2.70	-	3.30	V
V_{STG}	Short to ground threshold	(Nominal 1.0 V)	0.90	-	1.10	V
V_{I_th}	MOS test load voltage detection	-	100	-	300	mV
I_{SRC}	Resistance measurement current source	V_{DD} = 5.0 V; V8BUCK = 7.0 V to 26.5 V	38	-	42	mA
I_{SINK}	Resistance measurement current sink	-	45	-	55	mA
R_{DSon}	Total high and low-side MOS On resistance	High-side MOS + Low-side MOS V_{RES} = 6.9 V; I = 1.2 A @95 °C	-	-	2.0	Ω
R_{DSon}	High-side MOS on resistance	V_{RES} = 35 V; I_{VRES} = 1.2 A; T_{amb} = 95 °C	-	-	0.8	Ω
R_{DSon}	Low-side MOS on resistance	V_{RES} = 35 V; I_{VRES} = 1.2 A; T_{amb} = 95 °C	-	-	1.2	Ω
I_{DEPL_12A}	Deploiment current	MOSI Register mode bit D10=”0” R_{LOAD} = 1.7 Ω; V_{RES} = 6.9 to 35 V	1.20	-	1.47	A
I_{DEPL_175A}		MOSI Register mode Bit D10=”1” R_{LOAD} = 1.7 Ω; ; V_{RES} = 12 to 35 V	1.75	-	2.14	A
I_{LIM}	Low-side MOS current limit	R_{LOAD} = 1.75 Ω	2.15	-	3.5	A
$R_{L\ RANGE}$	Load resistance range(2)		0	-	10.0	Ω

1. Not applicable during a diagnostic.
2. Test conditions for load resistance measurements

V_{DD} = 4.9 to 5.1 V, V_{8BUCK} = 7.0 V to 8.5 V, T_{amb} = -40 °C to +95 °C.

Table 8. Satellite interface DC specifications

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I_Lim	Current limit	High-side short to -0.3 V	(-)75	-	(-)150	mA
		High-side short to Battery	-	-	5	mA
		V8BUCK =Vcc=0 measured @ V8BUCK	-	-	5	mA
Vhdp	High-side voltage drop	I=50 mA @105°C; V8BUCK=7.0V	-	-	1	V
		I=25 mA @105°C; V8BUCK=7.0V	-	-	0.5	V
Itr	Low to high transition current threshold	SPI channel configuration				
		Bit <2:0≥111	54.00	-	66.00	mA
		Bit <2:0≥110	43.65	-	53.35	mA
		Bit <2:0≥101	35.10	-	42.90	mA
		Bit <2:0≥100	28.80	-	34.20	mA
		Bit <2:0≥011	24.85	-	29.15	mA
		Bit <2:0≥010	20.25	-	24.75	mA
		Bit <2:0≥001	17.10	-	20.90	mA
		Bit <2:0≥000	14.85	-	18.15	mA
Ihyst	Current threshold hysteresis	Sink current = Ithr at the output (ICHX). Ihyst=trip point high – trip point low	0.05*Itr	-	0.15*Itr	mA
Vos	Short to BAT feedback current	V(ICHX)-V8BUCK<50 mV	-	-	25	mA
Olkg	Output leakage current ICH_X	V=18 V @ pin under test	-	-	1	µA

3.3.2 AC characteristics

V_{RES} = 6.5 to 35 V, V_{DD} = 4.9 to 5.1 V, V_{8BUCK} = 7.0 V to 8.5 V, T_{amb} = -40 °C to +95 °C.

Table 9. AC specification: deployment drivers

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t_{POR}	POR de-glitch timer	Timer for V_{RST}	10	-	25	µs
T_{GLITCH}	De-glitch timer	-	5	-	20	µs
I_{ON}	Diagnostic current	DEPEN pins asserted ;Measured at 150 µs from falling edge CS_D or CS_A; See *Figure 4*	0.90	-		I_{FINAL}
t_{PULSE}	Pulse stretch timer	See *Table 17*	0	-	60	ms
t_{P_ACC}	Pulse stretch timer accuracy	-	-20	-	20	%
$t_{DEPLOY-2ms}$	Deployment time	V_{RES} = 6.9 to 35 V(1)	2	-	2.5	ms
$t_{DEPLOY-1ms}$	Deployment time	V_{RES} = 12 to 35 V(1)	1	-	1.25	ms
t_{FLT_DLY}	Fault detection filter(2)	-	10	-	50	µs
I_{SLEW}	Rmeas current di/dt	10 % - 90 % of I_{SRC}	2	-	8	mA/µs
t_{R_DLY}	Rmeas current delay	From the falling edge of CS to 10% of I_{SRC}		-	15	µs
t_{R_WAIT}	Rmeas wait time(2)	Wait time before AOUT voltage is stable for ADC reading	-	-	100	µs
$t_{TIMEOUT}$	MOS diagnostic on-time	-	-	-	2.5	ms
t_{ILIM}	SQL high current protection timer	-	90	-	110	µs
t_{PROP_DLY}	LS/HS MOS turn off propagation delay(2)	Time is measured from the valid LS/HS MOS fault to the LS/HS turn off	-	-	10	µs

1. Application Information; Test is not performed at high voltage.
2. Design Information Only

Figure 3. MOS settling time and turn-on time 1

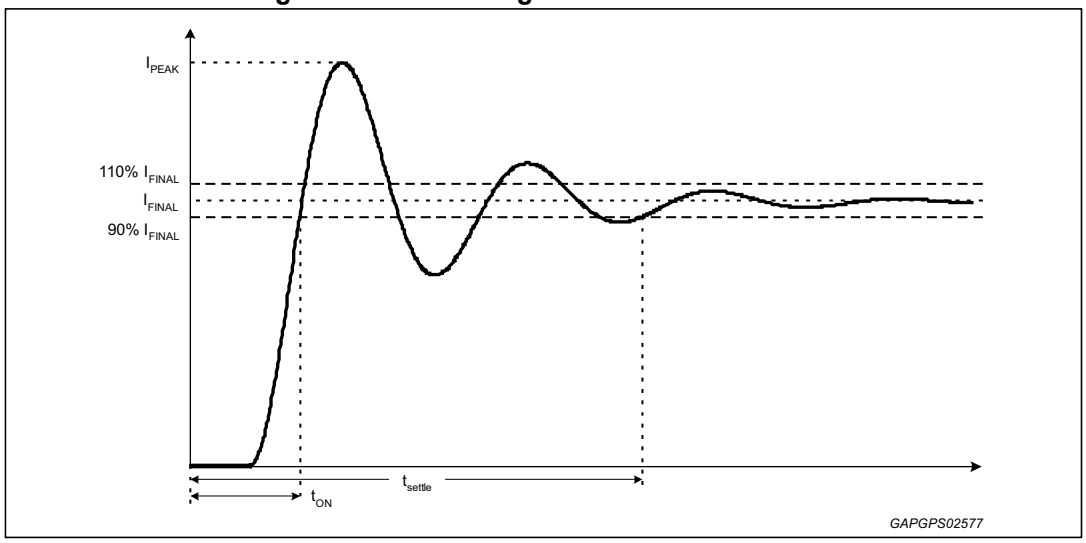
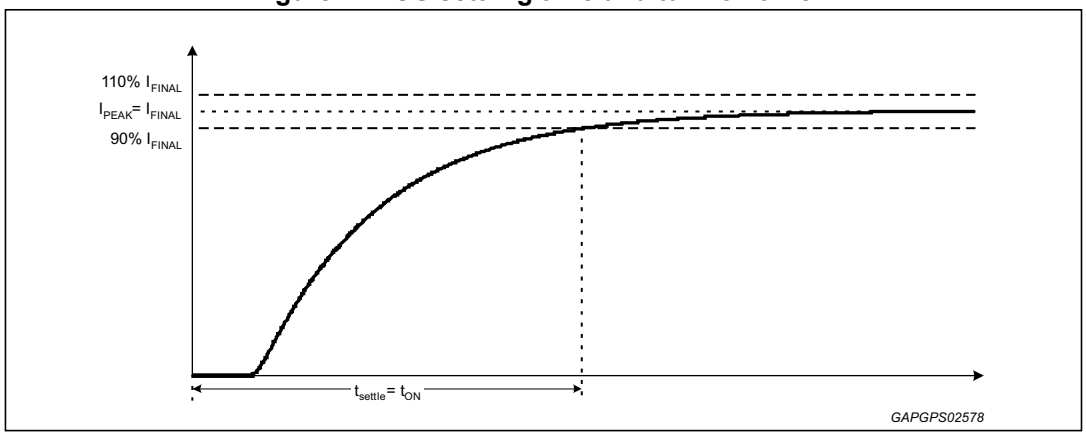


Figure 4. MOS settling time and turn-on time 2



V_{DD} = 4.9 to 5.1 V; V_{8BUCK} = 7.0 V to 8.5 V, T_{amb} = -40 °C to +95 °C

Table 10. AC specifications: satellite

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Osc	Internal oscillator frequency	Tested with 12.5 K 1% Iref resistor	4.45	-	5.55	MHz
Mdf	De-glitch filter as a function of protocol speed	Manchester Protocol Excluding Osc tolerance Bit<8:7≥ 00 Bit<8:7≥ 01 Bit<8:7≥ 10 Bit<8:7≥ 11	11.76 %*Bit-Time	-	23.53 % *Bit-Time	µs
Bitr	Minimum frequency operating range (Incoming messages fall within this operating range is guaranteed to be accepted by the IC)	Channel configurations				
		Bit<8:7≥ 00 Test at frq = 52.33 kHz Test at frq =13.32 kHz	13.32	-	52.33	kHz
		Bit<8:7≥01 Test at frq =110.74 kHz Test at frq = 26.32 kHz	26.32	-	110.74	kHz
		Bit<8:7≥10 Test at frq =164.20 kHz Test at frq = 43.50 kHz	43.50	-	164.20	kHz
		Bit<8:7≥11 Test at frq =250.63 kHz Test at frq = 62.66 kHz	62.66	-	250.63	kHz
Bitr	Maximum frequency operating range (Incoming messages fall outside this operating range is guaranteed to be rejected by the IC)	Channel configurations				
		Bit<8:7≥ 00 Test at frq>59.14 kHz Test at frq <11.99 kHz	11.99	-	59.14	kHz
		Bit<8:7≥01 Test at frq>128.37 kHz Test at frq <23.57 kHz	23.57	-	128.37	kHz
		Bit<8:7≥10 Test at frq>194.93 kHz Test at frq <38.71 kHz	38.71	-	194.93	kHz
		Bit<8:7≥11 Test at frq>309.6 kHz Test at frq <55.37 kHz	55.37	-	309.6	kHz
Idle	Idle time	Manchester	2	-		Bit Times
Flt	Output fault timer	I_sensor>I_lim	300	-	500	µs

V_{RES} = 6.5 to 35 V, V_{DD} = 4.9 to 5.1V. V_{8BUCK} = 7.0 V to 8.5 V, T_{amb} = -40 °C to +95 °C
All SPI timing is performed with a 200 pF load on MISO unless otherwise noted.

Table 11. SPI timing

No.	Symbol	Parameter	Min	Typ	Max	Unit
-	fop	Transfer frequency	dc	-	5.50	MHz
1	t_{SCK}	SCLK, SCLK_A Period	181	-	-	ns
2	t_{LEAD}	Enable Lead Time	65	-	-	ns
3	t_{LAG}	Enable Lag Time	50	-	-	ns
4	t_{SCLKHS}	SCLK, SCLK_A High Time	65	-	-	ns
5	t_{SCLKLS}	SCLK, SCLK_A Low Time	65	-	-	ns
6	t_{SUS}	MOSI, MOSI_A Input Setup Time	20	-	-	ns
7	t_{HS}	MOSI, MOSI_A Input Hold Time	20	-	-	ns
8	t_A	MISO, MISO_A Access Time	-	-	60	ns
9	t_{DIS}	MISO, MISO_A Disable Time (1)	-	-	100	ns
10	t_{VS}	MISO, MISO_A Output Valid Time	-	-	66	ns
11	t_{HO}	MISO, MISO_A Output Hold Time (1)	0	-	-	ns
12	t_{RO}	Rise Time (Design Information)	-	-	30	ns
13	t_{FO}	Fall Time (Design Information)	-	-	30	ns
14	t_{CSN}	CS_A, CS_D, CS_S Negated Time	640	-	-	ns

1. Parameters t_{DIS} and t_{HO} shall be measured with no additional capacitive load beyond the normal test fixture capacitance on the MISO pin. Additional capacitance during the disable time test erroneously extends the measured output disable time, and minimum capacitance on MISO is the worst case for output hold time.

Figure 5. SPI timing diagram

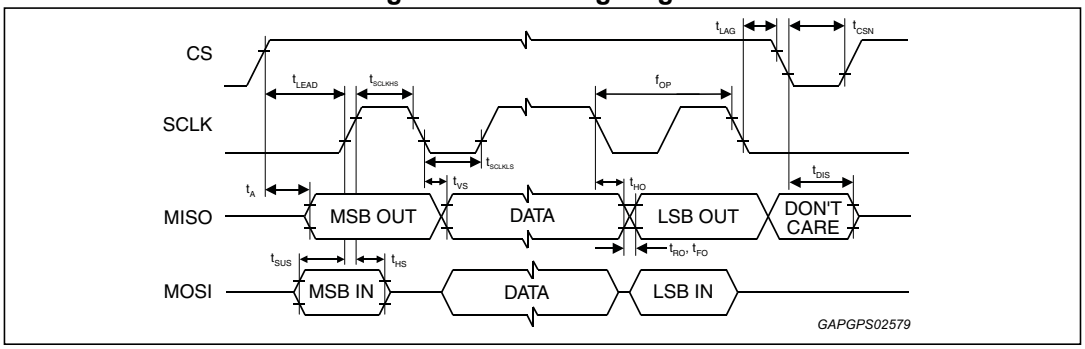
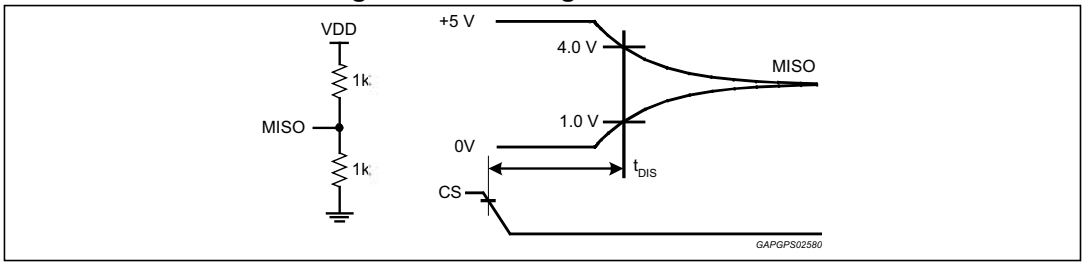


Figure 6. SPI timing measurement



4 Functional description

4.1 Overview

L9654 is an integrated circuit to be used in air bag systems. Its main functions include deployment of air bags, switched-power sources to satellite sensors, diagnostics of SDM (Sensing Deployment Module) and arming inputs. L9654 supports 4 deployment loops, 2 satellite-sensor interfaces, and SPI arming inputs.

4.2 Power on reset (POR)

L9654 has a power on reset (POR) circuit, which monitors V_{DD} voltage. When V_{DD} voltage falls below V_{RST} for longer than or equal to t_{POR}, all outputs are disabled and all internal registers are reset to their default condition.

When V_{DD} falls below V_{RST_L}, all outputs are disabled and all internal registers are reset to their default condition. No delay filter shall be used along with V_{RST_L} threshold.

If V_{DD} voltage falls below V_{RST} for less than t_{POR}, operation shall not be interrupted.

When V_{DD} rises above V_{RST}, the outputs are enabled. Before V_{DD} reaches V_{RST}, and during t_{POR}, none of the outputs turn on.

4.3 RESETB

RESETB pin is active low. The effects of RESETB are similar to those of a POR event, except during a deployment. When L9654 has a deployment in-progress, it ignores the RESETB signal.

However, it shall shut itself down as soon as it detects a POR condition. When the deployment is completed and the RESETB signal is asserted, the device disables its outputs and resets its internal registers to their default states.

A de-glitch timer is provided to the RESETB pin. The timer protects this pin against spurious glitches. UT48 neglects the RESETB signal if it is asserted for shorter than t_{GLITCH}. RESETB has an internal pull-up in case of open circuit. This pin has a de-glitch timer.

4.4 MSG

MSG pin is used to reflect the FIFO status. Its polarity can be configured as well as the strategy of activation.

Polling mode: Message pin shall be active as soon as one of the 4 FIFO is not empty and becomes inactive when all 4 FIFO are empty. A microcontroller can periodically monitor the status of line to understand if there are data received from satellite.

Interrupt mode: Message pin shall be active as soon one of the 4 FIFO is not empty and becomes inactive when an SPI communication on CS_S interface starts. At the end of the SPI communication it shall be active if one of the 4 FIFO is not empty, otherwise it shall be kept inactive. A microcontroller can wait until an edge is present on the line and manage the data available in the FIFO.

4.5 IREF

I_{REF} pin shall be connected to V_{DD} supply through a resistor, R_{IREF}. When the device detects the resistor on I_{REF} pin is larger than R_{IREF_H} or smaller than R_{IREF_L}, it goes in reset condition. All outputs are disabled and all internal registers are reset to their default conditions.

4.6 Loss of ground

When GND pin is disconnected from PC-board ground, L9654 goes in reset condition. All outputs are disabled and all internal registers are reset to their default conditions. A loss of power-ground (GND0 – GND3) pin/s disables the respective channel/s. In other words, the channel that loses its power ground connection is not able to deploy. The rest of the device is not affected by a loss of power-ground condition.

A_{OUT_GND} pin is a reference for A_{OUT} pin. When AOUT_GND loses its connection the reset loses it as well.

4.7 Deployment and reset

The following conditions reset and terminate deployments:

- Power On Reset (POR)
- IREF resistance is larger than RIREF_H or smaller than RIREF_L
- Loss of ground condition on GND pin

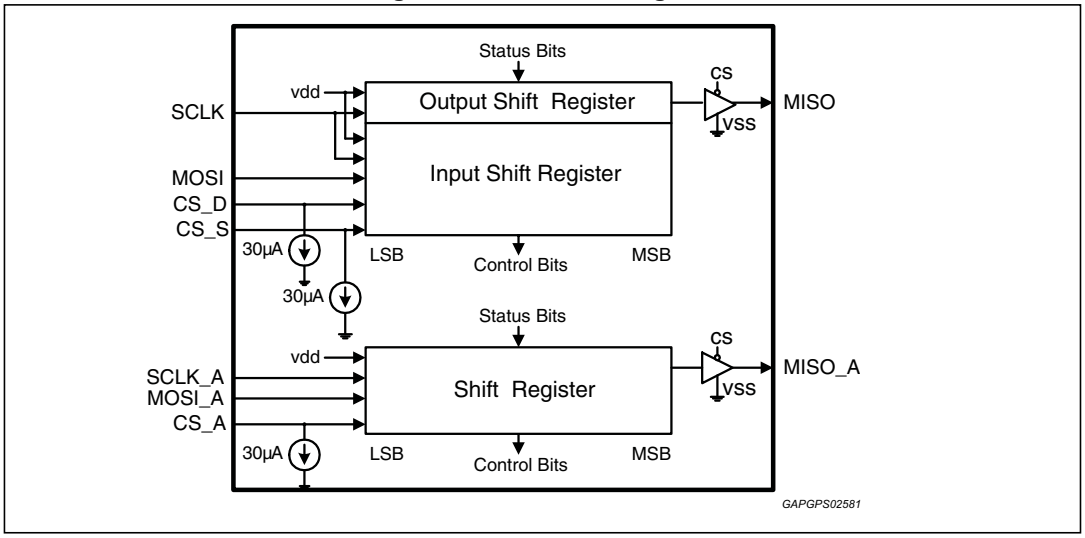
The following conditions are ignored when there is a deployment in-progress:

- RESETB
- Valid soft reset sequences

4.8 Serial peripheral interface (SPI)

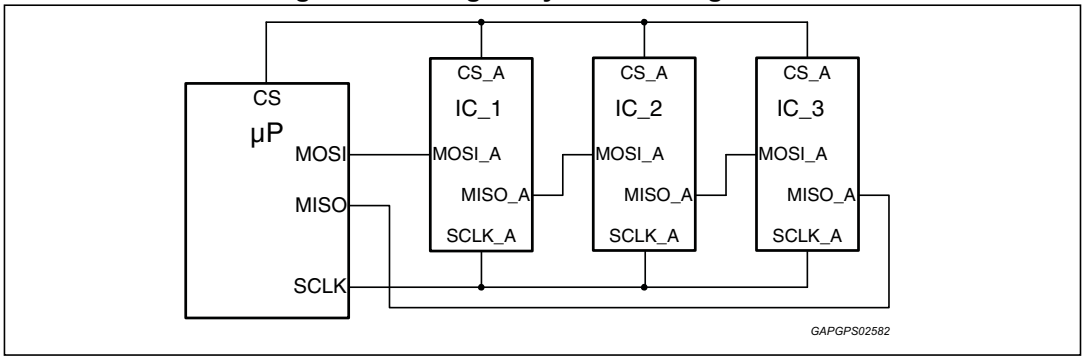
The device contains a serial peripheral interface consisting of Serial Clock (SCLK, SCLK_A), Serial Data Out (MISO, MISO_A), Serial Data In (MOSI, MOSI_A), and two Chip Selects (CS_A, CS_D and CS_S). This device is configured as an SPI slave. The idle state of the communication, Serial Clock (SCLK, SCLK_A) should be in low state.

Figure 7. SPI block diagram



L9654 has a counter to verify the number of clocks in SCLK and SCLK_A. If the number of clocks in SCLK is not equal to 16 clocks while CS_D is asserted, it ignores the SPI message and sends an SPI fault response. If the number of clocks in SCLK is not equal to 64 clocks while CS_S is asserted, it ignores the entire SPI message and pushes the Bad SPI Bit Count fault code into the FIFO. If the number of clocks in SCLK_A is not a multiple of 8, it ignores the command in the arming shift register. Otherwise, the device latches-in the command.

Figure 8. Arming daisy-chain configuration



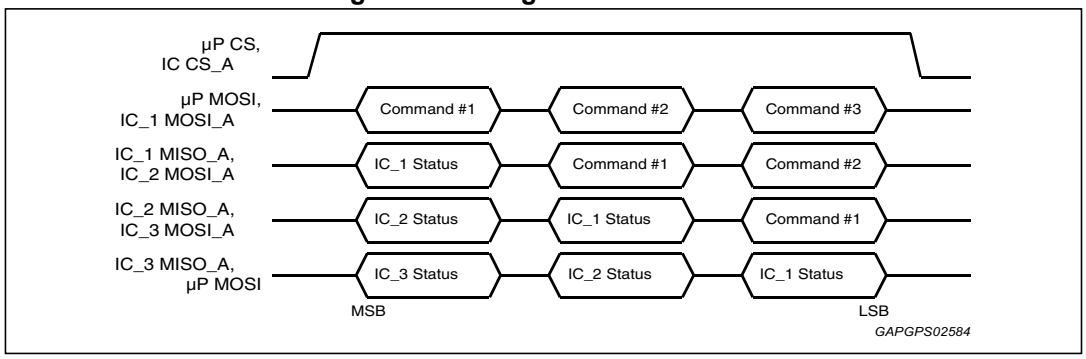
Arming SPI interface is based on 8-bit data transfer. The device is capable of receiving a multiple of 8-bit commands. The first byte of data coming out of MISO_A is the arming status bits. The subsequent bits are the arming command bits received through MOSI_A pin. Refer to below figure for an example of arming SPI transmission. This is an example of arming SPI transmission based on the daisy-chain configuration.

In case of daisy chain connection for arming SPI, device works as following:

All devices IC_1, IC_2, IC_3 shift out data on the falling edge of SCLK_A for the first 8 bits and shift out data on the rising edge of SCLK_A for the bits after 8 bits. Therefore µP, IC_3, IC_2 strobe 24 bits on rising edge of SCLK_A:

- the first 8 bits are produced (by IC_3, IC_2, IC_1 respectively) on the falling edge of SCLK_A.
- the remaining 16 bits are shifted out on the rising edge.

Figure 9. Arming SPI transmission



4.8.1 Chip select (CS_A, CS_D, CS_S)

Chip-select inputs select L9654 for serial transfers. CS_A is independent of CS_D and CS_S.

CS_A can be asserted regardless of CS_D and CS_S. However, either CS_D or CS_S can be asserted at any given time. If both CS_D and CS_S inputs are selected simultaneously, the device ignores MOSI command. When chip-select is asserted, the respective MISO/MISO_A pin is released from tri-state mode, and all status information is latched in the SPI shift register. While chip-select is asserted, register data is shifted into MOSI/MOSI_A pin and shifted out of MISO/MISO_A pin on each subsequent SCLK/SCLK_A. When chip-select is negated, MISO/MISO_A pin is tri-stated. To allow sufficient time to reload the registers, chip-select pin shall remain negated for at least tCSN.

Chip-select is also immune to spurious pulses of 50 ns or shorter (MISO/MISO_A may come out of tri-state, but no status bits are cleared and no control bits are changed).

Chip-select inputs have current sinks on the pins, which pull these pins to the negated state when an open circuit condition occurs. These pins have TTL level compatible input voltages allowing proper operation with microprocessors using a 3.3 to 5.0 volt supply.

4.8.2 Serial clock (SCLK, SCLK_A)

SCLK/SCLK_A input is the clock signal input for synchronization of serial data transfer. This pin has TTL level compatible input voltages allowing proper operation with microprocessors using a 3.3 to 5.0 volt supply. When chip select is asserted, both the SPI master and this device shall latch input data on the rising edge of SCLK/SCLK_A. L9654 shift data out on the falling edge of SCLK/SCLK_A. The SCLK/SCLK_A must be taken in idle state (LOW) when the CS_A,CS_D,CS_S are in idle state (LOW). [a]

4.8.3 Serial data output (MISO, MISO_A)

MISO/MISO_A output pin shall be in a tri-state condition when chip select is negated. When chip select is asserted, the MSB is the first bit of the word/byte transmitted on MISO/MISO_A and the LSB is the last bit of the word/byte transmitted. This pin supplies a rail to rail output, so if interfaced to a microprocessor that is using a lower VDD supply, the appropriate microprocessor input pin shall not sink more than $I_{OH(min)}$ and shall not clamp the MISO/MISO_A output voltage to less than $V_{OH(min)}$ while MISO/MISO_A pin is in a logic “1” state.

a. Only in daisy chain, it is needed to guarantee on SCLK_A a clock skew of 3ns maximum between any devices.

4.8.4 Serial data input (MOSI, MOSI_A)

MOSI/MOSI_A input takes data from the master processor while chip select is asserted.

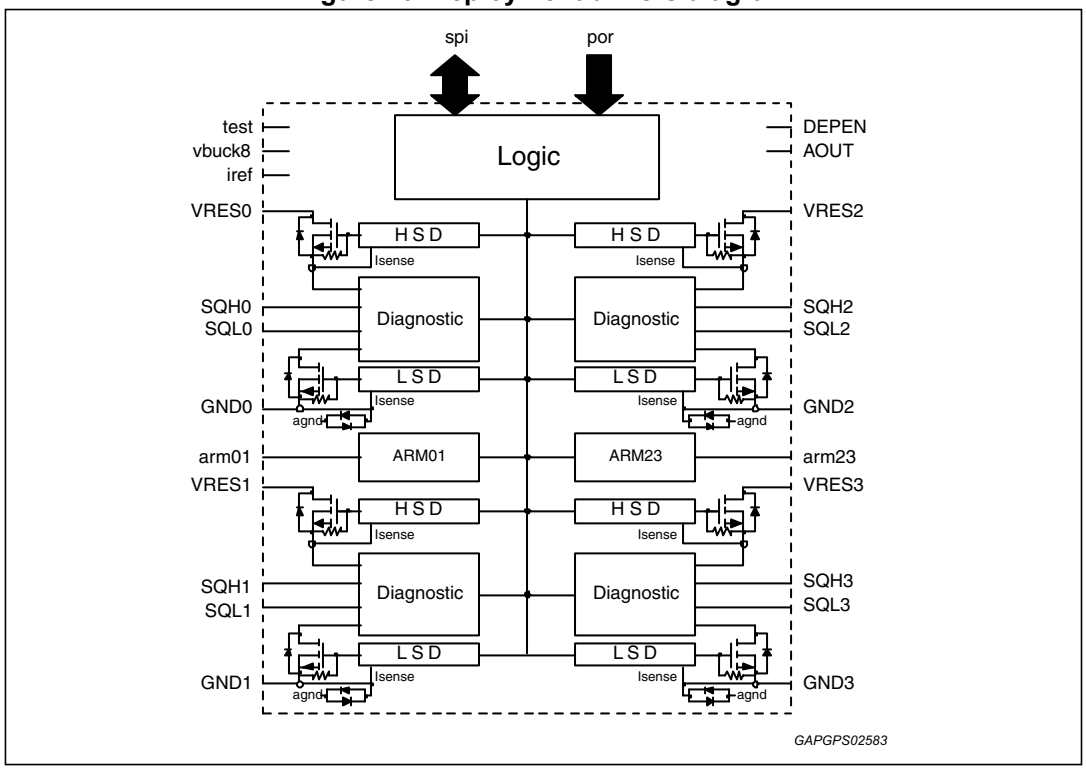
The MSB shall be the first bit of each word/byte received on MOSI/MOSI_A and the LSB shall be the last bit of each word/byte received. This pin has TTL level compatible input voltages allowing proper operation with microprocessors using a 3.3 to 5.0 volt supply.

4.9 Deployment drivers

The on-chip deployment drivers are designed to deliver 1.2 A (mi.n) at 6.9 V VRES. Deployment current is 1.2 A (min.) for 2 ms (min.). The high-side driver survives deployment with 1.47 A, 35 V at VRES and SQL is shorted to ground for 2.5 ms. Minimum load resistance is 1.7. At the end of a deployment, a deploy success flag is asserted via SPI. Each VRES and GND connection are used to accommodate 4 loops that can be deployed simultaneously.

Upon receiving a valid deployment condition, the respective SQH and SQL drivers are turned on. SQH and SQL drivers are also turned on momentarily during a MOS diagnostic. Otherwise, SQH and SQL are inactive under any normal, fault, or transient conditions. Upon a successful deployment of the respective SQH and SQL drivers, a deploy command success flag is asserted via SPI. Refer to "deployment sequence" *Figure 10* for the valid condition and the deploy success flag timing.

Figure 10. Deployment drivers diagram



The following power-up conditions are considered as normal operations . VRES input can be connected to either a power supply output or an ignition voltage. VDD is connected to 5 V output of power supply. When VRES is connected to the power supply, VDD voltage

reaches its regulation voltage before VRES voltage is stabilized. In this condition, the device has the control of its internal logic and that prevents an inadvertent turn-on of the drivers.

When VRES is connected to the ignition, VRES voltage is stabilized before VDD reaches its regulation voltage. In this condition, all drivers are inactive. A pull-down on the gates of high-side drivers (SQH) is provided to prevent these drivers from momentarily turning-on. Any loop driver fault conditions do not turn on the SQH and SQL drivers. Only a valid deployment condition can turn on the respective SQH and SQL drivers.

4.9.1 Arming interface

The arming interface is used as a fail-safe to prevent inadvertent airbag deployment. Along with deployment command, these signals provide redundancy. Pulse stretch timer is provided for each channel/loop. Either ARM signal or deployment command shall start the pulse stretch timer.

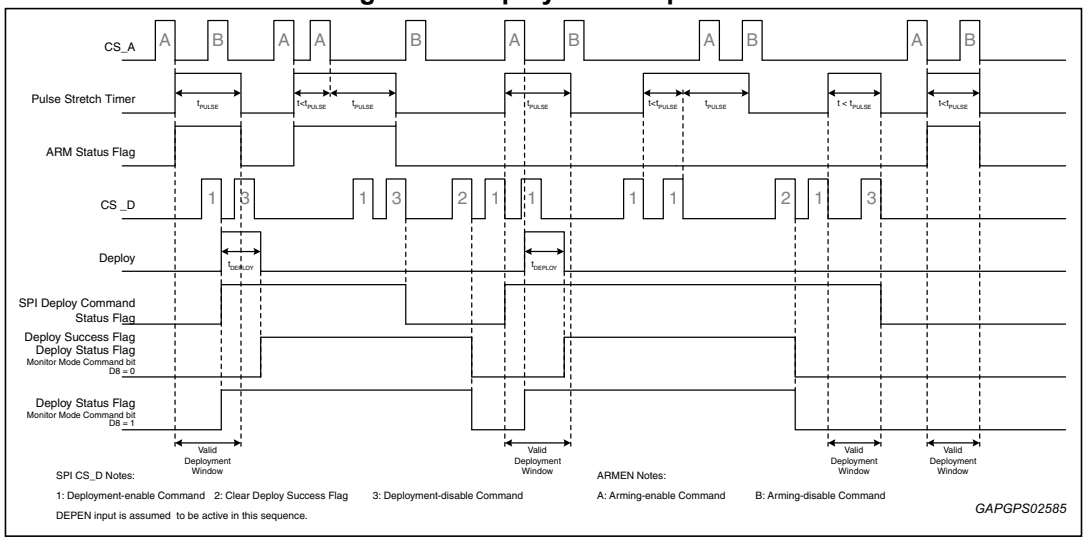
Arming interface has a dedicated 8-bit SPI interface.

When CS_A is negated, L9654 latches ARM signal from the shift register and starts the pulse stretch timer for the respective channel/s. The device can deploy a channel, ONLY when DEPEN is asserted and any of the following conditions are satisfied:

- the respective deployment command is sent during a valid pulse stretch timer, which is initiated by ARM signal
- the respective SPI ARM command is sent during a valid pulse stretch timer, which is initiated by deployment command

During a deployment, the device turns on the respective high-side (SQH) and low-side (SQL) drivers for duration of t_{DEPLOY}. When a deployment is initiated, it can't be terminated, except during a reset event.

Figure 11. Deployment sequence

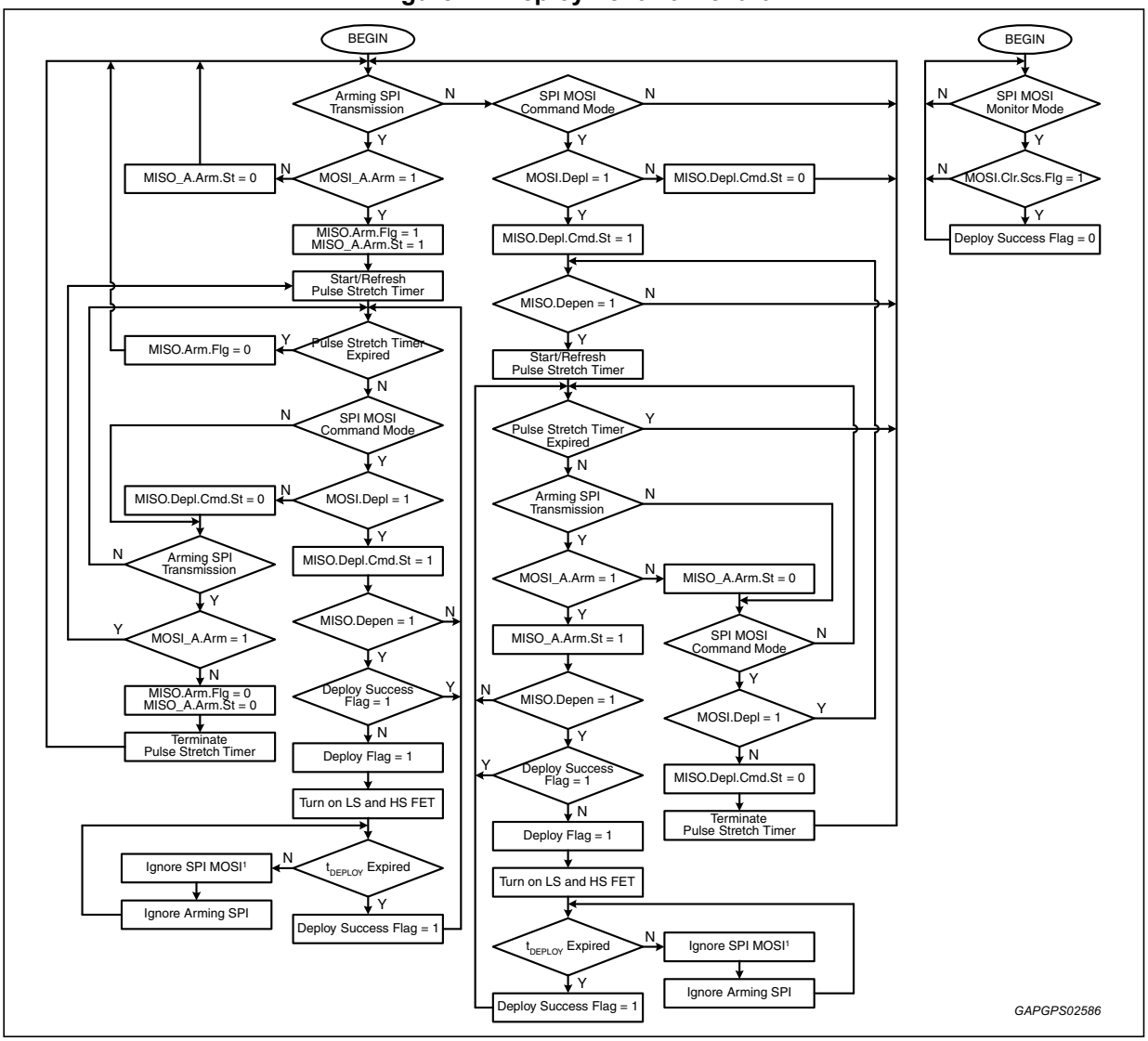


When a deployment-enable command is sent through SPI, the pulse stretcher shall be initiated immediately following the falling edge of CS_D. When another deployment-enable command is sent before the timer for the previous command expired, the timer is refreshed. Sending a deployment-disable command terminates the pulse stretch timer operation. ONLY a timer operation started by a deployment-enable command can be terminated.

A deployment-en/disable command does not affect the timer operation started by arming signal.

When an arming-enable command is sent through SPI, the pulse stretcher is initiated immediately following the falling edge of CS_A. When another arming-enable command is sent before the timer for the previous command expired, the timer is refreshed. Sending an arming disable command terminate the pulse stretch timer operation. ONLY a timer operation started by an arming-enable command can be terminated. An arming-en/disable command does not affect the timer operation started by a valid deployment command.

Figure 12. Deployment flow chart



1. MOSI Register Mode: ignored. Next MISO: SPI fault response
MOSI Command Mode: execute for channels NOT in deployment, NO effect to deploying channel. Next MISO: Command mode response
MOSI Diagnostic Mode: ignored. Next MISO: SPI fault response
MOSI Monitor Mode: execute for all channels. Next MISO: Status response

During the deployment, L9654 turns on the respective high (SQH) and low-side (SQL) drivers for t_{DEPLOY}. Once deployment is initiated it cannot be terminated. When a channel is in deployment, this particular channel shall only act upon certain SPI messages. These SPI

messages and their responses are summarized in the below table. The rest of the channels shall resume their operations and respond to specific SPI commands.

During a deployment, the device ignores arming commands. and does not refresh or terminate the pulse stretch timer when it receives an arming command.

Table 12. SPI transmission during a deployment

SPI MOSI	SPI MISO(1)	Notes
Register mode	SPI fault response	MOSI register mode message shall be ignored
Command mode	Command mode	Execute for channels not in deployment; no effect to deploying channel
Diagnostic mode	SPI fault response	MOSI diagnostic mode message shall be ignored
Monitor mode	Status response	Execute for all channels

1. SPI MISO sent in the next SPI transmission.

4.10 DEPEN

DEPEN is a deployment enable input, which is an active high input. When this pin is asserted, L9654 is able to turn on its high and low-side drivers upon receiving a valid deployment command or a MOS diagnostic request. DEPEN cannot interrupt a deployment that is already in-progress.

When DEPEN is negated, it inhibits the low-side and the high-side MOS from turning on (inhibit the deployment). When a MOS diagnostic is requested, the device executes the diagnostic even without the ability to turn on the MOS. It sets the proper SPI threshold bits. SPI remains functional while this pin is pulled low.

When DEPEN is negated, SPI deploy command is prevented from initiating the pulse stretch timer. Regardless of DEPEN, “SPI deploy command” status bits reports the state of “SPI deploy command” bits sent in the previous SPI transfer. This feature is required so that the processor can diagnose SPI deploy command bits with DEPEN negated.

Regardless of DEPEN, arming signal is able to initiate the pulse stretch timer. This feature is used for the processor to diagnose the arming signal.

When the pulse stretch timer has been running, changes in the state of DEPEN do not affect the pulse stretch timer. The pulse stretch timer is not affected regardless of the pulse stretch timer being started by an arming signal or an SPI deploy command.

A de-glitch timer is provided to DEPEN pin. The timer protects this pin against spurious glitches. The device neglects DEPEN signal if it is asserted/negated for shorter than t_{GLITCH}.

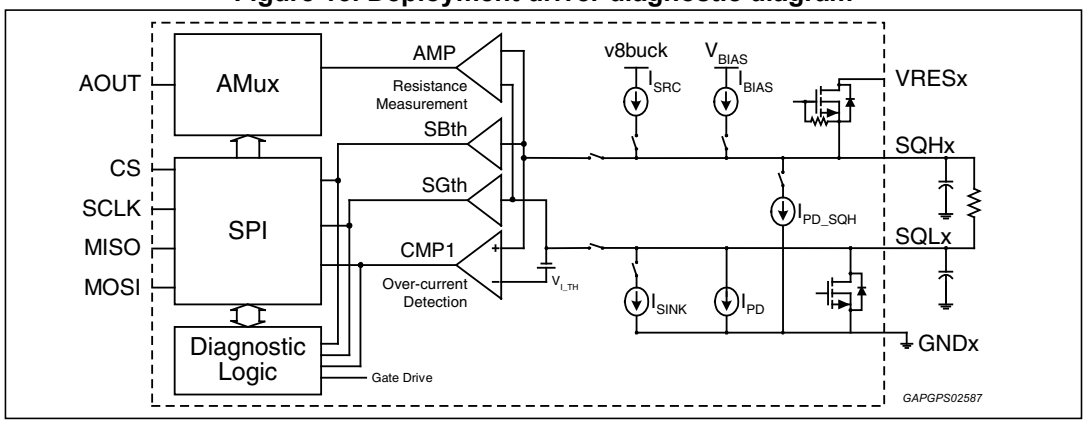
4.10.1 Deployment driver diagnostic

L9654 is able to perform a short to battery, a short to ground, a resistance measurement and a MOS diagnostics on its deployment drivers. A short to ground and an open circuit conditions are distinguished using a resistance measurement. Here below is shown the diagram of deployment driver diagnostic.

The diagnostic is performed when a valid SPI command is received. Each current source (I_{SRC} and I_{BIAS}) and current sink (I_{SINK}, I_{PD_SQH}) is turned on or off by an SPI command. I_{PD_SQH} is turned on when I_{BIAS} is turned on. This pull-down (I_{PD_SQH}) is used to deplete the charge left on the SQH and SQL capacitors. IPD is permanently connected to SQL. This current sink pulls down SQL pin during an open circuit condition.

Diagnostic current source or sink and comparator or amplifier are independent. It is possible to turn on or off the current source or sink on a specific channel, while monitoring the comparator or amplifier on a different channel. This feature is used to run a short between loop diagnostic.

Figure 13. Deployment driver diagnostic diagram

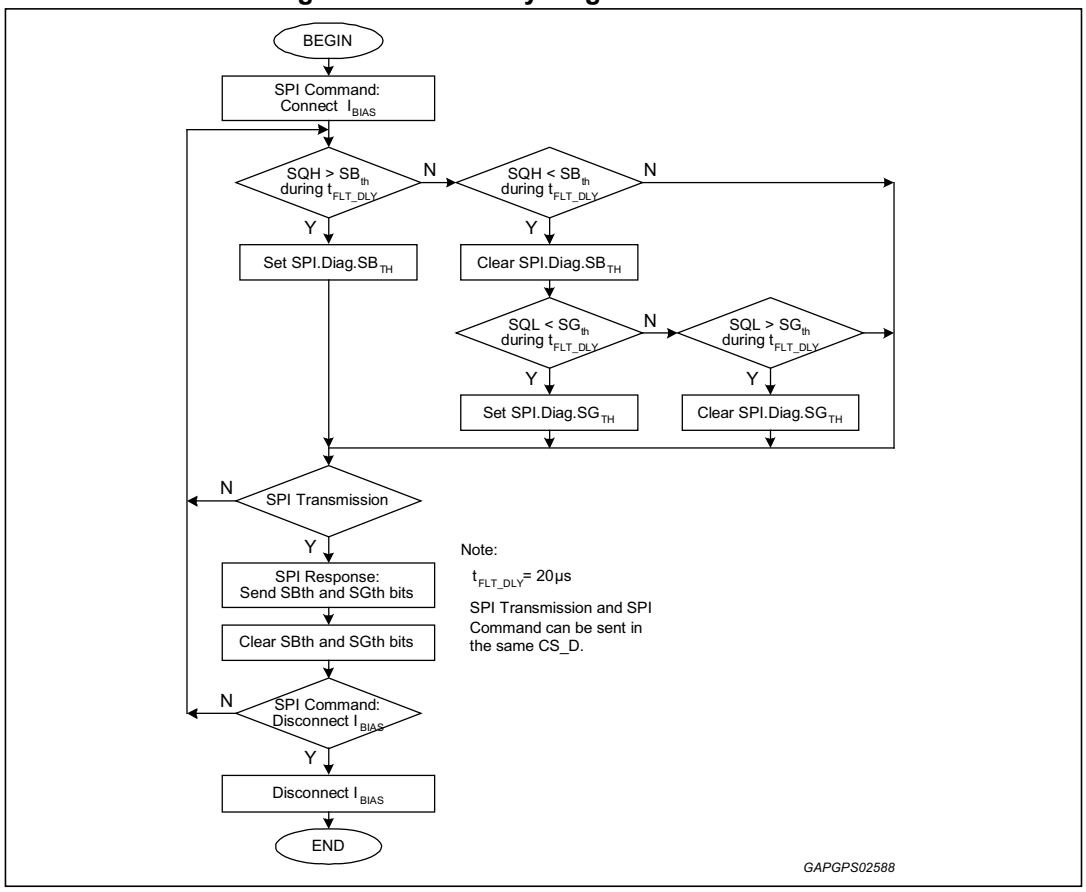


4.10.2 Continuity diagnostic

A continuity diagnostic includes a short to battery, a short to ground and an open circuit diagnostic.

During a continuity diagnostic, IBIAS is switched on. On a normal loading condition, SQH voltage is below SBTH threshold and SQL voltage is above SGTH threshold.

Figure 14. Continuity diagnostic flow chart



4.10.3 Short to battery

A short to battery condition is detected when the voltage on SQH is greater than SBTH threshold voltage.

4.10.4 Short to ground and open circuit

A short to ground or an open circuit condition is detected when the voltage on SQL is less than SGTH threshold voltage. A resistance measurement is utilized to differentiate between a short to ground or an open circuit condition.

4.10.5 Resistance measurement

During a resistance measurement, both I_{SRC} and I_{SINK} are switched on. An analog voltage on A_{OUT} pin is provided. A_{OUT} pin is a 5V analog pin, which is connected to the ADC input of a processor. This pin provides the resistance-measurement voltage, which corresponds to the voltage difference across SQH and SQL according to the following formula:

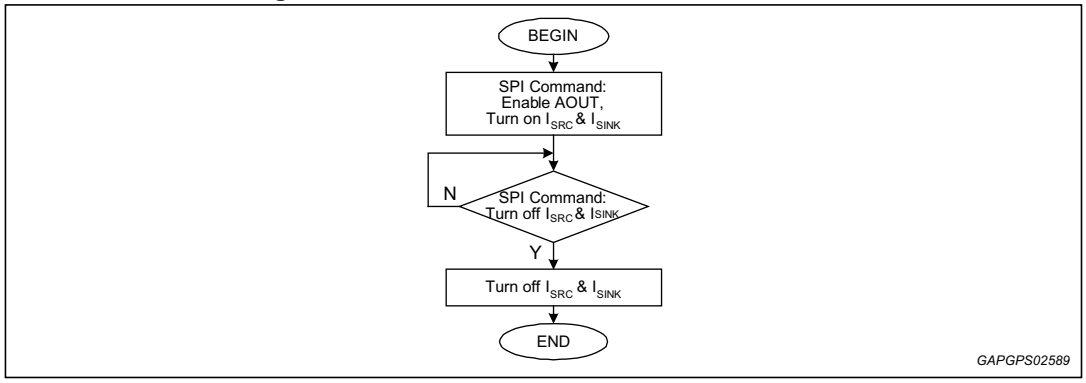
$$V_{aout} = V_{DD}/10 + R_{squib} \cdot I_{src} \cdot 10.$$

The accuracy in the range of R_{squib} is classified as followings:

$0 < R_{squib} \leq 3.5\ \Omega$ ±95 mV
$3.5 < R_{squib} \leq 10\ \Omega$ ±5 %

A low pass filter (10 kΩ + 330 pF) is recommended in order to cancel the noise caused by internal offset compensation.

Figure 15. Resistance measurement flow chart



4.10.6 MOS diagnostics

During diagnostic, I_{BIAS} is connected to SQH pin. In a normal condition, SQH voltage is below SB_{TH} and SQL voltage is higher than SGTH. Prior to turning on the MOS, the processor is expected to check for a short to battery and a short to ground fault. This step is intended to prevent a large amount of current from flowing through the MOS. Also, this step is intended to precondition SQH and SQL pins prior to diagnostics. DEPEN pin is asserted in order to turn on the low or high-side driver. If DEPEN is negated during diagnostic, the MOS is not turned on and a fail MOS diagnostic is expected.

4.10.7 Low-side MOS diagnostic

When L9654 receives an SPI command to initiate the low-side driver diagnostic, verification of following conditions is done before turning on the low-side driver:

- V_{SQL} greater than SG_{TH} threshold voltage
- V_{SQH} less than SBT_H threshold voltage

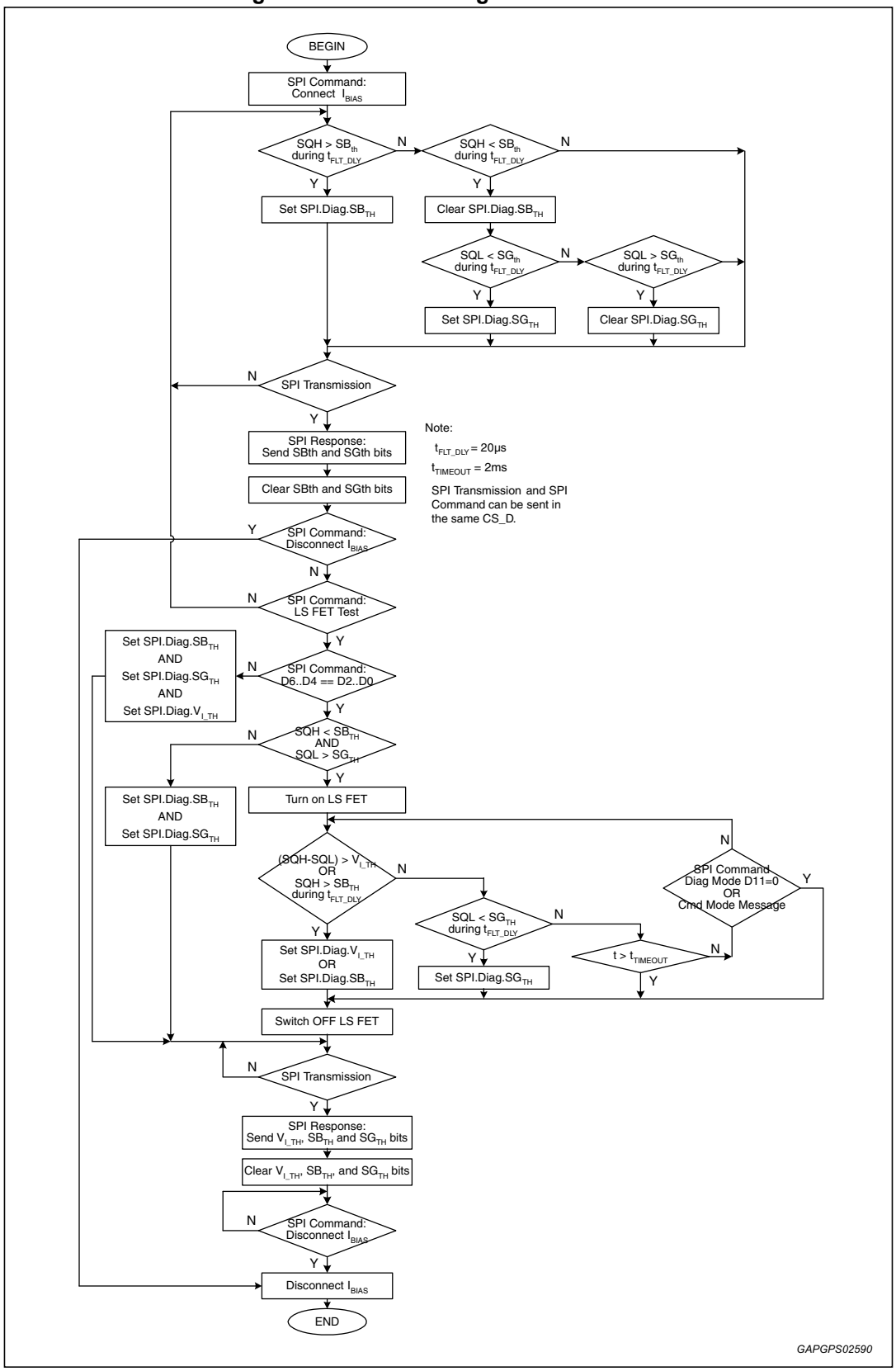
If both conditions above are satisfied, execution of low-side driver diagnostic is performed. Otherwise, the low-side MOS diagnostic request is ignored and both bit D13 and bit D7 in SPI diagnostic mode response are set. Upon detection of the following conditions, the device turns the low-side driver off and terminates the diagnostic within the specified time, t_{PROP_DLY}.

- V_{SQL} less than SG_{TH} threshold voltage
- (V_{SQHx} – V_{SQLx}) greater than V_{I_TH}
- V_{SQH} greater than SB_{TH} threshold voltage

The state of each comparator above is reported through SPI. When the device detects one of the above conditions, the respective SPI status bit indicates that the condition is set. Any of the above conditions is considered as normal in a low-side MOS diagnostic.

The low-side driver is turned off when $t_{TIMEOUT}$ is expired. A fault detection filter, t_{FLT_DLY}, is provided to protect against short-transients on SQH and SQL pins.

Figure 16. Low-side diagnostic flow chart



4.10.8 High-side MOS diagnostic

When L9654 receives an SPI command to initiate the high-side MOS diagnostic, the following conditions are verified before turning on the high-side MOS:

- V_{SQL} greater than SG_{TH} threshold voltage
- V_{SQH} less than SB_{TH} threshold voltage

If both conditions above are satisfied, the high-side MOS diagnostic is executed. Otherwise, it is ignored and both bit D13 and bit D7 in SPI diagnostic are set.

Upon detection of the following conditions, the high-side driver is turned off and the diagnostic, within the specified time, t_{PROP_DLY}, is terminated

- V_{SQH} greater than SB_{TH} threshold voltage
- (V_{SQHx} – V_{SQLx}) greater than V_{I_TH}
- V_{SQL} less than SG_{TH} threshold voltage

The state of each comparator above is reported through SPI. When L9654 detects one of the above conditions, it sets the respective SPI status bit to indicate the condition. Any of the above conditions is considered as normal in a high-side MOS diagnostic.

The high-side driver is turned off when $t_{TIMEOUT}$ is expired. A fault detection filter, t_{FLT_DLY}, is provided to protect against short-transients on SQH and SQL pins.

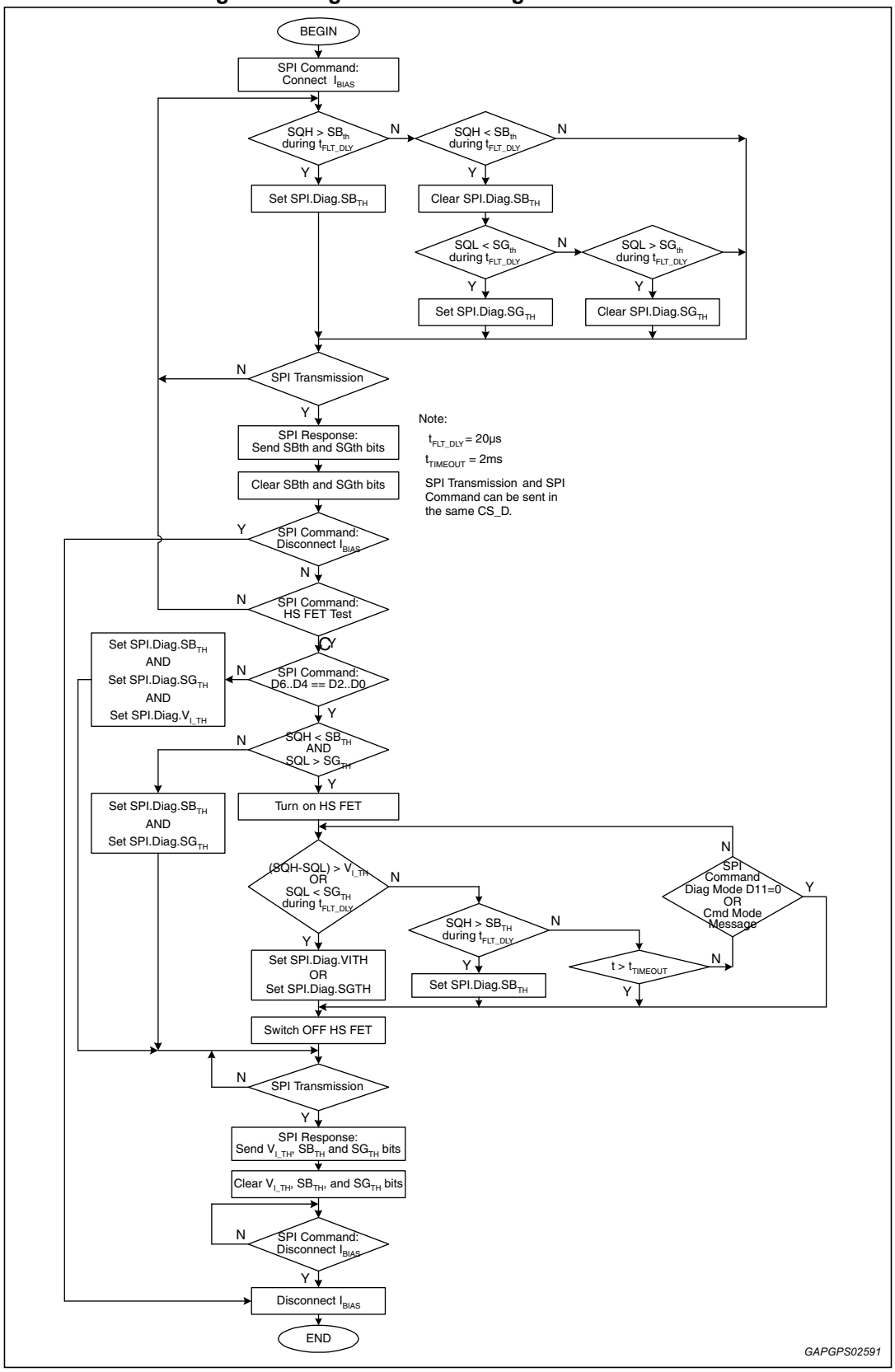
4.10.9 Loss of ground

When any of the power grounds (GND0 – 7) are lost, no deployment can occur to the respective deployment channels. A loss of ground condition on one or several channels does not affect the operation of the remaining channels.

When a loss of ground condition occurs, the source of the low-side MOS is floating. In this case, no current flows through the low-side driver.

This condition is detected as a fault by a low-side MOS diagnostic. Also, the resistance measurement result is on the low end of the resistance range.

Figure 17. High-side driver diagnostic flow chart



4.11 Deployment driver SPI bit definition

The SPI provides access to read/write in the registers which are internal to the device, whose responses to various deployment driver commands are summarized in the table below.

L9654 response to the previous command is sent in the next valid CS_D.

Table 13. Deployment driver SPI response

Mode bits		MOSI command	Mode bits			MISO response
D15	D14		D15	D14	D13	
0	0	Register Mode	0	0	0	Register Mode
0	1	Command Mode	0	1	0	Command Mode
1	0	Diagnostic Mode	1	0	X	Diagnostic Mode
1	1	Monitor Mode	1	1	0	Status Response
X	X	SPI Transmission Fault	1	1	1	SPI Fault Response

4.11.1 Deployment driver MOSI bit definition

Table 14. MOSI bit layout

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

MOSI mode bits are defined as shown in the below table.

Table 15. MOSI mode bits definition

Bit D15	Bit D14	Description
0	0	Register Mode
0	1	Command Mode
1	0	Diagnostic Mode
1	1	Monitor Mode

4.11.2 Deployment driver register mode

Register mode message are defined here below.

Table 16. MOSI register mode message definition

Bit	State	Description
D15	0	Mode bits
D14	0	
D13		Odd Parity
D12	0	Read (default)
	1	Write
D11	0	Pulse Stretch Timer Period
	1	Soft Reset Sequence
D10	0	Deployment Condition: I_{DEPLOY_12A} and t_{DEPLOY_2ms}
	1	Deployment Condition: I_{DEPLOY_175A} and t_{DEPLOY_1ms}
Bit	State	Description
D9		Pulse Stretch timer (see table 17)
D8		
D7		Soft Reset Sequence
D6		
D5		
D4		
D3		
D2		
D1		
D0		

Odd parity check includes all 16 bits. “Don’t care” bit is included in the parity check as well.

When bit D12 is set to ‘0’, device ignores bit D11 through bit D0. This is a read request. In the next valid CS_D, a register mode response contains the pulse stretch timer register.

If bit D12 is set to ‘1’, bit D11 determines whether the message is intended to program the duration of the pulse stretch timer or to address the soft reset sequence.

When bit D11 is set to ‘0’, device ignores bit D7 through bit D0. When bit D11 is set to ‘1’, bit D9 and bit D8 are ignored.

Bit D10 is used to select between two deployment conditions. When bit D10 is set to 0, deployment events on all channels shall have the deployment current of I_{DEPL_12A} and the deployment period of t_{DEPL_2ms}. When bit D10 is set to 1, deployment events on all channels shall have the deployment current of I_{DEPL_175A} and the deployment period of t_{DEPL_1ms}. The default state of this bit shall be ‘0’.

Bit D9 and bit D8 are used to set the period of pulse stretch timer.

The device have 8 independent timers. Either a valid arming signal or a SPI deployment command is able to start the pulse stretch timer. These bits sets the timer duration. These values default to ‘00’ after a POR event.

Table 17. Pulse stretch timer table

Bit D9	Bit D8	Stretch period (ms)
0	0	7.5
0	1	15
1	0	30
1	1	60

Bit D7 through bit D0 are used for a soft reset sequence. The soft reset for the deployment driver is achieved by writing $AA and $55 within two subsequent 16-bit SPI transmissions. If the sequence is broken, the processor is required to re-transmit the sequence.

L9654 does not reset if the sequence is not completed within two subsequent 16-bit SPI transmissions. This soft reset function is available only to deployment drivers.

When soft reset command is received, the device resets its deployment driver’s internal logic and timer. The effects of soft reset to the deployment driver is the same as the one of POR event, except for MISO response.

During a deployment, soft reset sequence is ignored.

4.11.3 Deployment driver command mode

Command Mode message is defined as shown below.

Table 18. MOSI command mode message definition

Bit	State	Description
D15	0	Mode bits
D14	1	
D13		Odd Parity
D12	-	Don’t Care
D11	-	Don’t Care
D10	-	Don’t Care
D9	-	Don’t Care
D8	-	Don’t Care
D7	0	Channel 7 Idle (default)
	1	Deploy Channel 7
D6	0	Channel 6 Idle (default)
	1	Deploy Channel 6

Table 18. MOSI command mode message definition (continued)

Bit	State	Description
D5	0	Channel 5 Idle (default)
	1	Deploy Channel 5
D4	0	Channel 4 Idle (default)
	1	Deploy Channel 4
D3	0	Channel 3 Idle (default)
	1	Deploy Channel 3
D2	0	Channel 2 Idle (default)
	1	Deploy Channel 2
D1	0	Channel 1 Idle (default)
	1	Deploy Channel 1
D0	0	Channel 0 Idle (default)
	1	Deploy Channel 0

Odd parity check includes all 16 bits. “Don’t care” bit is included in the parity check as well.

Bit D7 to bit D0 are used to start the deployment or the pulse stretch timer. L9654 provides an independent timer for each channel. When any of these bits are set to ‘1’, device starts the deployment or the pulse stretch timer for the respective channels.

If any of these bits is set to ‘0’ when the pulse stretch timer is still active, the pulse stretch timer for the respective channels is terminated. Once deployment is initiated, it cannot be terminated.

During a deployment, any commands directed to the channel that are in deployment are ignored.

4.11.4 Deployment driver diagnostic mode

Diagnostic Mode message are defined as shown here below.

Table 19. MOSI diagnostic mode message definition

Bit	State	Description
D15	1	Mode bits
D14	0	
D13		Odd Parity
D12	0	Read Diagnostic Mode Response (default)
	1	Write Diagnostic Mode Command
D11	0	MOS Diagnostic Disable (default)
	1	MOS Diagnostic Enable
D10	0	LS MOS Diagnostic Enable
	1	HS MOS Diagnostic Enable

Table 19. MOSI diagnostic mode message definition (continued)

Bit	State	Description
D9	0	Diagnostic Current Disable (default)
	1	Diagnostic Current Enable
D8	0	Diagnostic Bias Current, I_{BIAS}, Enable
	1	Resistance Measurement Current, I_{SRC}, Enable
D7	0	AOUT Disable (default)
	1	AOUT Enable
D6		AOUT/Comparator Channel Select
D5		
D4		
D3	0	AOUT: Resistance Measurement (default)
	1	AOUT: Calibration
D2		Diagnostic Current: Channel Select
D1		
D0		

Odd parity check includes all 16 bits. “Don’t care” bit is included in the parity check as well.

When bit D12 is set to ‘1’, device executes bit D12 through bit D0. Otherwise, bit D12 through bit D0 is ignored. Diagnostic Mode Response is sent in the subsequent SPI transmission regardless of bit D12.

The diagnostic currents comprise of diagnostic bias current (I_{BIAS}) and resistance measurement current (I_{SRC}). Diagnostic bias current is used to run continuity tests, e.g. short to battery, short to ground, and open circuit tests. During a resistance measurement, I_{SRC} and I_{SINK} is turned on.

I_{SRC} and I_{SINK} are turned on when bit D8 is ‘1’, bit D9 is ‘1’, bit D11 is ‘0’, and bit D12 is ‘1.’ Otherwise, I_{SRC} and I_{SINK} are off. When bit D11 is set to ‘1’, MOS diagnostic is enabled. Depending upon the state of bit D10, either a low-side MOS or a high-side MOS is switched on. When bit D 11 is set to ‘0’, MOS diagnostic is disabled and bit D10 ignored. When bit D9 is set to ‘1’, a diagnostic current source is enabled. Bit D8 determines if I_{BIAS} or I_{SRC} is switched on. When bit D9 is set to ‘0’, the diagnostic current sources is disabled and bit D8 ignored. Bit D2 through bit D0 selects a specific channel, which is connected.
The decoding scheme of this channel selection is shown ahead.

It is possible to select current source and AOUT independently. Only one channel can source a diagnostic current at a given time. AOUT is connected to one channel at one time as well. The diagnostic current and AOUT can be connected to the same channel as well as to different channels. In this configuration, a short between loop diagnostic can run. Diagnostic of multiple devices requires the ability to turn on a current source in one device, while reading AOUT voltage of another device. The differential amplifier reflects the scaled voltage across SQH and SQL pins. AOUT is connected to the differential amplifier. Externally, AOUT pin is connected to an ADC input of a processor. When bit D7 is set to ‘1’, AOUT output is enabled. Otherwise, AOUT is in a high impedance state. Multiple devices

may be connected to a single ADC input of a processor. If an AOUT is driven, the rest of AOUT shall be driven to the high-impedance state.

Bit D6 through bit D4 select a specific channel, which is monitored. If AOUT output is enabled, AOUT shall reflect the voltage on the selected channel. Also, SB_{TH} and SG_{TH} status bits shall report the status of the respective channel. The decoding scheme of this channel selection is shown in the following table. The default states of these bits are '0' (channel 0 selected).

Table 20. Channel selection decoding

Bit D6	Bit D5	Bit D4	Channel selected
Bit D2	Bit D1	Bit D0	
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	X	X	Don't' Care

Bit D3 is used to calibrate AOUT. If this bit is set to '1', AOUT pin contains the calibration voltage. The processor can use this calibration voltage to make adjustment to the subsequent resistance measurement reading. This is intended to improve the accuracy of the resistance measurement. When this bit is set to '0', AOUT pin contains the resistance measurement results.

The default state of this bit is '0.'

4.11.5 Deployment driver monitor mode

Monitor Mode message is defined as shown in the following table.

Table 21. MOSI monitor mode message definition

Bit	State	Description
D15	1	Mode bits
D14	1	
D13	-	Odd Parity
D12	-	Don't Care
D11	-	Don't Care
D10	-	Don't Care
D9	-	Don't Care
D8	0	Report Deploy Success Flag (default)
	1	Report Deployment OR Deploy Success Flag
D7	-	Don't Care
D6	-	Don't Care

Table 21. MOSI monitor mode message definition (continued)

Bit	State	Description
D5	-	Don't Care
D4	-	Don't Care
D3	0	Keep Deploy Success Flag Channel 0 (default)
	1	Clear Deploy Success Flag Channel 0
D2	0	Keep Deploy Success Flag Channel 2 (default)
	1	Clear Deploy Success Flag Channel 2
D1	0	Keep Deploy Success Flag Channel 1 (default)
	1	Clear Deploy Success Flag Channel 1
D0	0	Keep Deploy Success Flag Channel 0 (default)
	1	Clear Deploy Success Flag Channel 0

Odd parity check includes all 16 bits. "Don't care" bit is included in the parity check as well.

Bit D8 is used to select the meaning of bit D3 through bit D0 in the status response message.

When this bit is set to '1', bit D3 through D0 in the status response message report the deployment status OR the deploy success flag. Once the deployment starts, bit D3 through bit D0 report '1' until the deploy success flag is cleared. Bit D3 through bit D0 shall not report '0' before the deploy success flag is cleared.

The default state of this bit is '0.' When this bit is '0', bit D3 through bit D0 in the status response message report the deploy success flag. Deploy success flags are cleared by bit D3 through bit D0 in the monitor mode command. Deployment status bits report the deployment state. If the deployment is active during a rising edge of CS_D, deployment status bits is set to '1.' Otherwise, is set to '0.'

If bit D8 in the monitor mode command changes state, bit D3 through bit D0 report the proper states of the internal signals/flags. Deploy command success bit indicates if the corresponding channel has finished its deployment sequence. This bit is set when deployment period, t_{DEPLOY}, has expired.

Once this bit is set, it inhibits the subsequent deployment command until a SPI command, to clear this deployment success flag, is received. Bit D3 through bit D0 is used to clear/keep the deploy success flag. When these bits are set to '1', the flag can be cleared. Otherwise, the state of these flags is not affected.

4.11.6 Deployment driver MISO bit definition

Table 22. MISO bit layout

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

MISO mode bits are defined as below table.

Table 23. MISO mode bits definition

Bit D15	Bit D14	Description
0	0	Register Mode Response
0	1	Command Mode Response
1	0	Diagnostic Mode Response
1	1	Status Response/SPI Fault Response

4.11.7 Deployment driver register mode response

Register Mode Response is the default response to the processor. After a POR event, a RESETB negated, and a loss of GND, the device sends $0000 in MISO for the first SPI transmission. Register Mode Response is defined as shown in the following table.

Table 24. MISO register mode response definition

Bit	State	Description
D15	0	Mode bits
D14	0	
D13	0	Don't Care
D12	-	Echo of MOSI Read/Write bit
D11	0	Pulse Stretch Timer Duration
	1	Soft Reset Sequence
D10	0	Deployment Condition: I_{DEPLOY_12A} and t_{DEPLOY_2ms}
	1	Deployment Condition: I_{DEPLOY_175A} and t_{DEPLOY_1ms}
D9	-	Pulse Stretch timer (see table 17)
D8	-	
D7	-	Don't Care
D6	-	Don't Care
D5	-	Don't Care
D4	-	Don't Care
D3	-	Don't Care
D2	1	Always 1
D1	-	Hard Reset Status
D0	-	Soft Reset Sequence Status

Bit D12 is used to reflect the status of MOSI Read/Write bit.

Bit D11 is used to reflect the MOSI bit D11 in the previous command.

Bit D10 is used to indicate the deployment condition set in L9654. Refer to *Section 4.11.1* for deployment condition bit in MOSI register mode message.

Bit D9 and bit D8 are used to report the period of the pulse stretch timer.

Bit D1 is used to indicate a "hard-reset" event. This bit is de-asserted ('0'), when POR is detected, RESETB is asserted, RIREF is out-of-range, or GND connection is lost. This bit is set to '1,' after the bit has been read. A soft reset sequence does not affect this bit.

Bit D0 is used to report the soft reset sequence status. If valid soft reset sequences are received, bit D0 is set to ‘1.’ Otherwise, bit D0 is set to ‘0.’

When L9654 receives valid soft reset sequences, it sends MISO register mode response containing $0001 in the next SPI transmission.

4.12 MISO register mode response summary

Table 24 below summarizes the MISO register mode response of various events and MOSI messages. The MOISO response shown here is the one received in the next valid SPI transmission after each event or MOSI write.

Table 25. MISO register mode response summary

Event/MOSI message	MISO response
POR	$0004
RESETB	$0004
Loss of GND	$0004
R_{IREF} out of range	$0004
MOSI Write Soft Reset: $AA	$1806
MOSI Write Soft Reset: $55 (after $AA)	$0007
MOSI Write Pulse Stretch Timer	$1X06

4.12.1 Deployment driver command mode response

Command Mode response is defined as shown here after.

Table 26. MISO command mode response definition

Bit	State	Description
D15	0	Mode bits
D14	1	
D13	-	Don't Care
D12	0	DEPEN Negated
	1	DEPEN Asserted
D11	0	Don't Care
D10	0	Don't Care
D9	0	ARM23 Negated
	1	ARM23 Asserted
D8	0	ARM01 Negated
	1	ARM01 Asserted
D7	-	Don't Care
D6	-	Don't Care
D5	-	Don't Care
D4	-	Don't Care
D3	-	SPI Deploy Command Status: Channel 3
D2	-	SPI Deploy Command Status: Channel 2
D1	-	SPI Deploy Command Status: Channel 1
D0	-	SPI Deploy Command Status: Channel 0

DEPEN status flag (bit D12) indicates the state of DEPEN pin.

ARM status flag (bit D11 through bit D8) indicates the state of the respective arming signal, including the pulse stretch timer. If the pulse stretch timer is initiated by a deployment command, it shall not assert the arming status flag. This flag is negated as soon as the de-glitch timer is expired. ARM status flag is an OR-function of arming states from two channels.

SPI deploy command status flag indicates the SPI deployment status for the respective channel. These flags reflect bit D3 through bit D0 of the most recent SPI command mode message.

These bits do not include the status of pulse stretch timer. These bits are overwritten by the most recent SPI command mode message.

4.12.2 Deployment driver diagnostic mode response

Diagnostic mode response is defined as shown in table.

Table 27. MISO diagnostic mode response definition

Bit	State	Description
D15	1	Mode bits
D14	0	
D13	0	SQH voltage below SB_{TH} threshold
	1	SQH voltage above SB_{TH} threshold
D12	0	DEPEN Negated
	1	DEPEN Asserted
D11	0	MOS Diagnostic Completed
	1	MOS Diagnostic In-progress
D10	0	LS MOS Diagnostic selected
	1	HS MOS Diagnostic selected
D9	0	Diagnostic Current OFF
	1	Diagnostic Current ON
D8	0	Diagnostic Bias Current, I_{BIAS} selected
	1	Resistance Measurement Current, I_{SRC} selected
D7	0	SQL voltage above SG_{TH} threshold
	1	SQL voltage below SG_{TH} threshold
D6	-	AOUT/Comparator Channel Selection
D5	-	
D4	-	
D3	0	Squib Current below V_{I_TH} threshold
	1	Squib Current above V_{I_TH} threshold
D2	-	Diagnostic Current: Channel Selection
D1	-	
D0	-	

SB_{TH} threshold status flag (bit D13) indicates the state of SB_{TH} comparator. SB_{TH} comparator monitors the voltage on SQH pin.

DEPEN status flag (bit D12) indicates the state of DEPEN pin.

MOS Diagnostic status flag (bit D11) reports the status of a driver diagnostic. This bit is not latched. When a MOS diagnostic is completed, this bit is cleared. Low-side or high-side MOS diagnostic status flag (D10) indicates if there is an on-going low or high-side driver diagnostic. This bit shall be used in conjunction with bit D11.

Diagnostic current status flag (D9) indicates the state of diagnostic current. Bit D8 indicates which diagnostic current is selected. This bit shall be used along with bit D9 to indicate if a diagnostic bias current or resistance measurement current is on or off.

SG_{TH} threshold status flag (bit D7) indicates the state of SG_{TH} comparator. SG_{TH} comparator monitors the voltage on SQL pin.

AOUT/Comparator channel select bits (bit D6..4) indicate which channel is being monitored by AOUT or SB_{TH}, SG_{TH}, V_{I_TH} comparators.

V_{I_TH} threshold status flag (bit D3) indicates the state of V_{I_TH} comparator. V_{I_TH} comparator monitors the voltage across SQH and SQL pins.

Diagnostic current channel select bits (bit D2..0) indicate which channel is being applied by the diagnostic current.

4.12.3 Deployment driver status response

Status response is defined as in the following table.

Table 28. MISO status response definition

Bit	State	Description
D15	1	Mode bits
D14	1	
D13	0	Always 0
D12	0	DEPEN Negated
	1	DEPEN Asserted
D11	0	Don't care
D10	0	Don't care
D9	0	ARM23 Negated
	1	ARM23 Asserted
D8	0	ARM01 Negated
	1	ARM01 Asserted
D7	0	Don't care
D6	0	Don't care
D5	0	Don't care
D4	0	Don't care
D3	0	No Deployment Event: Channel 3
	1	Deploy Status: Channel 3
D0	0	No Deployment Event: Channel 0
	1	Deploy Status: Channel 0

DEPEN status flag (bit D12) indicates the state of DEPEN pin.

ARM status flag indicates the state of the respective arming signal, including the pulse stretch timer. If the pulse stretch timer is initiated by a deployment command, it does not assert the arming status flag. This flag is de/asserted as soon as the de-glitch timer is expired.

Deploy status bits (bit D3 through bit D0) report the status of internal deployment. Bit D8 in the monitor mode command determines which status information device needs to be reported in D3 through bit D0.

4.12.4 Deployment driver SPI fault response

This SPI fault response indicates a fault in the last MOSI transmission. The device uses the parity bit to determine the integrity of the MOSI command transmission. This response is defined as shown in the following table.

Table 29. MISO SPI fault response

Bit	State	Description
D15	1	Always ‘1’
D14	1	Always ‘1’
D13	1	Always ‘1’
D12	0	Parity error or message error during a deployment(1)
	1	Incorrect number of clocks/bits
D11	0	Parity error or message error during a deployment(1)
	1	Invalid channel address in diagnostic command
D11 – D0	0	Don’t Care

1. See *Table 12* for the summary of SPI transmission during a deployment.
When a parity error is detected, L9654 reports E000h. During a deployment, when an invalid message is detected, L9654 also reports E000h. Refer to *Table 12* for the description of an invalid message during a deployment. Bit D12 reports an incorrect number of clocks/bits. When an incorrect number of clocks/bits is detected, bit D12 is asserted (F000h).
Bit D11 reports an invalid channel-address in diagnostic command. Since L9654 has four deployment channels, addressing channel 4 through channel 7 is considered invalid. Upon detecting this invalid channel-address, L9654 asserts bit D11 (E800h).

4.13 Arming SPI bit definition

4.13.1 Arming MOSI_A bit definition

Arming MOSI_A is defined as shown in the table below.

Table 30. Arming MOSI_A bit definition

7	6	5	4	3	2	1	0
X	X	ARM23	ARM01	X*	X*	ARM23*	ARM01*

4.13.2 ARM[01..23]

Arming command. These bits are used to enable/disable arming signal. A value of 1 enables the arming signal for the respective loop-pair. A value of 0 disables the arming signal for the respective loop-pair. When device is in reset, all arming signals are disabled.

4.13.3 ARM[01..23]*

Arming-command complement. These bits are the complements of ARM[01..23] bits and are used to confirm the transmission of arming signals. If L9654 does not receive valid complement bits, it ignores the arming command.

4.13.4 Arming MISO_A bit definition

Arming MISO_A is defined in the table below.

Table 31. Arming MISO_A bit definition

7	6	5	4	3	2	1	0
X	X	ARM23	ARM01	X	X	ARM23	ARM01

4.13.5 ARM[01..23]

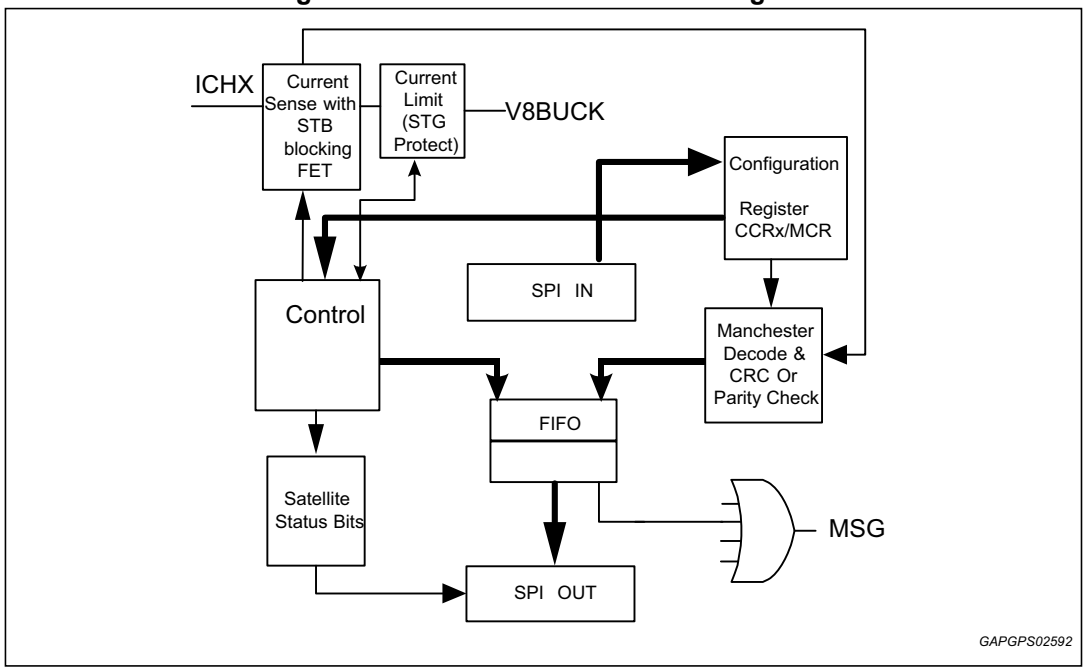
Arming status. These bits are used to echo arming bits sent in the previous arming command. A value of 1 indicates that arming signal is enabled for the respective loop-pair. A value of 0 indicates that arming signal is disabled for the respective loop-pair.

The default state of these arming signals is ‘0’ (disabled).

4.14 Satellite sensor interface

The device provides four currents limited to 60mA each through outputs ICH1 and ICH2. The voltage at these two channels is supplied by the V8BUCK input. Channels 1 and 2 serve as switched power sources to remote mounted satellite sensors, each draws 2 current levels. The L9654 monitors the current flow from its output pin and “demodulates” the current to be decoded using Manchester protocol. Decoded satellite message is communicated to an external microprocessor via SPI.

Figure 18. Satellite interface block diagram



4.14.1 Current sensor

Each output channel senses the current drawn by the remote satellite sensor; the circuit modulates the load current into logic voltage levels for post processing by a Manchester decoder. Each channel has an internal comparator with programmable currents trip points selectable through the appropriate setting in the CCR Register for each of the 2 satellite channels. The current sense comparator provides a hysteresis, which can be enabled through appropriate setting in the CCR Register. Each comparator output has a de-glitch filter as a function of the protocol speed as defined in the AC characteristic table. Each current is limited to 150mA maximum and includes a fault timer.

If the output for a given channel is in current limited for a period of time exceeding the output fault timer, the IC reports an over current fault via SPI and latches off the affected channel, the channel remains in latch off mode until the user sends an SPI command to re-activate the channel. When the output is shorted to battery, an internal comparator senses the output voltage level then turns off an internal series transistor to provide blocking diode for the current going through the output channel, the output resumes normal operation once the fault condition is removed. The comparator has 20 to 50mV input offset to prevent turning off the output under an open circuit condition. In case of loss of VCC all outputs remain off.

4.14.2 Manchester decoding

The L9654 decodes satellite messages based on Manchester decoding, each of the two satellite channels has a Manchester decoder that can be enabled or disabled through the CCR register. An example of Manchester decoding is given below; logic 0 is defined as a signal transition from 0 to 1 at 50% Duty cycle, logic 1 is defined as a signal transition from 1 to 0 at 50% Duty cycle.

The IC starts decoding the satellite message after it receives two SYNC bits defined as logic 00, the SYNC bits are used to determine the bit rate of the incoming message and are used as the time base in decoding the following bits; different bit rates ranges are programmable via SPI, in case the measured bit rate obtained using the 2 SYNC bits doesn't fall within the range selected by the SPI as defined in *Table 35*, the device declares a bit time error, reverts to the minimum bit time of the selected range, and waits for idle.

Figure 19. Manchester decoding

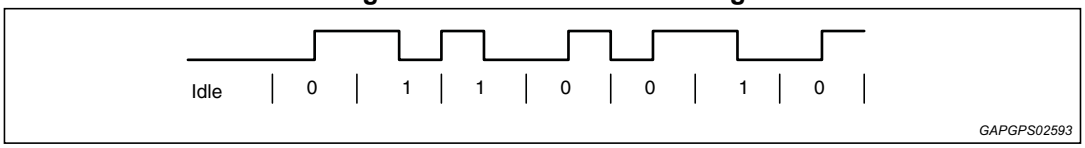
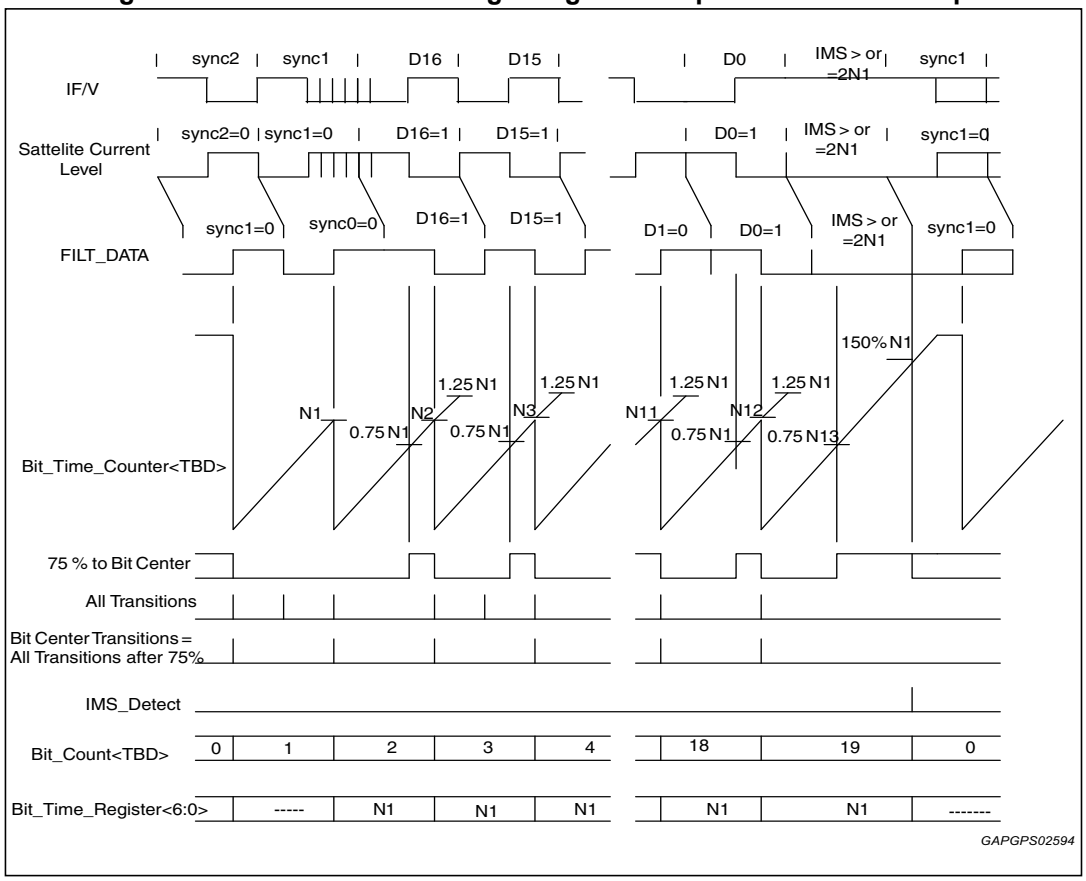


Figure 20. Manchester decoding using satellite protocol as an example



The decoder uses a counter to track the high to low and low to high transitions at the bit center. A transition is considered a bit center only when an edge is detected 75% to 125% of the reference bit time. When a single edge occurs below 75% of the reference bit time it is considered to be a bit edge but it is ignored. When the decoder detects a second edge below 75% of the reference bit time the device declares a bit time error via SPI, reverts to the minimum bit time of the selected range, and waits for idle. When a valid bit center is detected the counter resets and start counting again until another edge is detected. If the message is not complete and no edge is detected in the range of 75% to 125% of measured bit time, the device declares a bit time error via SPI, reverts to the minimum bit time of the selected range, and waits for idle. The idle time is defined as 150% of the minimum bit time of the selected protocol speed range. If there is no bit transition detected for that period of time and the correct number of bits was received, the message is considered complete.

Bit time error and too many bits faults are stored directly into the FIFO once they are detected without the need to wait till an idle time. Since a bit time error is reported directly once it is detected before Idle time, too few bits error may never be reported since bit time error is detected first.

Bit time errors and too many bits errors cause the decoder to revert to the minimum bit time of the selected range, and discard the message. In case of a message containing multiple errors only one error code is reported per message, errors detected in the decoding phase have the following reporting priority; bit time errors, too many bits errors then communication errors (CRC/Parity).

Upon power up or after a reset, the device requires at least 1.5 Idle bit-time based on 52.33 kHz protocol speed or 28.65 µs before starting to decode the first message, bit-time shall adapt to the period obtained based on the two sync bits there after.

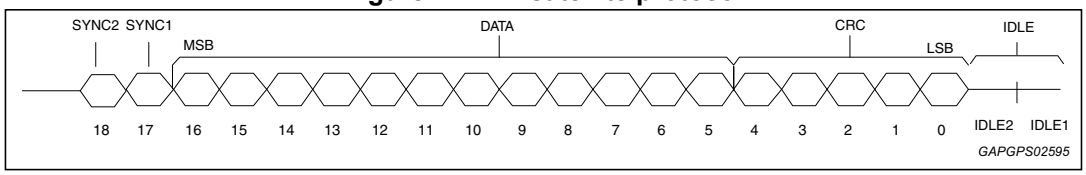
4.14.3 Communication protocols

The L9654 supports two different communication protocols that are widely used by different automotive manufactures. One is based on the protocol used by "A" satellite sensors and the other is "B" protocol that supports variable length messages based on BOSCH, PAS3 and PAS4 protocols. Bits D11D12 in the CCR Register are used to configure the device in order to use any of these protocols.

4.14.4 "A" protocol

The "A" sensors satellites protocol supported by this device is shown below. The message consists of 5 bits CRC cyclic redundancy check error, 12 bit of data and two sync bits. This information could be sensor's trace-ability data, or crash severity or velocity data. The two most significant bits in the data field sent by the sensor can identify these data types.

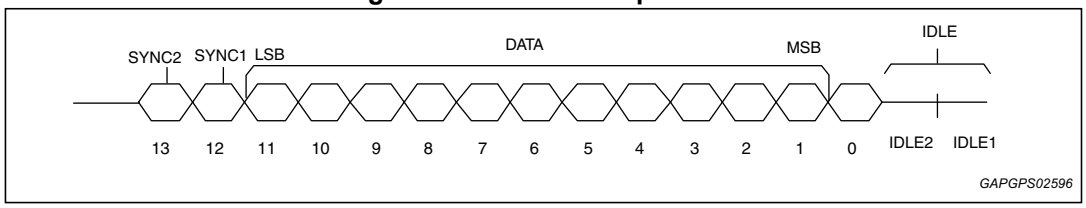
Figure 21. "A" satellite protocol



The CRC error detection code is based on the polynomial $x^5 + x^2 + 1$. The L9654 processes all incoming message through the CRC verification and reports an error message via SPI in case of a CRC mismatch. CRC is performed after a complete message is received, and in case of CRC error, the device sets a fault code via SPI.

4.14.5 "B" variable length protocol

Figure 22. "B" satellite protocol



The L9654 IC supports "B" satellite protocol, which is based on Bosch sensors PAS3\PAS4 protocols (In *Figure 22* bit order is opposite to PAS3/PAS4 protocol in which LSB is sent first and MSB last.) with added flexibility that the message length in the data field can be programmed to accept any number of bits between 8 and 11. The protocol consists of a parity bit, a data field (configurable between 8 to 11 bits) and two sync bits. The IC can be enabled to use this protocol through the appropriate setting in the MCR register. Once the protocol is enabled for a specific channel, the protocol speed is configured by setting the appropriate bits in the CCR register for that particular channel. A parity check is performed after a complete message is received, and in case of a parity error, the device sets a fault code via SPI.

4.14.6 FIFO buffer

The IC includes 2 internal FIFO buffers; one for each output channel, each one is 12 bits and two levels deep. When D1 in the MCR register is set to 0 (default condition), MSG pin is asserted and remains asserted as long as there is a message in any of the 2 internal FIFO buffers.

The FIFO provides error flag via SPI in case of buffer data loss. When writing to a full FIFO the old data is lost. For example if the FIFO content at the bottom of the stack is $0AA, an incoming message of $090 occupies the upper level of the FIFO stack, at this stage the FIFO is full, but the Data lost flag is not set. When writing another message to the FIFO, for example $066, the Data lost flag is set and the final FIFO content is $066 (top of stack) and $090(bottom of stack). When a FIFO read operation is performed via SPI, The FIFO content $090 is carried over by MISO and Data lost flag is unset. The Data lost flag is also unset when the FIFO is flushed via SPI command.

4.14.7 Satellite continuity check

Each output has a short circuit protection by independent current limit. When a short circuit occurs the output becomes current limited, a fault timer latches the output off and a fault condition bit is reported via SPI.

That output returns to normal operation when it is re-enabled via SPI and the current limit condition was removed, this fault condition does not interfere with the operation of any of the other output channels

4.14.8 Message waiting

The MSG pin is asserted when there is a message in any of the 2 internal FIFO buffers. This pin is TTL level and is configurable to be either active high or active low signal.

The Pin shall also be programmable via SPI to remain either active during CS_S once is set or inactive during CS. If the pin is configured to remain active during CS_S and there is a message in any of the internal FIFO it remains active even if CS_S is de-asserted. However if there are no messages in any of the internal 2 FIFOs the pin is forced to inactive state.

4.14.9 Satellite serial data input (MOSI)

The MOSI input takes data from the master microprocessor while CS_S is asserted. The MSB is the first bit of each word received on MOSI and the LSB is the last bit of each word received on MOSI. This pin has TTL level compatible input voltages allowing proper operation with microprocessors using a 3.3 to 5.0 volt supply. MOSI bits layout is provided here below.

4.14.10 Satellite MOSI bits definition

Table 32. Satellite MOSI bits layout

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P	S	DATA (12:0)													

There is a total of 5 internal registers that are used to configure all of the satellite channels. These registers are addressed by setting MOSI bit 14 according to this table and by sending

the SPI commands sequentially in the correct order so that CH1 command is the first significant word and CH2 command is the Last word.

Table 33. MOSI satellite interface registers map

Bit	State	Description
D15		SPI Odd Parity
D14	0	MCR Master Configuration Register (CH1 Only)
	1	CCR1 Channel Configuration Register for CH1
	1	CCR2 Channel Configuration Register for CH2

The SPI command sequence is such that the first word communicates with channel 1, the second SPI word communicates with channel 2.

4.14.11 Satellite module configuration register (CH1 only)

This register defines global configuration to the satellite module, in order to be executed correctly it has to be written for CH1 as the first word after the rising edge of CS_S. When an MCR command is written to any other channel than CH1, the IC ignores this command and reply with SPI message $E000.

Table 34. Master configuration register definition (CH1 only)

Bit	State	Description	
D13	0	Not Used	
D12	0	"B" protocol setup for even parity	(default)
	1	"B" protocol setup for odd parity	
D11	0	Not Used	
D10	0	Not Used	
D9	0	CH2 "A" Protocol Mode	(default)
	1	CH2 "B" Protocol Mode	
D8	0	CH1 "A" Protocol Mode	(default)
	1	CH1 "B" Protocol Mode	
D7	X	Not Used	
D6	X	Not Used	
D5	X	Not Used	
D4	X	Not Used	
D3	X	Not Used	
D2	X	Not Used	
D1	0	MSG Output remains active when CS_S asserted	(default)
	1	MSG Output inactive when CS_S asserted	
D0	0	MSG Output Active High	(default)
	1	MSG Output Active Low	

Bits[1:0]

These bits configure the polarity and the behavior of the MSG

Bits[9:8]

These bits are used to configure the output channels for both sensor protocols. In the "B" protocol mode a parity bit is used to verify communication between the satellite sensors and the IC. The L9654 calculates the parity of the incoming massage based on either odd parity or even parity, which is determined by the setting of bit D12.

In case of communication parity mismatch a communication parity error shall be reported via SPI. If none of the channels is configured for the "B" protocol a write operation to this bit is ignored.

Bit [12]

This bit controls the parity calculation for incoming sensor messages to either even or odd parity; the selected setting applies to all channels operating in "B" protocol node.

The setting of this bit is ignored by the IC for the channels configured for "A" protocol. The MCR register has to be written at least once in order for the device to be configured correctly, however it can be superseded with a CCR command.

4.14.12 Channel configuration registers (CCR1, CCR2, CCR3, CCR4)

This register is used to configure individual channels for proper satellite communication as required by the application. Please refer to the below *Table 35* for bits definition.

Table 35. Channel configuration register definition

Bit	State	Description
D13	0	Don’t Flush FIFO (Default)
	1	Flush FIFO
D12	0	Write to bits <D9-D0>, D12 and D13 only
	1	Write to D4, D5, D10, D11, D12 and D13 only. All other CCR bits shall keep previous setting.
D11		Mode Select (refer to *Table 40*)
D10		
D9		Bit Time Selection (refer to *Table 39*)
D8		
D7	0	"B" Protocols configuration bits (refer to *Table 38*) Only applies when CHx is configured to use "B" Only applies when CHx is configured to use "B" protocol through MCR otherwise treated as DON’TCARE
D6	1	
D5		Satellite/Decoder Control (refer to *Table 37*)
D4		
D3	0	Current Trip Point Hysteresis Disabled (default)
	1	Current Trip Point Hysteresis Enabled

Table 35. Channel configuration register definition

Bit	State	Description
D2		Current Trip Point threshold (refer to *Table 36*)
D1		
D0		

Bits[2:0]

These bits program the threshold for the current demodulation affecting each individual channel. The current ranges supported are given in *Table 36*.

Table 36. Current ranges supported are given in following table

Bit D2	Bit D1	Bit D0	Current Threshold (mA)
0	0	0	16.50(default)
0	0	1	19.00
0	1	0	22.50
0	1	1	26.50
1	0	0	32.00
1	0	1	39.00
1	1	0	48.50
1	1	1	60.00

All incoming satellite signals are processed through deglitch filter before reaching the decoder. D3 enables a hysteresis around the current threshold for added noise immunity.

Bits[5:4]

These bits are used to enable the satellite channels and the internal decoders to be commanded on or off according to the following table. The suggested sequence to avoid spurious error code inside FIFO is to switch on the channel first, and enable decoder only once satellite is powered.

Table 37. Satellite/decoder control

Bit D5	Bit D4	Definition	
		Satellite	Decoder
0	0	OFF (default)	OFF (default)
0	1	ON	OFF
1	0	ON	ON
1	1	OFF	OFF

Bits[7:6]

These bits are used to configure the number of bits in the "B" protocol data field. For these bits to execute on any given channel, the channel has to be configured for "B" protocol through bits <11:8> in the MCR register.

Table 38. "B" protocol configuration

Bit D7	Bit D6	Protocol Data Field
0	0	8bits(default)
0	1	9bits
1	0	10bits
1	1	11bits

Bits[9:8]

These bits shall configure speed selection for any of the satellite channels and they apply to both "A" and the "B" Manchester protocol. Upon power up or reset the protocol configuration shall initialize to the default speed as it is shown in the below table.

Table 39. Bit time selection

Bit D9	Bit D8	Guaranteed frequency operating range (Hz)
0	0	13.3k to 52.33k (default)
0	1	26.32k to 110.74k
1	0	43.50k to 164.20k
1	1	62.66k to 250k

Bits[11:10]

These bits are used to determine the requested information from each of the satellite channels internal registers. At power up or in case of POR condition these bits are initialized to 00 by the IC and MISO bits <12:0> shall default to the content of the MCR register.

Table 40. Mode select

Bit D11	Bit D10	Definition
00/01/10		Report This on Next MISO Bit 13 = SPI odd parity Bits<15:14≥11 (Configuration Reports Mode)
0	0	If the previous command is a write to the MCR Register (default) Report <12:0> *Table 35* (MCR) only for CH1
		If previous command is a write to the CCRx Register Report <12:0> *Table 36* (CCR)
0	1	Report <12:0>*Table 35* (MCR) (CH1 Only)
1	0	Report <12:0>*Table 36* (CCR)
11		Report This on Next MISO Bit 13 = SPI odd parity Bits<15:14≥ (Satellite Status 00,01 or 10)
1	1	Report FIFO data

In the auto reply mode where D11 D10 are set to 00, the IC tests every incoming MOSI command. If the command is a write command to a CCRx register then during the following CS_S the device reports back the content of the respective CCRx channel register. If the incoming command is a write to the MCR register for CH1 then in the following CS_S the device reports back the content of the MCR register.

If the MOSI command is a write to the CCRx register with bits <11:10> are set to 11 the IC reports the content of the FIFO. MISO bits layout when reporting FIFO data is provided, The MISO layout when reporting configuration report is provided in previous figure.

When reporting a configuration report for either the MCR or the CCR register MOSI bits<15:14> are set to 11 to indicate a configuration report. Otherwise they report the status of the satellite channel.

In some cases the user may request a configuration report for either the MCR or CCRx registers without first performing the write operation mentioned above. In this condition if bits <11:10> are set to 01 by the user, device reports the content of the MCR register on the subsequent chip select. If bits <11:10> are set to 10 the IC reports the content of the CCR register. In case of an SPI command to CH2 with bits D11D10 are set to 00 while D14 is set to 0, or if D11D10 are set to 01 with D14 is set to either 0 or 1, the affected channel reports $E000.

Table 41. SPI mode selects reply for satellite channels

D11	D10	CH1	CH2
0	0	Reply with CCR1 if D14 is 1	Reply with CCR2 if D14 is 1
		Reply with MCR if D14 is 0	Reply with $E000 if D14 is 0
0	1	Reply with MCR	Reply with $E000
1	0	Reply with CCR1	Reply with CCR2
1	1	Report FIFO	Report FIFO

Bit[12]

This bit is used to Control the write operation for the CCR Register. When it is set to 0 the user can modify bits <D9-D0>, D12 and D13 only, all other CCR bits keep previous setting. When it is set to 1 the user can only modify the following bits D4, D5, D10, D11, D12 and D13, all other CCR bits keep previous setting.

Bit[13]

This bit is used to Flush FIFO content, when set to 1 the IC flushes the available two FIFO locations for the specified channel, all FIFO connect is lost in this case.

Table 42. Satellite MISO bits definition

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M1	M0	P	DL	FIFO Data											

Table 43. SPI MISO bits layout when reporting FIFO data

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M1	M0	P	Configuration Report												

4.14.13 SPI MISO bits layout for configuration report

Status bits <15:14> indicate the status of L9654 output channels, status bits are updated at the falling edge of CS_S and defined by bits <15:14>. Fault codes are pushed into the FIFO and then removed form FIFO on rising edge of CS_S and reported through MISO.

Global and channels faults are encoded in the hexadecimal range between $001 to $01F. “Global faults” cover all satellite channels. “Channel Fault” covers only a particular channel.

Channel Fault codes are pushed once into the FIFO each time they occur while global faults are pushed once into the FIFO even if the fault is still present. Bit 15 is set by the IC to satisfy an odd parity for each of the transmitted word, therefore it sets to 1 if the total number of 1’s for bits is even and to 0 if the total number of 1’s for bits is odd.

Table 44. MISO Manchester message data definition

Bit	State	Description
D15	-	Status bits (refer to table 44)
D14	-	
D13	-	Odd Parity
D12	0	No FIFO Data has been lost
	1	FIFO Data has been lost
D11:0	-	FIFO Contents

Table 45. Status bits definition

Bit D15	Bit D14	Definition
0	0	Current Channel is Off
0	1	Channel ON, Message processing Disabled
1	0	Channel ON, Message processing Enabled
1	1	Configuration report

Table 46. Satellites fault codes definition supporting "A" protocol

Bit D11:0 value	Fault definition	Function
$0	No Faults (FIFO empty value)	Global Fault Codes Definition (Reported back for CH1 only & latched only once)
$1	Unassigned	
$2	Bad MOSI bit Count	
$3 - $F	Unassigned	
$10	High-side Current Limit Exceeded	Channel Fault Codes
$11	Unassigned	
$12	SPI Odd Parity Communication error	
$13 - $17	Unassigned	
$18	Reserved Message Received	
$19	Manchester Bit Time Error	
$1A	Manchester Bit Time Error or Too Few Bits	
$1B	Reserved	
$1C	CRC Error	
$1D - $1F	Unassigned	
$020 - $FFF	Manchester sensor’s data range	Manchester Data

Buffer data values from $0 to $1F are reserved and not transmitted by the "A" Manchester data sensor. All "A" satellite sensors use values between $020 and $FFF, therefore values fallen within this range are interpreted by the system software as satellite only data. If a satellite data is found to be in the range between $00 to $01F the IC asserts the reserved message error flag or fault code. In case there is no fault condition present, the device returns to $000.

Data is lost when a data word is written to a full buffer. To alarm the user for this condition the DL (buffer data lost) flag shall be set.

Table 47. Satellites fault codes definition supporting "B" protocol

Bit D11:0 value	Fault definition	Function
$0	No Faults (FIFO empty value)	Global Fault Codes Definition (Reported back for CH1 only & latched only once)
$1	Unassigned	
$2	Bad MOSI Bit Count	
$3 - $F	Unassigned	
$10	High-side Current Limit Exceeded	Channel Fault Codes
$11	Unassigned	
$12	SPI Odd Parity Communication error	
$13 - $17	Unassigned	
$18	Unassigned	
$19	Manchester Bit Time Error OR Too Few Bits	
$1A	Too Many Bits	
$1B	Reserved	
$1C	Satellite Communication Parity error	
$800 - $FFF	Manchester sensor’s data range D11 shall be set to 1 by the IC when receiving sensor data. When reporting faults D11 shall be set internally by the IC to 0	Manchester Data

As mentioned earlier the L9654 supports "B" Manchester data protocol, the data field for this protocol can be configured to any number of bits between 8 to 11 bits. Incoming data from the sensor using "B" protocol shall be right justified by the IC. For example if the incoming message has only 8 bits in the data filed, the device transmits this message on MISO so that it occupies bits <7:0> bits 8, 9 and 10 are set to 000.

Too Many Bits and Too Few Bits faults can be calculated based on the number of bits in the data field. So if we consider the 8 bit "B" protocol example discussed above a message with 9 bits in the data field should set the too many bits fault flag, on the other hand a message with 7 bits in the data field should set the too few bits fault flag. When the L9654 is configured to use a the Manchester "B" protocol, the device set SPI MOSI D11 to 0 when reporting fault data and to 1 when reporting satellite data. This operation should allow both sensors "A" based or "B" based to use the same fault codes.

Upon power on, after a reset or POR conditions the MISO data is initialized as follows:

- CH1 returns to MCR configuration in report mode with parity bit set accordingly
- CH2 returns $E000.

5 Package information

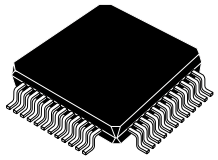
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

Figure 23. LQFP48 mechanical data and package dimensions

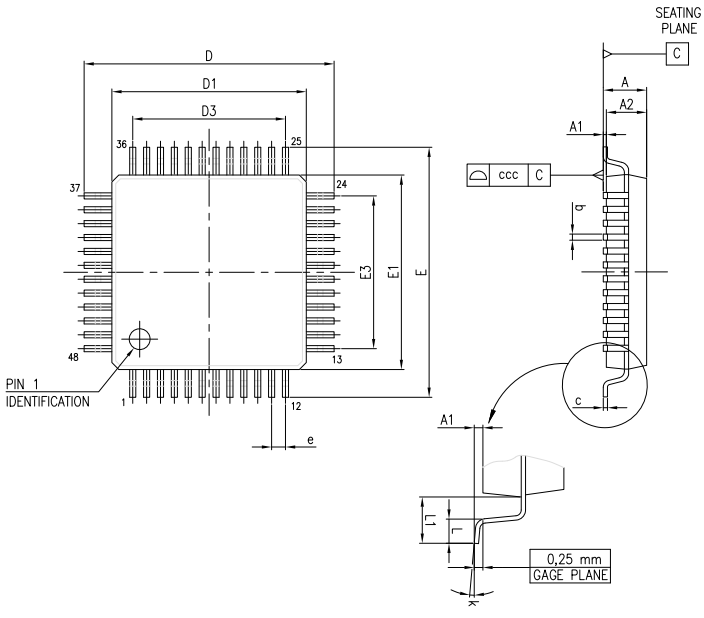
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.006	0.008	0.010
c	0.09		0.20	0.004		0.008
D	8.80	9.00	9.20	0.346	0.354	0.362
D1	6.80	7.00	7.20	0.268	0.276	0.283
D3		5.50			0.217	
E	8.80	9.00	9.20	0.346	0.354	0.362
E1	6.80	7.00	7.20	0.268	0.276	0.283
E3		5.50			0.217	
e		0.50			0.019	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
k	0°(min.), 3.5°(typ.), 7°(max.)					
ccc			0.08			0.0031

OUTLINE AND MECHANICAL DATA



Body: 7 x 7 x 1.4mm

LQFP48



GAPGPS01859

6 Revision history

Table 48. Document revision history

Date	Revision	Changes
03-Dec-2009	1	Initial release.
27-Sep-2013	2	Updated disclaimer. Document status promoted from preliminary data to production data.
12-Nov-2013	3	Document reformatted no content change.

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001
Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
moschip.ru
moschip.ru_4
moschip.ru_6
moschip.ru_9