TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

SSM3K09FU

High Speed Switching Applications

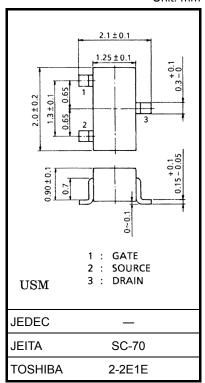
Unit: mm

- Small package
- Low on resistance
 - : $R_{on} = 0.7 \Omega \text{ (max) } (@V_{GS} = 10 \text{ V})$
 - : $R_{on} = 1.2 \Omega \text{ (max) } (@V_{GS} = 4 \text{ V})$

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit	
Drain-Source voltage		V_{DS}	30	V	
Gate-Source voltage		V _{GSS}	±20	V	
Drain current	DC	ΙD	400	mA	
	Pulse	I _{DP}	800		
Drain power dissipation (Ta = 25°C)		P _D (Note 1)	150	mW	
Channel temperature		T _{ch}	150	°C	
Storage temperature		T _{stg}	-55 to 150	°C	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.



Weight: 0.006 g (typ.)

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on FR4 board (25.4 mm \times 25.4 mm \times 1.6 t, Cu Pad: 0.6 mm² \times 3) Figure 1.

Marking

D J

Equivalent Circuit (top view)

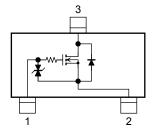
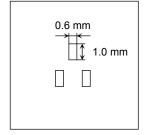


Figure 1: 25.4 mm \times 25.4 mm \times 1.6 t, Cu Pad: 0.6 mm² \times 3



Handling Precaution

When handling individual devices (which are not yet mounting on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

Start of commercial production 2000-01

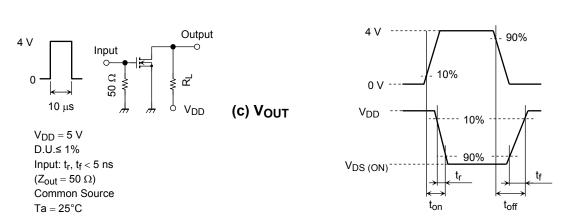
Electrical Characteristics (Ta = 25°C)

Chara	cteristics	Symbol	Test Condition		Min	Тур.	Max	Unit
Gate leakage curr	ent	I _{GSS}	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0$		_	_	±1	μА
Drain-Source brea	akdown voltage	V (BR) DSS	I _D = 1 mA, V _{GS} = 0		30	_	_	V
Drain cut-off curre	nt	I _{DSS}	$V_{DS} = 30 \ V, \ V_{GS} = 0$		_	_	1	μА
Gate threshold vo	Itage	V _{th}	$V_{DS} = 5 \text{ V}, I_{D} = 0.1 \text{ mA}$		1.1	_	1.8	V
Forward transfer a	admittance	Y _{fs}	$V_{DS} = 5 \text{ V}, I_{D} = 200 \text{ mA}$	(Note2)	270	_	_	mS
Drain-Source ON resistance		R _{DS} (ON)	$I_D = 200 \text{ mA}, V_{GS} = 10 \text{ V}$	(Note2)	_	0.5	0.7	Ω
			I _D = 200 mA, V _{GS} = 4 V	(Note2)	_	0.8	1.2	
			$I_D = 200 \text{ mA}, V_{GS} = 3.3 \text{ V}$	(Note2)	_	1.0	1.7	
Input capacitance		C _{iss}	V _{DS} = 5 V, V _{GS} = 0, f = 1 MHz		_	20	_	pF
Reverse transfer capacitance		C _{rss}	V _{DS} = 5 V, V _{GS} = 0, f = 1 MHz		_	7	_	pF
Output capacitance		Coss	V _{DS} = 5 V, V _{GS} = 0, f = 1 MHz		_	16	_	pF
Switching time	Turn-on time	t _{on}	V _{DD} = 5 V, I _D = 200 mA,		_	72	_	ns
	Turn-off time	t _{off}	V _{GS} = 0 to 4 V		_	68	_	ns

Note2: Pulse test

Switching Time Test Circuit





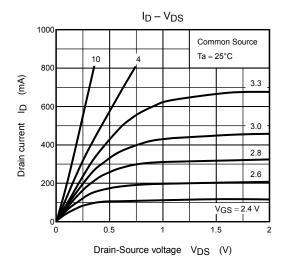
Precaution

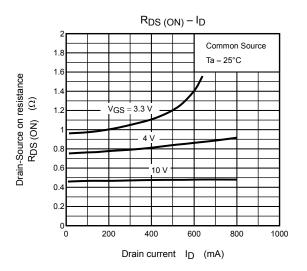
 V_{th} can be expressed as voltage between gate and source when low operating current value is ID = 100 μA for this product. For normal switching operation, V_{GS} (on) requires higher voltage than V_{th} and V_{GS} (off) requires lower voltage than V_{th} .

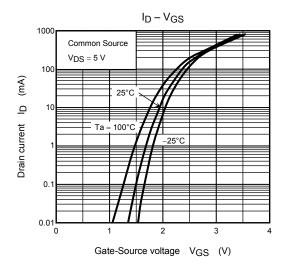
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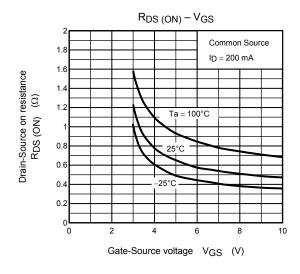
(relationship can be established as follows: $V_{GS (off)} < V_{th} < V_{GS (on)}$)

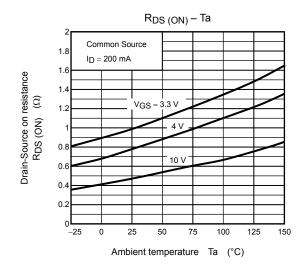
Please take this into consideration for using the device.

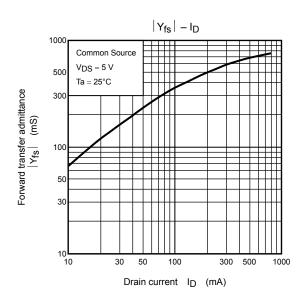




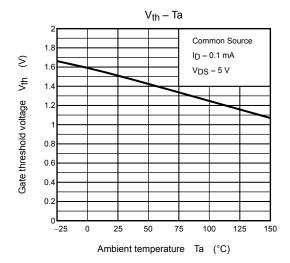


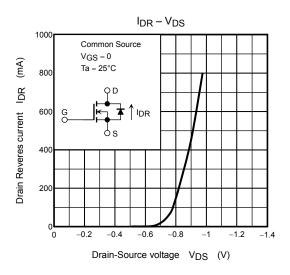


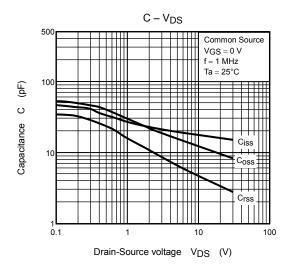


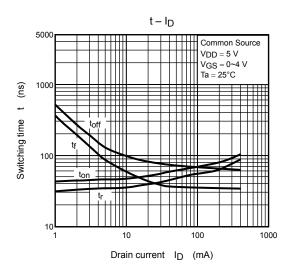


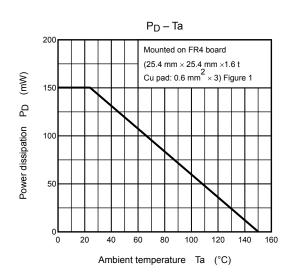
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