34AA04

4K I²C™ Serial EEPROM with Software Write-Protect

Device Selection Table

Part Number	Vcc Range	Max. Clock Frequency	Temp Ranges
34AA04	1.7-3.6	1 MHz(1)	I, E

Note 1: 400 kHz for 1.8V ≤ VCC < 2.2V
100 kHz for VCC < 1.8V

Features

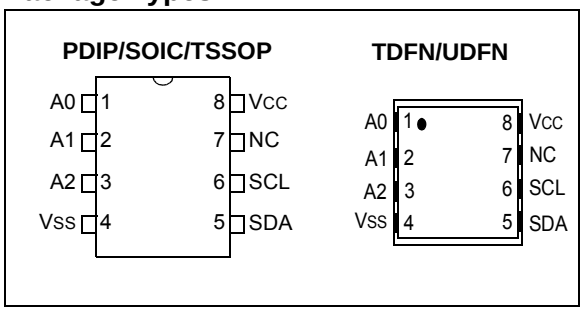
- 4 Kbit EEPROM:
  - Internally organized as two 256 x 8-bit banks
  - Byte or page writes (up to 16 bytes)
  - Byte or sequential reads within a single bank
  - Self-timed write cycle (5 ms max.)
- JEDEC® JC42.4 (EE1004-v) Serial Presence Detect (SPD) Compliant for DRAM (DDR4) modules
- High-Speed I²C™ Interface:
  - Industry standard 1 MHz, 400 kHz, and 100 kHz
  - Schmitt Trigger inputs for noise suppression
  - SMBus-compatible bus time out
  - Cascadable up to eight devices
- Write Protection:
  - Reversible software write protection for four individual 128-byte blocks
- Low-Power CMOS Technology:
  - Voltage range: 1.7V to 3.6V
  - Write current: 1.5 mA at 3.6V
  - Read current: 200 µA at 3.6V, 400 kHz
  - Standby current: 1 µA at 3.6V
- High Reliability:
  - More than one million erase/write cycles
  - Data retention: > 200 years
  - ESD protection: > 4000V
- 8-lead PDIP, SOIC, TSSOP, TDFN, and UDFN Packages
- Available Temperature Ranges:
  - Industrial (I): -40°C to +85°C
  - Automotive (E): -40°C to +125°C

Description

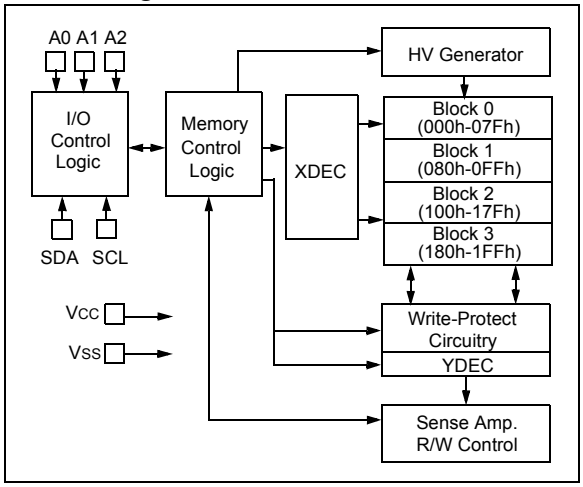
The Microchip Technology Inc. 34AA04 is a 4 Kbit Electrically Erasable PROM which utilizes the I²C serial interface and is capable of operation across a broad voltage range (1.7V to 3.6V). This device is JEDEC JC42.4 (EE1004-v) Serial Presence Detect (SPD) compliant and includes reversible software write protection for each of four independent 128 x 8-bit blocks. The device features a page write capability of up to 16 bytes of data. Address pins allow up to eight devices on the same bus.

The 34AA04 is available in the 8-lead PDIP, SOIC, TSSOP, TDFN, and UDFN packages.

Package Types



Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

VCC.....6.5V

All Inputs and Outputs (except A0) w.r.t. VSS.....-0.3V to 6.5V

A0 Input w.r.t. VSS..... -0.3 to 12V

Storage Temperature.....-65°C to +150°C

Ambient Temperature with Power Applied.....-40°C to +125°C

ESD Protection on All Pins.....≥ 4 kV

† **NOTICE:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC SPECIFICATIONS

DC CHARACTERISTICS			VCC = +1.7V to +3.6V Industrial (I): TA = -40°C to +85°C Automotive (E): TA = -40°C to +125°C			
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
	—	**A0, A1, A2, SCL, and SDA**	—	—	—	
D1	VIH	High-Level Input Voltage	0.7 VCC	VCC + 0.5	V	
D2	VIL	Low-Level Input Voltage	—	0.3 VCC 0.2 VCC	V V	VCC ≥ 2.5V VCC < 2.5V
D3	VHYS	Hysteresis of Schmitt Trigger Inputs	0.0 VCC	—	V	**(Note)**
D4	VOL	Low-Level Output Voltage	—	0.40 0.40	V V	IOL = 20.0 mA, VCC = 2.2V IOL = 6.0 mA, VCC = 1.7V
D5	VHV	High-Voltage Detect (A0 pin only)	7	10	V	VCC < 2.2V
			VCC + 4.8	10	V	VCC ≥ 2.2V
D6	ILI	Input Leakage Current	—	±1	µA	VIN = VSS or VCC
D7	ILO	Output Leakage Current	—	±1	µA	VOUT = VSS or VCC
D8	CIN, COUT	Pin Capacitance (all inputs/outputs)	—	10	pF	VCC = 5.5V **(Note)** TA = 25°C, FCLK = 1 MHz
D9	ICC write	Operating Current	—	1.5	mA	VCC = 3.6V
D10	ICC read		—	200	µA	VCC = 3.6V, SCL = 400 kHz
D11	ICCS	Standby Current	— —	1 5	µA µA	Industrial Automotive SDA, SCL, VCC = 3.6V A0, A1, A2 = VSS

Note: This parameter is periodically sampled and not 100% tested.

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TABLE 1-2: AC SPECIFICATIONS

AC CHARACTERISTICS			V_{CC} = +1.7V to +3.6V Industrial (I): T_A = -40°C to +85°C Automotive (E): T_A = -40°C to +125°C			
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
1	F_{CLK}	Clock Frequency **(Note 2)**	10 10 10	100 400 1000	kHz	1.7V ≤ V_{CC} < 1.8V 1.8V ≤ V_{CC} ≤ 2.2V 2.2V ≤ V_{CC} ≤ 3.6V
2	T_{HIGH}	Clock High Time	4000 600 260	— — —	ns	1.7V ≤ V_{CC} < 1.8V 1.8V ≤ V_{CC} ≤ 2.2V 2.2V ≤ V_{CC} ≤ 3.6V
3	T_{LOW}	Clock Low Time	4700 1300 500	— — —	ns	1.7V ≤ V_{CC} < 1.8V 1.8V ≤ V_{CC} ≤ 2.2V 2.2V ≤ V_{CC} ≤ 3.6V
4	T_R	SDA and SCL Rise Time **(Note 1)**	— — —	1000 300 120	ns	1.7V ≤ V_{CC} < 1.8V 1.8V ≤ V_{CC} ≤ 2.2V 2.2V ≤ V_{CC} ≤ 3.6V
5	T_F	SDA and SCL Fall Time **(Note 1)**	— — —	300 300 120	ns	1.7V ≤ V_{CC} < 1.8V 1.8V ≤ V_{CC} ≤ 2.2V 2.2V ≤ V_{CC} ≤ 3.6V
6	$T_{HD:STA}$	Start Condition Hold Time	4000 600 260	— — —	ns	1.7V ≤ V_{CC} < 1.8V 1.8V ≤ V_{CC} ≤ 2.2V 2.2V ≤ V_{CC} ≤ 3.6V
7	$T_{SU:STA}$	Start Condition Setup Time	4700 600 260	— — —	ns	1.7V ≤ V_{CC} < 1.8V 1.8V ≤ V_{CC} ≤ 2.2V 2.2V ≤ V_{CC} ≤ 3.6V
8	$T_{HD:DAT}$	Data Input Hold Time	0	—	ns	**(Note 3)**
9	$T_{SU:DAT}$	Data Input Setup Time	250 100 50	— — —	ns	1.7V ≤ V_{CC} < 1.8V 1.8V ≤ V_{CC} ≤ 2.2V 2.2V ≤ V_{CC} ≤ 3.6V
10	$T_{SU:STO}$	Stop Condition Setup Time	4000 600 260	— — —	ns	1.7V ≤ V_{CC} < 1.8V 1.8V ≤ V_{CC} ≤ 2.2V 2.2V ≤ V_{CC} ≤ 3.6V
11	T_{AA}	Output Valid from Clock **(Note 3)**	200 200 —	3450 900 350	ns	1.7V ≤ V_{CC} < 1.8V 1.8V ≤ V_{CC} ≤ 2.2V 2.2V ≤ V_{CC} ≤ 3.6V
12	T_{BUF}	Bus Free Time: Time the bus must be free before a new transmission can start	4700 1300 500	— — —	ns	1.7V ≤ V_{CC} < 1.8V 1.8V ≤ V_{CC} ≤ 2.2V 2.2V ≤ V_{CC} ≤ 3.6V
13	T_{SP}	Input Filter Spike Suppression (SDA and SCL pins)	—	50	ns	**(Note 1)**
14	T_{WC}	Write Cycle Time (byte or page)	—	5	ms	—
15	$T_{TIMEOUT}$	Bus Timeout Time	25	35	ms	—
16	—	Endurance	1M	—	cycles	Page mode, 25°C, V_{CC} = 3.6V **(Note 4)**

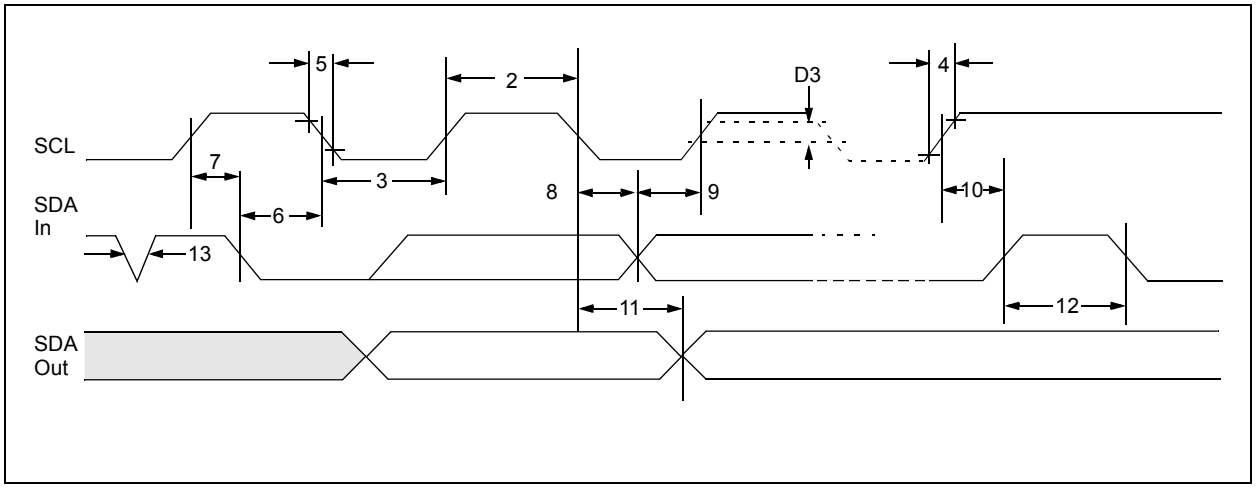
Note 1: Not 100% tested.

2: The minimum clock frequency of 10 kHz is to prevent the bus timeout from occurring.

3: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 200 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

4: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from Microchip's web site at www.microchip.com.

FIGURE 1-1: BUS TIMING DATA



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2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Symbol	PDIP	SOIC	TSSOP	UDFN	TDFN	Description
A0/VHV	1	1	1	1	1	Chip Address Input, High-Voltage Input
A1	2	2	2	2	2	Chip Address Input
A2	3	3	3	3	3	Chip Address Input
VSS	4	4	4	4	4	Ground
SDA	5	5	5	5	5	Serial Address/Data I/O
SCL	6	6	6	6	6	Serial Clock
NC	7	7	7	7	7	Not Connected
VCC	8	8	8	8	8	+1.7V to 3.6V Power Supply

Note: Exposed pad on TDFN/UDFN can be connected to VSS or left floating.

2.1 A0, A1, A2 Chip Address Inputs

The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to eight 34AA04 devices may be connected to the same bus by using different Chip Select bit combinations. These inputs must be connected to either VSS or VCC.

The A0 pin also serves as the high-voltage input for enabling the SWPn and CWP instructions.

Note:	The comparison between the A0, A1, and A2 pins and the corresponding Chip Select bits is disabled for software Write-Protect and Bank Select commands.

2.2 Serial Address/Data Input/Output (SDA)

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal. Therefore, the SDA bus requires a pull-up resistor to VCC (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz and 1 MHz).

For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

2.3 Serial Clock (SCL)

This input is used to synchronize the data transfer to and from the device.

3.0 FUNCTIONAL DESCRIPTION

The 34AA04 supports a bidirectional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter, and a device receiving data, as a receiver. The bus has to be controlled by a master device, which generates the Serial Clock (SCL), controls the bus access and generates the Start and Stop conditions, while the 34AA04 works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

The 4 Kbit array of the 34AA04 is divided into two separate banks of 2 Kbits each. The 34AA04 also offers reversible software write protection for each of four 1 Kbit blocks.

4.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 4-1).

4.1 Bus Not Busy (A)

Both data and clock lines remain high.

4.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

4.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must be ended with a Stop condition.

4.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of data bytes transferred between the Start and Stop conditions is determined by the master device and is, theoretically, unlimited; although only the last sixteen will be stored when doing a write operation. When an overwrite does occur, it will replace data in a first-in, first-out (FIFO) fashion.

4.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an Acknowledge after the reception of each byte. Exceptions to this rule relating to software write protection are described in **Section 9.0 "Software Write Protection"**. The master device must generate an extra clock pulse, which is associated with this Acknowledge bit.

Note:	The 34AA04 does not generate any Acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end-of-data to the slave by not generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (34AA04) will leave the data line high to enable the master to generate the Stop condition.

4.6 Bus Timeout

If SCL remains low for the time specified by $T_{TIMEOUT}$, the 34AA04 will reset the serial interface and ignore all further communication until another Start condition is detected (Figure 4-2). This dictates the minimum clock speed as defined by F_{CLK}.

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FIGURE 4-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

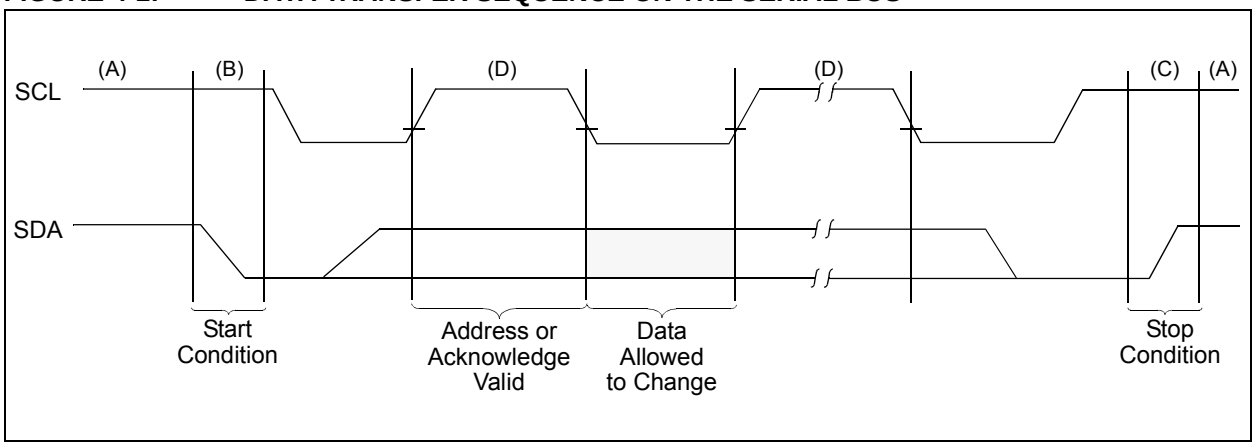
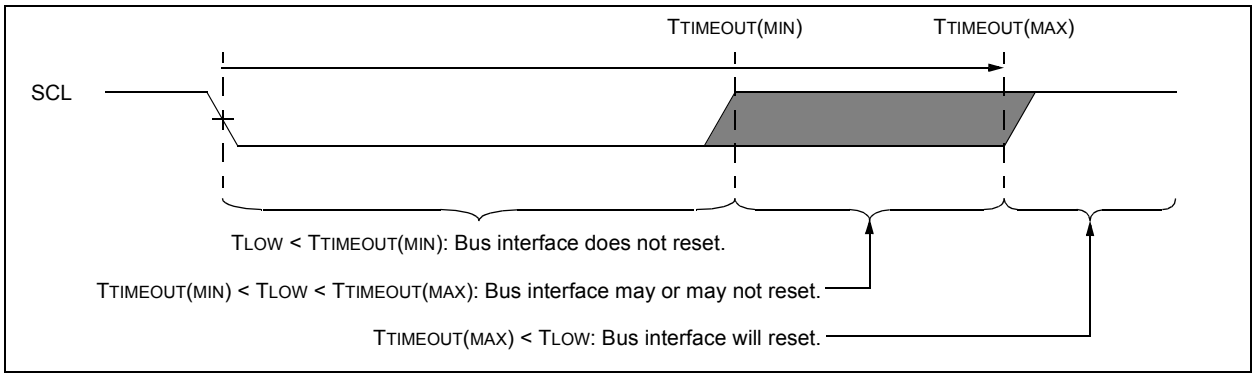


FIGURE 4-2: BUS TIMEOUT



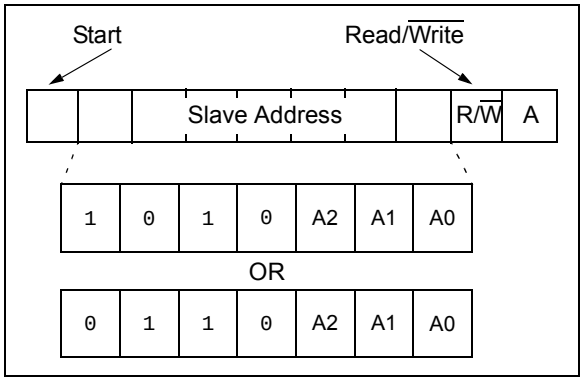
4.7 Device Addressing

A control byte is the first byte received following the Start condition from the master device. The first part of the control byte consists of a 4-bit control code which is set to '1010' for normal read and write operations and '0110' for accessing the software write-protect features and bank selection. The control byte is followed by three Chip Select bits (A2, A1, A0). The Chip Select bits allow the use of up to eight 34AA04 devices on the same bus and are used to determine which device is accessed. The Chip Select bits in the control byte must correspond to the logic levels on the corresponding A2, A1 and A0 pins for the device to respond.

The eighth bit of slave address determines if the master device wants to read or write to the 34AA04 (Figure 4-3). When set to a one, a read operation is selected. When set to a zero, a write operation is selected.

Operation	Control Code	Chip Select	R/$\overline{W}$
Read	1010	A2 A1 A0	1
Write	1010	A2 A1 A0	0
Read Write-Protect/ Bank Address	0110	A2 A1 A0	1
Set Write-Protect/ Bank Address	0110	A2 A1 A0	0

FIGURE 4-3: CONTROL BYTE ALLOCATION



5.0 BANK ADDRESSING

To support backwards-compatibility with DDR2/3 (JEDEC EE1002) SPD EEPROMs, the memory array of the 34AA04 is divided into two separate 256-byte banks. The Set Bank Address (SBA) commands are used to set the bank address to either 0 or 1. The Read Bank Address (RBA) command is used to determine which bank is currently selected.

Note 1: The bank address is volatile and is reset to Bank 0 upon power-up.

2: The comparison between the A0, A1, and A2 pins and the corresponding Chip Select bits is disabled for Bank Select commands.

Note: Sequential read operations cannot cross a bank boundary and will roll over back to the beginning of the selected bank.

TABLE 5-1: BANK ADDRESS RANGE

Bank	Logical Array Address
Bank 0	000h-0FFh
Bank 1	100h-1FFh

TABLE 5-2: BANK ADDRESSING INSTRUCTION SET

Function	Abbr	Control Byte								A0 Pin
		Control Code				Chip Select Bits			R/$\overline{W}$	
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Set Bank Address to 0	SBA0	0	1	1	0	1	1	0	0	0, 1, or V_{HV}
Set Bank Address to 1	SBA1					1	1	1	0	0, 1, or V_{HV}
Read Bank Address	RBA					1	1	0	1	0, 1, or V_{HV}

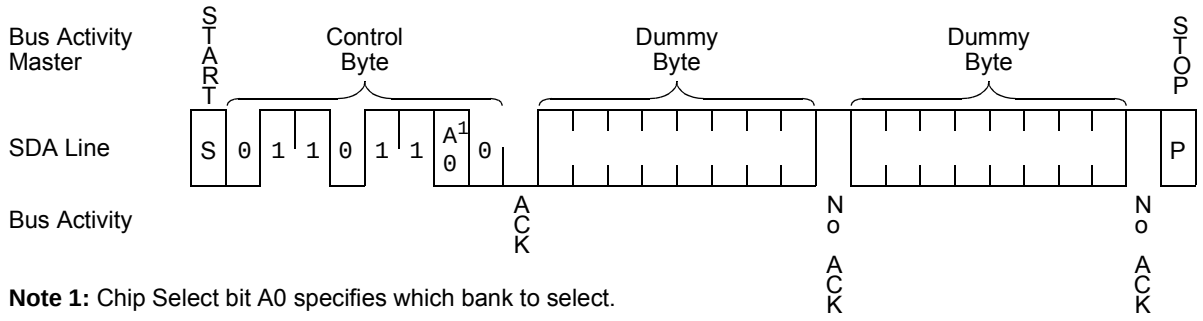
5.1 Set Bank Address (SBA)

The Set Bank Address (SBA) commands are used to select the array bank for future read and write operations.

The master generates a Start condition followed by the corresponding control byte for the chosen SBA command (Table 5-2), with the R/$\overline{W}$ bit set to a logic '0'. Note that Chip Select bit A0 of the control byte effectively determines which bank is selected. The 34AA04 will respond with an Acknowledge, and then the master transmits two dummy bytes. The 34AA04 will not acknowledge either dummy byte. Finally, the master generates a Stop condition to end the operation (Figure 5-1).

Array Read and Write commands will operate in the newly-selected bank until another SBA command is executed, or the 34AA04 experiences a POR or BOR event.

FIGURE 5-1: SET BANK ADDRESS



Note 1: Chip Select bit A0 specifies which bank to select.

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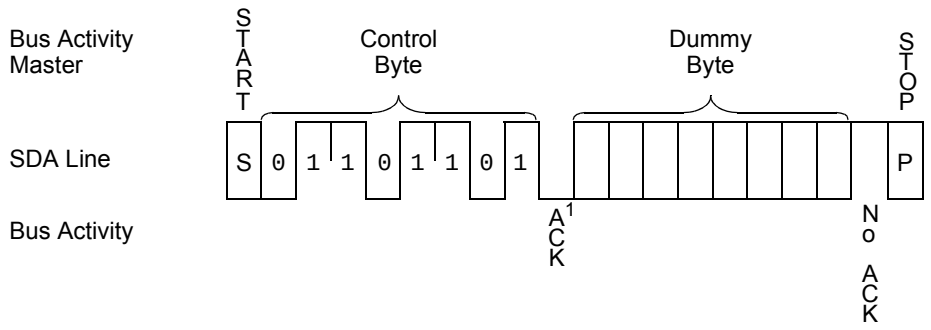
5.2 Read Bank Address (RBA)

The Read Bank Address (RBA) command allows the 34AA04 to indicate which array bank is currently selected.

The master generates a Start condition and transmits the RBA control byte (Table 5-2), with the R/$\overline{W}$ bit set to logic '1'. If Bank 0 is currently selected, the 34AA04 will respond with an Acknowledge signal. If Bank 1 is currently selected, an Acknowledge will not be generated. Regardless of the result, the master must read at least one dummy byte from the 34AA04, transmitting a Not Acknowledge signal after each byte, and generate a Stop condition to end the command (Figure 5-2).

FIGURE 5-2: READ BANK ADDRESS



Note 1: The 34AA04 will only acknowledge if Bank 0 is currently selected.
2: In accordance with the JEDEC spec, the master is allowed to read multiple dummy bytes, transmitting a Not Acknowledge after each byte.

6.0 WRITE OPERATIONS

6.1 Byte Write

Following the Start signal from the master, the control code (4 bits), the Chip Select bits (3 bits) and the R/$\overline{W}$ bit, which is a logic low, are placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that the array address byte will follow, once it has generated an Acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the array address and will be written into the Address Pointer of the 34AA04.

After receiving another Acknowledge signal from the 34AA04, the master device will transmit the data byte to be written into the addressed memory location. The 34AA04 acknowledges again and the master generates a Stop condition. This initiates the internal write cycle, which means that during this time, the 34AA04 will not generate Acknowledge signals (Figure 6-1).

Note:	It is recommended to perform a Set Bank Address command before initiating a Write command to ensure the desired bank is selected.

If an attempt is made to write to a software write-protected portion of the array, the 34AA04 will not acknowledge the data byte, no data will be written, and the device will immediately accept a new command.

6.2 Page Write

The write control byte, array address and the first data byte are transmitted to the 34AA04 in the same way as in a byte write. Instead of generating a Stop condition, the master transmits up to 15 additional data bytes to the 34AA04, which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a Stop condition. Upon receipt of each word, the four lower order Address Pointer bits are internally incremented by one. The higher order four bits of the array address, as well as the bank selection, remain constant. If the master should transmit more than 16 bytes prior to generating the Stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the Stop condition is received, an internal write cycle will begin (Figure 6-2). If an attempt is made to write to a software write-protected portion of the array, the 34AA04 will not acknowledge the data byte, no data will be written, and the device will immediately accept a new command.

Note:	When doing a write of less than 16 bytes, the data in the rest of the page is refreshed along with the data bytes being written. This will force the entire page to endure a write cycle. For this reason, endurance is specified per page.

Note:	Page write operations are limited to writing bytes within a single physical page, regardless of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and end at addresses that are integer multiples of [page size – 1]. If a Page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page, as might be expected. It is, therefore, necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

TABLE 6-1: DEVICE RESPONSE WHEN WRITING DATA

Status	Command	ACK	Address	ACK	Data Byte	ACK	Write Cycle
Protected with SWPn	Page or Byte Write in Protected Block	ACK	Address	ACK	Data	NoACK	No
Not Protected	Page or Byte Write	ACK	Address	ACK	Data	ACK	Yes

FIGURE 6-1: BYTE WRITE

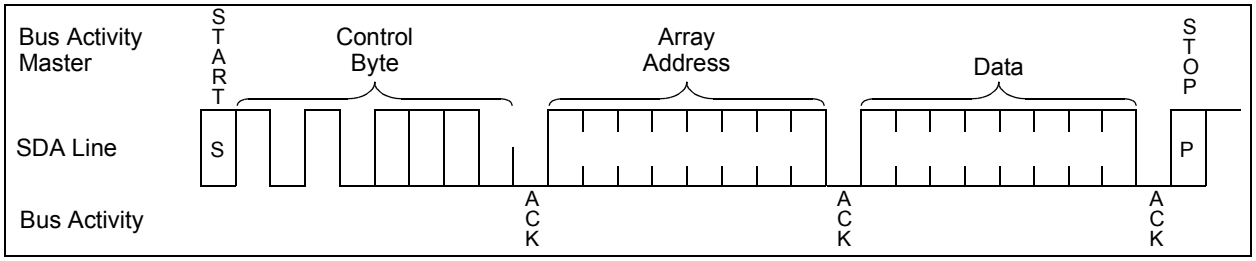


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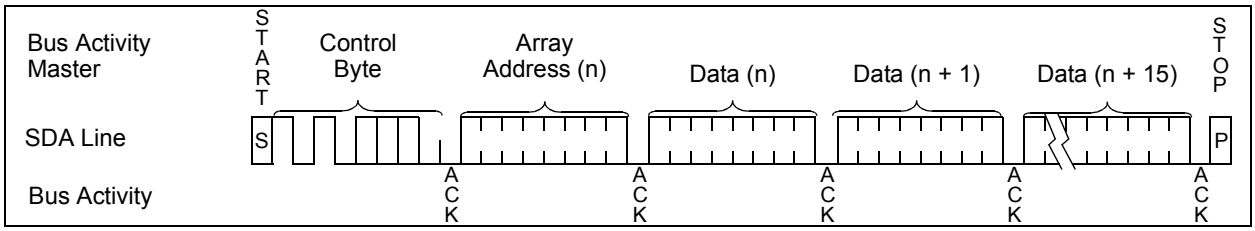
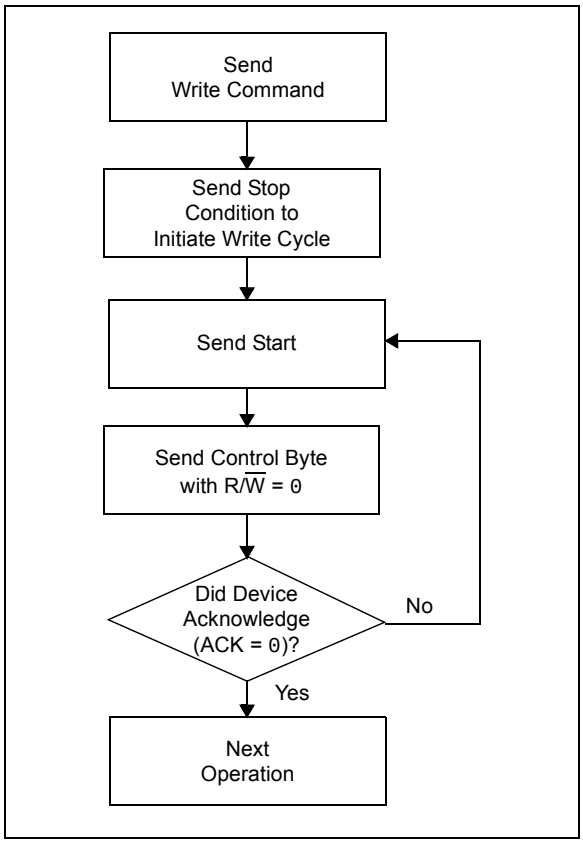
FIGURE 6-2: PAGE WRITE



7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the Stop condition for a Write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a Start condition followed by the control byte for a Write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next Read or Write command. See Figure 7-1 for flow diagram.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW



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8.0 READ OPERATION

Read operations are initiated in the same way as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to '1'. There are three basic types of read operations: current address read, random read and sequential read.

8.1 Current Address Read

The 34AA04 contains an address counter that maintains the address of the last byte accessed, internally incremented by '1'. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n+1. Upon receipt of the slave address with R/$\overline{W}$ bit set to '1', the 34AA04 issues an acknowledge and transmits the 8-bit data value. The master will not acknowledge the transfer, but does generate a Stop condition and the 34AA04 discontinues transmission (Figure 8-1).

8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, the array address must first be set. This is done by sending the array address to the 34AA04 as part of a write operation. Once the array address is sent, the master generates a Start condition following the acknowledge. This terminates the write operation, but not before the internal Address Pointer is set. The master then issues the control byte again, but with the R/$\overline{W}$ bit set to a '1'. The 34AA04 then issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer, but does generate a Stop condition and the 34AA04 discontinues transmission (Figure 8-2).

Note:	It is recommended to perform a Set Bank Address command before initiating a Read command to ensure the desired bank is selected.

8.3 Sequential Read

Sequential reads are initiated in the same way as a random read, with the exception that after the 34AA04 transmits the first data byte, the master issues an acknowledge, as opposed to a Stop condition in a random read. This directs the 34AA04 to transmit the next sequentially addressed 8-bit word (Figure 8-3).

To provide sequential reads, the 34AA04 contains an internal Address Pointer, which is incremented by one at the completion of each operation. Sequential reads are limited to a single bank per operation, so the Address Pointer allows the entire memory contents of the current bank to be serially read during one operation.

8.4 Noise Protection and Brown-Out

The 34AA04 employs a VCC threshold detector circuit which disables the internal erase/write logic if the VCC is below 1.35V at nominal conditions.

The SCL and SDA inputs have Schmitt Trigger and filter circuits which suppress noise spikes to assure proper device operation, even on a noisy bus.

FIGURE 8-1: CURRENT ADDRESS READ

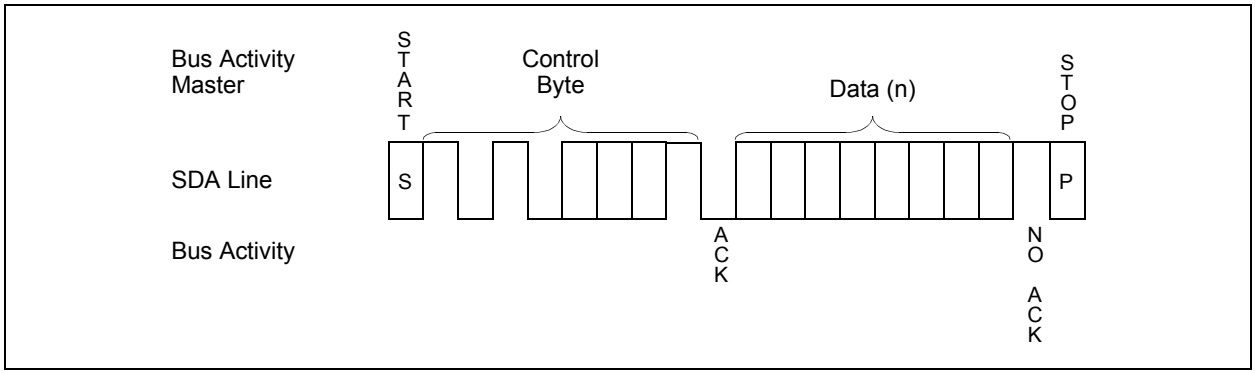


FIGURE 8-2: RANDOM READ

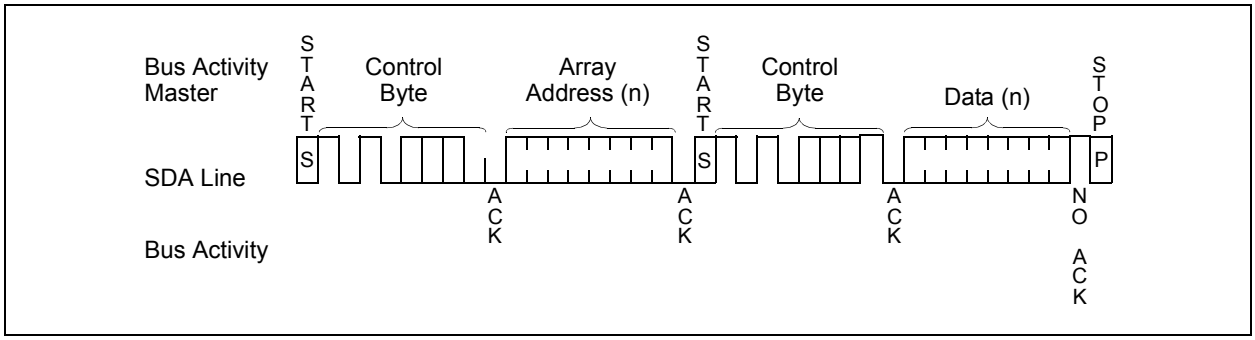
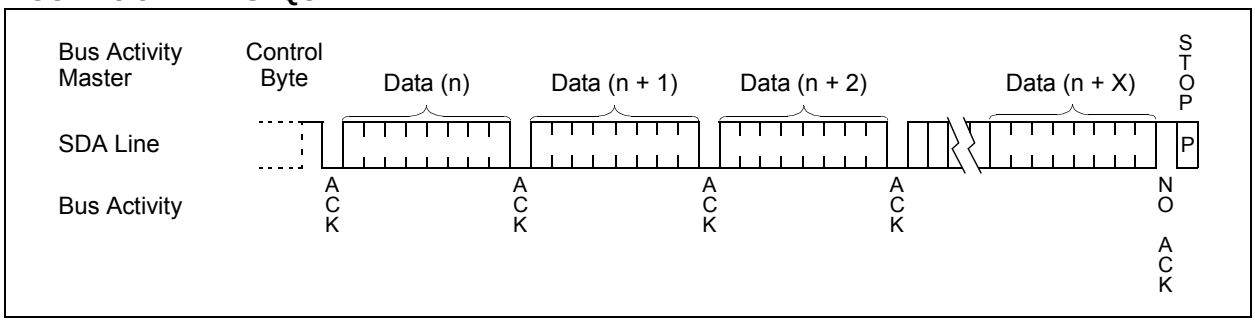


FIGURE 8-3: SEQUENTIAL READ



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9.0 SOFTWARE WRITE PROTECTION

The 34AA04 has a reversible software write-protect feature that allows each of four 128-byte blocks to be individually write-protected. The write protection is set by executing the Set Write Protect (SWPn) commands. The Clear All Write Protect (CWP) command is used to unprotect all of the blocks at once. It is not possible to unprotect blocks individually. The Read Protection Status (RPS) commands are used to determine if a given block is currently write-protected.

The 34AA04 will not respond with an Acknowledge following the data bytes of write operations that are attempted within a write-protected block.

Note: The write-protect state of each block is stored in nonvolatile bits.

TABLE 9-1: BLOCK ADDRESS RANGE

Block	Logical Array Address
Block 0	000h - 07Fh
Block 1	080h - 0FFh
Block 2	100h - 17Fh
Block 3	180h - 1FFh

Note: The comparison between the A0, A1, and A2 pins and the corresponding Chip Select bits is disabled for software Write-Protect commands.

TABLE 9-2: SOFTWARE WRITE PROTECTION INSTRUCTION SET

Function	Abbr	Control Byte								A0 Pin
		Control Code				Chip Select Bits			R/$\overline{W}$	
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Set Write Protection, block 0	SWP0	0	1	1	0	0	0	1	0	V_{HV}
Set Write Protection, block 1	SWP1					1	0	0	0	V_{HV}
Set Write Protection, block 2	SWP2					1	0	1	0	V_{HV}
Set Write Protection, block 3	SWP3					0	0	0	0	V_{HV}
Clear All Write Protection	CWP					0	1	1	0	V_{HV}
Read Protection Status, block 0	RPS0					0	0	1	1	0, 1, or V_{HV}
Read Protection Status, block 1	RPS1					1	0	0	1	0, 1, or V_{HV}
Read Protection Status, block 2	RPS2					1	0	1	1	0, 1, or V_{HV}
Read Protection Status, block 3	RPS3					0	0	0	1	0, 1, or V_{HV}

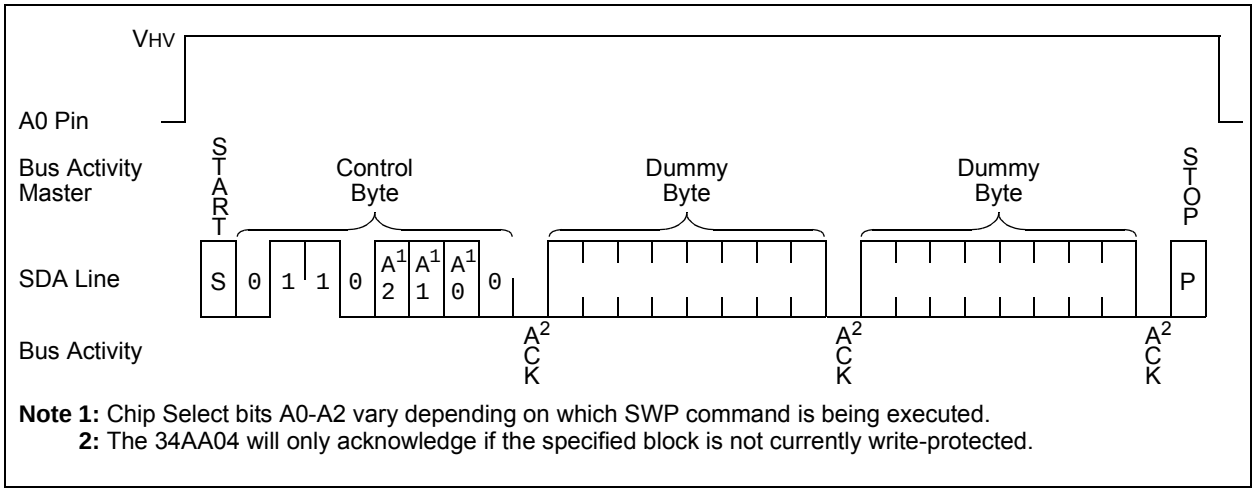
9.1 Set Write Protection (SWPn)

The Set Write Protection (SWP) commands are used to set the reversible write protection for individual array blocks. There are four different SWP commands, one for each block.

V_{HV} must be applied to the A0 pin for the entire SWP command. Then, the command is executed in a manner similar to an array byte Write command. Following the Start condition, the '0110' control code and the three Chip Select bits that correspond to the desired SWP command (Table 9-2) are transmitted by the master, along with the R/$\overline{W}$ bit as a logic '0'. After the 34AA04 responds with an Acknowledge, the master transmits two dummy bytes, after each of which the 34AA04 responds with an Acknowledge. Finally, the master generates a Stop condition, which initiates the internal write cycle and, during this time, the 34AA04 will not generate Acknowledge signals (Figure 9-1).

If the specified block is already write-protected, the SWP command is ignored, no Acknowledges will be sent, and the internal write cycle will not be executed.

FIGURE 9-1: SET WRITE PROTECTION



Note 1: Chip Select bits A0-A2 vary depending on which SWP command is being executed.
2: The 34AA04 will only acknowledge if the specified block is not currently write-protected.

TABLE 9-3: DEVICE RESPONSE WHEN DEFINING WRITE PROTECTION

Status	Command	ACK	Address	ACK	Data Byte	ACK	Write Cycle
Protected with SWPn	SWPn	NoACK	Don't Care	NoACK	Don't Care	NoACK	No
	CWP	ACK	Don't Care	ACK	Don't Care	ACK	Yes
Not Protected	SWPn or CWP	ACK	Don't Care	ACK	Don't Care	ACK	Yes

9.2 Clear All Write Protection (CWP)

The Clear All Write Protection (CWP) command resets all of the write protection in a single operation. It is executed in the same manner as a SWP command, except using the CWP control byte (Table 9-2).

The 34AA04 will always acknowledge and execute a CWP command if an internal write cycle is not in progress, regardless of the state of write protection.

9.3 Read Protection Status (RPS)

The Read Protection Status (RPS) commands provide a way of determining whether or not the specified block is currently write-protected.

Following the Start condition, the master transmits the control byte for the desired RPS command (Table 9-2), with the R/$\overline{W}$ bit set to logic '1'. If the specified block is not write-protected, the 34AA04 will respond with an Acknowledge signal. If the block is currently write-protected, an Acknowledge will not be generated. Regardless of the result, the master must read at least one dummy byte from the 34AA04, transmitting a Not Acknowledge signal after each byte, and generate a Stop condition to end the command (Figure 9-3).

FIGURE 9-2: CLEAR ALL WRITE PROTECTION

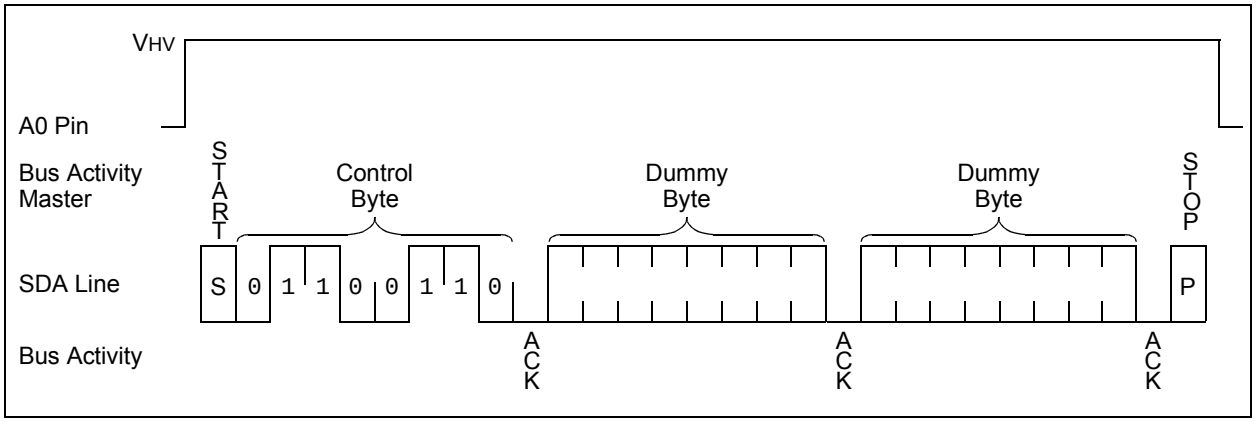


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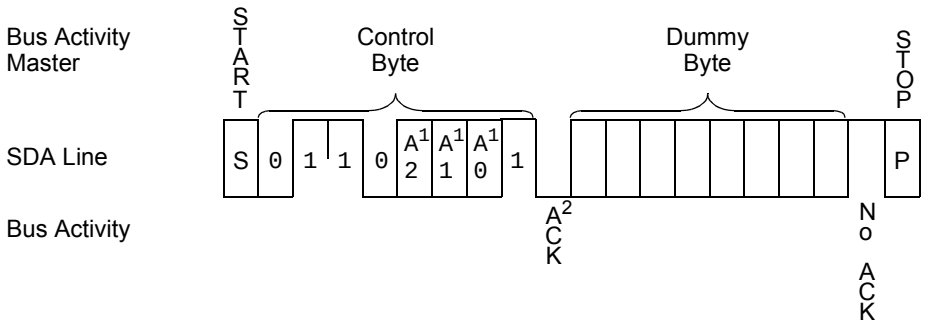
FIGURE 9-3: READ PROTECTION STATUS



Note 1: Chip Select bits A0-A2 vary depending on which RPS command is being performed.
2: The 34AA04 will only acknowledge if the specified block is not currently write-protected.
3: In accordance with the JEDEC spec, the master is allowed to read multiple dummy bytes, transmitting a Not Acknowledge after each byte.

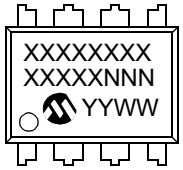
TABLE 9-4: DEVICE RESPONSE WHEN READING WRITE PROTECTION STATUS

Status	Command	ACK	Data Byte	ACK
Protected with SWPn	RPSn	NoACK	Don't Care	NoACK
Not Protected	RPSn	ACK	Don't Care	NoACK

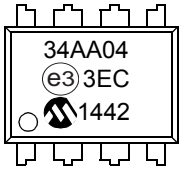
10.0 PACKAGING INFORMATION

10.1 Package Marking Information

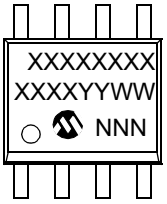
8-Lead PDIP (300 mil)



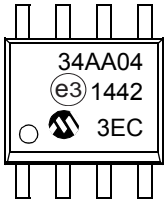
Example:



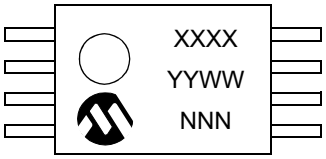
8-Lead SOIC (3.90 mm)



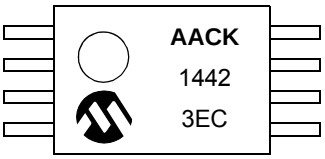
Example:



8-Lead TSSOP

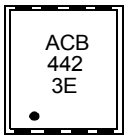


Example:



8-Lead 2x3 TDFN

Example:



8-Lead 2x3 UDFN

Example:

1st Line Marking Codes					
Part Number	**PDIP**	**SOIC**	**TSSOP**	**TDFN**	**UDFN**
34AA04	34AA04	34AA04	AACK	ACB	CAC

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Legend:	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	JEDEC® designator for Matte Tin (Sn)

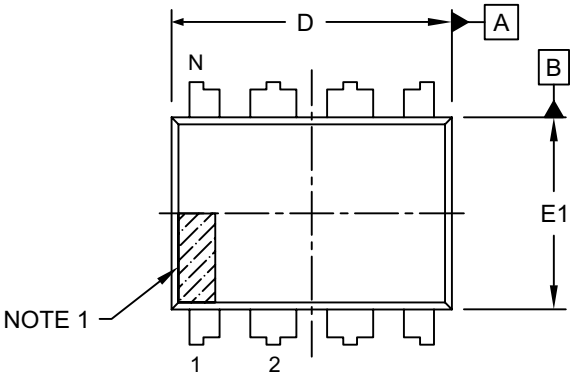
Note: For very small packages with no room for the JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

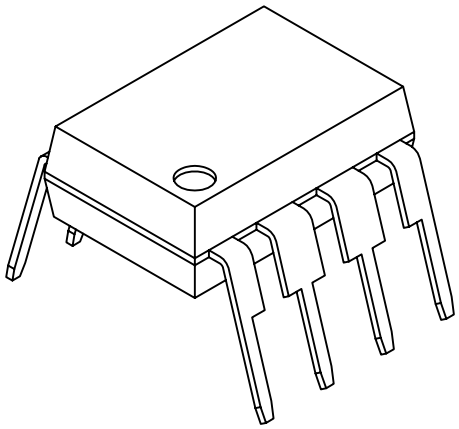
*****Standard OTP marking consists of Microchip part number, year code, week code, and traceability code.

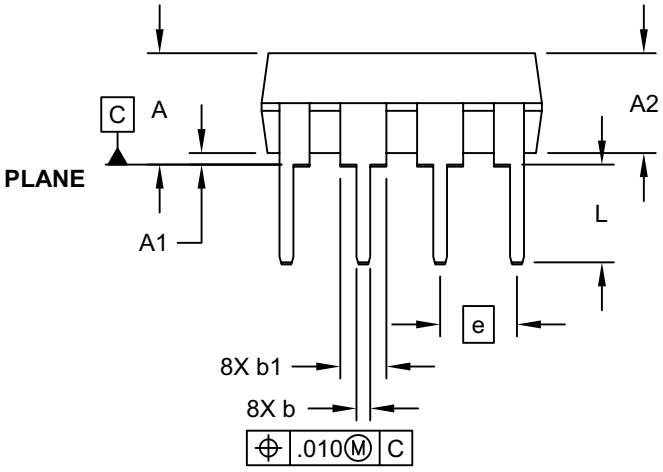
8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

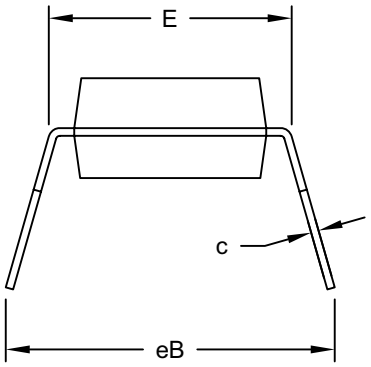


TOP VIEW





SIDE VIEW



END VIEW

Microchip Technology Drawing No. C04-018D Sheet 1 of 2

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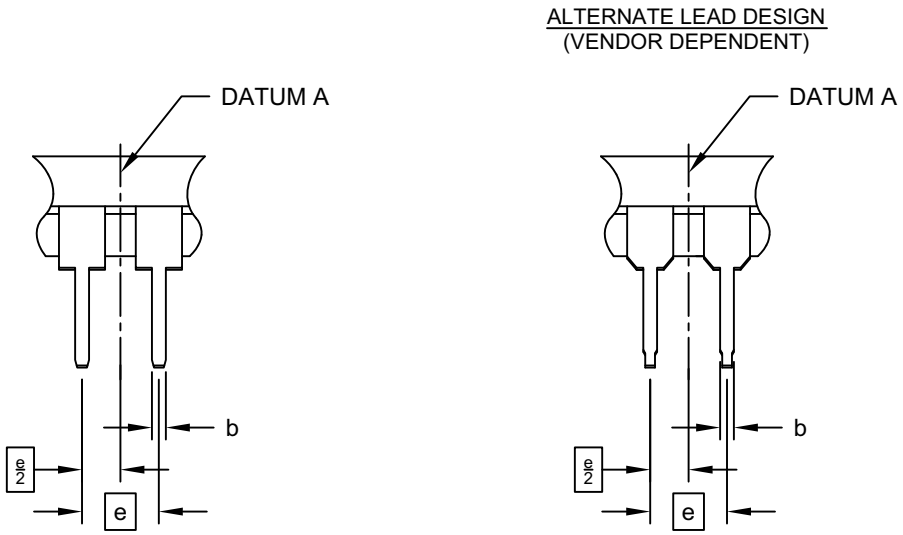
8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	-	-	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-018D Sheet 2 of 2

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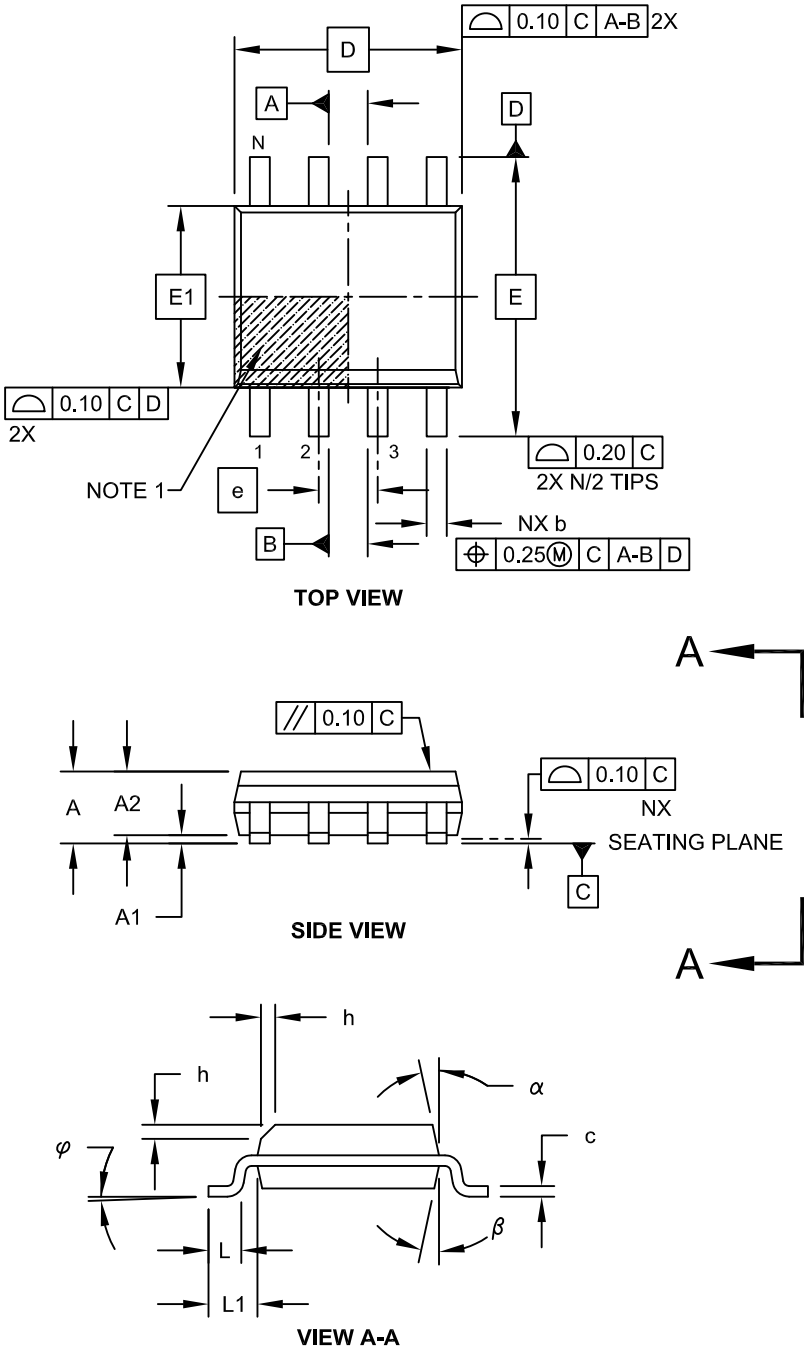
8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057C Sheet 1 of 2

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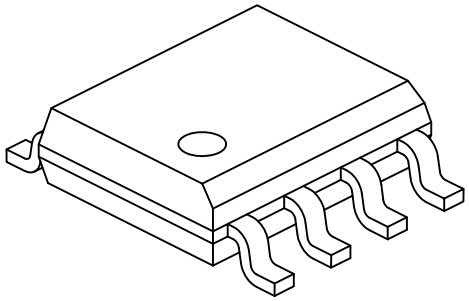
8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

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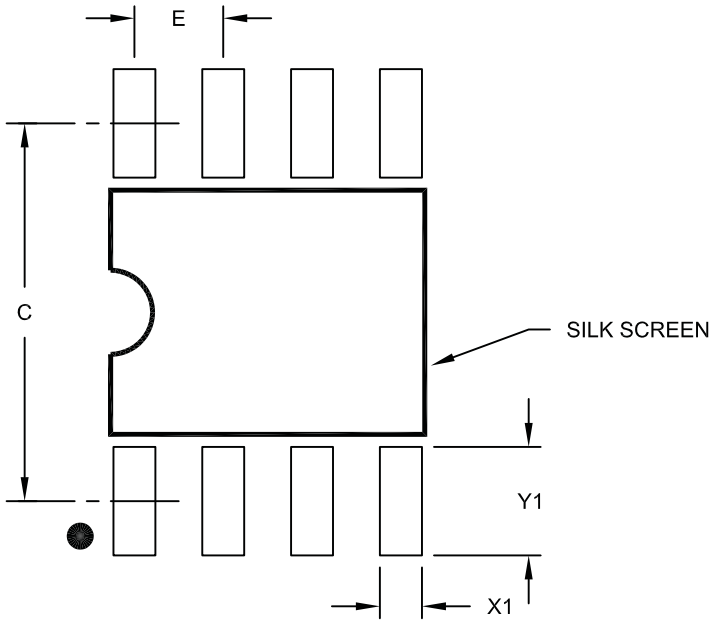
8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

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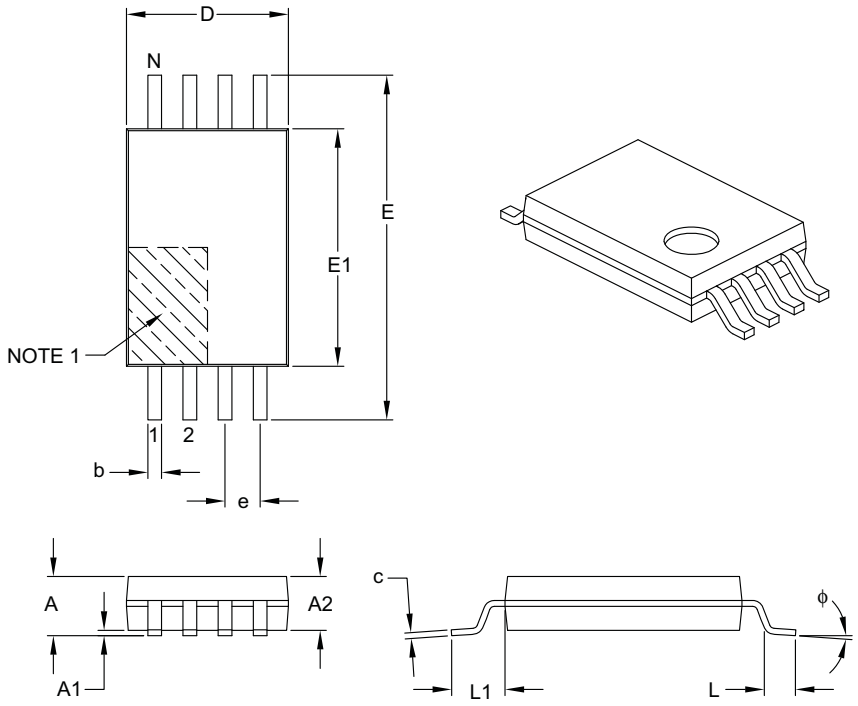
8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	2.90	3.00	3.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

Notes:

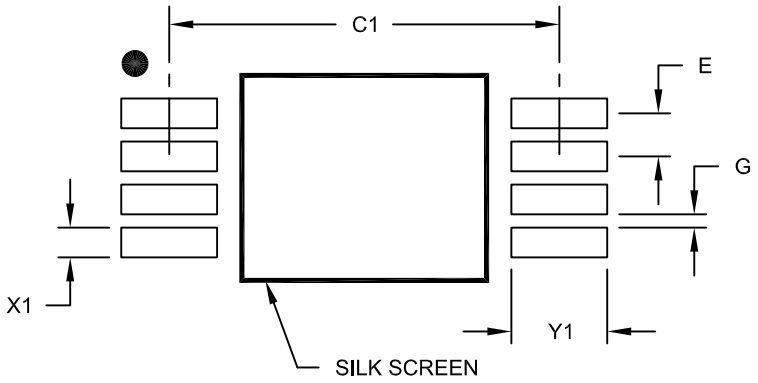
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086B

8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C1		5.90	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2086A

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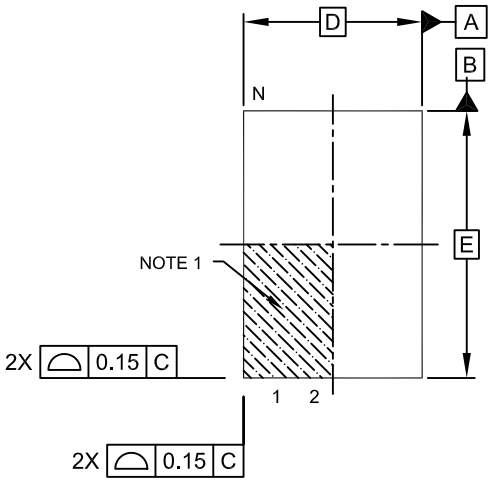
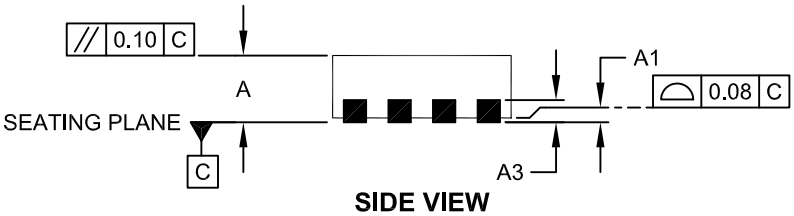
8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75mm Body [TDFN]

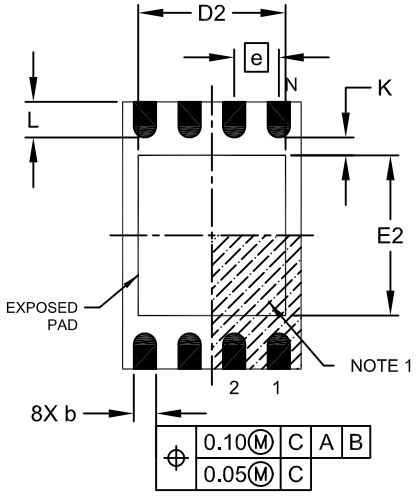
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

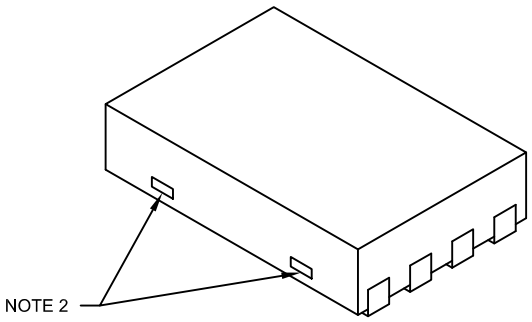


BOTTOM VIEW

Microchip Technology Drawing No. C04-129C Sheet 1 of 2

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.20	-	1.60
Exposed Pad Width	E2	1.20	-	1.60
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.25	0.30	0.45
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-129C Sheet 2 of 2

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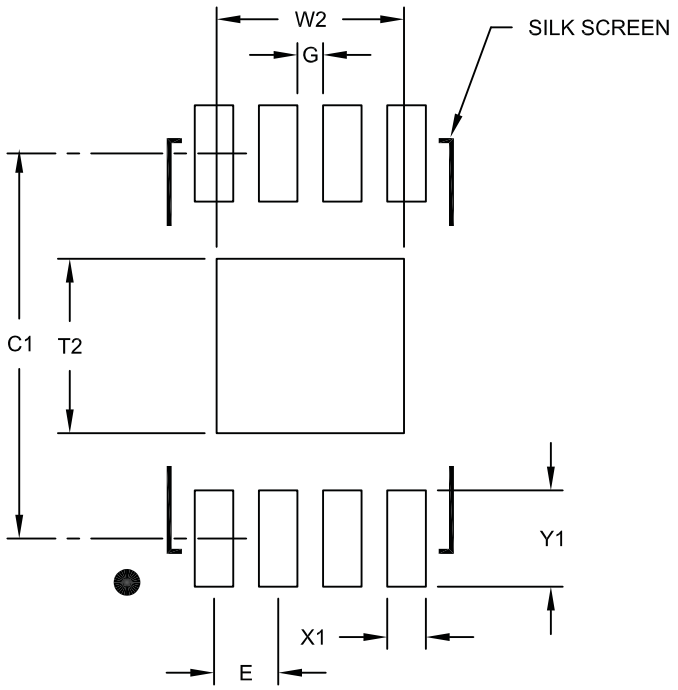
8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75 mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			1.46
Optional Center Pad Length	T2			1.36
Contact Pad Spacing	C1		3.00	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.75
Distance Between Pads	G	0.20		

Notes:

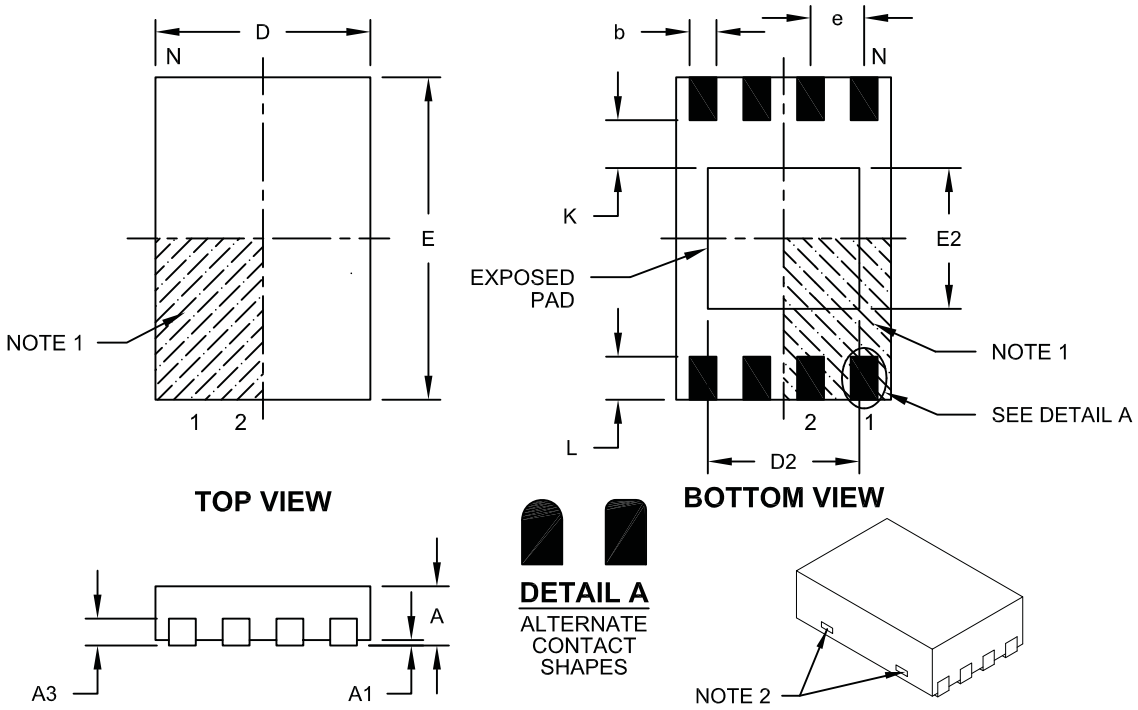
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2129A

8-Lead Plastic Dual Flat, No Lead Package (MU) – 2x3x0.5 mm Body [UDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.45	0.50	0.55
Standoff	A1			0.07
Contact Thickness	A3		0.127 REF	
Overall Length	D	1.95	2.00	2.05
Overall Width	E	2.95	3.00	3.05
Exposed Pad Length	D2	1.30	1.40	1.50
Exposed Pad Width	E2	1.20	1.30	1.40
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.25	0.30	0.35
Contact-to-Exposed Pad	K		0.55 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

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Microchip Technology Drawing No. C04-136B

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8-Lead Plastic Dual Flat, No Lead Package (MU) – 2x3x0.5 mm Body [UDFN]

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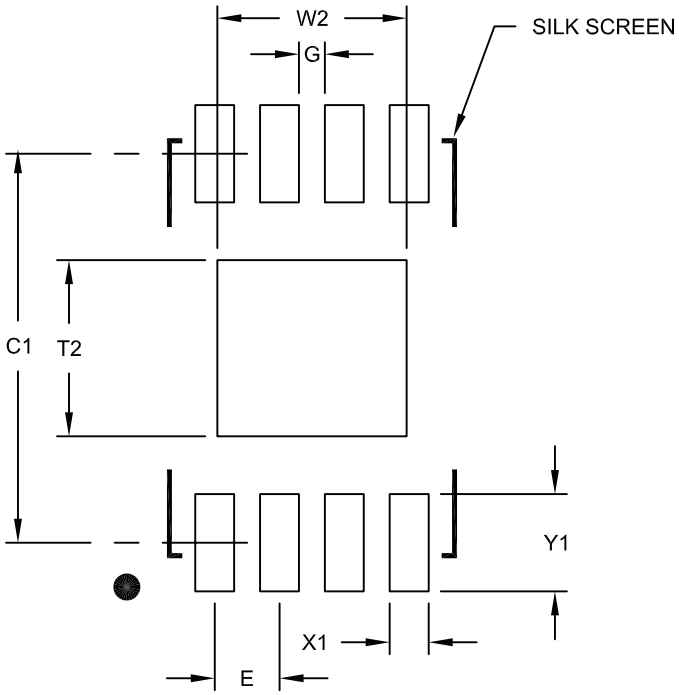

RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	W2			1.46
Optional Center Pad Length	T2			1.36
Contact Pad Spacing	C1		3.00	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2136A

APPENDIX A: REVISION HISTORY

Revision B (10/2014)

- Removed “Preliminary” condition.
- Updated Section 10.0, Packaging Information.
- Minor typographical corrections.

Revision A (03/2014)

Original release of this document.

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PART NO. – X /XX	Examples:
Device / Temperature Range / Package	a) 34AA04-I/P: Industrial Temperature, 1.7V, PDIP package
Device: 34AA04: = 1.7V, 4 Kbit I^2C Serial EEPROM 34AA04T: = 1.7V, 4 Kbit I^2C Serial EEPROM (Tape and Reel)	b) 34AA04-I/SN: Industrial Temperature, 1.7V, SOIC package
Temperature Range: I = -40°C to +85°C E = -40°C to +125°C	c) 34AA04T-E/MUY: Tape and Reel, Automotive Temperature, 1.7V, UDFN package
Package: P = Plastic DIP (300 mil body), 8-lead SN = Plastic SOIC (3.90 mm body), 8-lead ST = Plastic TSSOP (4.4 mm), 8-lead MNY(1) = Plastic Dual Flat, No Lead Package (2x3x0.75 mm body), 8-lead MUY(1) = Plastic Dual Flat, No Lead Package (2x3x0.5 mm body), 8-lead	d) 34AA04T-I/MNY: Tape and Reel, Industrial Temperature, 1.7V, TDFN package
	e) 34AA04-E/ST: Automotive Temperature, 1.7V, TSSOP package

Note 1: "Y" indicates a Nickel Palladium Gold (NiPdAu) finish.

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