



RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This 87 W asymmetrical Doherty RF power LDMOS transistor is designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 2110 to 2200 MHz.

2100 MHz

- Typical Doherty Single-Carrier W-CDMA Characterization Performance:
 $V_{DD} = 30$ Vdc, $I_{DQA} = 600$ mA, $V_{GSB} = 0.5$ Vdc, $P_{out} = 87$ W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

| Frequency | G_{ps} (dB) | η_D (%) | Output PAR (dB) | ACPR (dBc) |
|-----------|---------------|--------------|-----------------|------------|
| 2110 MHz | 15.1 | 48.5 | 8.1 | -30.2 |
| 2155 MHz | 15.7 | 48.9 | 7.9 | -30.2 |
| 2200 MHz | 15.3 | 47.2 | 7.8 | -33.7 |

Features

- Advanced high performance in-package Doherty
- Designed for wide instantaneous bandwidth applications
- Greater negative gate-source voltage range for improved Class C operation
- Able to withstand extremely high output VSWR and broadband operating conditions
- Designed for digital predistortion error correction systems

A3T21H450W23SR6

2110–2200 MHz, 87 W AVG., 30 V AIRFAST RF POWER LDMOS TRANSISTOR



ACP-1230S-4L2S

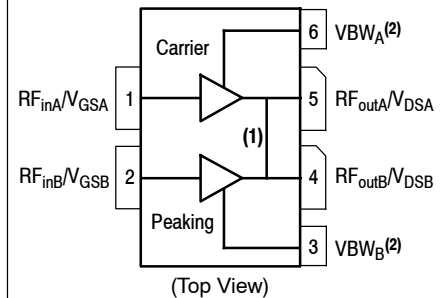


Figure 1. Pin Connections

- Pin connections 4 and 5 are DC coupled and RF independent.
- Device cannot operate with V_{DD} current supplied through pin 3 and pin 6.

Table 1. Maximum Ratings

| Rating | Symbol | Value | Unit |
|--|-----------|-------------|------|
| Drain-Source Voltage | V_{DSS} | -0.5, +65 | Vdc |
| Gate-Source Voltage | V_{GS} | -6.0, +10 | Vdc |
| Operating Voltage | V_{DD} | 32, +0 | Vdc |
| Storage Temperature Range | T_{stg} | -65 to +150 | °C |
| Case Operating Temperature Range | T_C | -40 to +150 | °C |
| Operating Junction Temperature Range (1,2) | T_J | -40 to +225 | °C |

Table 2. Thermal Characteristics

| Characteristic | Symbol | Value (2,3) | Unit |
|--|-----------------|-------------|------|
| Thermal Resistance, Junction to Case Case Temperature 78°C, 87 W Avg., W-CDMA, 30 Vdc, $I_{DQA} = 600$ mA, $V_{GSB} = 0.5$ Vdc, 2155 MHz | $R_{\theta JC}$ | 0.16 | °C/W |

Table 3. ESD Protection Characteristics

| Test Methodology | Class |
|---------------------------------------|-------|
| Human Body Model (per JESD22-A114) | 2 |
| Charge Device Model (per JESD22-C101) | C3 |

Table 4. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|------|

Off Characteristics (4)

| | | | | | |
|---|-----------|---|---|----|-----------------|
| Zero Gate Voltage Drain Leakage Current ($V_{DS} = 65$ Vdc, $V_{GS} = 0$ Vdc) | I_{DSS} | — | — | 10 | μAdc |
| Zero Gate Voltage Drain Leakage Current ($V_{DS} = 32$ Vdc, $V_{GS} = 0$ Vdc) | I_{DSS} | — | — | 5 | μAdc |
| Gate-Source Leakage Current ($V_{GS} = 5$ Vdc, $V_{DS} = 0$ Vdc) | I_{GSS} | — | — | 1 | μAdc |

On Characteristics - Side A, Carrier

| | | | | | |
|---|--------------|-----|------|-----|-----|
| Gate Threshold Voltage ($V_{DS} = 10$ Vdc, $I_D = 180$ μAdc) | $V_{GS(th)}$ | 1.4 | 1.8 | 2.3 | Vdc |
| Gate Quiescent Voltage ($V_{DD} = 30$ Vdc, $I_D = 600$ mAdc, Measured in Functional Test) | $V_{GSA(Q)}$ | 2.2 | 2.6 | 3.0 | Vdc |
| Drain-Source On-Voltage ($V_{GS} = 10$ Vdc, $I_D = 1.8$ Adc) | $V_{DS(on)}$ | 0.0 | 0.15 | 0.3 | Vdc |

On Characteristics - Side B, Peaking

| | | | | | |
|--|--------------|-----|------|-----|-----|
| Gate Threshold Voltage ($V_{DS} = 10$ Vdc, $I_D = 360$ μAdc) | $V_{GS(th)}$ | 0.8 | 1.2 | 1.6 | Vdc |
| Drain-Source On-Voltage ($V_{GS} = 10$ Vdc, $I_D = 3.6$ Adc) | $V_{DS(on)}$ | 0.0 | 0.15 | 0.3 | Vdc |

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.nxp.com/RF/calculators>.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.nxp.com/RF> and search for AN1955.
4. Side A and Side B are tied together for these measurements.

(continued)

Table 4. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted) (continued)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|----------|------|-------|-------|------|
| Functional Tests ^(1,2,3) (In NXP Doherty Production Test Fixture, 50 ohm system) $V_{DD} = 30\text{ Vdc}$, $I_{DQA} = 600\text{ mA}$, $V_{GSB} = 0.5\text{ Vdc}$, $P_{out} = 87\text{ W Avg.}$, $f = 2200\text{ MHz}$, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ $\pm 5\text{ MHz}$ Offset. | | | | | |
| Power Gain | G_{ps} | 14.2 | 15.4 | 16.2 | dB |
| Drain Efficiency | η_D | 44.0 | 47.0 | — | % |
| P_{out} @ 3 dB Compression Point, CW | P3dB | 55.0 | 55.9 | — | dBm |
| Adjacent Channel Power Ratio | ACPR | — | -35.2 | -30.9 | dBc |

Load Mismatch ⁽³⁾ (In NXP Doherty Production Test Fixture, 50 ohm system) $I_{DQA} = 600\text{ mA}$, $V_{GSB} = 0.5\text{ Vdc}$, $f = 2155\text{ MHz}$, 12 μsec (on), 10% Duty Cycle

| | |
|---|-----------------------|
| VSWR 10:1 at 32 Vdc, 400 W Pulsed CW Output Power (3 dB Input Overdrive from 251 W Pulsed CW Rated Power) | No Device Degradation |
|---|-----------------------|

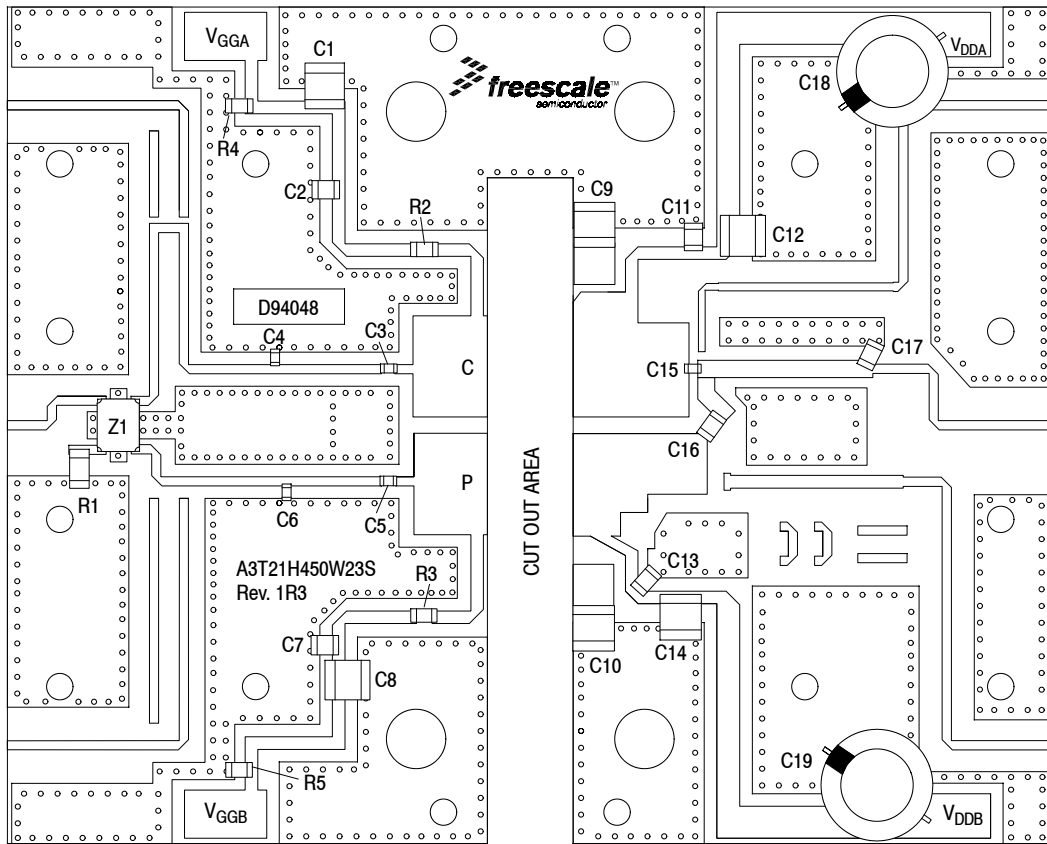
Typical Performance ⁽³⁾ (In NXP Doherty Characterization Test Fixture, 50 ohm system) $V_{DD} = 30\text{ Vdc}$, $I_{DQA} = 600\text{ mA}$, $V_{GSB} = 0.5\text{ Vdc}$, 2110–2200 MHz Bandwidth

| | | | | | |
|--|------------------|---|-------|---|----------|
| P_{out} @ 3 dB Compression Point ⁽⁴⁾ | P3dB | — | 501 | — | W |
| AM/PM (Maximum value measured at the P3dB compression point across the 2110–2200 MHz bandwidth) | Φ | — | -19 | — | $^\circ$ |
| VBW Resonance Point (IMD Third Order Intermodulation Inflection Point) | VBW_{res} | — | 180 | — | MHz |
| Gain Flatness in 90 MHz Bandwidth @ $P_{out} = 87\text{ W Avg.}$ | G_F | — | 0.7 | — | dB |
| Gain Variation over Temperature (-30°C to +85°C) | ΔG | — | 0.007 | — | dB/°C |
| Output Power Variation over Temperature (-30°C to +85°C) | ΔP_{1dB} | — | 0.007 | — | dB/°C |

Table 5. Ordering Information

| Device | Tape and Reel Information | Package |
|-----------------|---|----------------|
| A3T21H450W23SR6 | R6 Suffix = 150 Units, 56 mm Tape Width, 13-inch Reel | ACP-1230S-4L2S |

- V_{DDA} and V_{DDB} must be tied together and powered by a single DC power supply.
- Part internally matched both on input and output.
- Measurements made with device in an asymmetrical Doherty configuration.
- P3dB = $P_{avg} + 7.0\text{ dB}$ where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.



Note: V_{DDA} and V_{ddb} must be tied together and powered by a single DC power supply.

Figure 2. A3T21H450W23SR6 Characterization Test Circuit Component Layout

Table 6. A3T21H450W23SR6 Characterization Test Circuit Component Designations and Values

| Part | Description | Part Number | Manufacturer |
|---------------------------|---|----------------------|--------------|
| C1, C8, C9, C10, C12, C14 | 10 μ F Chip Capacitor | C5750X7S2A106M230KB | TDK |
| C2, C7, C11, C13 | 9.1 pF Chip Capacitor | ATC100B9R1CT500XT | ATC |
| C3, C5 | 9.1 pF Chip Capacitor | ATC600F9R1BT250XT | ATC |
| C4 | 1 pF Chip Capacitor | ATC100B1R0CT500XT | ATC |
| C6 | 0.4 pF Chip Capacitor | ATC100B0R4CT500XT | ATC |
| C15 | 5.1 pF Chip Capacitor | ATC600F5R1BT250XT | ATC |
| C16 | 15 pF Chip Capacitor | ATC100B150JT500XT | ATC |
| C17 | 0.2 pF Chip Capacitor | ATC100B0R2BT500XT | ATC |
| C18, C19 | 470 μ F, 63 V Electrolytic Capacitor | MCGPR63V477M13X26-RH | Multicomp |
| R1 | 50 Ω , 10 W Chip Resistor | C10A50Z4 | Anaren |
| R2, R3 | 3.9 Ω , 1/4 W Chip Resistor | CRCW12063R90FKEA | Vishay |
| R4, R5 | 1.8 k Ω , 1/4 W Chip Resistor | CRCW12061K80FKEA | Vishay |
| Z1 | 2000–2300 MHz Band, 90°, 5 dB Directional Coupler | X3C21P1-05S | Anaren |
| PCB | Rogers RO4350B, 0.020", $\epsilon_r = 3.66$ | D94048 | MTL |

TYPICAL CHARACTERISTICS — 2110–2200 MHz

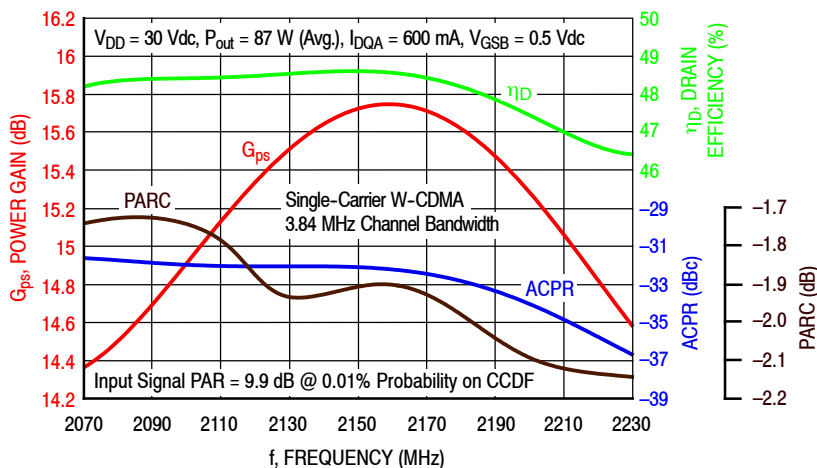


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ $P_{out} = 87$ Watts Avg.

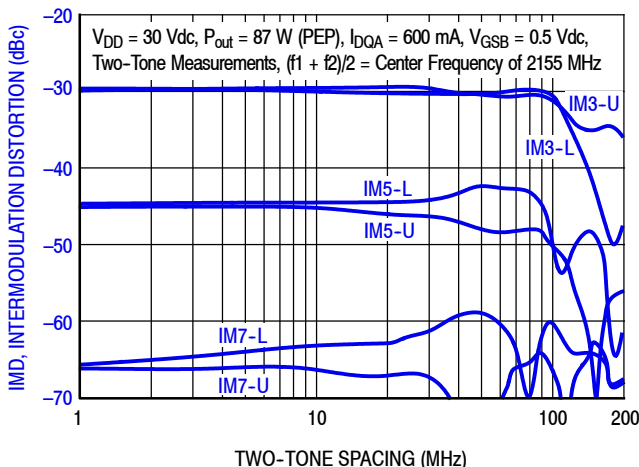


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

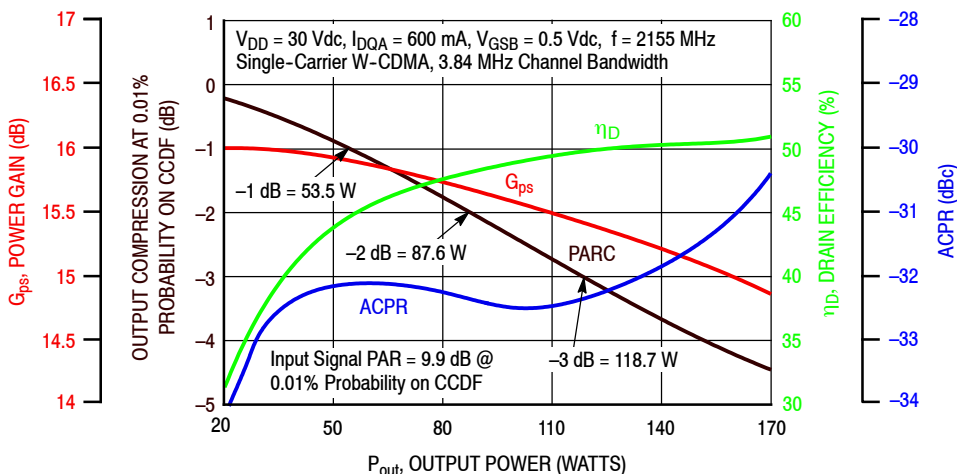


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS — 2110–2200 MHz

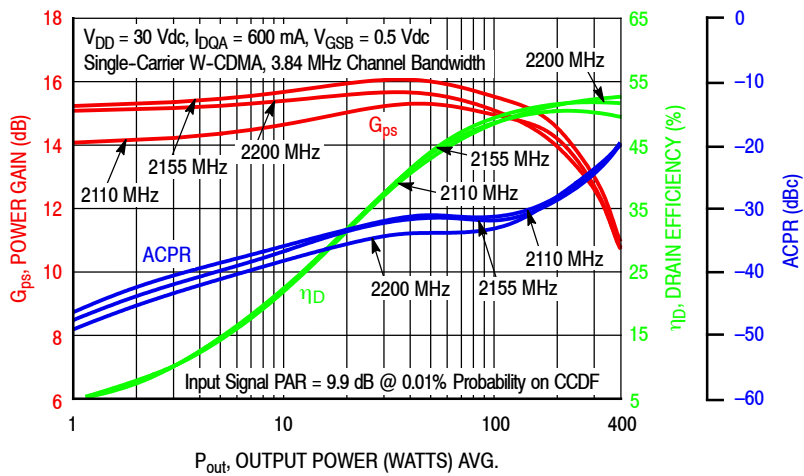


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

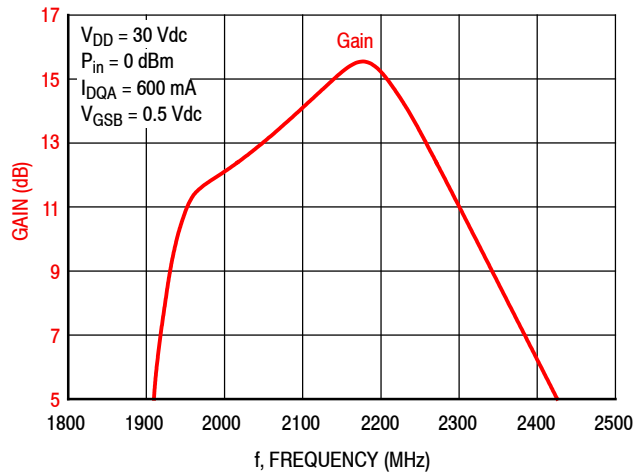


Figure 7. Broadband Frequency Response

Table 7. Carrier Side Load Pull Performance — Maximum Power Tuning

$V_{DD} = 30$ Vdc, $I_{DQA} = 804$ mA, Pulsed CW, 10 μ sec(on), 10% Duty Cycle

| f (MHz) | Z_{source} (Ω) | Z_{in} (Ω) | Max Output Power | | | | | |
|---------|---------------------------|-----------------------|-------------------------------|-----------|-------|-----|--------------|--------------------|
| | | | P1dB | | | | | |
| | | | $Z_{load}^{(1)}$ (Ω) | Gain (dB) | (dBm) | (W) | η_D (%) | AM/PM ($^\circ$) |
| 2110 | 2.26 – j6.69 | 2.28 + j6.33 | 1.26 – j4.31 | 18.2 | 53.5 | 224 | 58.7 | -14 |
| 2140 | 2.79 – j7.42 | 2.93 + j7.10 | 1.32 – j4.37 | 18.3 | 53.4 | 218 | 58.1 | -15 |
| 2170 | 4.03 – j8.18 | 3.88 + j7.96 | 1.29 – j4.36 | 18.3 | 53.3 | 216 | 57.9 | -14 |
| 2200 | 5.37 – j9.47 | 5.43 + j8.78 | 1.32 – j4.37 | 18.3 | 53.3 | 213 | 56.4 | -15 |

| f (MHz) | Z_{source} (Ω) | Z_{in} (Ω) | Max Output Power | | | | | |
|---------|---------------------------|-----------------------|-------------------------------|-----------|-------|-----|--------------|--------------------|
| | | | P3dB | | | | | |
| | | | $Z_{load}^{(2)}$ (Ω) | Gain (dB) | (dBm) | (W) | η_D (%) | AM/PM ($^\circ$) |
| 2110 | 2.26 – j6.69 | 2.20 + j6.63 | 1.24 – j4.55 | 15.9 | 54.2 | 263 | 59.3 | -19 |
| 2140 | 2.79 – j7.42 | 2.87 + j7.50 | 1.30 – j4.58 | 16.1 | 54.1 | 257 | 59.0 | -19 |
| 2170 | 4.03 – j8.18 | 3.90 + j8.49 | 1.31 – j4.57 | 16.1 | 54.1 | 256 | 58.7 | -18 |
| 2200 | 5.37 – j9.47 | 5.62 + j9.53 | 1.31 – j4.54 | 16.0 | 54.0 | 253 | 57.6 | -19 |

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 8. Carrier Side Load Pull Performance — Maximum Efficiency Tuning

$V_{DD} = 30$ Vdc, $I_{DQA} = 804$ mA, Pulsed CW, 10 μ sec(on), 10% Duty Cycle

| f (MHz) | Z_{source} (Ω) | Z_{in} (Ω) | Max Drain Efficiency | | | | | |
|---------|---------------------------|-----------------------|-------------------------------|-----------|-------|-----|--------------|--------------------|
| | | | P1dB | | | | | |
| | | | $Z_{load}^{(1)}$ (Ω) | Gain (dB) | (dBm) | (W) | η_D (%) | AM/PM ($^\circ$) |
| 2110 | 2.26 – j6.69 | 2.33 + j6.54 | 2.68 – j3.37 | 20.7 | 51.7 | 148 | 69.2 | -20 |
| 2140 | 2.79 – j7.42 | 3.03 + j7.31 | 2.73 – j3.29 | 20.9 | 51.4 | 138 | 67.3 | -20 |
| 2170 | 4.03 – j8.18 | 3.98 + j8.13 | 2.24 – j3.62 | 20.3 | 52.1 | 163 | 67.2 | -18 |
| 2200 | 5.37 – j9.47 | 5.53 + j9.11 | 2.19 – j3.17 | 20.7 | 51.6 | 144 | 65.5 | -19 |

| f (MHz) | Z_{source} (Ω) | Z_{in} (Ω) | Max Drain Efficiency | | | | | |
|---------|---------------------------|-----------------------|-------------------------------|-----------|-------|-----|--------------|--------------------|
| | | | P3dB | | | | | |
| | | | $Z_{load}^{(2)}$ (Ω) | Gain (dB) | (dBm) | (W) | η_D (%) | AM/PM ($^\circ$) |
| 2110 | 2.26 – j6.69 | 2.25 + j6.72 | 2.63 – j3.88 | 18.3 | 52.7 | 187 | 68.7 | -24 |
| 2140 | 2.79 – j7.42 | 3.04 + j7.57 | 2.84 – j3.95 | 18.3 | 52.5 | 177 | 66.4 | -22 |
| 2170 | 4.03 – j8.18 | 4.05 + j8.54 | 2.49 – j4.00 | 18.1 | 52.9 | 193 | 66.8 | -21 |
| 2200 | 5.37 – j9.47 | 5.86 + j9.55 | 2.54 – j3.69 | 18.3 | 52.6 | 184 | 66.3 | -23 |

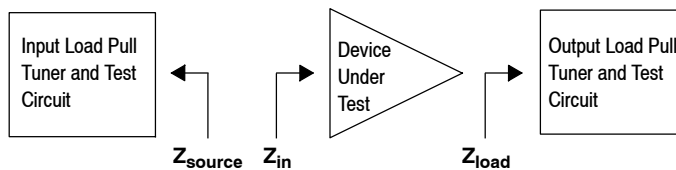
(1) Load impedance for optimum P1dB efficiency.

(2) Load impedance for optimum P3dB efficiency.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



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Table 9. Peaking Side Load Pull Performance — Maximum Power Tuning

$V_{DD} = 30$ Vdc, $V_{GSB} = 1.8$ Vdc, Pulsed CW, 10 μ sec(on), 10% Duty Cycle

| f (MHz) | Z_{source} (Ω) | Z_{in} (Ω) | Max Output Power | | | | | |
|---------|---------------------------|-----------------------|-------------------------------|-----------|-------|-----|--------------|--------------------|
| | | | P1dB | | | | | |
| | | | $Z_{load}^{(1)}$ (Ω) | Gain (dB) | (dBm) | (W) | η_D (%) | AM/PM ($^\circ$) |
| 2110 | 2.11 – j7.12 | 1.48 + j6.12 | 3.76 – j4.75 | 17.7 | 56.1 | 405 | 54.5 | –15 |
| 2140 | 2.61 – j7.79 | 1.78 + j6.77 | 4.05 – j4.63 | 18.1 | 56.0 | 399 | 54.4 | –15 |
| 2170 | 3.53 – j8.88 | 2.25 + j7.54 | 4.56 – j4.43 | 18.2 | 56.0 | 395 | 54.3 | –16 |
| 2200 | 4.62 – j10.2 | 2.97 + j8.37 | 4.94 – j4.19 | 18.3 | 55.9 | 388 | 53.6 | –17 |

| f (MHz) | Z_{source} (Ω) | Z_{in} (Ω) | Max Output Power | | | | | |
|---------|---------------------------|-----------------------|-------------------------------|-----------|-------|-----|--------------|--------------------|
| | | | P3dB | | | | | |
| | | | $Z_{load}^{(2)}$ (Ω) | Gain (dB) | (dBm) | (W) | η_D (%) | AM/PM ($^\circ$) |
| 2110 | 2.11 – j7.12 | 1.48 + j6.40 | 4.35 – j5.05 | 15.6 | 56.6 | 460 | 54.9 | –20 |
| 2140 | 2.61 – j7.79 | 1.82 + j7.12 | 4.95 – j4.79 | 16.0 | 56.6 | 453 | 54.5 | –21 |
| 2170 | 3.53 – j8.88 | 2.35 + j7.96 | 5.17 – j4.46 | 16.1 | 56.5 | 449 | 54.6 | –22 |
| 2200 | 4.62 – j10.2 | 3.21 + j8.90 | 5.69 – j4.11 | 16.1 | 56.4 | 440 | 53.7 | –23 |

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 10. Peaking Side Load Pull Performance — Maximum Efficiency Tuning

$V_{DD} = 30$ Vdc, $V_{GSB} = 1.8$ Vdc, Pulsed CW, 10 μ sec(on), 10% Duty Cycle

| f (MHz) | Z_{source} (Ω) | Z_{in} (Ω) | Max Drain Efficiency | | | | | |
|---------|---------------------------|-----------------------|-------------------------------|-----------|-------|-----|--------------|--------------------|
| | | | P1dB | | | | | |
| | | | $Z_{load}^{(1)}$ (Ω) | Gain (dB) | (dBm) | (W) | η_D (%) | AM/PM ($^\circ$) |
| 2110 | 2.11 – j7.12 | 1.30 + j6.07 | 3.28 – j2.25 | 19.4 | 55.1 | 323 | 61.4 | –21 |
| 2140 | 2.61 – j7.79 | 1.55 + j6.69 | 2.94 – j2.24 | 19.8 | 54.9 | 312 | 61.8 | –23 |
| 2170 | 3.53 – j8.88 | 1.92 + j7.43 | 2.66 – j1.97 | 20.1 | 54.6 | 288 | 62.3 | –25 |
| 2200 | 4.62 – j10.2 | 2.55 + j8.26 | 2.72 – j2.01 | 20.1 | 54.6 | 291 | 61.8 | –26 |

| f (MHz) | Z_{source} (Ω) | Z_{in} (Ω) | Max Drain Efficiency | | | | | |
|---------|---------------------------|-----------------------|-------------------------------|-----------|-------|-----|--------------|--------------------|
| | | | P3dB | | | | | |
| | | | $Z_{load}^{(2)}$ (Ω) | Gain (dB) | (dBm) | (W) | η_D (%) | AM/PM ($^\circ$) |
| 2110 | 2.11 – j7.12 | 1.33 + j6.35 | 3.83 – j2.30 | 17.3 | 55.8 | 377 | 59.4 | –27 |
| 2140 | 2.61 – j7.79 | 1.64 + j7.05 | 3.63 – j2.16 | 17.7 | 55.7 | 372 | 59.7 | –28 |
| 2170 | 3.53 – j8.88 | 2.09 + j7.87 | 3.22 – j1.97 | 17.9 | 55.5 | 353 | 59.9 | –30 |
| 2200 | 4.62 – j10.2 | 2.85 + j8.81 | 3.24 – j1.95 | 17.9 | 55.5 | 352 | 59.7 | –31 |

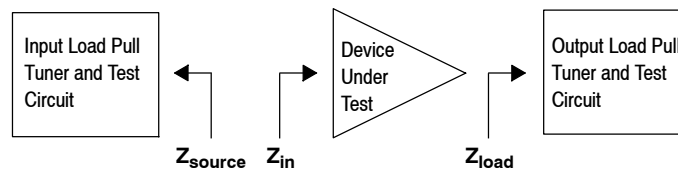
(1) Load impedance for optimum P1dB efficiency.

(2) Load impedance for optimum P3dB efficiency.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



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P1dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 2140 MHz

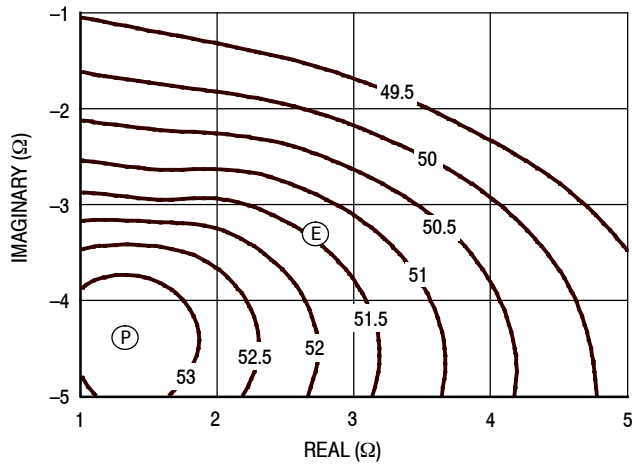


Figure 8. P1dB Load Pull Output Power Contours (dBm)

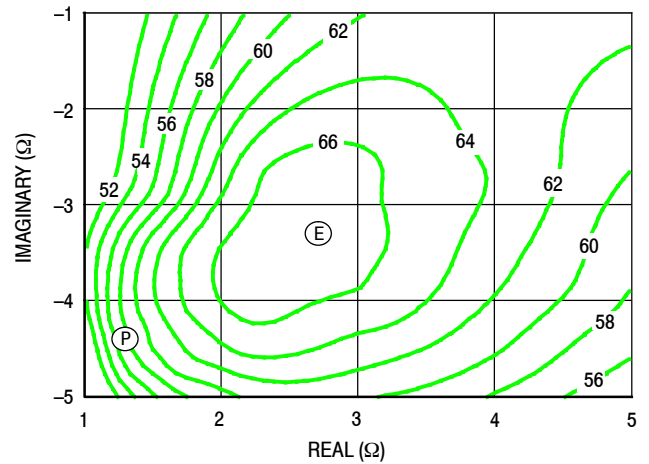


Figure 9. P1dB Load Pull Efficiency Contours (%)

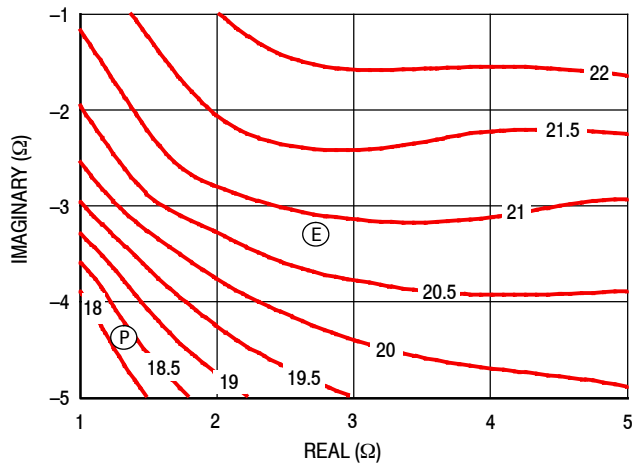


Figure 10. P1dB Load Pull Gain Contours (dB)

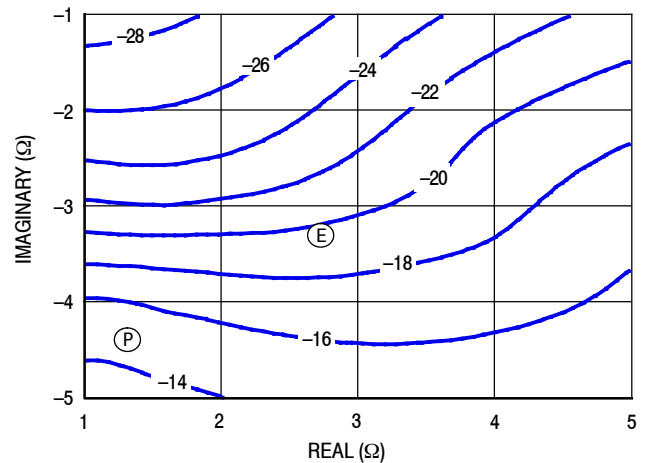


Figure 11. P1dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

P3dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 2140 MHz

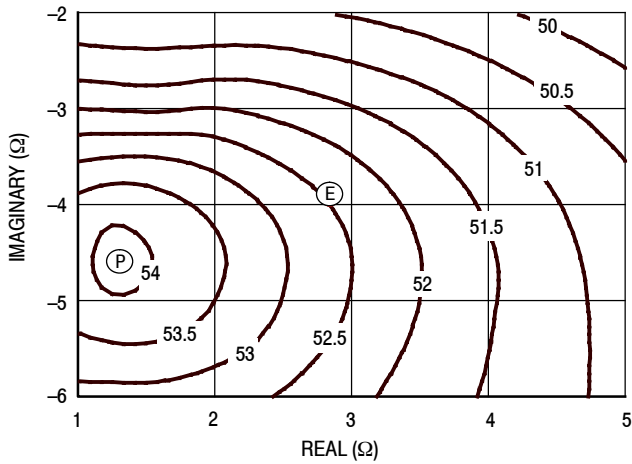


Figure 12. P3dB Load Pull Output Power Contours (dBm)

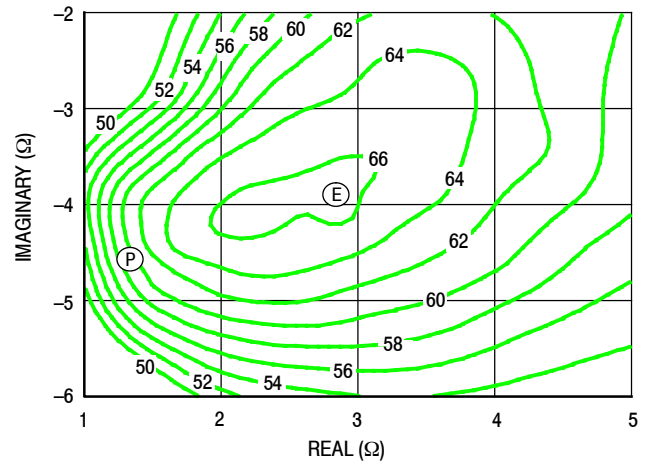


Figure 13. P3dB Load Pull Efficiency Contours (%)

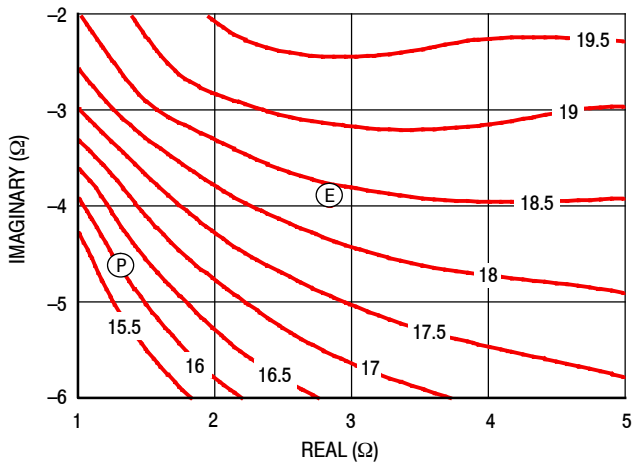


Figure 14. P3dB Load Pull Gain Contours (dB)

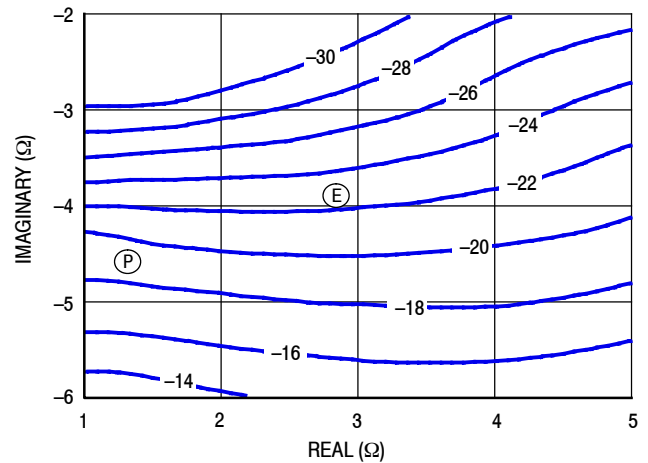


Figure 15. P3dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

P1dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 2140 MHz

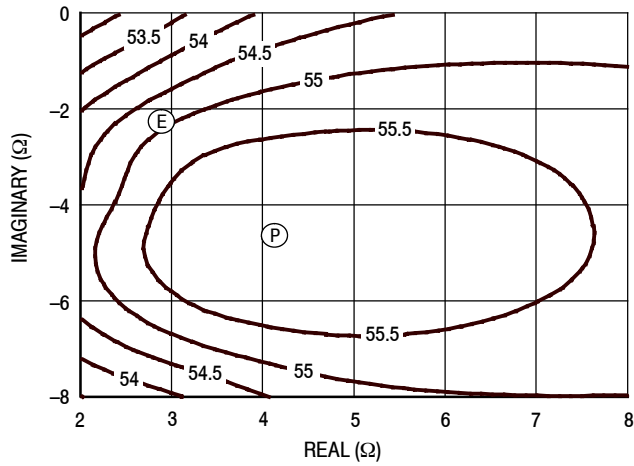


Figure 16. P1dB Load Pull Output Power Contours (dBm)

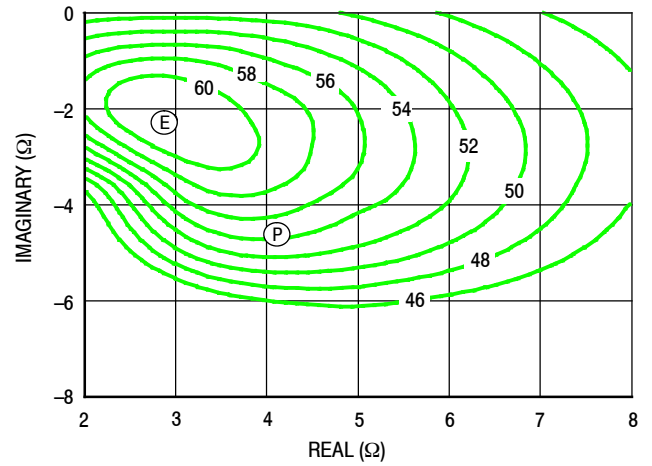


Figure 17. P1dB Load Pull Efficiency Contours (%)

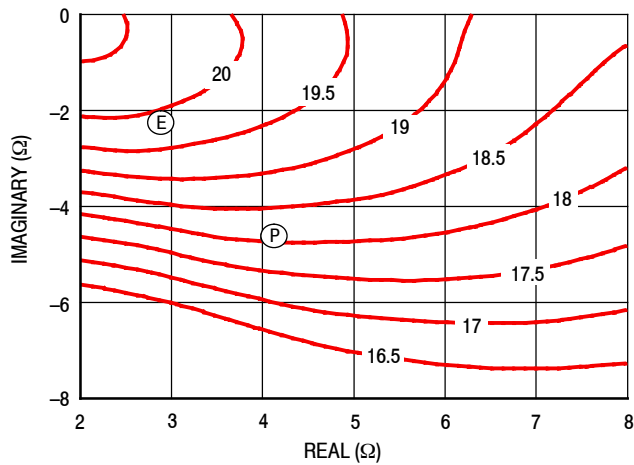


Figure 18. P1dB Load Pull Gain Contours (dB)

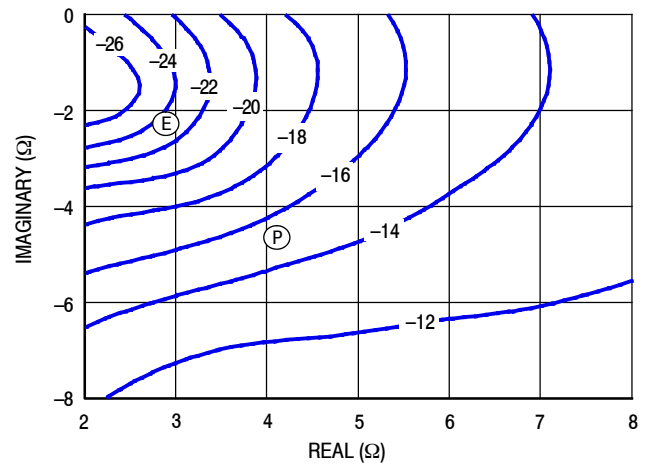


Figure 19. P1dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power

(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

P3dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 2140 MHz

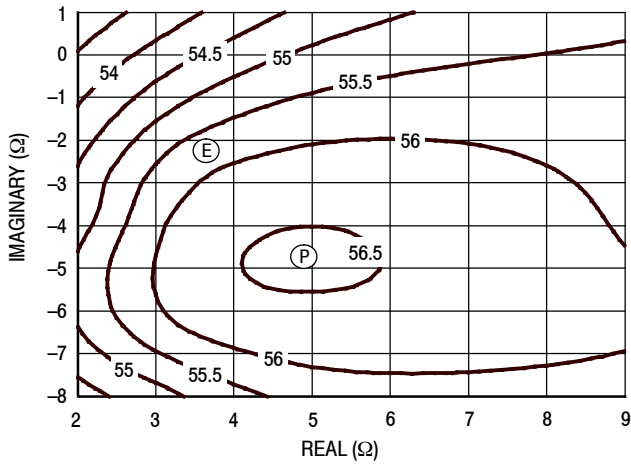


Figure 20. P3dB Load Pull Output Power Contours (dBm)

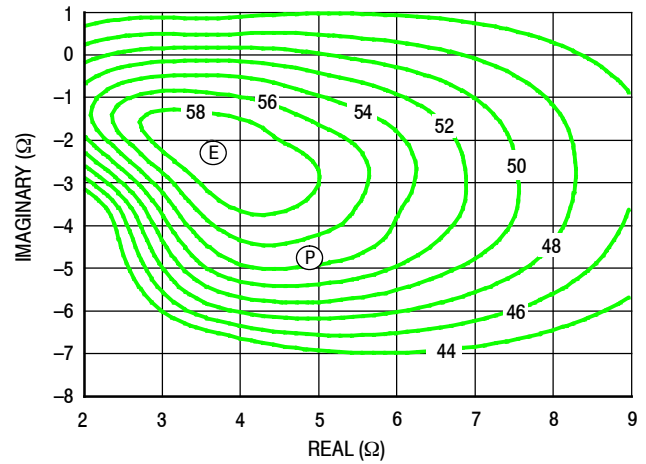


Figure 21. P3dB Load Pull Efficiency Contours (%)

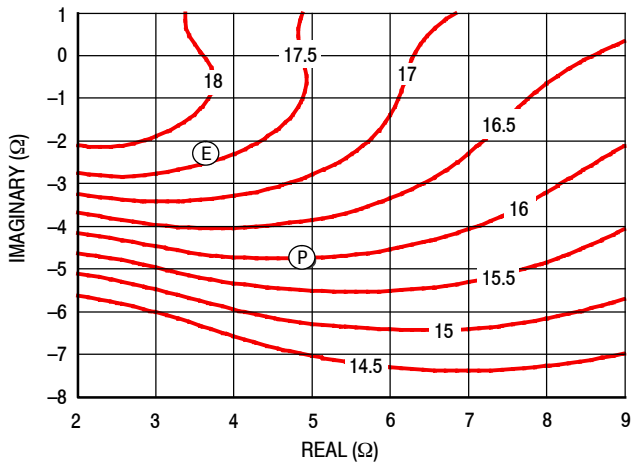


Figure 22. P3dB Load Pull Gain Contours (dB)

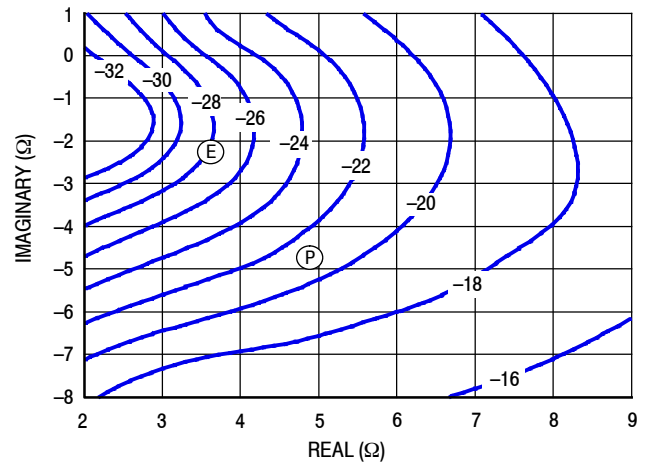
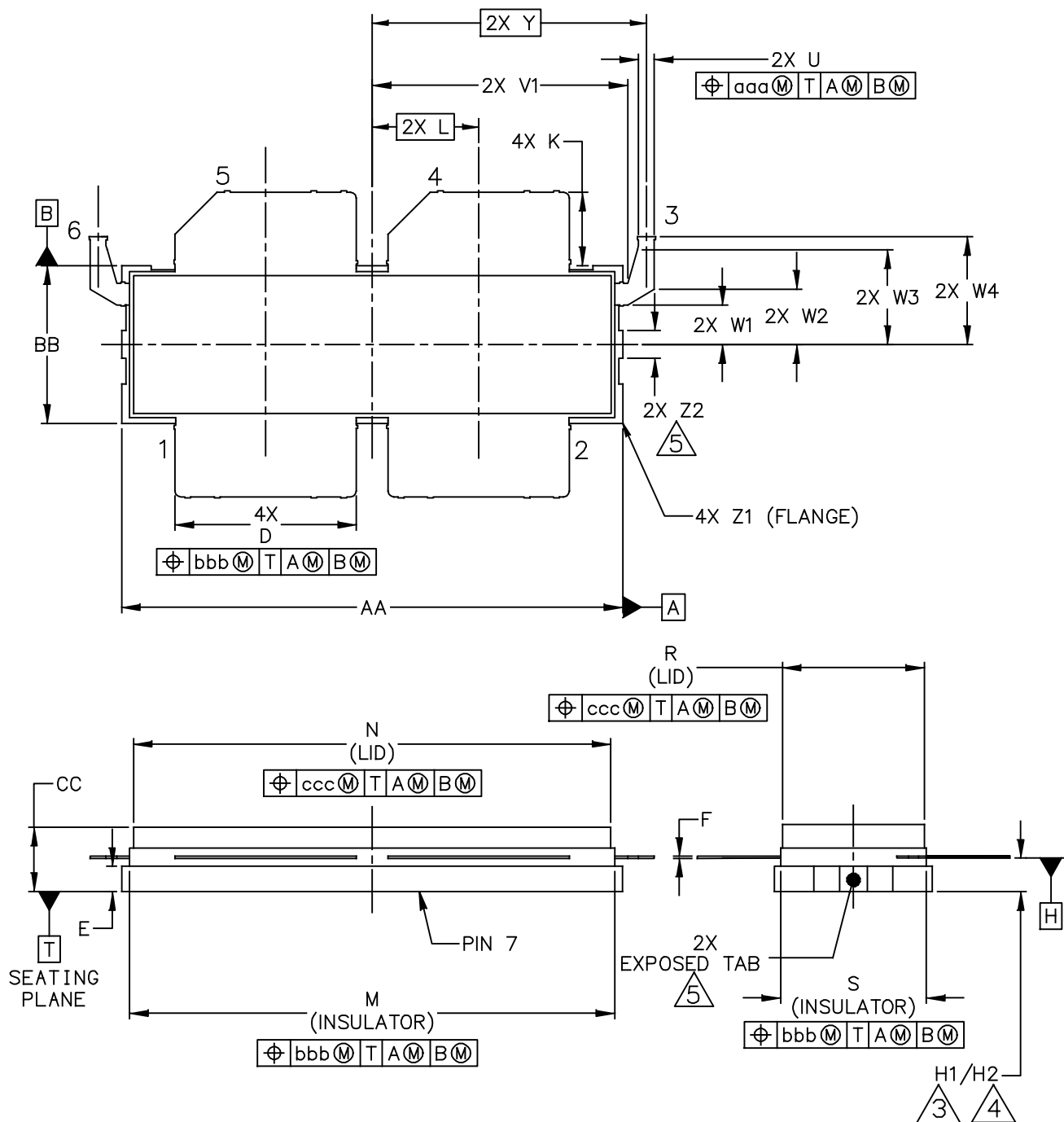


Figure 23. P3dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

PACKAGE DIMENSIONS



| | | |
|---|--------------------------|----------------------------|
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| TITLE: ACP-1230S-4L2S | DOCUMENT NO: 98ASA00974D | REV: A |
| | STANDARD: NON-JEDEC | |
| | SOT1800-4 | 21 JUN 2017 |

A3T21H450W23SR6

NOTES:

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH
3. DIMENSIONS H1 AND H2 ARE MEASURED .030 INCH (0.762 MM) AWAY FROM FLANGE PARALLEL TO DATUM B. H1 APPLIES TO PINS 1, 2, 4 & 5. H2 APPLIES TO PINS 3 & 6.
4. TOLERANCE OF DIMENSION H2 IS TENTATIVE.
5. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.
6. DATUM H IS LOCATED AT THE BOTTOM OF THE LEAD FRAME AND IS COINCIDENT WITH THE LEAD WHERE THE LEADS EXIT THE PLASTIC BODY.
7. DIMENSIONS M AND S DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .012 INCH (0.30 MM) PER SIDE. DIMENSIONS M AND S DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
8. DIMENSIONS D, U AND K DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .010 INCH (0.25 MM) TOTAL IN EXCESS OF THE D, U AND K DIMENSION AT MAXIMUM MATERIAL CONDITION.
9. DATUM A AND B TO BE DETERMINED AT DATUM T.

| DIM | INCHES | | MILLIMETERS | | DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX | | MIN | MAX | MIN | MAX |
| AA | 1.265 | 1.275 | 32.13 | 32.39 | S | .365 | .375 | 9.27 | 9.53 |
| BB | .395 | .405 | 10.03 | 10.29 | U | .035 | .045 | 0.89 | 1.14 |
| CC | .160 | .190 | 4.06 | 4.83 | V1 | .640 | .655 | 16.26 | 16.64 |
| D | .455 | .465 | 11.56 | 11.81 | W1 | .105 | .115 | 2.67 | 2.92 |
| E | .062 | .069 | 1.57 | 1.75 | W2 | .135 | .145 | 3.43 | 3.68 |
| F | .004 | .007 | 0.10 | 0.18 | W3 | .245 | .255 | 6.22 | 6.48 |
| H1 | .082 | .090 | 2.08 | 2.29 | W4 | .265 | .281 | 6.73 | 7.14 |
| H2 | .078 | .094 | 1.98 | 2.39 | Y | 0.695 BSC | | 17.65 BSC | |
| K | .175 | .195 | 4.45 | 4.95 | Z1 | R.000 | R.040 | R0.00 | R1.02 |
| L | 0.270 BSC | | 6.86 BSC | | Z2 | .060 | .100 | 1.52 | 2.54 |
| M | 1.219 | 1.241 | 30.96 | 31.52 | aaa | .015 | | 0.38 | |
| N | 1.218 | 1.242 | 30.94 | 31.55 | bbb | .010 | | 0.25 | |
| R | .365 | .375 | 9.27 | 9.53 | ccc | .020 | | 0.51 | |

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MECHANICAL OUTLINE

PRINT VERSION NOT TO SCALE

TITLE:

ACP-1230S-4L2S

DOCUMENT NO: 98ASA00974D

REV: A

STANDARD: NON-JEDEC

SOT1800-4

21 JUN 2017

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1908: Solder Reflow Attach Method for High Power RF Devices in Air Cavity Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- .s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to <http://www.nxp.com/RF>
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

| Revision | Date | Description |
|----------|-----------|---|
| 0 | July 2017 | • Initial release of data sheet |
| 1 | Aug. 2017 | • Typical Characteristic 2110–2200 MHz performance graphs: added Figs. 3–7, pp. 5–6 |

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