Title	***Reference Design Report for a 20 W Standby Power Supply Using TinySwitch™-4 TNY290PG***
Specification	90 VAC – 295 VAC (110 VDC – 420 VDC) Input; 5 V, 4 A Output
Application	General PC Standby
Author	Applications Engineering Department
Document Number	RDR-295
Date	September 25, 2012
Revision	1.5

Summary and Features

- EcoSmart™ – Meets all existing and proposed harmonized energy efficiency standards including: CECP (China), CEC, EPA, AGO, European Commission
- No-load consumption <40 mW at 230 VAC
- >81% active-mode efficiency (exceeds standards requirement of 76%)
- BP/M capacitor value selects MOSFET current limit for greater design flexibility
- Output overvoltage protection (OVP) using primary bias winding sensed shutdown feature
- Precision OVP circuit guarantees precise selection of over voltage detection threshold
- Tightly toleranced I^2f parameter (–10%, +12%) reduces system cost:
  - Increases MOSFET and magnetics power delivery
  - Reduces overload power, which lowers output diode and capacitor costs
- Integrated TinySwitch-4 Safety/Reliability features:
  - Accurate (±5%), auto-recovering, hysteretic thermal shutdown function maintains safe PCB temperatures under all conditions
  - Auto-restart protects against output short circuit and open loop fault conditions
  - >3.2 mm creepage on package enables reliable operation in high humidity and high pollution environments
- Meets EN550022 and CISPR-22 Class B conducted EMI

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This engineering report describes a universal input 5 V, 4 A power supply designed around a TNY290PG device from the TinySwitch-4 family of ICs. Although designed as an auxiliary or bias supply for a personal computer (PC) power supply, this design can also be used as a general-purpose evaluation platform for TinySwitch-4 devices.

Typically, PC power supplies have a power factor corrected (PFC) input stage. However, since the bias supply must operate before the PFC stage is active, this supply has been designed for universal input operation.

Input rectification and input storage capacitance have been included, for evaluation purposes. This stage and the EMI filter components would normally be part of the main PC supply, in an actual application.

This report contains the power supply specification, the circuit diagram, a complete bill of materials (BOM), the PIXls transformer spreadsheet design results, complete transformer documentation, the printed circuit board (PCB) layout and relevant performance data.

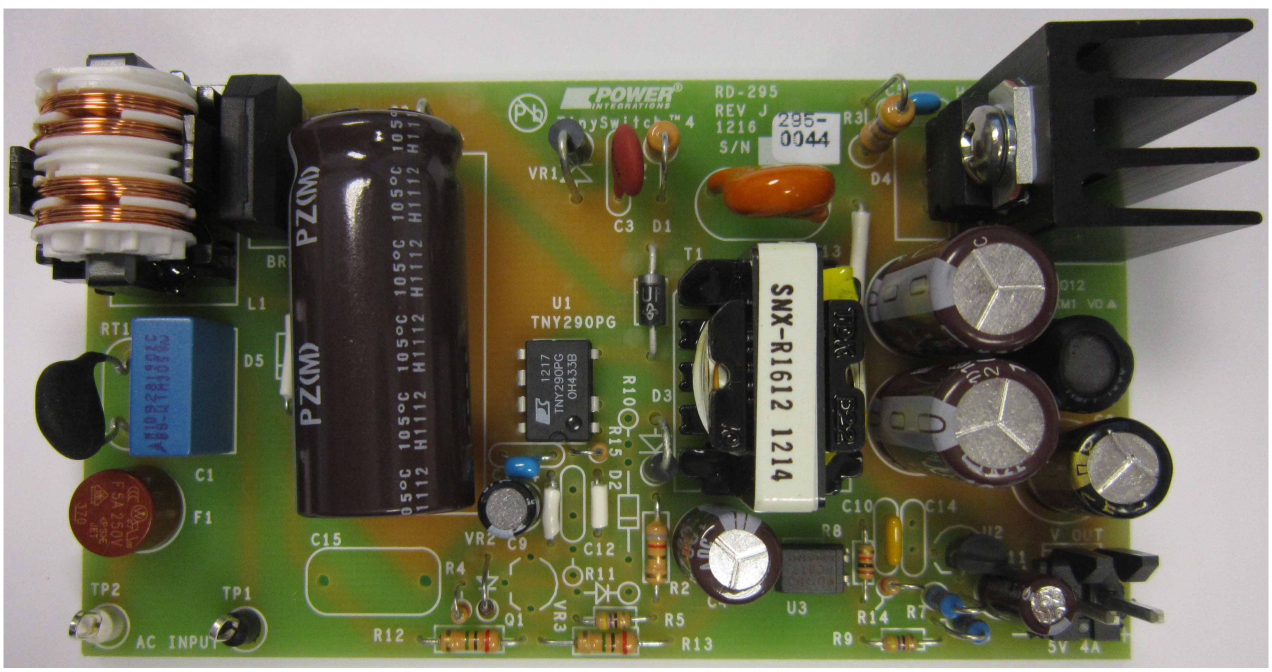

Figure 1 – Populated Circuit Board Photograph**.**

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		295	VAC	Equivalent to 100 – 420 VDC
Frequency	f_{LINE}	47	50/60	64	Hz	2 Wire – no P.E.
No-load Input Power (230 VAC)				0.035	W	AC sense configuration
Output						
Output Voltage	V_{OUT}	4.75	5	5.25	V	± 5%
Output Ripple Voltage	V_{RIPPLE}		50		mV	20 MHz bandwidth
Output Current	I_{OUT}			4	A	
Total Output Power						
Continuous Output Power	P_{OUT}			20	W	
Efficiency						
Full Load	η	80			%	Measured at P_{OUT} 25 °C V_{IN} > 90 VAC and no thermistor at input
Average efficiency at 20, 50 and 100 % of P_{OUT}	$\eta_{average}$	80			%	
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Safety		Designed to meet IEC950, UL1950 Class				
Surge		1 2			kV, D.M. kV, C.M.	1.2/50 µs surge, IEC 1000-4-5, Series Impedance: Differential Mode: 2 Ω Common Mode: 12 Ω
Ambient Temperature	T_{AMB}	0		50	°C	Free convection, sea level

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3 Schematic

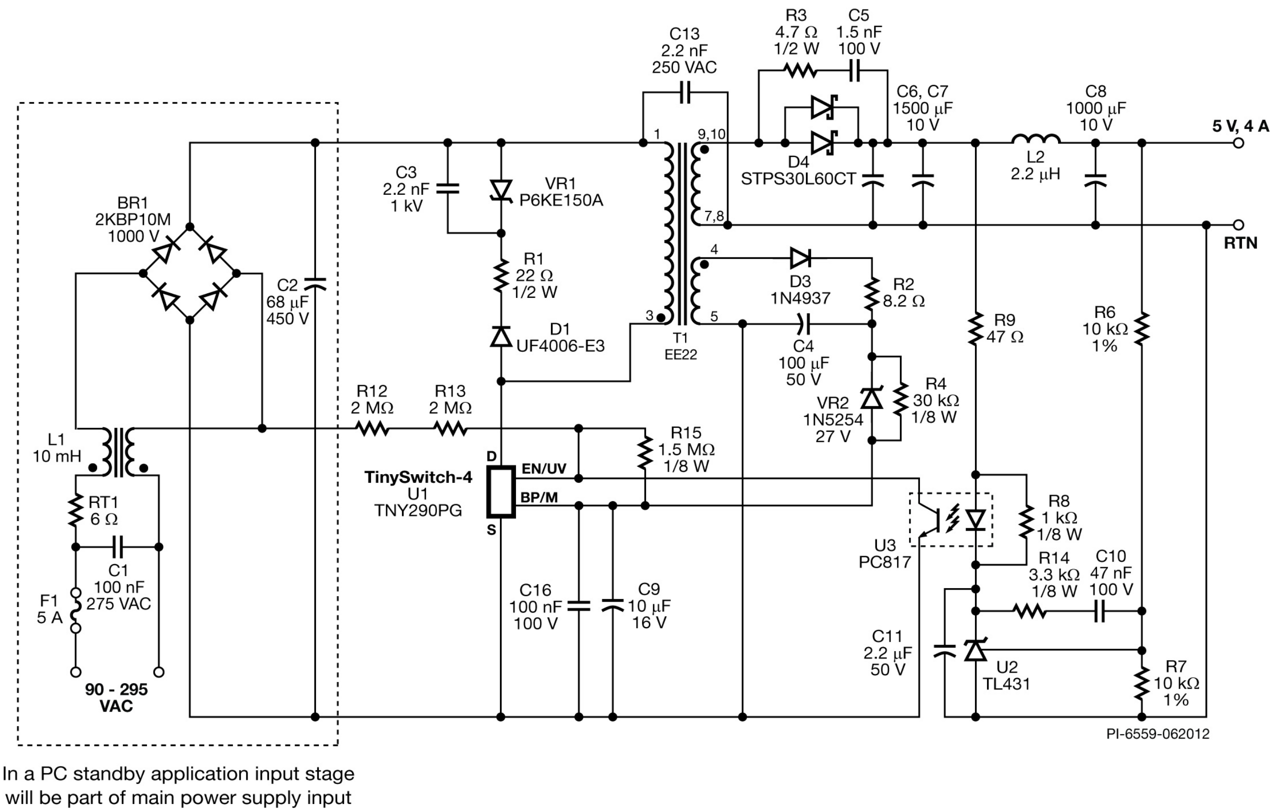
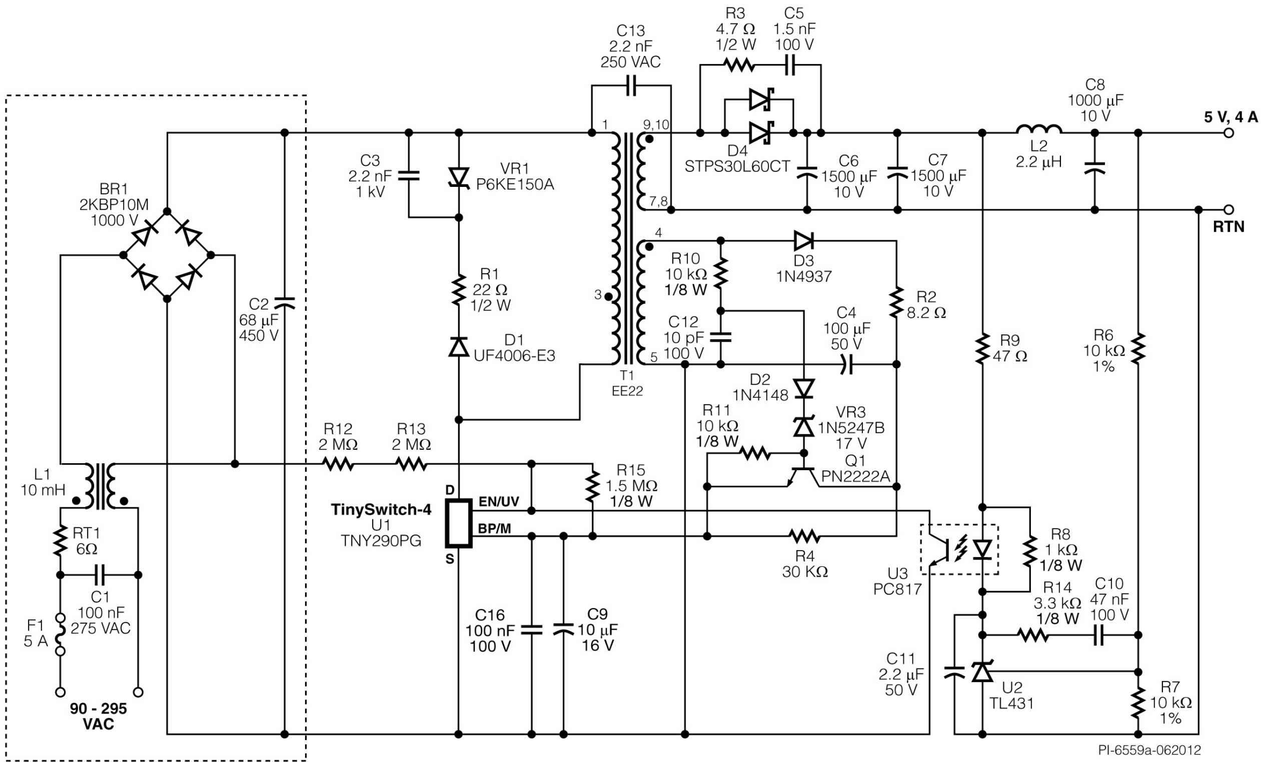


Figure 2 – Schematic (Configuration – 1: AC Sense with Simple OVP Circuit).



In a PC standby application input stage will be part of main power supply input

Figure 3 – Schematic (Configuration – 2: AC Sense with Precision OVP Detection Circuit).

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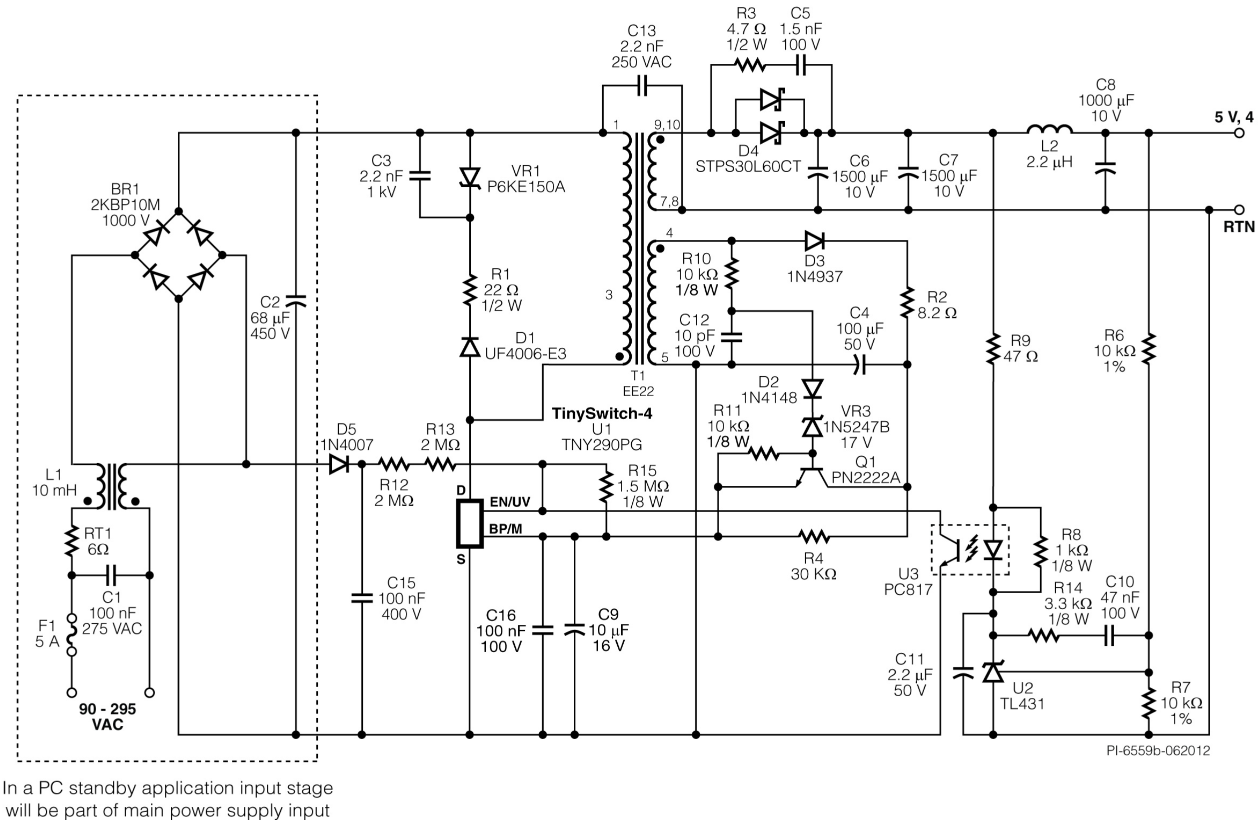

Figure 4 – Schematic (Configuration – 3: Fast AC Reset with Latching Precision OVP Detection Circuit).

4 Circuit Description

This converter is configured as a flyback. The output provides 4 A at 5 V. The converter will operate over an input voltage range of 90 VAC to 295 VAC or 100 VDC – 420 VDC. The output is regulated using a TL431 regulator IC located on the secondary side. An optocoupler is used to isolate the feedback signal in this circuit.

4.1 Input Rectifier and Filter

This circuit is designed for standby applications and components F1, RT1, C1, L1 and BR1 are only provided for standalone testing. Fuse F1 will effectively isolate the converter from the supply source in the event of short-circuit failure. Thermistor RT1 limits the inrush current at start-up. Bridge rectifier BR1 rectifies the input supply and charges the bulk storage capacitor C2.

In order to determine the efficiency of this board when used as a PC standby power supply, it is recommended that the input thermistor be replaced with a wire jumper and capacitor C2 increased to a value equal to the PFC output capacitor used in the circuit. The efficiency measured using this method should closely resemble the performance that can be achieved in a PC power supply assuming there are no significant differences in the bridge rectifier and the EMI filter sections.

4.2 TNY290PG Primary

The TNY290PG device (U1) is an integrated circuit, which includes a power MOSFET, an oscillator, control, start-up and protection functions.

A clamp circuit (D1, VR1, R1 and C3) limits the voltage that appears on the drain of U1 each time its power MOSFET turns off. This clamp design maximizes efficiency at light load.

The output of the bias/auxiliary supply winding is rectified by diode D3 and filtered by capacitor C4. The rectified and filtered output of the bias winding can be used to power external circuitry on the primary side, such as the PFC and main converter control circuits. The bias winding is also used to supply current to the TNY290PG BYPASS/MULTIFUNCTION (BP/M) pin during steady state operation. The value of resistor R4 is selected to deliver the IC supply current to the BP/M pin, thereby inhibiting the internal high-voltage current source that normally charges the BP/M pin capacitor (C9). This results in reduced input power consumption under light load and no-load conditions.

Capacitor C16 provides high frequency decoupling of the internally generated 5.85 V IC supply voltage. Three different capacitor values could be used for C9, which would select one of three internal current limit sets. A 10 μF capacitor was used in this design, which selects the increased current limit set for a TNY290PG.

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The transistor of optocoupler U3 pulls current out of the ENABLE/UNDER-VOLTAGE (EN/UV) pin of U1. The IC keeps switching as long as the current drawn from its EN/UV pin is less than 90 μA. It stops switching whenever the current drawn from the EN/UV pin exceeds that threshold, which ranges from 90 μA to 150 μA (with the typical value being 115 μA). By enabling and disabling switching pulses, the feedback loop regulates the output voltage of the power supply.

An internal state machine sets the power MOSFET current limit to one of four levels, depending on the main output load current. This ensures that the effective switching frequency remains above the audible frequency range. The lowest current limit (used at no-load) makes the transformer flux density so low that dip-varnished transformers produce no perceptible audible noise.

4.3 Output Rectification

Schottky diode D4 provides output rectification, while capacitors C6 and C7 are the main output filter capacitors. Inductor L2 and capacitor C8 form the LC post filter to reduce the amplitude of switching ripple in the power supply output. Capacitor C8 also provides improved transient response.

4.4 Output Feedback

Resistors R6 and R7 form a voltage divider network. A portion of the output voltage is fed into the input terminal of the TL431 (U2). The TL431 varies its cathode voltage in an attempt to keep its input voltage constant (equal to 2.5 V, ±2%). As the cathode voltage changes, the current through the LED and transistor within U3 change. Whenever the EN/UV pin current exceeds its threshold, the next switching cycle is disabled. Whenever the EN/UV pin current falls below the threshold, the next switching cycle is enabled. As the load is reduced, the number of enabled switching cycles decreases, which lowers the effective switching frequency and the switching losses. This results in almost constant efficiency down to very light loads, which is ideal for meeting energy efficiency requirements. Capacitor C10 rolls off the gain of U3 with frequency, to ensure stable operation. Capacitor C11 prevents the output voltage from overshooting at start-up.

4.5 UV Lockout

Resistors R12 and R13 which are connected between input to the bridge rectifier BR1 and the EN/UV pin of U1 enable the undervoltage lockout function. When these resistors are used, start-up is inhibited until the current into the EN/UV pin exceeds 25 μA. The values of R12 and R13 sets a start-up voltage threshold that prevents output voltage glitches when the input voltage is abnormally low, such as when the AC input capacitor is discharging during shutdown. Additionally, the UVLO status is checked whenever a loss of regulation occurs, such as during an output overload or short-circuit. This effectively latches U1 off until the input voltage is removed and reapplied. With the values of R12, R13 and R15 shown in Figure 2, the UVLO threshold is approximately 100 VDC (71 VAC).

Three possible configurations can be made using the circuit board and the schematic for each of the configurations is shown in this report.

1. **Configuration 1 (AC Sense with Simple OVP Detection Circuit)**

This is the default configuration and represents the circuit assembled on the board as shipped. The board is shipped with the configuration shown in Figure.2 which senses the input voltage directly at the input of the bridge rectifier. This AC sensing technique reduces no-load power consumption and hence is preferred. When using this technique it is necessary to use the resistor R15 which ensures that sufficient current is injected into the EN/UV pin even when no current flows through the resistors R12 and R13 which is for approximately 50% of each line cycle. This ensures that the UV detection feature is enabled at all times thereby preventing any hiccup during a slow brown-in or during a line dropout.

The OV fault is automatically reset in each line cycle in this configuration

2. **Configuration 2 (AC Sense with Precision OVP Detection Circuit)**

Configuration 2 is shown in Figure 3. This configuration is same as Configuration 1 except that it uses a precision OVP detection circuit which is described in section 4.6 of the report

The OV fault is automatically reset in each line cycle in this configuration

3. **Configuration 3 (Fast AC Reset with Precision OVP Detection Circuit)**

Configuration 3 as shown in Figure 4 shows a way of sensing the line voltage while simultaneously providing the ability of latching the OV fault. The fault is reset in less than 3 seconds after the input supply is removed. In this configuration, resistor R15 could be eliminated unless if it is permissible to allow output voltage hiccup during a line dropout.

4.6 Overvoltage Protection (OVP)

The OVP function is provided by VR2 and the latching shutdown function built into U1. If the feedback loop became an open circuit, due to the failure of U3, for example, the main output voltage and the bias winding voltage would both rise. Once the bias voltage exceeded the sum of the voltage across VR2 and the BP/M pin voltage, current would flow into the BP/M pin. When that current exceeds the OV shutdown threshold (≈5.5 mA), the latching shutdown function is triggered and MOSFET switching is disabled. MOSFET switching is enabled in each line cycle with the AC-sense configuration used. When Configuration 3 as described above is used, switching remains disabled until capacitor C5 discharges on removal of the input supply or the BP/M pin capacitor (C9) is discharged below 4.8 V.

A precision OVP circuit is shown in Figure 3 and Figure 4. The precision OVP detection circuit has the ability to ensure that the detection threshold remains approximately the same from no-load to full load and for any line voltage within the specified range. Resistor

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R10 and capacitor C12 shown in Figure 3 form a low pass filter that removes any high frequency switching noise in the bias winding voltage waveform. The waveform across capacitor C12 is a clean rectangular waveform with its level corresponding to the voltage induced in the bias winding based on the turn's ratio between the bias winding and the main output. During a condition such as failure of the feedback circuit, the output voltage and the voltage at the output of the bias winding starts rising which results in a voltage across C12 which exceeds the sum of diode drop of diode D2, Zener voltage of VR3, base-emitter voltage of transistor Q1 and the voltage at the BP pin of U1. This causes the transistor to conduct resulting in a current flow into the BP pin that exceeds the OV shutdown threshold.

5 PCB Layout

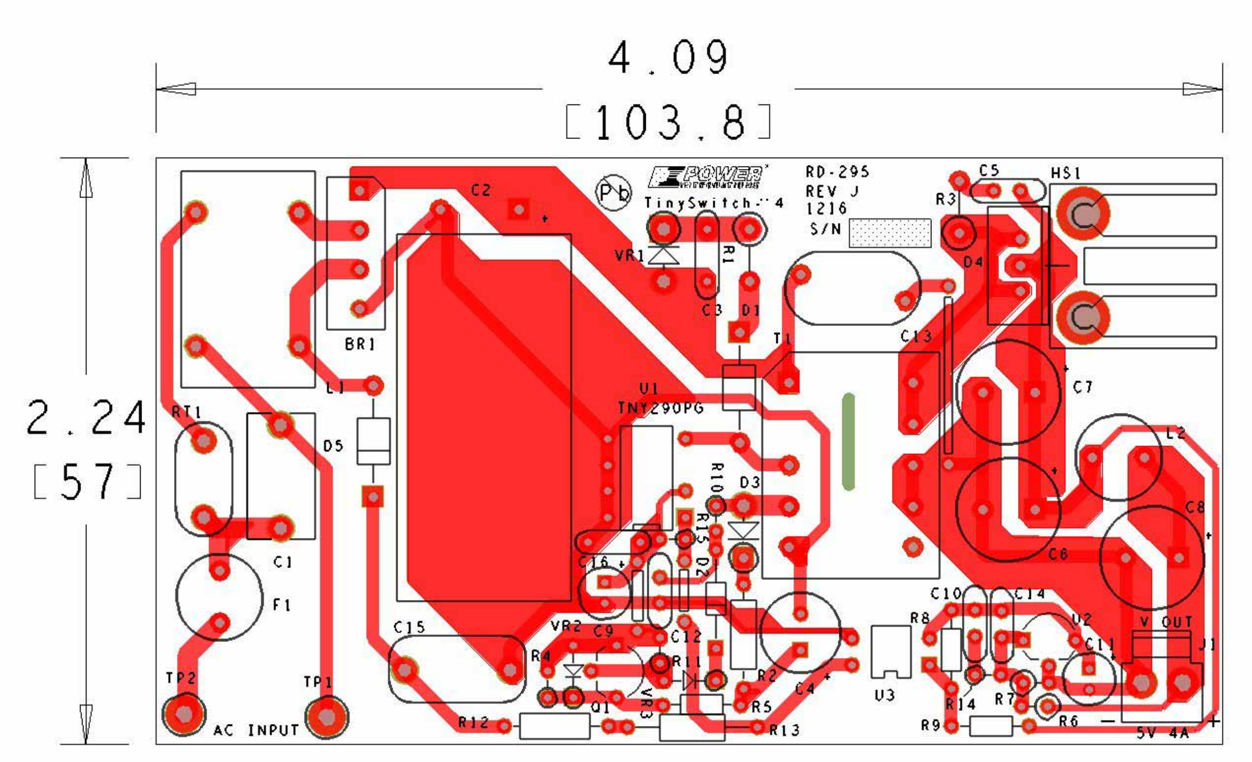

Figure 5 – Printed Circuit Layout.

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6 Bill of Materials

(Material list for Configuration-1 as shipped from the factory)

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	1000 V, 2 A, Bridge Rectifier, KBPM	2KBP10M-E4/51	Vishay
2	1	C1	100 nF, 275 VAC, Film, X2	B32921C3104M	Epcos
3	1	C2	68 μF, 450 V, Electrolytic, Low ESR, (16 x 35)	EKXG451ELL680MMN3S	United Chemi-Con
4	1	C3	2.2 nF, 1 kV, Disc Ceramic	562R5GAD22	Vishay
5	1	C4	100 μF, 50 V, Electrolytic, Gen. Purpose, (8 x 11.5)	EKZE500ELL101MHB5D	Nippon Chemi-Con
6	1	C5	1.5 nF, 100 V, Ceramic, X7R	RPER72A152K2P1A03B	MURATA
7	2	C6 C7	1500 μF, 10 V, Electrolytic, Very Low ESR, 22 mΩ, (10 x 25)	EKZE100ELL152MJ25S	Nippon Chemi-Con
8	1	C8	1000 μF, 10 V, Electrolytic, Gen. Purpose, (10 x 16)	EEU-FM1A102L	Panasonic
9	1	C9	10 μF, 16 V, Electrolytic, Gen. Purpose, (5 x 11)	UVR1C100MDD	Nichicon
10	1	C10	47 nF, 100 V, Ceramic, X7R	SR201C473KAR	AVX
11	1	C11	2.2 μF, 50 V, Electrolytic, Gen. Purpose, (5 x 11)	EKME500ELL2R2ME11D	Nippon Chemi-Con
12	1	C13	2.2 nF, Ceramic, Y1	440LD22-R	Vishay
13	1	C16	100 nF, 100 V, Ceramic, X7R	RPER71H104K2K1A03B	Murata
14	1	D1	800 V, 1 A, Ultrafast Recovery, 75 ns, DO-41	UF4006-E3	Vishay
15	1	D3	600 V, 1 A, Fast Recovery Diode, 200 ns, DO-41	1N4937RLG	On Semi
16	1	D4	60 V, 30 A, Dual Schottky, TO-220AB	STPS30L60CT	ST
17	1	F1	5 A, 250 V,Fast, TR5	37015000410	Littlefuse
18	1	HS1	Heat sink, TO220_Power Vertical Mount With Pins/6-32 Thds, Black (16.26 mm) W X (25.40 mm) H X (18 mm)	581002B02500G	Aavid/Thermalloy
19	1	J1	2 Position (1 x 2) header, 0.156 pitch, Vertical, Straight-Friction Lock Header	26-48-1025	Molex
20	2	JP1 JP2	Wire Jumper, Insulated, #24 AWG, 0.3 in	C2003A-12-02	Gen Cable
21	1	L1	10 mH, 0.6 A, Common Mode Choke	ELF-18D290G	Panasonic
22	1	L2	2.2 μH, 6.0 A	RLPI-1008	Renco Elecronics
23	1	R1	22 Ω, 5%, 1/2 W, Carbon Film	CFR-50JB-22R	Yageo
24	1	R2	8.2 Ω, 5%, 1/4 W, Carbon Film	CFR-25JB-8R2	Yageo
25	1	R3	4.7 Ω, 5%, 1/2 W, Carbon Film	CFR-50JB-4R7	Yageo
26	1	R4	30 kΩ, 5%, 1/8 W, Carbon Film	CFR-12JB-30K	Yageo
27	1	R9	47 Ω, 5%, 1/8 W, Carbon Film	CFR-12JB-47R	Yageo
28	2	R6 R7	10 kΩ, 1%, 1/4 W, Metal Film	ERO-S2PHF1002	Panasonic
29	1	R8	1 kΩ, 5%, 1/8 W, Carbon Film	CFR-12JB-1K0	Yageo
30	2	R12 R13	2.0 MΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-2M0	Yageo
31	1	R14	3.3 kΩ, 5%, 1/8 W, Carbon Film	CFR-12JB-3K3	Yageo
32	1	R15	1.5 MΩ, 5%, 1/8 W, Carbon Film	CFR-12JB-1M5	Yageo
33	1	RT1	NTC Thermistor, 6 Ohms, 2 A	MF72-006D9	Cantherm
34	1	SCREW1	SCREW MACHINE PHIL 6-32 X 1/4 SS	PMSSS 632 0025 PH	Building Fasteners
35	1	T1	Bobbin, EE22, Vertical, 10 pins Transformer	BE-22-1110CPFR SNX-R1612	TDK Santronics USA
36	1	TP1	Test Point, BLK,THRU-HOLE MOUNT	5011	Keystone
37	1	TP2	Test Point, WHT,THRU-HOLE MOUNT	5012	Keystone
38	1	U1	TinySwitch-4,DIP-8C	TNY290PG	Power Integrations
39	1	U2	2.495 V Shunt Regulator IC, 2%, 0 to 70C, TO-92	TL431CLPG	On Semi
40	1	U3	Optocoupler, 35 V, CTR 300-600%, 4-DIP	PC817X4NSZ0F	Sharp
41	1	VR1	150 V, 5 W, 5%, TVS, DO204AC (DO-15)	P6KE150A	LittleFuse
42	1	VR2	27 V, 5%, 500 mW, DO-35	1N5254B	Microsemi
43	1	WASHER1	WASHER FLAT #6 SS	620-6Z	Olander Co

Note: Diode D5 is substituted with a wire jumper (#22 AWG) for Configuration 1 and 2.

Additional components required for Configuration-2:

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	C12	10 pF, 100 V, Ceramic, COG	B37979N1100J000	Epcos
2	1	D2	75 V, 300 mA, Fast Switching, DO-35	1N4148TR	Vishay
3	1	Q1	NPN, Small Signal BJT, 40 V, 0.6 A, TO-92	PN2222AG	On Semi
4	2	R10 R11	10 kΩ, 5%, 1/8 W, Carbon Film	CFR-12JB-10K	Yageo
5	1	VR3	17 V, 5%, 500 mW, DO-35	1N5247B-T	Diodes, Inc.

Note: VR2 is not required for Configuration-2 and 3.

Additional components required for Configuration-3:

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	C15	100 nF, 400 V, Film	ECQ-E4104KF	Panasonic
2	1	D5	1000 V, 1 A, Rectifier, DO-41	1N4007-E3/54	Vishay

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7 Transformer Specification

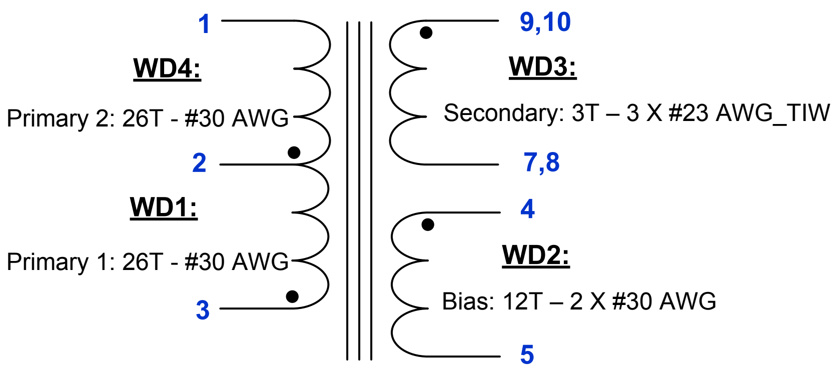

Figure 6 – Transformer Electrical Diagram.

7.1 *Electrical Specifications*

Electrical Strength	1 second, 60 Hz, from pins 1-6 to pins 6-10	3000 VAC
Primary Inductance	Pins 1-3, all other windings open, measured at 100 kHz, 0.4 V_{RMS}	661 μH ±10%
Resonant Frequency	Pins 1-3, all other windings open	2,500 kHz (Min.)
Primary Leakage Inductance	Pins 1-3, with pins 7-10 shorted, measured at 100 kHz, 0.4 V_{RMS}	14 μH (Max)

7.2 *Materials*

Item	Description
[1]	Core: TDK PC-40 or equivalent.
[2]	Bobbin: TDK-BE-22-1110CP, 10 pins, vertical, (5/5), PI#: 25-00892-00, or equivalent.
[3]	Tape, Polyester film, 3M 1350F-1 or equivalent, 8.6 mm wide.
[4]	Magnet wire: #30 AWG, solderable double coated.
[5]	Triple Insulated Wire: #23 AWG.
[6]	Varnish, Dolph BC-359 or equivalent.

7.3 Transformer Build Diagram

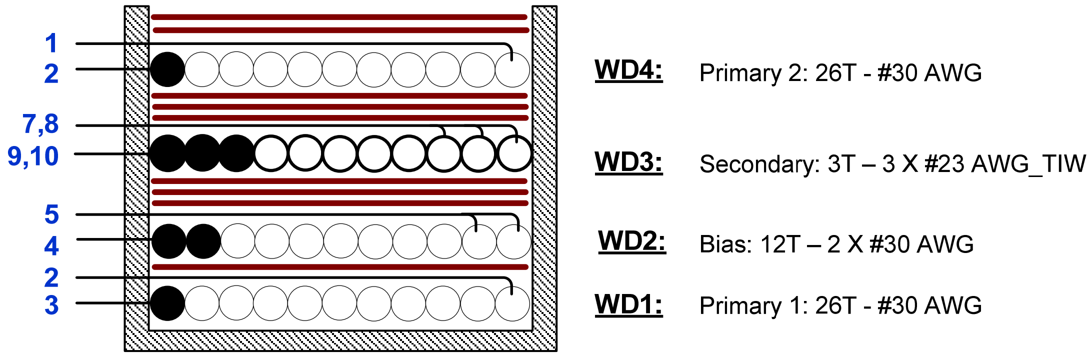

Figure 7 – Transformer Build Diagram.

7.4 Transformer Construction

Bobbin Preparation	Place the bobbin item [2] on the mandrel such that pin side on the left side. Winding direction is the clockwise direction.
WD1 (Primary 1)	Starting at pin 3, wind 26 turns of wire item [4] from left to right in one layer. At the last turn bring the wire back to the left and terminate at pin 2.
Insulation	Apply 1 layer of tape item [3].
WD2 (Bias)	Starting at pin 4, wind 12 bi-filar turns of wire item [4] from left to right in one layer. At the last turn bring the wires back to the left and terminate at pin 5.
Insulation	Apply 3 layers of tape item [3].
WD3 (Secondary)	Starting at pin 9, 10 wind 3 tri-filar turns of wire item [5] from left to right in one layer. At the last turn bring the wires back to the left and terminate at pin 7,8.
Insulation	Apply 3 layers of tape item [3].
WD4 (Primary 2)	Starting at pin 2, wind 26 turns of wire item [4] from left to right in one layer. At the last turn bring the wire back to the left and terminate at pin 1.
Insulation	Apply 2 layers of tape item [3].
Final Assembly	Grind core to get 659 μH inductance. Cut pin 2 short to 3 mm. Assemble and secure core halves with tape. Dip impregnate using varnish item [6].

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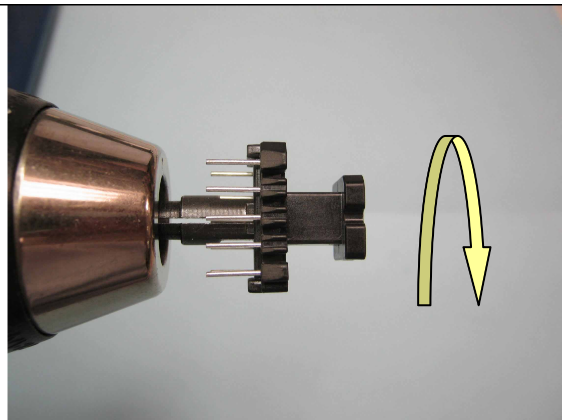
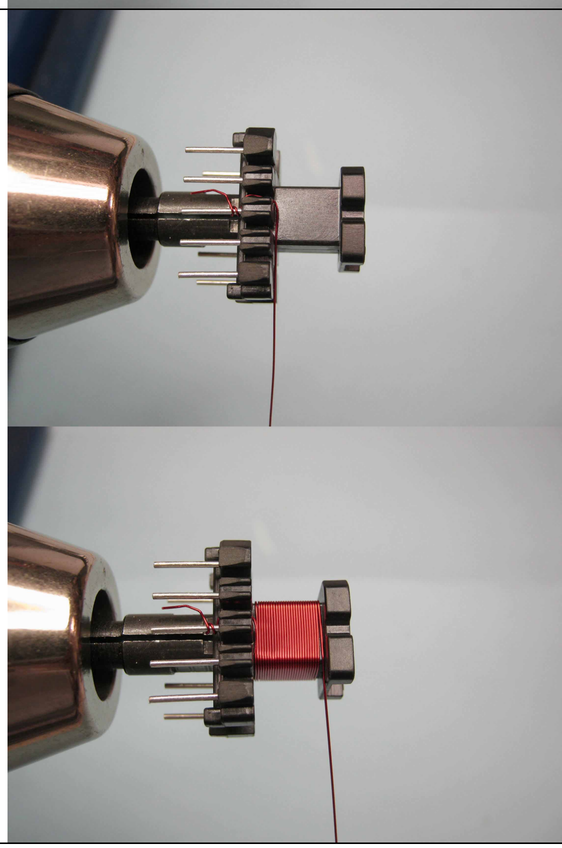
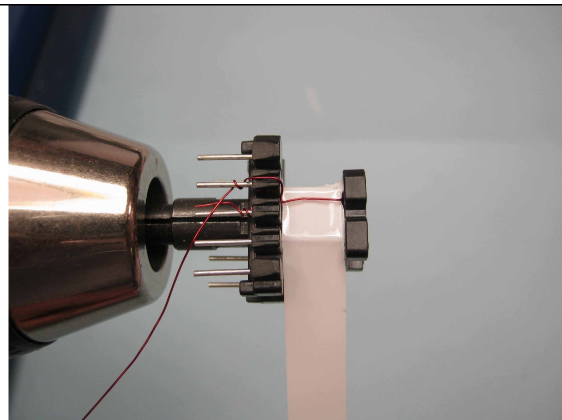
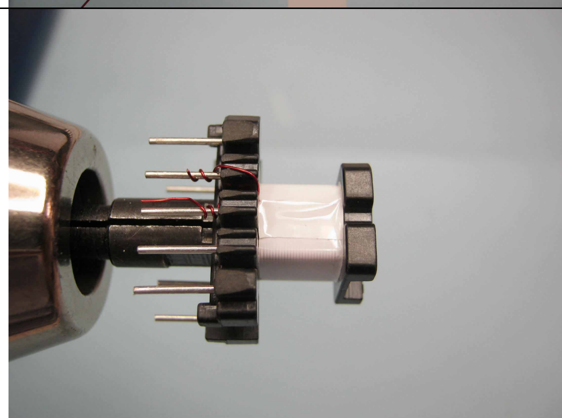
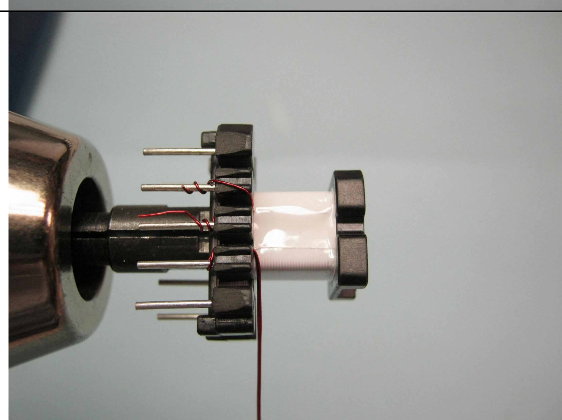
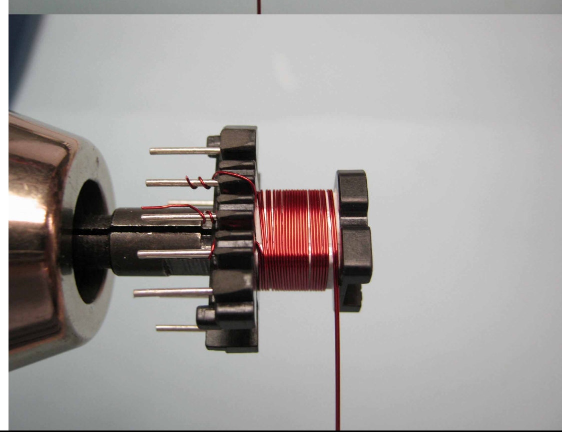
7.5 Transformer Illustrations

Bobbin Preparation		Place the bobbin item [2] on the mandrel such that pin side on the left side. Winding direction is the clockwise direction.
WD1 **(Primary 1)**		Starting at pin 3, wind 26 turns of wire item [4] from left to right in one layer. At the last turn bring the wire back to the left and terminate at pin 2.

		
Insulation		Apply one layer of tape item [3].
WD2 **(Bias)**	 	Starting at pin 4, wind 12 bi-filar turns of wire item [4] from left to right in one layer. At the last turn bring the wires back to the left and terminate at pin 5.

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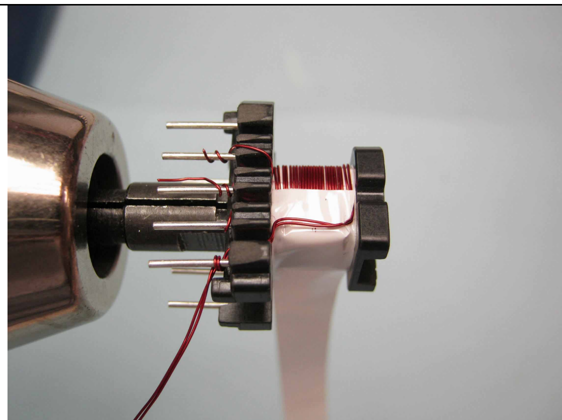
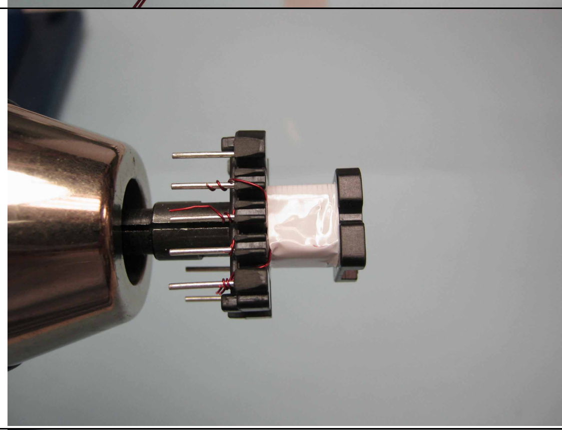
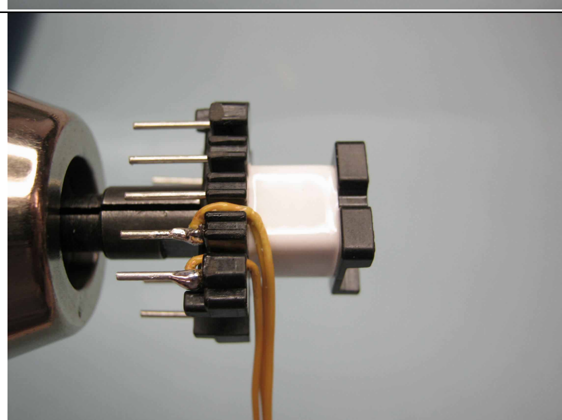
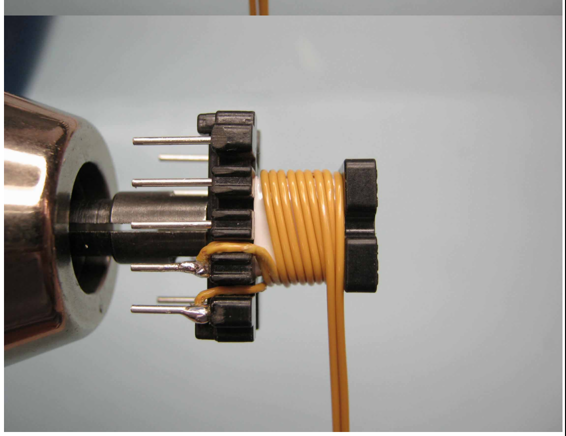
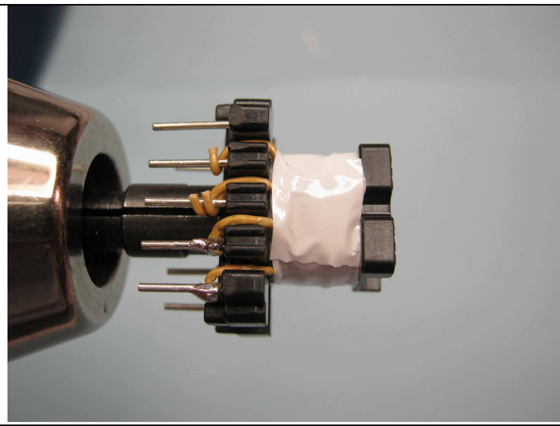
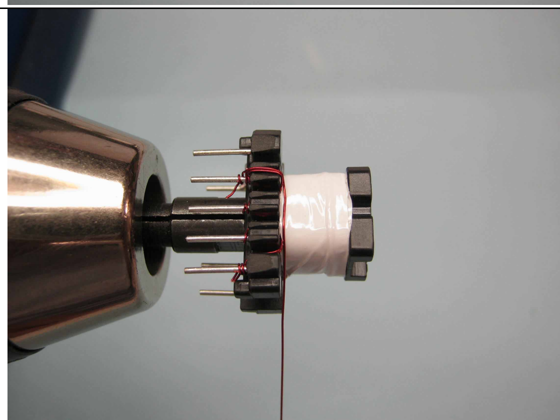
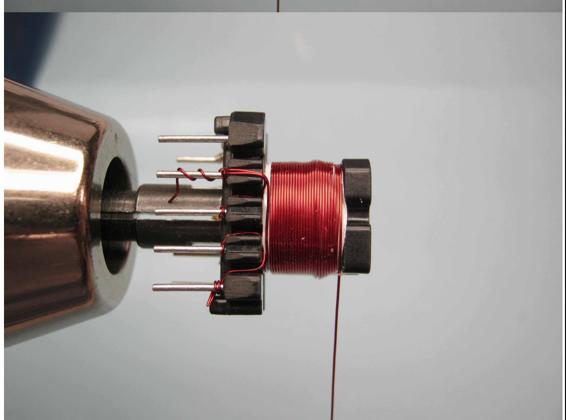
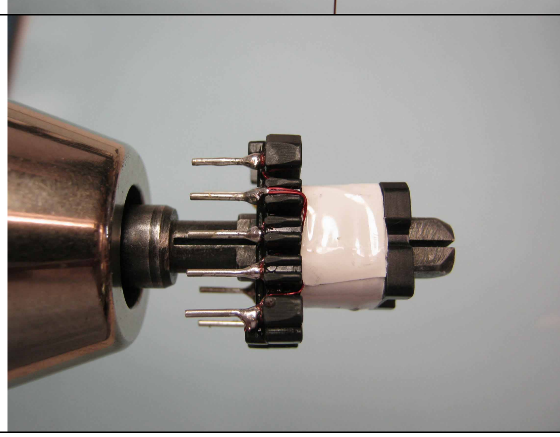
		
Insulation		Apply 3 layers of tape item [3].
WD3 (Secondary)	 	Starting at pin 9, 10 wind 3 tri-filar turns of wire item [5] from left to right in one layer. At the last turn bring the wires back to the left and terminate at pin 7 and 8.

Insulation		Apply 3 layers of tape item [3].
WD4 (Primary 2)	 	Starting at pin 2, wind 26 turns of wire item [4] from left to right in one layer. At the last turn bring the wire back to the left and terminate at pin 1.
Insulation		Apply 2 layers of tape item [3].

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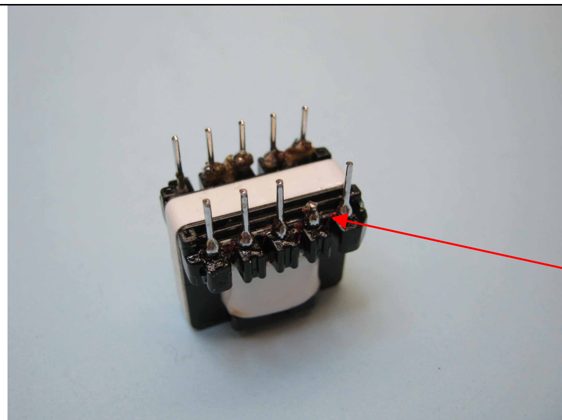
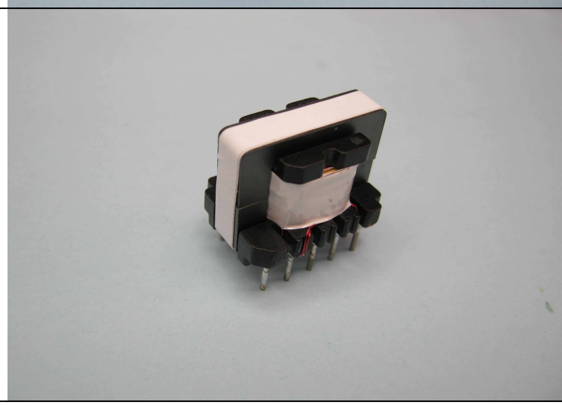
Final Assembly		Grind core to get 659 μH inductance. Assemble and secure core halves with tape. <u>Cut pin 2 short to 3 mm.</u>
		Dip impregnate using varnish item [6].

8 Transformer Design Spreadsheet

ACDC_TinySwitch-IV_012512; Rev.0.5; Copyright Power Integrations 2011	**INPUT**	**INFO**	**OUTPUT**	**UNIT**	**ACDC_TinySwitch-IV_012512_Rev0-5.xls; TinySwitch-IV Continuous/Discontinuous Flyback Transformer Design Spreadsheet**
ENTER APPLICATION VARIABLES					
VACMIN	90		90	Volts	Minimum AC Input Voltage
VACMAX	295		295	Volts	Maximum AC Input Voltage
fL	50		50	Hertz	AC Mains Frequency
VO	5.00		5.00	Volts	Output Voltage (at continuous power)
IO	4.00		4.00	Amps	Power Supply Output Current (corresponding to peak power)
Power			20	Watts	Continuous Output Power
n	0.80		0.80		Efficiency Estimate at output terminals. Under 0.7 if no better data available
Z	0.50		0.50		Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.5 if no better data available
tC	3.00		3.00	mSeconds	Bridge Rectifier Conduction Time Estimate
CIN	68.00		68	uFarads	Input Capacitance
ENTER TinySwitch-IV VARIABLES					
TinySwitch-IV	**TNY290P**		**TNY290P**		User defined TinySwitch-IV
Chosen Device		TNY290P			
Chose Configuration	**INC**		Increased Current Limit		Enter "RED" for reduced current limit (sealed adapters), "STD" for standard current limit or "INC" for increased current limit (peak or higher power applications)
ILIMITMIN			0.791	Amps	Minimum Current Limit
ILIMITTYP			0.850	Amps	Typical Current Limit
ILIMITMAX			0.943	Amps	Maximum Current Limit
fSmin			124000	Hertz	Minimum Device Switching Frequency
I^2fmin			85.833	A^2kHz	I^2f (product of current limit squared and frequency is trimmed for tighter tolerance)
VOR	95.00		95	Volts	Reflected Output Voltage (VOR < 135 V Recommended)
VDS			10	Volts	TinySwitch-IV on-state Drain to Source Voltage
VD			0.5	Volts	Output Winding Diode Forward Voltage Drop
KP			0.80		Ripple to Peak Current Ratio (KP < 6)
KP_TRANSIENT			0.36		Transient Ripple to Peak Current Ratio. Ensure KP_TRANSIENT > 0.25
ENTER BIAS WINDING VARIABLES					
VB			22.00	Volts	Bias Winding Voltage
VDB			0.70	Volts	Bias Winding Diode Forward Voltage Drop
NB			12.00		Bias Winding Number of Turns
VZOV			28.00	Volts	Over Voltage Protection zener diode voltage.
UVLO VARIABLES					
V_UV_TARGET			115.65	Volts	Target DC under-voltage threshold, above which the power supply with start
V_UV_ACTUAL			119.70	Volts	Typical DC start-up voltage based on standard value of RUV_ACTUAL
RUV_IDEAL			4.54	Mohms	Calculated value for UV Lockout resistor
RUV_ACTUAL			4.70	Mohms	Closest standard value of resistor to RUV_IDEAL
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	**EE22**		**EE22**		Enter Transformer Core

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Core		EE22		P/N:	PC40EE22-Z
Bobbin				P/N:	EE22_BOBBIN
AE			0.41	cm^2	Core Effective Cross Sectional Area
LE			3.96	cm	Core Effective Path Length
AL			1610	nH/T^2	Ungapped Core Effective Inductance
BW			8.45	mm	Bobbin Physical Winding Width
M			0	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	2.00		2		Number of Primary Layers
NS	3		3		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS					
VMIN			105	Volts	Minimum DC Input Voltage
VMAX			417	Volts	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.50		Duty Ratio at full load, minimum primary inductance and minimum input voltage
IAVG			0.26	Amps	Average Primary Current
IP			0.79	Amps	Minimum Peak Primary Current
IR			0.63	Amps	Primary Ripple Current
IRMS			0.43	Amps	Primary RMS Current
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			661	uHenries	Typical Primary Inductance. +/- 10% to ensure a minimum primary inductance of 594 uH
LP_TOLERANCE			10	%	Primary inductance tolerance
NP			52		Primary Winding Number of Turns
ALG			246	nH/T^2	Gapped Core Effective Inductance
BM			2934	Gauss	Maximum Operating Flux Density, BM<3000 is recommended
BAC			1169	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
Ur			1237		Relative Permeability of Ungapped Core
LG			0.18	mm	Gap Length (Lg > 0.1 mm)
BWE			16.9	mm	Effective Bobbin Width
OD			0.33	mm	Maximum Primary Wire Diameter including insulation
INS			0.05	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.27	mm	Bare conductor diameter
AWG			30	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			102	Cmils	Bare conductor effective area in circular mils
CMA			237	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)
TRANSFORMER SECONDARY DESIGN PARAMETERS					
Lumped parameters					
ISP			13.66	Amps	Peak Secondary Current
ISRMS			7.42	Amps	Secondary RMS Current
IRIPPLE			6.25	Amps	Output Capacitor RMS Ripple Current
CMS			1484	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			18	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
VOLTAGE STRESS PARAMETERS					
VDRAIN			637	Volts	Maximum Drain Voltage Estimate (Assumes 20% zener clamp tolerance and an additional 10% temperature tolerance)
PIVS			29	Volts	Output Rectifier Maximum Peak Inverse Voltage

1st output					
VO1			5	Volts	Main Output Voltage (if unused, defaults to single output design)
IO1			4.000	Amps	Output DC Current
PO1			20.00	Watts	Output Power
VD1			0.5	Volts	Output Diode Forward Voltage Drop
NS1			3.00		Output Winding Number of Turns
ISRMS1			7.421	Amps	Output Winding RMS Current
IRIPPLE1			6.25	Amps	Output Capacitor RMS Ripple Current
PIVS1			29	Volts	Output Rectifier Maximum Peak Inverse Voltage
Recommended Diodes			90SQ030		Recommended Diodes for this output
CMS1			1484	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1			18	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1			1.03	mm	Minimum Bare Conductor Diameter
ODS1			2.82	mm	Maximum Outside Diameter for Triple Insulated Wire
2nd output					
VO2				Volts	Output Voltage
IO2				Amps	Output DC Current
PO2			0.00	Watts	Output Power
VD2			0.7	Volts	Output Diode Forward Voltage Drop
NS2			0.38		Output Winding Number of Turns
ISRMS2			0.000	Amps	Output Winding RMS Current
IRIPPLE2			0.00	Amps	Output Capacitor RMS Ripple Current
PIVS2			3	Volts	Output Rectifier Maximum Peak Inverse Voltage
Recommended Diode					Recommended Diodes for this output
CMS2			0	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS2			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS2			N/A	mm	Minimum Bare Conductor Diameter
ODS2			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
3rd output					
VO3				Volts	Output Voltage
IO3				Amps	Output DC Current
PO3			0.00	Watts	Output Power
VD3			0.7	Volts	Output Diode Forward Voltage Drop
NS3			0.38		Output Winding Number of Turns
ISRMS3			0.000	Amps	Output Winding RMS Current
IRIPPLE3			0.00	Amps	Output Capacitor RMS Ripple Current
PIVS3			3	Volts	Output Rectifier Maximum Peak Inverse Voltage
Recommended Diode					Recommended Diodes for this output
CMS3			0	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS3			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS3			N/A	mm	Minimum Bare Conductor Diameter
ODS3			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
Total power			20	Watts	Total Output Power
Negative Output	N/A		N/A		If negative output exists enter Output number; eg: If VO2 is negative output, enter 2

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9 Performance Data

All measurements performed at room temperature, 60 Hz frequency for 90 VAC and 115 VAC; 50 Hz frequency for 230 VAC and 265 VAC.

9.1 Efficiency – 68 μF Input Capacitor C2 and Thermistor RT1 in Circuit

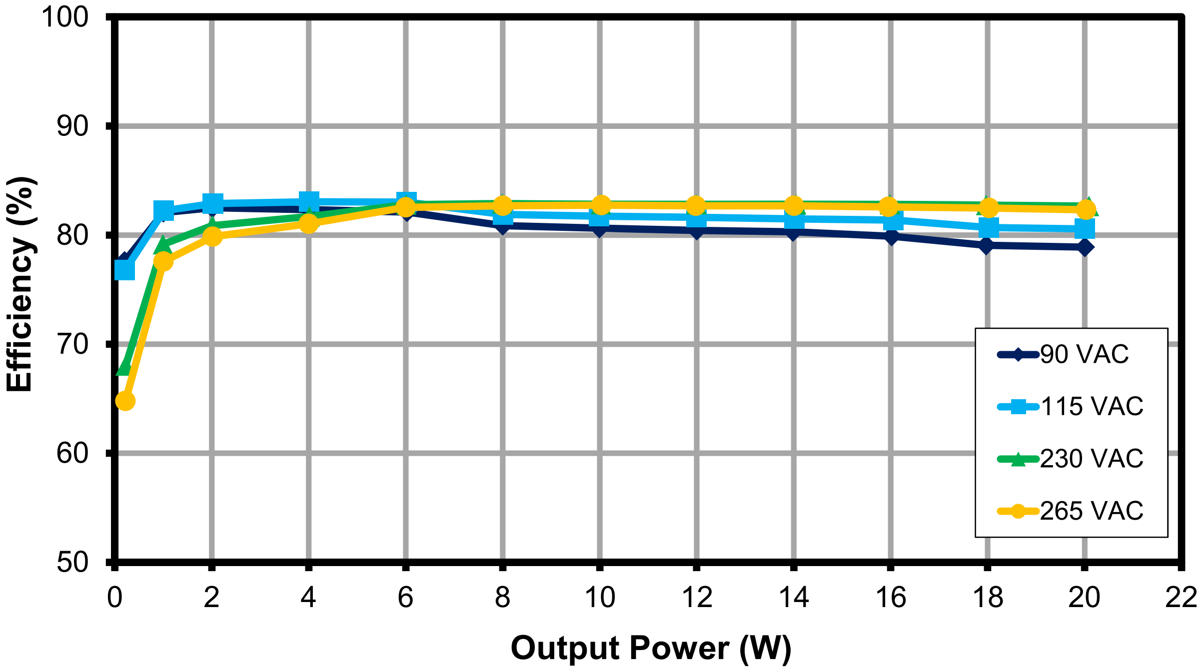

Figure 8 – Efficiency with 68 μF Input Capacitor and Thermistor In-Circuit, Room Temperature.

9.2 Efficiency – Without Thermistor RT1 in Circuit (Replaced with a Jumper)

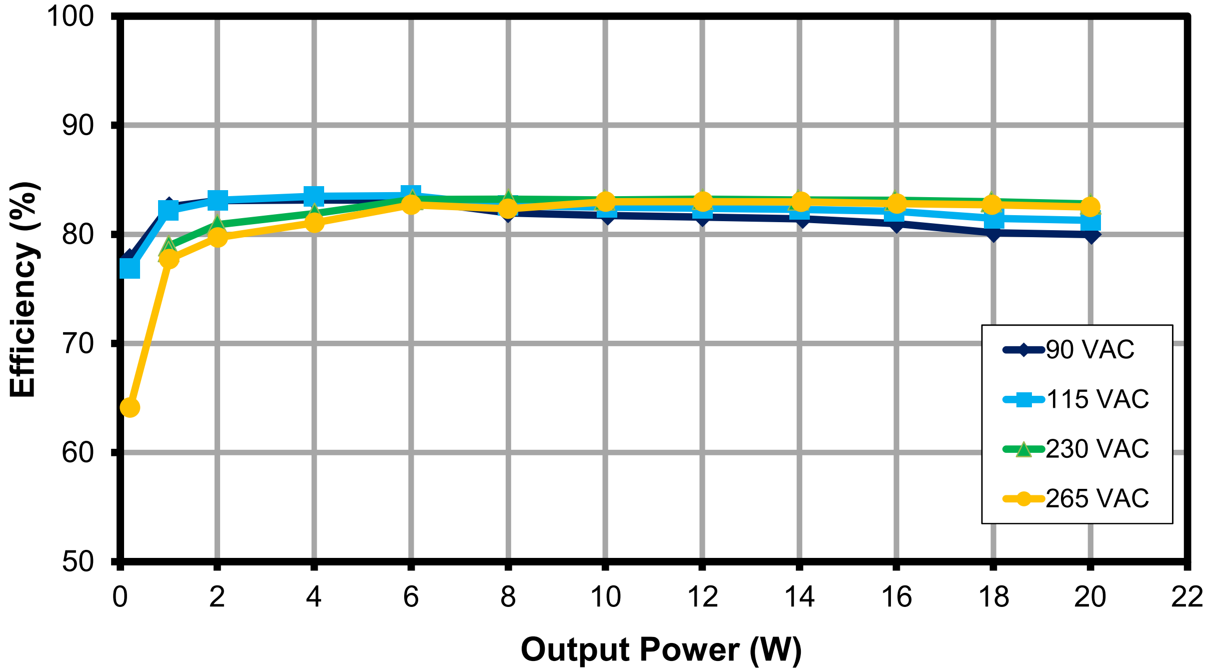

Figure 9 – Efficiency with 68 μF Input Capacitor, Room Temperature.

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9.3 Efficiency – 380 VDC Input Right at the 68 μF Input Bulk Capacitor

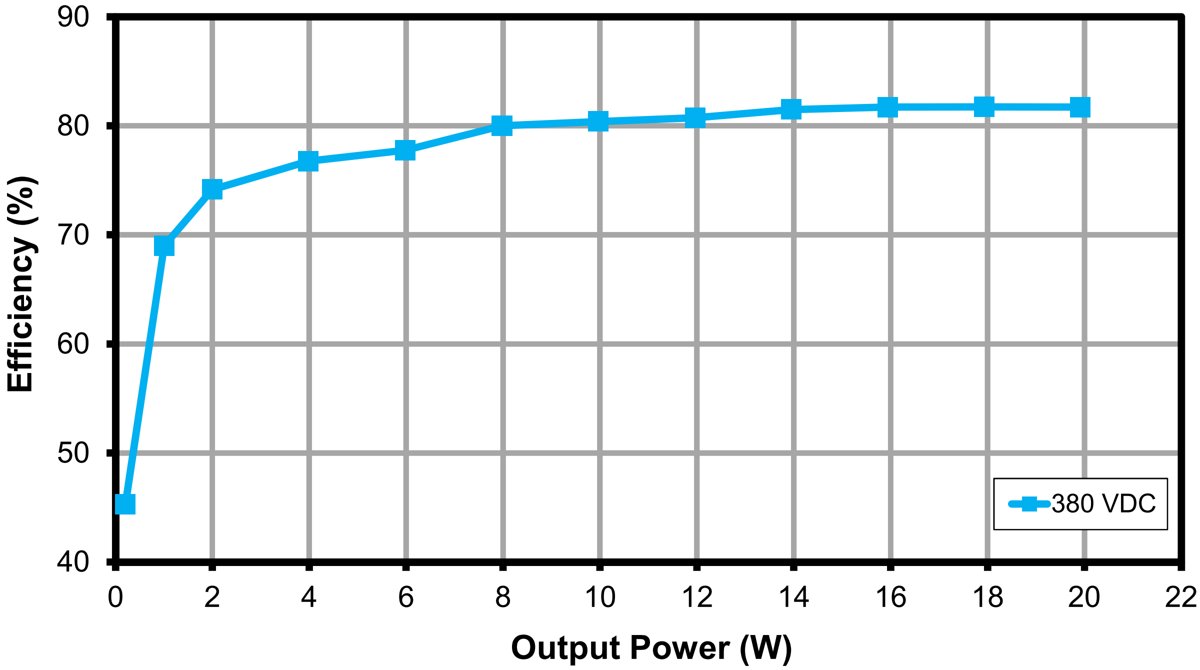

Figure 10 – Efficiency with 220 μF Input Capacitor, Room Temperature.

9.4 Maximum Output Power

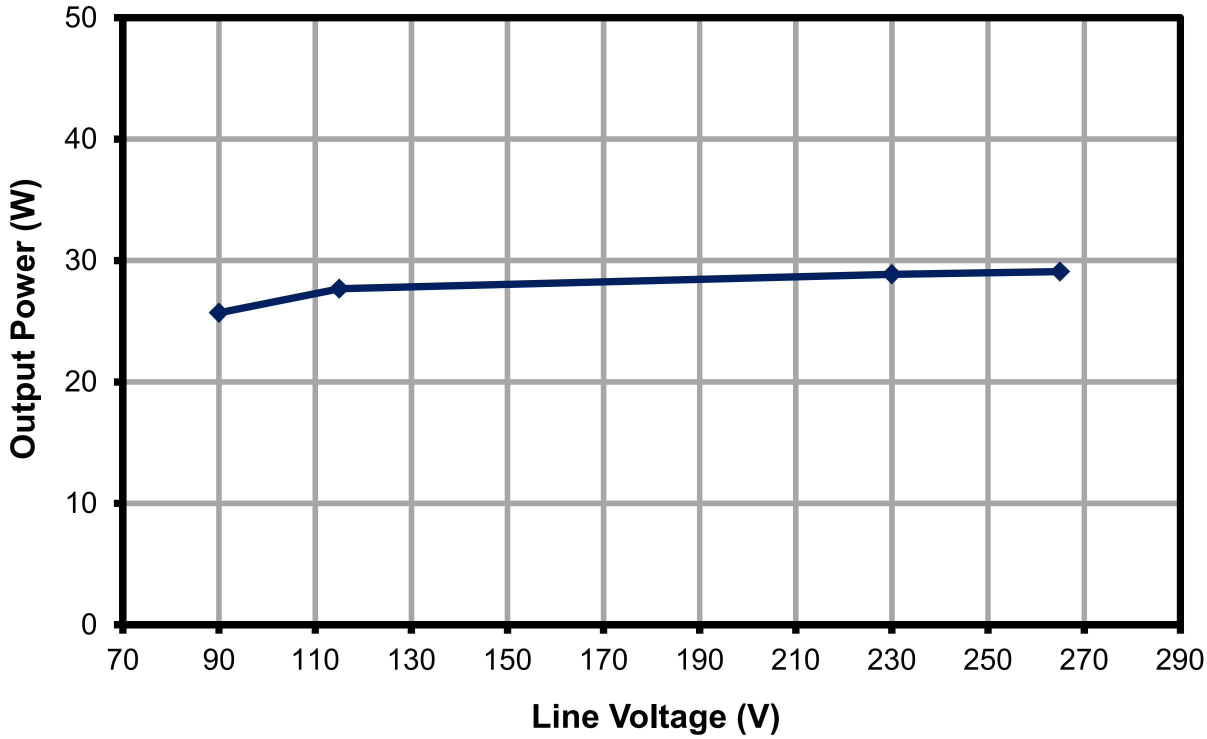

Figure 11 – Maximum Output Power.

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10 80 Plus Average Efficiency Measurement

Efficiency was measured at 325.2 VDC and 162.6 VDC, which were DC equivalent voltage for 230 VAC and 115 VAC. DC input was connected directly to the 68 μF bulk capacitor at primary side. The test results are listed in the following table.

Percentage of Full Load (%)	**Efficiency (%)**	
	162.6 VDC (115 VAC Equivalent)	**325.2 VDC (230 VAC Equivalent)**
20	81.52	78.16
50	82.76	81.29
100	82.41	82.14
Average	**82.23**	**80.53**

10.1 Input Power at No-Load

Input power at no load was tested with 2 minutes integration mode after power on about 1 hour. The 1 hour time can significantly reduce the leakage current of input capacitor and thus the no-load input power.

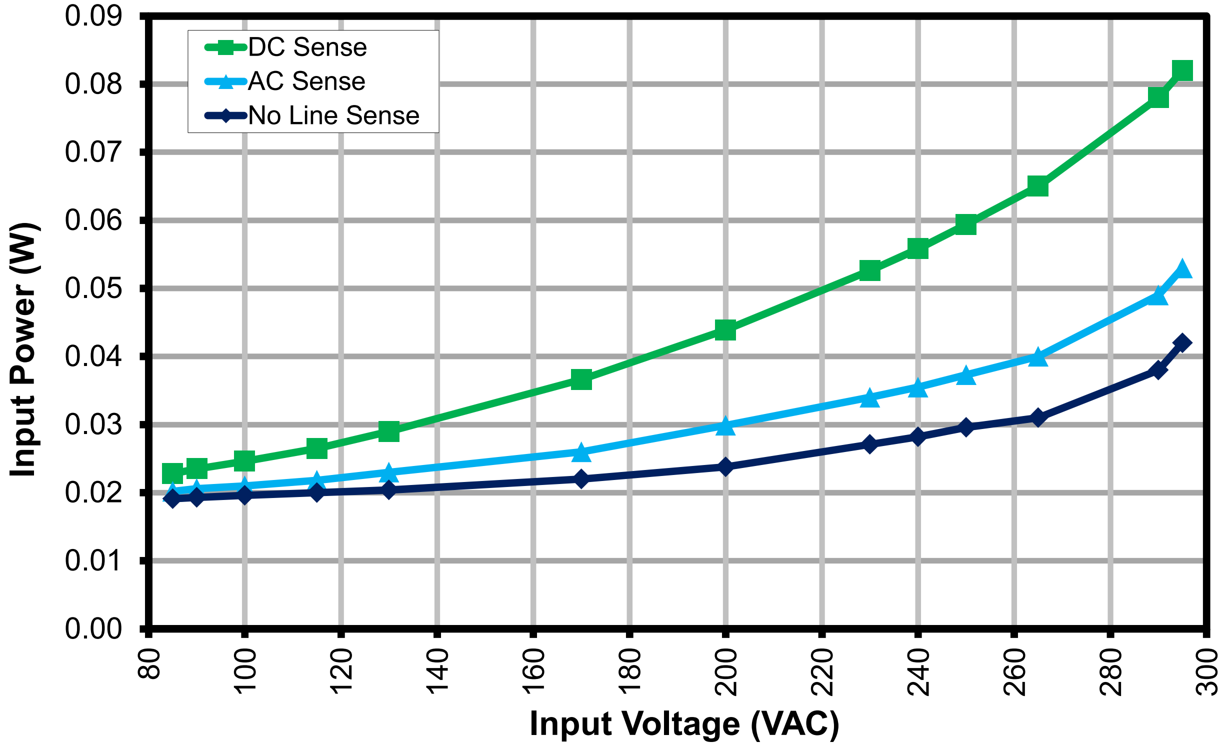

Figure 12 – Input Power at No-Load.

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10.2 Input Power for 250 mW Load

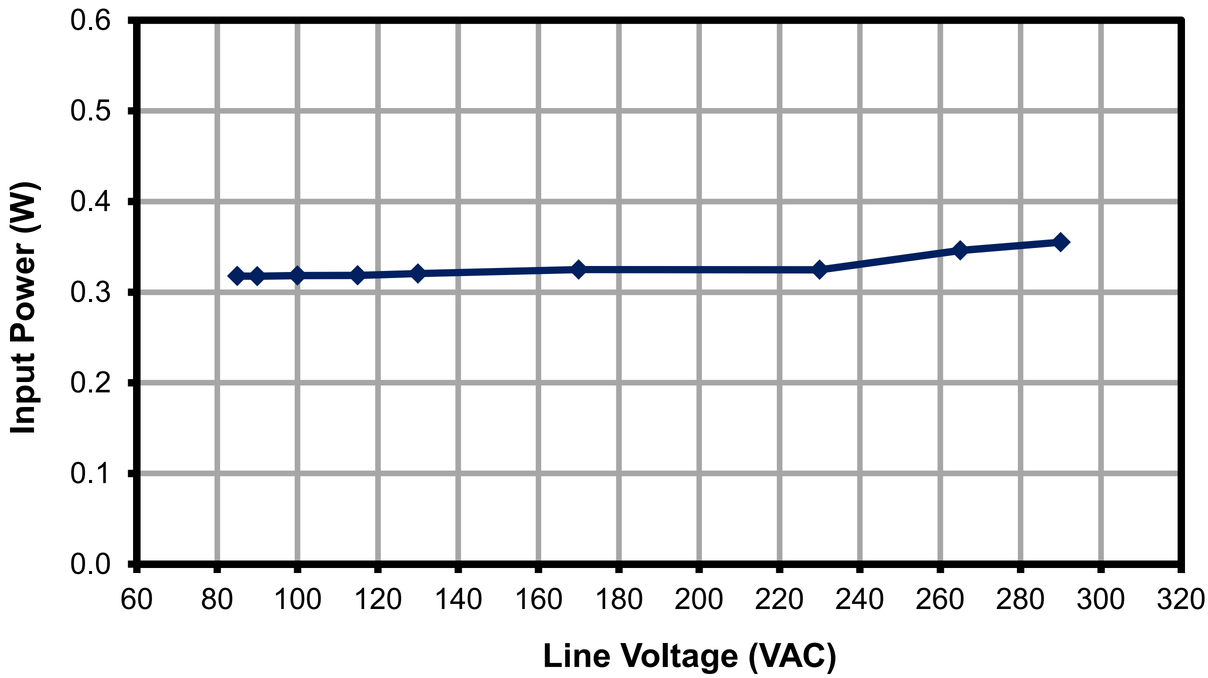

Figure 13 – Input Power at 250 mW Load, Room Temperature.

10.3 Available Standby Output Power

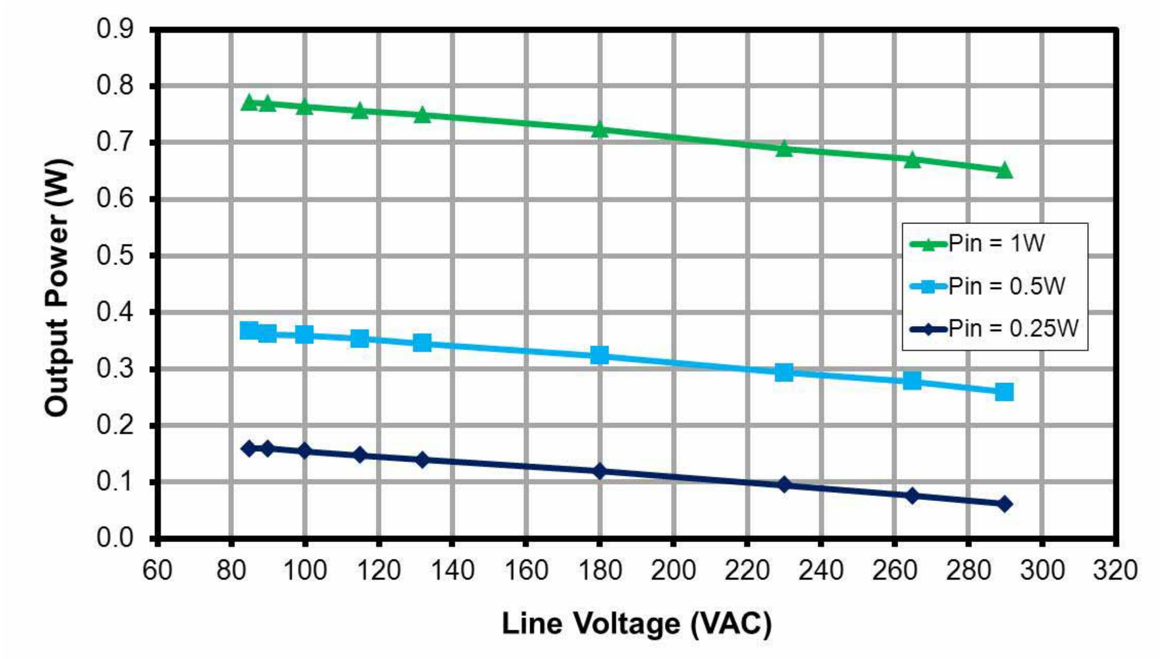

Figure 14 – Output Power at 0.25 W, 0.5 W and 1 W of Input Power, Room Temperature.

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10.4 Regulation

10.4.1 Load Regulation

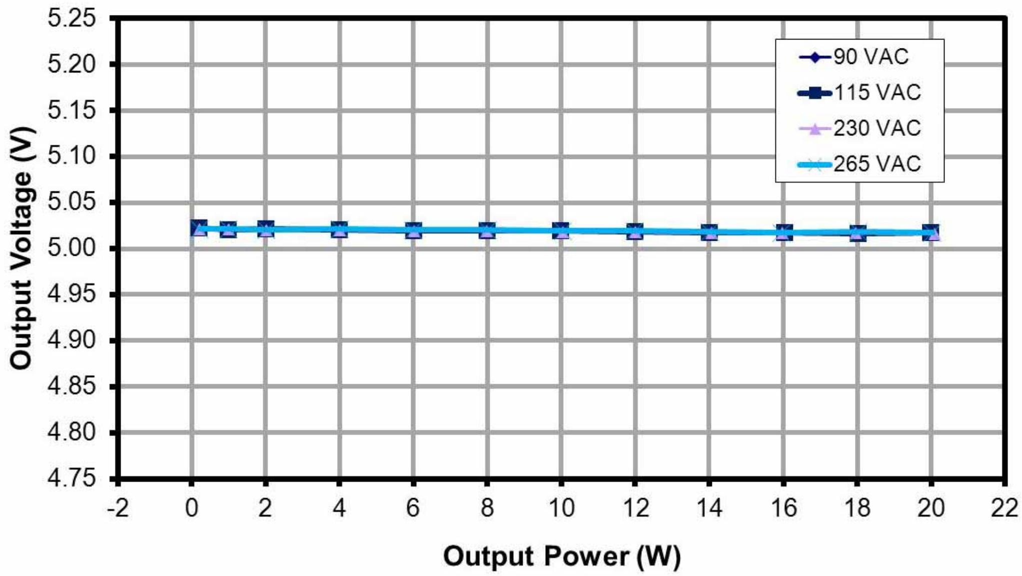

Figure 15 – Load Regulation, Room Temperature.

10.4.2 Line Regulation

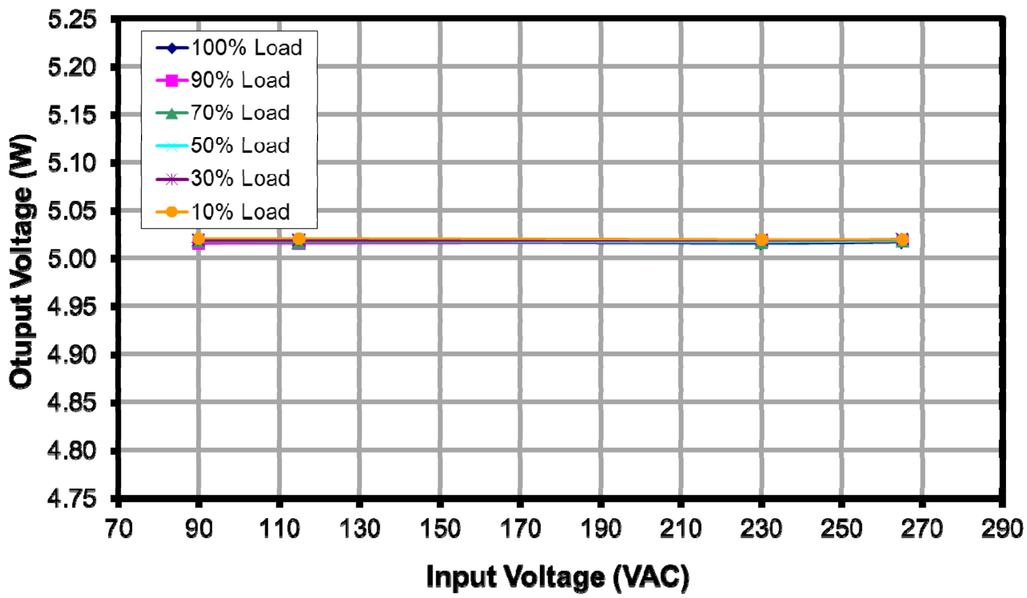

Figure 16 – Line Regulation, Room Temperature.

11 Thermal Performance

The unit was allowed to reach thermal equilibrium prior to the measurement. Figure 17 is the temperature profile of the board at room temperature.

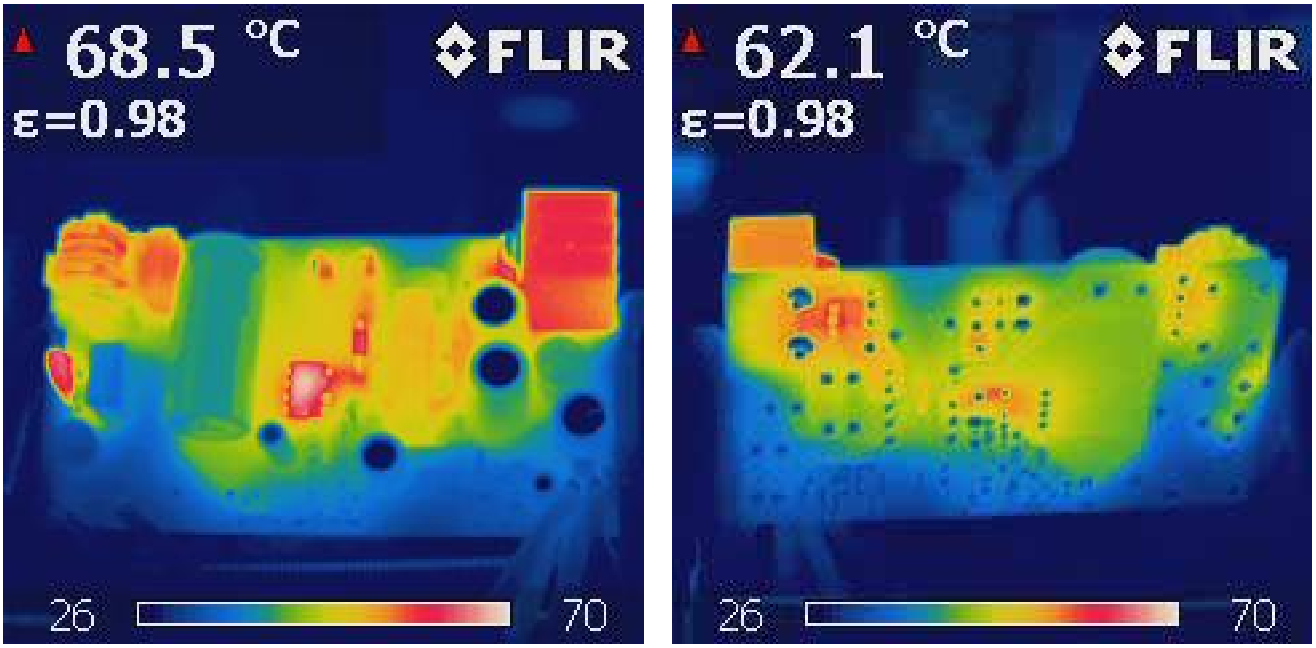

Figure 17 – Top and Bottom Side Thermal Images of the Board at 85 VAC, Full Load, Room Temperature.

Full load temperature of key components at 50°C ambient:

Item	Temperature (°C)
	85 VAC
Input Capacitor (C2)	61
Output Capacitor (C7)	69
Bridge Rectifier (BR1)	68
Transformer (T1), Core	74
Transformer (T1), Winding	73
Output Diode (D4)	72
Snubber Capacitor (C5)	65
Clamp Diode (D1)	72
TVS (VR1)	66
TinySwitch (U1) S Pin	81

Table 1 – Thermal Performance of Key Components at 85 VAC, Full Load, 50°C Ambient.

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12 Waveforms

12.1 Drain Voltage and Current, Normal Operation

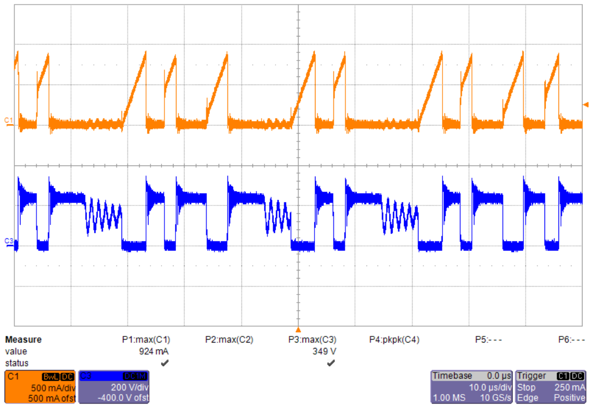

Figure 18 – 115 VAC, Full Load.
Upper: I_{DRAIN}, 0.5 A / div.
Lower: V_{DRAIN}, 200 V, 10 μs / div.

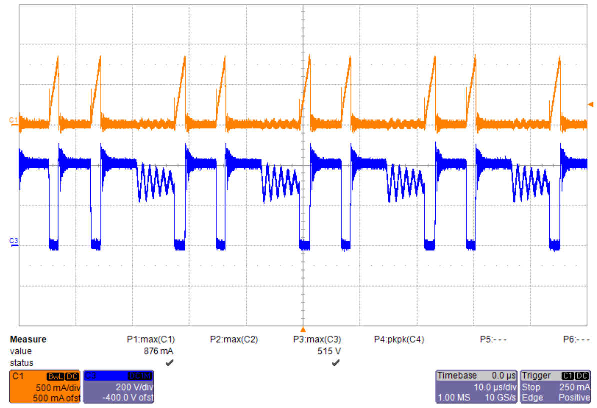

Figure 19 – 230 VAC, Full Load.
Upper: I_{DRAIN}, 0.5 A / div.
Lower: V_{DRAIN}, 200 V, 10 μs / div.

12.2 Drain Voltage and Current Start-up Profile

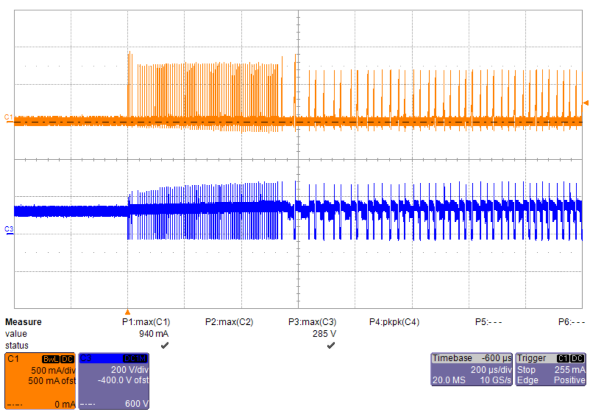

Figure 20 – Start-up Profile, 90 VAC, No-Load
Upper: I_{DRAIN}, 0.5 A, 200 μs / div.
Lower: V_{DRAIN}, 200 V / div.

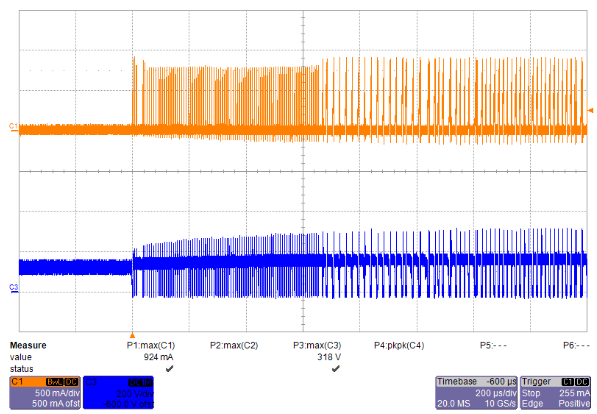

Figure 21 – Start-up Profile, 90 VAC, Full Load
Upper: I_{DRAIN}, 0.5 A, 200 μs / div.
Lower: V_{DRAIN}, 200 V / div.

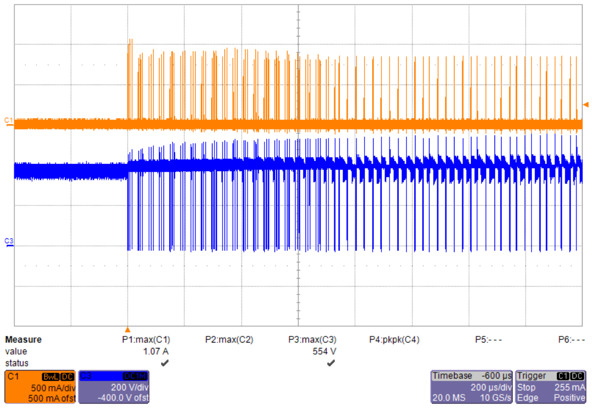

Figure 22 – Start-up Profile, 265 VAC, No-Load.
Upper: I_{DRAIN}, 0.5 A / div.
Lower: V_{DRAIN}, 200 V, 200 μs / div.

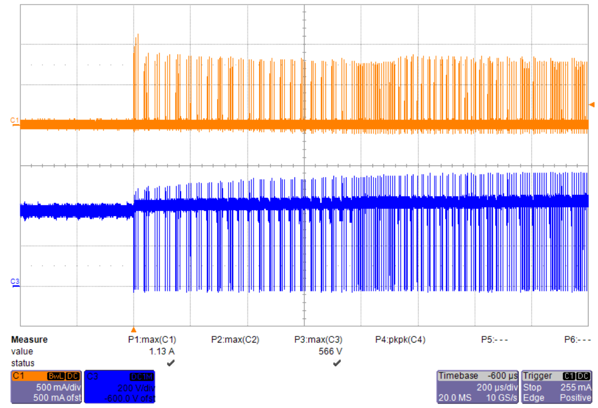

Figure 23 – Start-up Profile, 265 VAC, Full Load
Upper: I_{DRAIN}, 0.5 A / div.
Lower: V_{DRAIN}, 200 V, 200 μs / div.

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12.3 Output Voltage Start-up Profile

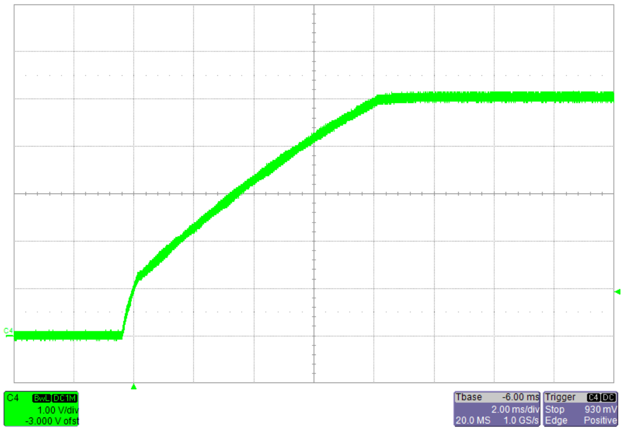

Figure 24 – Output Voltage, 90 VAC, No-Load
1 V, 2 ms / div.

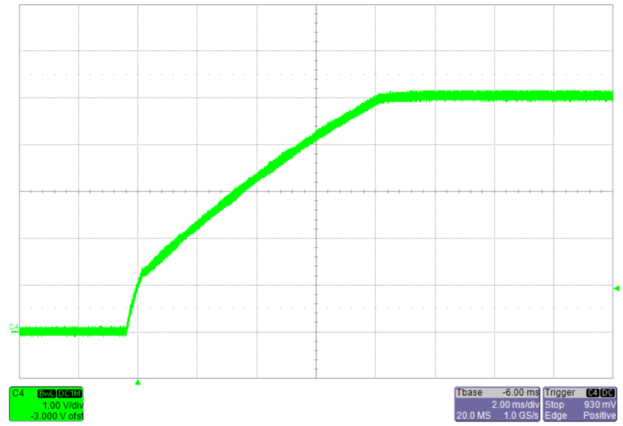

Figure 25 – Output Voltage, 90 VAC, Full Load
1 V, 2 ms / div.

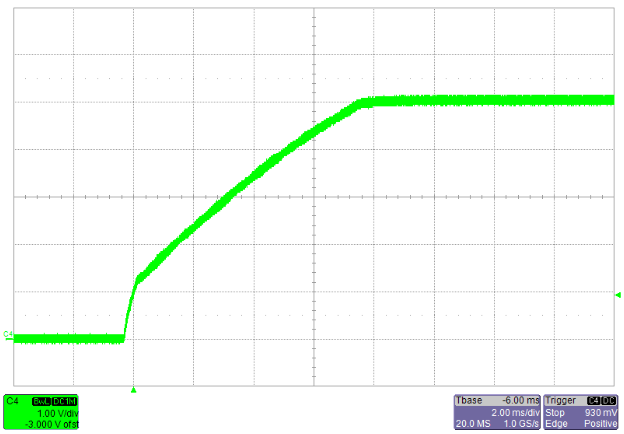

Figure 26– Output Voltage, 265 VAC, No-Load
1 V, 2 ms / div.

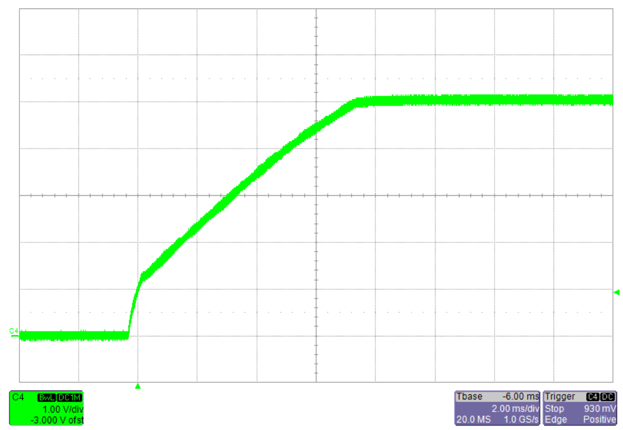

Figure 27 – Output Voltage, 265 VAC, Full Load
1 V, 2 ms / div.

12.4 Load Transient Response

Load transient setting:

Frequency = 75 Hz
Duty Cycle = 50%
Slew Rate = 0.1 A / µs

12.4.1 Load Step = 75 – 100 – 75%, with Soft-Finished Capacitor

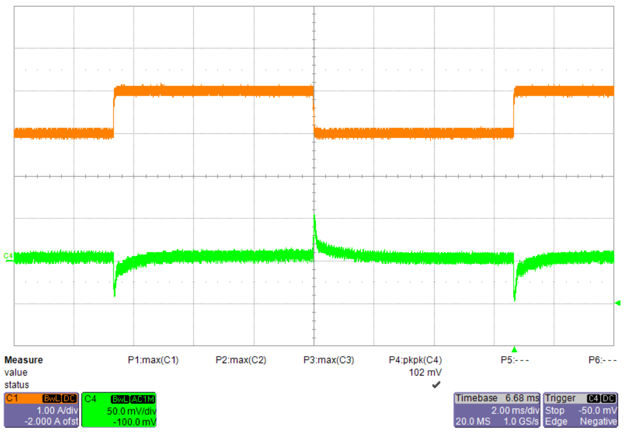

Figure 28 – Transient Response, 115 VAC.
Upper: I_{LOAD}, 1 A / div.
Lower: V_{OUT} (AC Coupled) 50 mV,
2 ms / div.

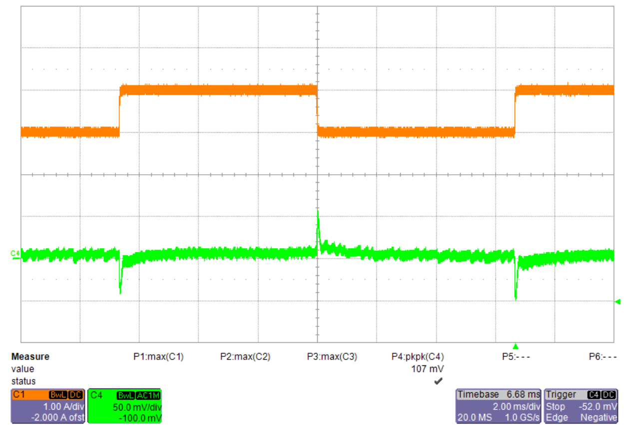

Figure 29 – Transient Response, 230 VAC.
Upper: I_{LOAD}, 1 A / div.
Lower: V_{OUT} (AC Coupled) 50 mV,
2 ms / div.

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12.5 *Output Ripple Measurements*

12.5.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF / 50 V ceramic type and one (1) 1.0 μF / 50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

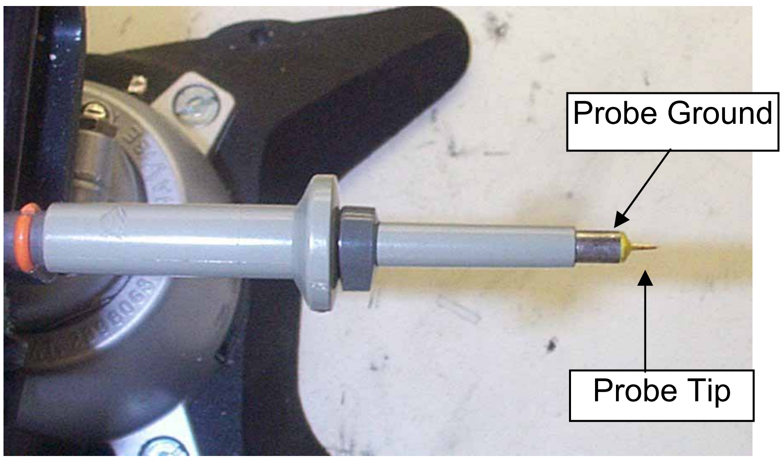

Figure 30 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed.)

Figure 31 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with Wires for Ripple Measurement, and Two Parallel Decoupling Capacitors Added.)

12.5.2 Measurement Results

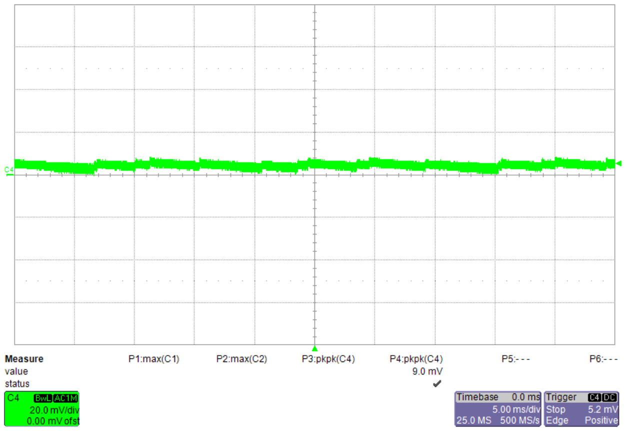

Figure 32 – Output Ripple, 85 VAC, No-Load
20 mV, 5 ms / div.

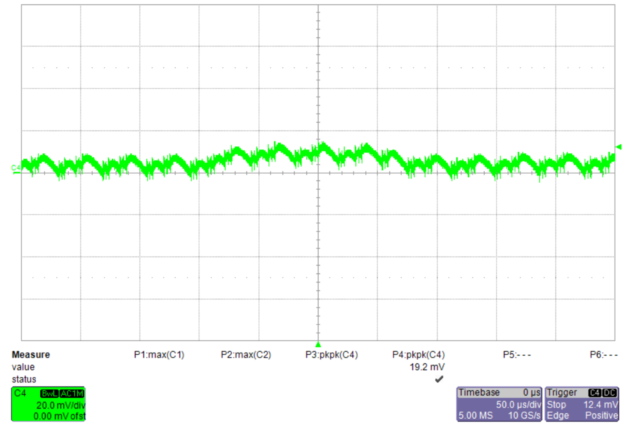

Figure 33 – Output Ripple, 85 VAC, Full Load
20 mV, 50 µs / div.

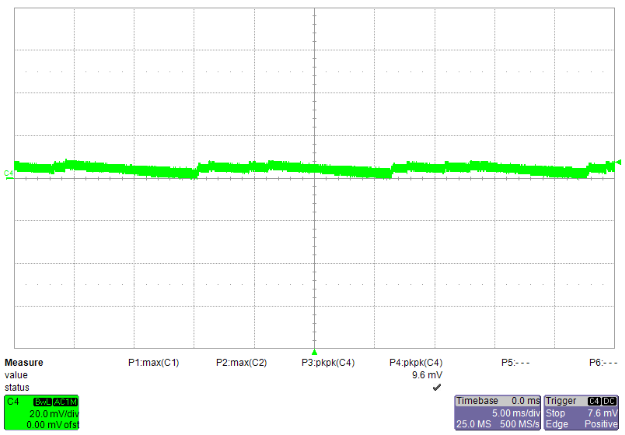

Figure 34 – Output Ripple, 115 VAC, No-Load
20 mV, 5 ms / div.

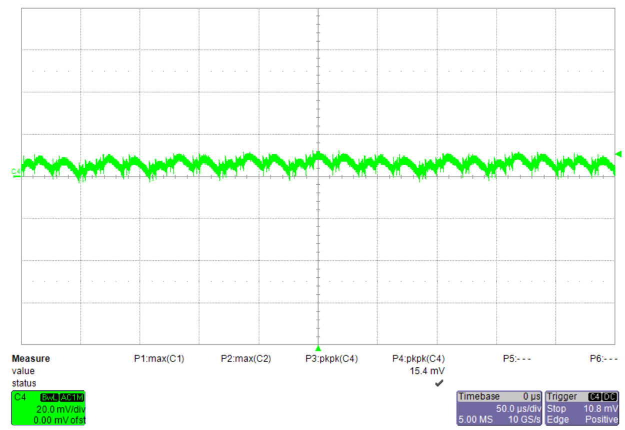

Figure 35 – Output Ripple, 115 VAC, Full Load
20 mV, 50 µs / div.

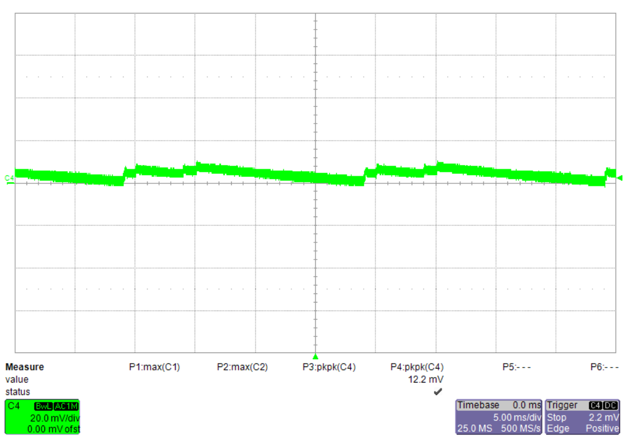

Figure 36 – Output Ripple, 230 VAC, No-Load
20 mV, 5 ms / div.

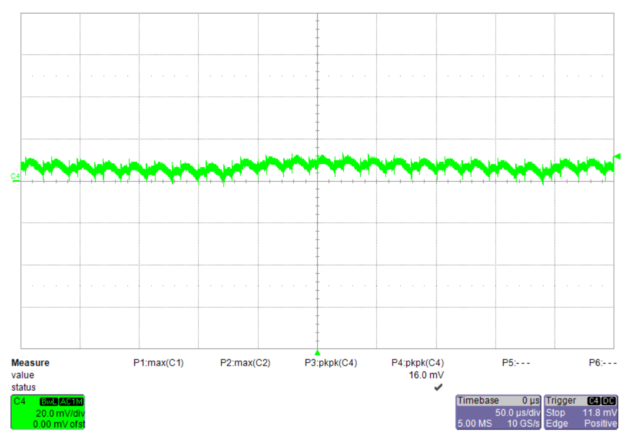

Figure 37 – Output Ripple, 230 VAC, Full Load
20 mV, 50 µs / div.

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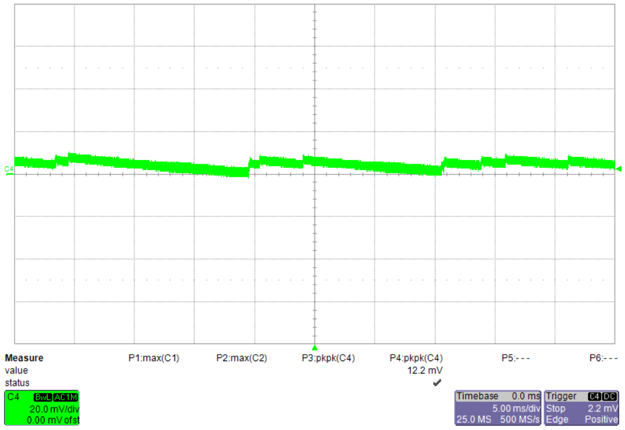

Figure 38 – Output Ripple, 265 VAC, No-Load
20 mV, 5 ms / div.

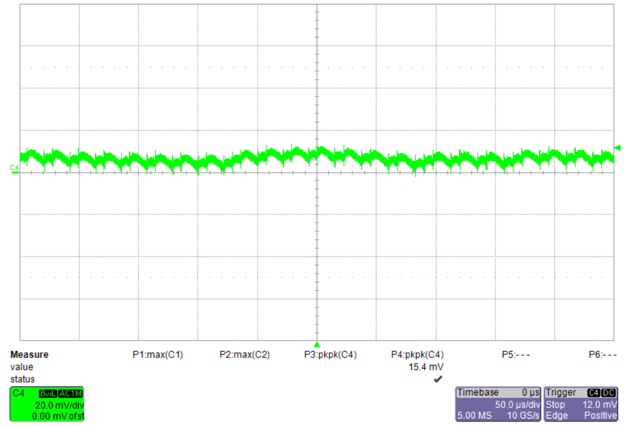

Figure 39 – Output Ripple, 265 VAC, Full Load
20 mV, 50 µs / div.

12.6 Brown In and Brown Out Test at Full Load

AC Input transient setting:

Frequency = 50 Hz
AC input= 0 VAC to 90 VAC, and 90 VAC to 0 VAC
Slew rate = 1 V / S

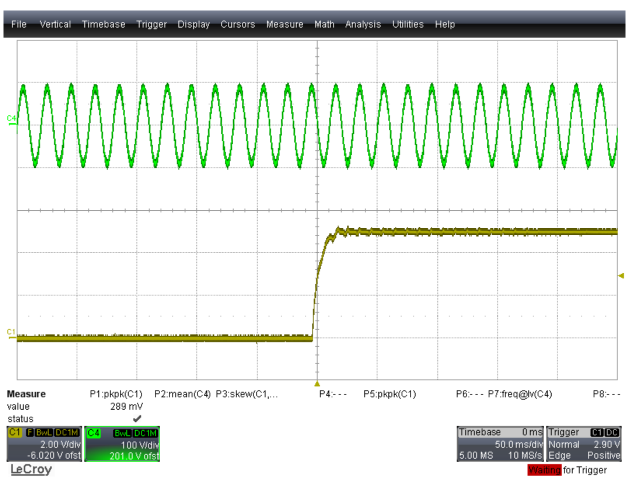

Figure 40 – AC Brown In Test., Full Load
Upper: V_{IN}, 100 V / div.
Lower: V_{OUT}, 2 V, 50 ms / div

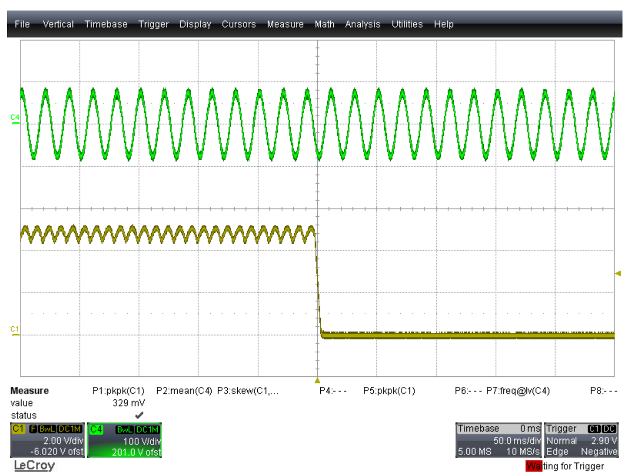

Figure 41 – AC Brown Out Test Full Load.
Upper: V_{IN}, 100 V / div.
Lower: $V_{OUT,}$ 2 V, 50 ms / div

13 Line Surge

Differential input line 1.2/50 μs surge testing was conducted on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC. Output was loaded at full load and operation was verified following each surge event.

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Results (Pass/Fail # Strikes)
D.M.		**(2Ω source)**		**10 Strikes each Level**
+1000	230	L1 to L2	90	Pass
–1000	230	L1 to L2	270	Pass
C.M.		**(12Ω source)**		
+2000	230	L1, L2 to PE	90	Pass
–2000	230	L1, L2 to PE	270	Pass

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14 Output Overvoltage Shutdown

All tests shown were conducted by shorting the optocoupler U3 LED while the power supply was in operation.

14.1 Test Results

Simple OVP Circuit

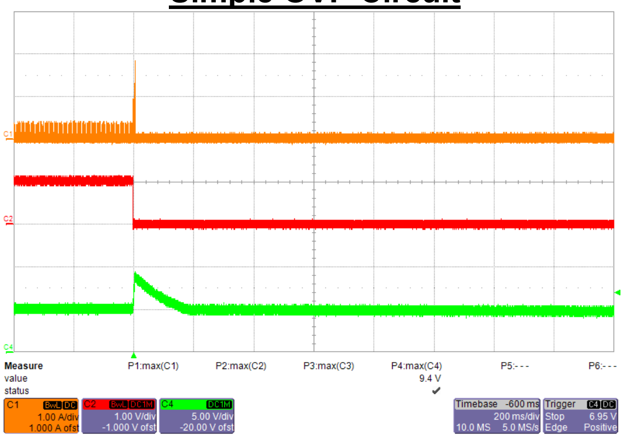

Figure 42 – Output Overvoltage (Open Loop),
90 VAC, No-Load
Upper: I_{DRAIN}, 1 A / div.
Middle: Opto Diode Voltage, 1 V / div.
Lower: V_{OUT}, 5 V, 200 ms / div.
OVP at 9.4 V

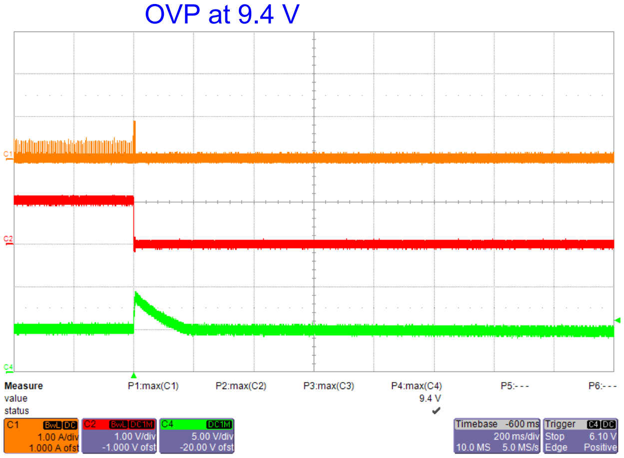

Figure 44 – Output Overvoltage (Open Loop),
265 VAC, No-Load
Upper: I_{DRAIN}, 1 A / div.
Middle: Opto Diode Voltage, 1 V / div.
Lower: V_{OUT}, 5 V, 200 ms / div.
OVP at 9.4 V

Precision OVP Circuit

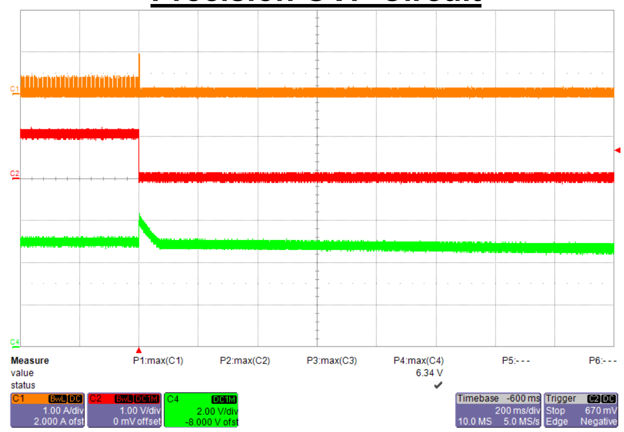

Figure 43 – Output Overvoltage (Open Loop),
90 VAC, No-Load
Upper: I_{DRAIN}, 1 A / div.
Middle: Opto Diode Voltage, 1 V / div.
Lower: V_{OUT} 2 V, 200 ms / div.
OVP at 6.34 V

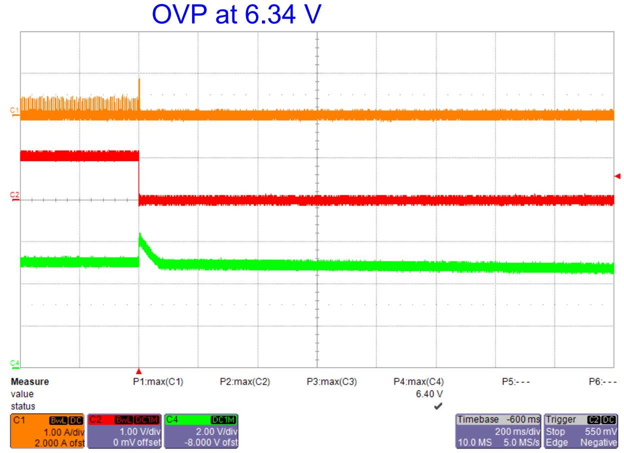

Figure 45 – Output Overvoltage (Open Loop),
265 VAC, No-Load
Upper: I_{DRAIN}, 1 A / div.
Middle: Opto Diode Voltage, 1 V / div.
Lower: V_{OUT}, 2 V, 200 ms / div.
OVP at 6.4 V

Simple OVP Circuit

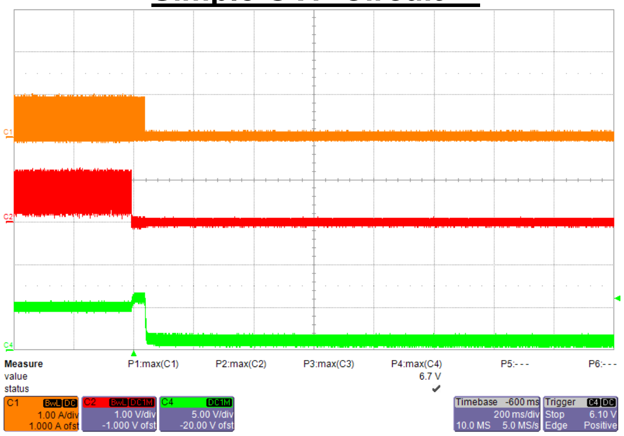

Figure 46 – Output Overvoltage (Open Loop),
90 VAC, Full Load
Upper: I_{DRAIN}, 1 A / div
Middle: Opto Diode Voltage, 1 V / div
Lower: V_{OUT}, 5 V, 200 ms / div.
OVP at 6.7 V

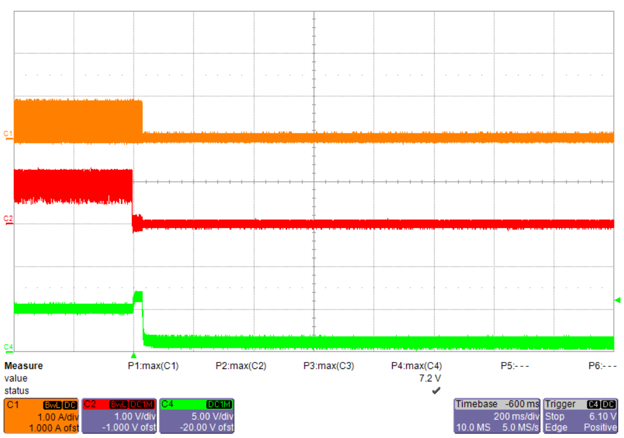

Figure 48 – Output Overvoltage (Open Loop),
265 VAC, Full Load
Upper: I_{DRAIN}, 1 A / div.
Middle: Opto Diode Voltage, 1 V / div.
Lower: V_{OUT}, 5 V, 200 ms / div.
OVP at 7.2 V

Precision OVP Circuit

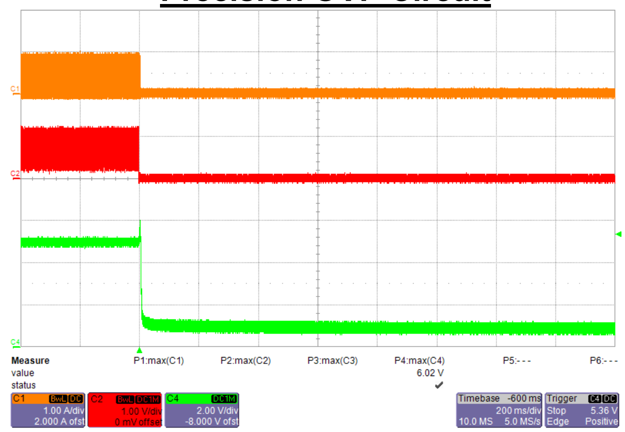

Figure 47 – Output Overvoltage (Open Loop),
90 VAC, Full Load
Upper: I_{DRAIN}, 1 A / div
Middle: Opto Diode Voltage, 1 V / div
Lower: V_{OUT}, 2 V, 200 ms / div.
OVP at 6.02 V

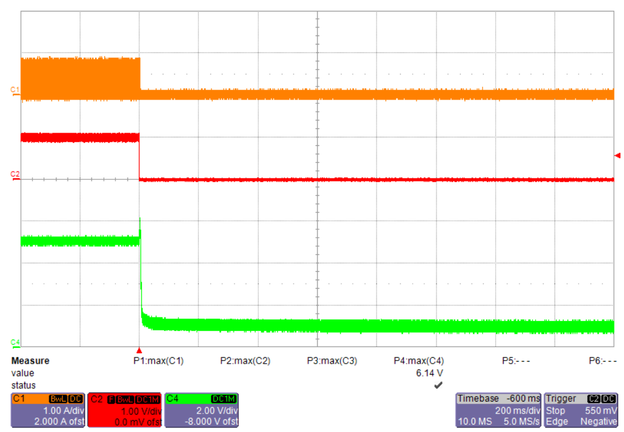

Figure 49 – Output Overvoltage (Open Loop),
265 VAC, Full Load
Upper: I_{DRAIN}, 1 A / div.
Middle: Opto Diode Voltage, 1 V / div.
Lower: V_{OUT}, 2 V, 200 ms / div.
OVP at 6.14 V

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15 EMI

Full load EMI was tested with resistor load after the board was powered on for 20 minutes.

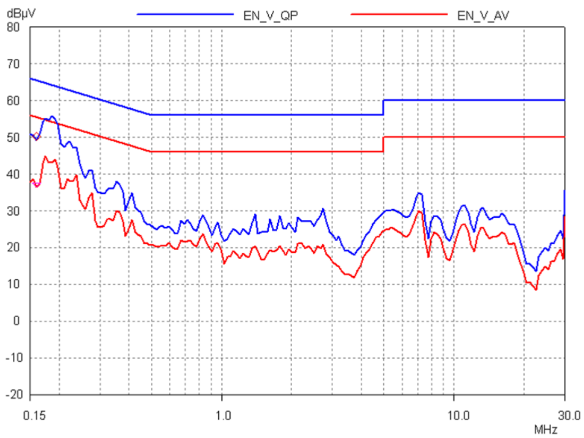

Figure 50 – 115 VAC, Line.

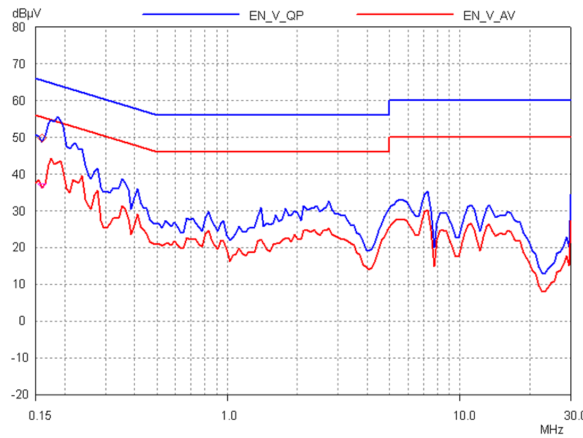

Figure 51 – 115 VAC, Neutral.

Figure 52 – 230 VAC, Line.

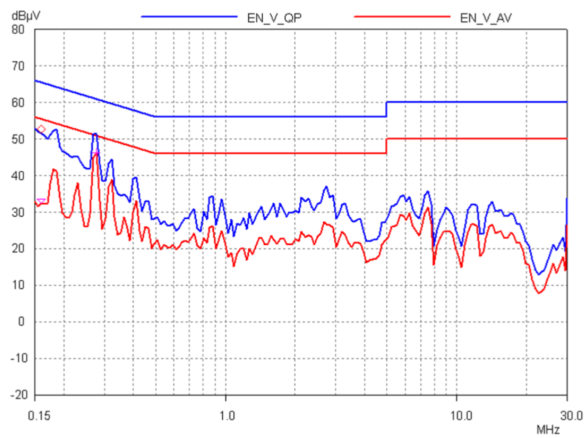

Figure 53 – 230 VAC, Neutral.

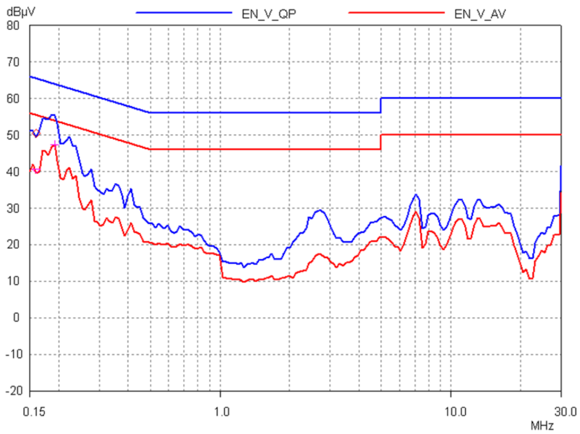

Figure 54 – 115 VAC, Line with Artificial Hand Connected to the Output.

Figure 55 – 115 VAC, Neutral with Artificial Hand Connected to the Output.

Figure 56 – 230 VAC, Line with Artificial Hand Connected to the Output.

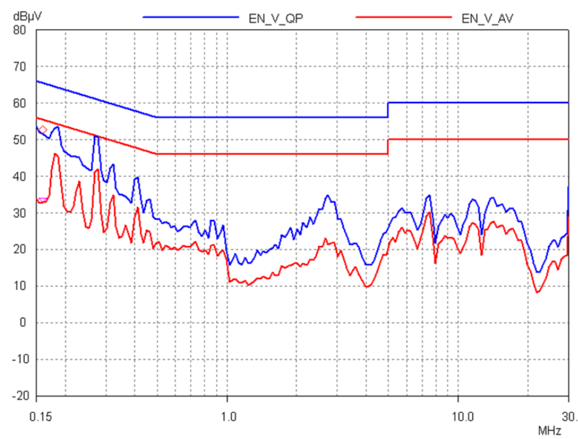

Figure 57 – 230 VAC, Neutral with Artificial Hand Connected to the Output.

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16 Revision Summary

Date	Author	Revision	Description and Changes	Reviewed
25-Sep-12	PL	1.5	Initial Release	Apps & Mktg

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