

# MC10E136, MC100E136

## 5V ECL 6-Bit Universal Up/Down Counter

### Description

The MC10E/100E136 is a 6-bit synchronous, presetable, cascadable universal counter. The device generates a look-ahead-carry output and accepts a look-ahead-carry input. These two features allow for the cascading of multiple E136's for wider bit width counters that operate at very nearly the same frequency as the stand alone counter.

The  $\overline{\text{CLOUT}}$  output will pulse LOW for one clock cycle one count before the E136 reaches terminal count. The  $\overline{\text{COUT}}$  output will pulse LOW for one clock cycle when the counter reaches terminal count. For more information on utilizing the look-ahead-carry features of the device please refer to the applications section of this data sheet. The differential COUT output facilitates the E136's use in programmable divider and self-stopping counter applications.

Unlike the H136 and other similar universal counter designs, the E136 carry-out and look-ahead-carry-out signals are registered on chip.

This design alleviates the glitch problem seen on many counters where the carry out signals are merely gated. Because of this architecture there are some minor functional differences between the E136 and H136 counters. The user, regardless of familiarity with the H136, should read this data sheet carefully. Note specifically (see logic diagram) the operation of the carry out outputs and the look-ahead-carry in input when utilizing the master reset.

When left open all of the input pins will be pulled LOW via an input pull-down resistor. The master reset is an asynchronous signal which when asserted will force the Q outputs LOW.

The Q outputs need not be terminated for the E136 to function properly, in fact if these outputs will not be used in a system it is recommended to save power and minimize noise that they be left open. This practice will minimize switching noise which can reduce the maximum count frequency of the device or significantly reduce margins against other noise in the system.

The 100 Series contains temperature compensation.

### Features

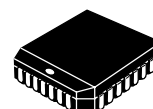
- 550 MHz Count Frequency
- Fully Synchronous Up and Down Counting
- Look-Ahead-Carry Input and Output
- Asynchronous Master Reset
- PECL Mode Operating Range:  $V_{CC} = 4.2 \text{ V}$  to  $5.7 \text{ V}$  with  $V_{EE} = 0 \text{ V}$
- NECL Mode Operating Range:  $V_{CC} = 0 \text{ V}$  with  $V_{EE} = -4.2 \text{ V}$  to  $-5.7 \text{ V}$
- Internal Input 50 k $\Omega$  Pulldown Resistors
- ESD Protection: Human Body Model: > 2 kV,  
Machine Model: > 200 V

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



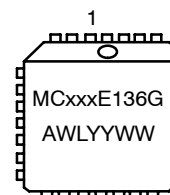
**ON Semiconductor®**

<http://onsemi.com>



PLCC-28  
FN SUFFIX  
CASE 776

### MARKING DIAGRAM\*



|     |                     |
|-----|---------------------|
| xxx | = 10 or 100         |
| A   | = Assembly Location |
| WL  | = Wafer Lot         |
| YY  | = Year              |
| WW  | = Work Week         |
| G   | = Pb-Free Package   |

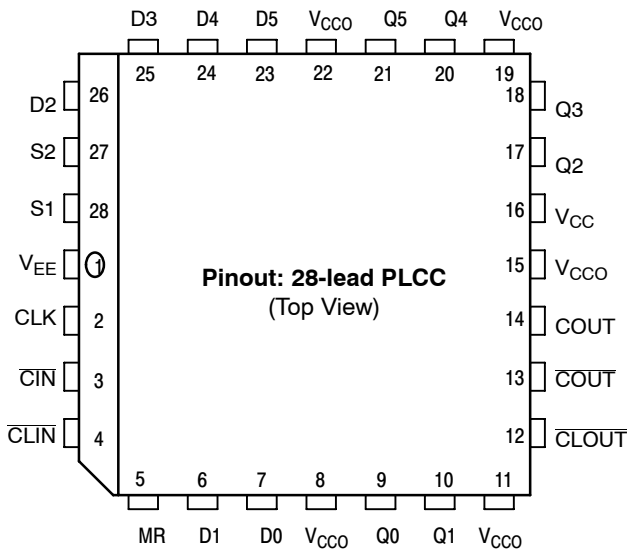
\*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

- Meets or Exceeds JEDEC Standard EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level: Pb = 1; Pb-Free = 3  
For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL 94 V-0 @ 0.125 in, Oxygen Index: 28 to 34
- Transistor Count = 506 devices
- Pb-Free Packages are Available\*

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\* All  $V_{CC}$  and  $V_{CCO}$  pins are tied together on the die.

Warning: All  $V_{CC}$ ,  $V_{CCO}$ , and  $V_{EE}$  pins must be externally connected to Power Supply to guarantee proper operation.

**Figure 1. 28-Lead Pinout**

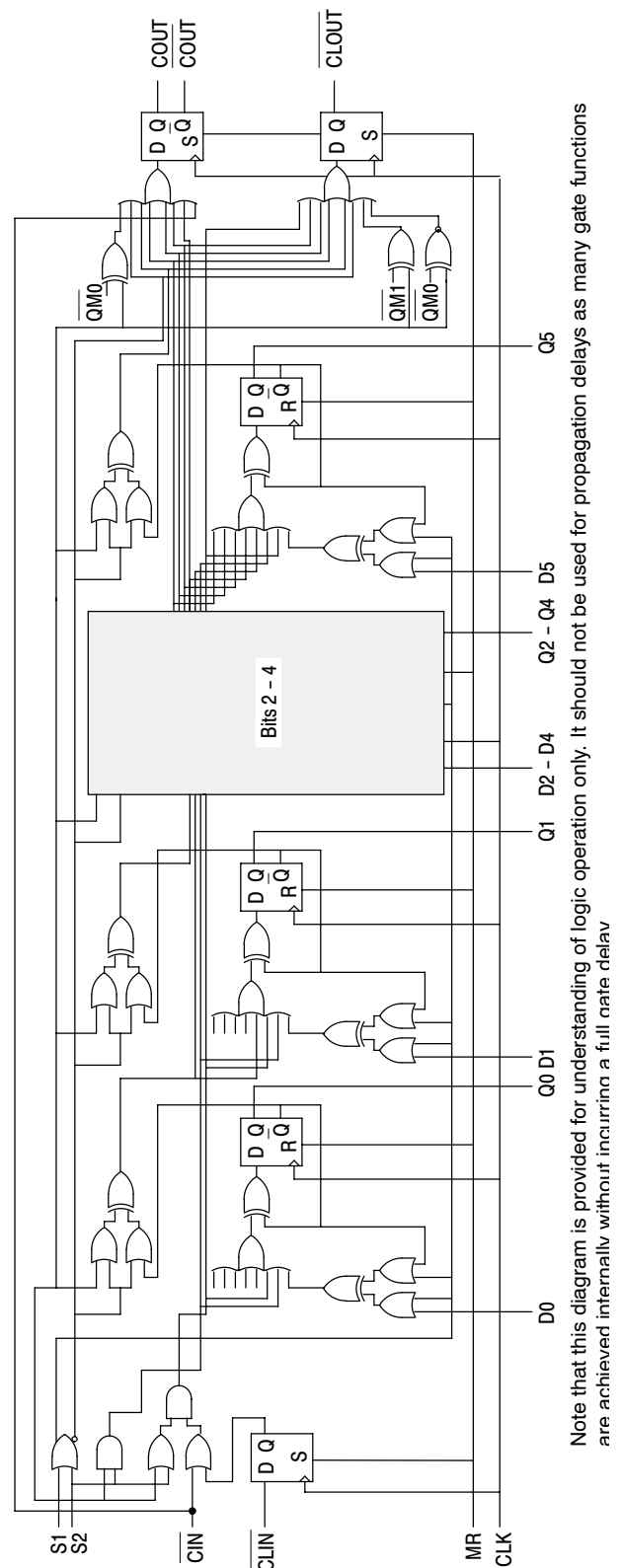
**Table 1. PIN DESCRIPTION**

| PIN                                   | FUNCTION                                       |
|---------------------------------------|--|
| $D_0 - D_5$                           | ECL Preset Data Inputs                         |
| $Q_0 - Q_5$                           | ECL Data Outputs                               |
| S1, S2                                | Mode Control Pins                              |
| MR                                    | Master Reset                                   |
| CLK                                   | ECL Clock Input                                |
| $\overline{COUT}$ , $\overline{COUT}$ | ECL Differential Carry-Out Output (Active LOW) |
| $\overline{CLOUT}$                    | ECL Look-Ahead-Carry Out (Active LOW)          |
| $\overline{CIN}$                      | ECL Carry-In Input (Active LOW)                |
| $\overline{CLIN}$                     | ECL Look-Ahead-Carry In Input (Active LOW)     |
| $V_{CC}$ , $V_{CCO}$                  | Positive Supply                                |
| $V_{EE}$                              | Negative Supply                                |

**Table 2. FUNCTION TABLE**

(Expanded Truth Table on page 3)

| S1 | S2 | $\overline{CIN}$ | MR | CLK | FUNCTION                     |
|----|----|------------------|----|-----|------------------------------|
| L  | L  | X                | L  | Z   | Preset Parallel Data         |
| L  | H  | L                | L  | Z   | Increment (Count Up)         |
| L  | H  | H                | L  | Z   | Hold Count                   |
| H  | L  | L                | L  | Z   | Decrement (Count Down)       |
| H  | L  | H                | L  | Z   | Hold Count                   |
| H  | H  | X                | L  | Z   | Hold Count                   |
| X  | X  | X                | H  | X   | Reset ( $Q_n = \text{LOW}$ ) |



Note that this diagram is provided for understanding of logic operation only. It should not be used for propagation delays as many gate functions are achieved internally without incurring a full gate delay

**Figure 2. E136 Universal Up/Down Counter Logic Diagram**

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**Table 3. EXPANDED TRUTH TABLE**

| Function                     | S1 | S2 | MR | CIN | CLIN | CLK | D5 | D4 | D3 | D2 | D1 | D0 | Q5 | Q4 | Q3 | Q2 | Q1 | Q0 | COU <sub>T</sub> | CLOU <sub>T</sub> |
|------------------------------|----|----|----|-----|------|-----|----|----|----|----|----|----|----|----|----|----|----|----|------------------|-------------------|
| Preset                       | L  | L  | L  | X   | X    | Z   | L  | L  | L  | L  | H  | H  | L  | L  | L  | L  | H  | H  | H                | H                 |
| Down                         | H  | L  | L  | L   | L    | Z   | X  | X  | X  | X  | X  | X  | L  | L  | L  | L  | H  | L  | H                | H                 |
|                              | H  | L  | L  | L   | L    | Z   | X  | X  | X  | X  | X  | X  | L  | L  | L  | L  | L  | L  | L                | L                 |
|                              | H  | L  | L  | L   | L    | Z   | X  | X  | X  | X  | X  | X  | L  | L  | L  | L  | L  | L  | L                | L                 |
|                              | H  | L  | L  | L   | L    | Z   | X  | X  | X  | X  | X  | X  | H  | H  | H  | H  | H  | H  | H                | H                 |
| Preset                       | L  | L  | L  | X   | X    | Z   | H  | H  | H  | H  | L  | L  | H  | H  | H  | H  | L  | L  | H                | H                 |
| Up                           | L  | H  | L  | L   | L    | Z   | X  | X  | X  | X  | X  | X  | H  | H  | H  | H  | L  | H  | H                | H                 |
|                              | L  | H  | L  | L   | L    | Z   | X  | X  | X  | X  | X  | X  | H  | H  | H  | H  | H  | L  | H                | L                 |
|                              | L  | H  | L  | L   | L    | Z   | X  | X  | X  | X  | X  | X  | H  | H  | H  | H  | H  | L  | H                | L                 |
|                              | L  | H  | L  | L   | L    | Z   | X  | X  | X  | X  | X  | X  | L  | L  | L  | L  | L  | L  | H                | H                 |
|                              | L  | H  | L  | L   | L    | Z   | X  | X  | X  | X  | X  | X  | L  | L  | L  | L  | L  | L  | H                | H                 |
|                              | L  | H  | L  | L   | L    | Z   | X  | X  | X  | X  | X  | X  | L  | L  | L  | L  | L  | L  | H                | H                 |
| Hold                         | H  | H  | L  | X   | X    | Z   | X  | X  | X  | X  | X  | X  | L  | L  | L  | L  | H  | L  | H                | H                 |
|                              | H  | H  | L  | X   | X    | Z   | X  | X  | X  | X  | X  | X  | L  | L  | L  | L  | H  | L  | H                | H                 |
| Down<br>Hold<br>Down<br>Hold | H  | L  | L  | L   | L    | Z   | X  | X  | X  | X  | X  | X  | L  | L  | L  | L  | L  | H  | L                | L                 |
|                              | H  | L  | L  | L   | L    | Z   | X  | X  | X  | X  | X  | X  | L  | L  | L  | L  | L  | L  | L                | L                 |
|                              | H  | L  | L  | L   | L    | Z   | X  | X  | X  | X  | X  | X  | L  | L  | L  | L  | L  | L  | L                | L                 |
|                              | H  | L  | L  | L   | L    | Z   | X  | X  | X  | X  | X  | X  | L  | L  | L  | L  | L  | L  | L                | L                 |
|                              | H  | L  | L  | L   | L    | Z   | X  | X  | X  | X  | X  | X  | L  | L  | L  | L  | L  | L  | L                | L                 |
|                              | H  | L  | L  | L   | L    | Z   | X  | X  | X  | X  | X  | X  | L  | L  | L  | L  | L  | L  | L                | L                 |
| Hold                         | H  | L  | L  | L   | H    | Z   | X  | X  | X  | X  | X  | X  | L  | L  | L  | L  | L  | L  | L                | L                 |
|                              | H  | L  | L  | L   | H    | Z   | X  | X  | X  | X  | X  | X  | L  | L  | L  | L  | L  | L  | L                | L                 |
|                              | H  | L  | L  | L   | H    | Z   | X  | X  | X  | X  | X  | X  | L  | L  | L  | L  | L  | L  | L                | L                 |
|                              | H  | L  | L  | L   | H    | Z   | X  | X  | X  | X  | X  | X  | L  | L  | L  | L  | L  | L  | L                | L                 |
|                              | H  | L  | L  | L   | H    | Z   | X  | X  | X  | X  | X  | X  | L  | L  | L  | L  | L  | L  | L                | L                 |
|                              | H  | L  | L  | L   | L    | Z   | X  | X  | X  | X  | X  | X  | L  | L  | L  | L  | L  | L  | L                | L                 |
| Hold<br>Preset<br>Up         | H  | H  | L  | L   | L    | Z   | X  | X  | X  | X  | X  | X  | L  | L  | L  | L  | L  | L  | L                | H                 |
|                              | L  | L  | L  | X   | X    | Z   | H  | H  | H  | H  | L  | L  | H  | H  | H  | H  | L  | L  | H                | H                 |
|                              | L  | H  | L  | L   | L    | Z   | X  | X  | X  | X  | X  | X  | H  | H  | H  | H  | L  | L  | H                | H                 |
|                              | L  | H  | L  | L   | L    | Z   | X  | X  | X  | X  | X  | X  | H  | H  | H  | H  | H  | L  | H                | L                 |
|                              | L  | H  | L  | L   | L    | Z   | X  | X  | X  | X  | X  | X  | H  | H  | H  | H  | H  | L  | H                | L                 |
|                              | L  | H  | L  | L   | L    | Z   | X  | X  | X  | X  | X  | X  | H  | H  | H  | H  | H  | L  | H                | L                 |
| Hold<br>Up<br>Hold           | L  | H  | L  | L   | L    | Z   | X  | X  | X  | X  | X  | X  | H  | H  | H  | H  | H  | L  | H                | L                 |
|                              | L  | H  | L  | L   | L    | Z   | X  | X  | X  | X  | X  | X  | H  | H  | H  | H  | H  | L  | H                | L                 |
|                              | L  | H  | L  | L   | L    | Z   | X  | X  | X  | X  | X  | X  | H  | H  | H  | H  | H  | L  | H                | L                 |
|                              | L  | H  | L  | L   | L    | Z   | X  | X  | X  | X  | X  | X  | H  | H  | H  | H  | H  | L  | H                | L                 |
| Hold                         | L  | H  | L  | L   | L    | Z   | X  | X  | X  | X  | X  | X  | H  | H  | H  | H  | H  | L  | H                | L                 |
|                              | L  | H  | L  | L   | L    | Z   | X  | X  | X  | X  | X  | X  | H  | H  | H  | H  | H  | L  | H                | L                 |
|                              | L  | H  | L  | L   | L    | Z   | X  | X  | X  | X  | X  | X  | H  | H  | H  | H  | H  | L  | H                | L                 |
|                              | L  | H  | L  | L   | L    | Z   | X  | X  | X  | X  | X  | X  | H  | H  | H  | H  | H  | L  | H                | L                 |
| Up                           | L  | H  | L  | L   | L    | Z   | X  | X  | X  | X  | X  | X  | L  | L  | L  | L  | L  | L  | H                | H                 |
|                              | L  | H  | L  | L   | L    | Z   | X  | X  | X  | X  | X  | X  | L  | L  | L  | L  | L  | H  | H                | H                 |
|                              | L  | H  | L  | L   | L    | Z   | X  | X  | X  | X  | X  | X  | L  | L  | L  | L  | L  | H  | H                | H                 |
|                              | L  | H  | L  | L   | L    | Z   | X  | X  | X  | X  | X  | X  | L  | L  | L  | L  | L  | H  | H                | H                 |
| Reset                        | X  | X  | H  | X   | X    | X   | X  | X  | X  | X  | X  | X  | L  | L  | L  | L  | L  | L  | H                | H                 |

Z = Low to High Transition

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**Table 4. MAXIMUM RATINGS**

| Symbol           | Parameter  | Condition 1                                    | Condition 2  | Rating                     | Unit         |
|------------------|--|--|--|----------------------------|--------------|
| V <sub>CC</sub>  | PECL Mode Power Supply                             | V <sub>EE</sub> = 0 V                          |  | 8                          | V            |
| V <sub>EE</sub>  | NECL Mode Power Supply                             | V <sub>CC</sub> = 0 V                          |  | –8                         | V            |
| V <sub>I</sub>   | PECL Mode Input Voltage<br>NECL Mode Input Voltage | V <sub>EE</sub> = 0 V<br>V <sub>CC</sub> = 0 V | V <sub>I</sub> ≤ V <sub>CC</sub><br>V <sub>I</sub> ≥ V <sub>EE</sub> | 6<br>–6                    | V<br>V       |
| I <sub>out</sub> | Output Current                                     | Continuous<br>Surge                            |  | 50<br>100                  | mA<br>mA     |
| T <sub>A</sub>   | Operating Temperature Range                        |  |  | 0 to +85                   | °C           |
| T <sub>stg</sub> | Storage Temperature Range                          |  |  | –65 to +150                | °C           |
| θ <sub>JA</sub>  | Thermal Resistance (Junction–to–Ambient)           | 0 lfpm<br>500 lfpm                             | PLCC–28<br>PLCC–28   | 63.5<br>43.5               | °C/W<br>°C/W |
| θ <sub>JC</sub>  | Thermal Resistance (Junction–to–Case)              | Standard Board                                 | PLCC–28  | 22 to 26                   | °C/W         |
| V <sub>EE</sub>  | PECL Operating Range<br>NECL Operating Range       |  |  | 4.2 to 5.7<br>–5.7 to –4.2 | V<br>V       |
| T <sub>sol</sub> | Wave Solder<br>Pb<br>Pb–Free                       |  |  | 265<br>265                 | °C           |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**Table 5. 10E SERIES PECL DC CHARACTERISTICS** V<sub>CCx</sub> = 5.0 V; V<sub>EE</sub> = 0.0 V (Note 1)

| Symbol          | Characteristic               | 0°C  |      |      | 25°C |      |      | 85°C |      |      | Unit |
|-----------------|------------------------------|------|------|------|------|------|------|------|------|------|------|
|                 |                              | Min  | Typ  | Max  | Min  | Typ  | Max  | Min  | Typ  | Max  |      |
| I <sub>EE</sub> | Power Supply Current         |      | 125  | 150  |      | 125  | 150  |      | 125  | 150  | mA   |
| V <sub>OH</sub> | Output HIGH Voltage (Note 2) | 3980 | 4070 | 4160 | 4020 | 4105 | 4190 | 4090 | 4185 | 4280 | mV   |
| V <sub>OL</sub> | Output LOW Voltage (Note 2)  | 3050 | 3210 | 3370 | 3050 | 3210 | 3370 | 3050 | 3227 | 3405 | mV   |
| V <sub>IH</sub> | Input HIGH Voltage           | 3830 | 3995 | 4160 | 3870 | 4030 | 4190 | 3940 | 4110 | 4280 | mV   |
| V <sub>IL</sub> | Input LOW Voltage            | 3050 | 3285 | 3520 | 3050 | 3285 | 3520 | 3050 | 3302 | 3555 | mV   |
| I <sub>IH</sub> | Input HIGH Current           |      |      | 150  |      |      | 150  |      |      | 150  | μA   |
| I <sub>IL</sub> | Input LOW Current            | 0.5  | 0.3  |      | 0.5  | 0.25 |      | 0.3  | 0.2  |      | μA   |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V<sub>CC</sub>. V<sub>EE</sub> can vary –0.46 V / +0.06 V.
2. Outputs are terminated through a 50 Ω resistor to V<sub>CC</sub> – 2.0 V.

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**Table 6. 10E SERIES NECL DC CHARACTERISTICS**  $V_{CCx} = 0.0\text{ V}$ ;  $V_{EE} = -5.0\text{ V}$  (Note 3)

| Symbol   | Characteristic               | 0°C   |       |       | 25°C  |       |       | 85°C  |       |       | Unit          |
|----------|------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
|          |                              | Min   | Typ   | Max   | Min   | Typ   | Max   | Min   | Typ   | Max   |               |
| $I_{EE}$ | Power Supply Current         |       | 125   | 150   |       | 125   | 150   |       | 125   | 150   | mA            |
| $V_{OH}$ | Output HIGH Voltage (Note 4) | -1020 | -930  | -840  | -980  | -895  | -810  | -910  | -815  | -720  | mV            |
| $V_{OL}$ | Output LOW Voltage (Note 4)  | -1950 | -1790 | -1630 | -1950 | -1790 | -1630 | -1950 | -1773 | -1595 | mV            |
| $V_{IH}$ | Input HIGH Voltage           | -1170 | -1005 | -840  | -1130 | -970  | -810  | -1060 | -890  | -720  | mV            |
| $V_{IL}$ | Input LOW Voltage            | -1950 | -1715 | -1480 | -1950 | -1715 | -1480 | -1950 | -1698 | -1445 | mV            |
| $I_{IH}$ | Input HIGH Current           |       |       | 150   |       |       | 150   |       |       | 150   | $\mu\text{A}$ |
| $I_{IL}$ | Input LOW Current            | 0.5   | 0.3   |       | 0.5   | 0.065 |       | 0.3   | 0.2   |       | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $-0.46\text{ V}$  /  $+0.06\text{ V}$ .

4. Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .

**Table 7. 100E SERIES PECL DC CHARACTERISTICS**  $V_{CCx} = 5.0\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  (Note 5)

| Symbol   | Characteristic               | 0°C  |      |      | 25°C |      |      | 85°C |      |      | Unit          |
|----------|------------------------------|------|------|------|------|------|------|------|------|------|---------------|
|          |                              | Min  | Typ  | Max  | Min  | Typ  | Max  | Min  | Typ  | Max  |               |
| $I_{EE}$ | Power Supply Current         |      | 125  | 150  |      | 125  | 150  |      | 140  | 170  | mA            |
| $V_{OH}$ | Output HIGH Voltage (Note 6) | 3975 | 4050 | 4120 | 3975 | 4050 | 4120 | 3975 | 4050 | 4120 | mV            |
| $V_{OL}$ | Output LOW Voltage (Note 6)  | 3190 | 3295 | 3380 | 3190 | 3255 | 3380 | 3190 | 3260 | 3380 | mV            |
| $V_{IH}$ | Input HIGH Voltage           | 3835 | 3975 | 4120 | 3835 | 3975 | 4120 | 3835 | 3975 | 4120 | mV            |
| $V_{IL}$ | Input LOW Voltage            | 3190 | 3355 | 3525 | 3190 | 3355 | 3525 | 3190 | 3355 | 3525 | mV            |
| $I_{IH}$ | Input HIGH Current           |      |      | 150  |      |      | 150  |      |      | 150  | $\mu\text{A}$ |
| $I_{IL}$ | Input LOW Current            | 0.5  | 0.3  |      | 0.5  | 0.25 |      | 0.5  | 0.2  |      | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $-0.46\text{ V}$  /  $+0.8\text{ V}$ .

6. Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .

**Table 8. 100E SERIES NECL DC CHARACTERISTICS**  $V_{CCx} = 0.0\text{ V}$ ;  $V_{EE} = -5.0\text{ V}$  (Note 7)

| Symbol    | Characteristic               | 0°C   |       |       | 25°C  |       |       | 85°C  |       |       | Unit          |
|-----------|------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
|           |                              | Min   | Typ   | Max   | Min   | Typ   | Max   | Min   | Typ   | Max   |               |
| $I_{EEf}$ | Power Supply Current         |       | 125   | 150   |       | 125   | 150   |       | 140   | 170   | mA            |
| $V_{OH}$  | Output HIGH Voltage (Note 8) | -1025 | -950  | -880  | -1025 | -950  | -880  | -1025 | -950  | -880  | mV            |
| $V_{OL}$  | Output LOW Voltage (Note 8)  | -1810 | -1705 | -1620 | -1810 | -1745 | -1620 | -1810 | -1740 | -1620 | mV            |
| $V_{IH}$  | Input HIGH Voltage           | -1165 | -1025 | -880  | -1165 | -1025 | -880  | -1165 | -1025 | -880  | mV            |
| $V_{IL}$  | Input LOW Voltage            | -1810 | -1645 | -1475 | -1810 | -1645 | -1475 | -1810 | -1645 | -1475 | mV            |
| $I_{IH}$  | Input HIGH Current           |       |       | 150   |       |       | 150   |       |       | 150   | $\mu\text{A}$ |
| $I_{IL}$  | Input LOW Current            | 0.5   | 0.3   |       | 0.5   | 0.25  |       | 0.5   | 0.2   |       | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

7. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $-0.46\text{ V}$  /  $+0.8\text{ V}$ .

8. Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .

# MC10E136, MC100E136

**Table 9. AC CHARACTERISTICS**  $V_{CCx} = 5.0\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  or  $V_{CCx} = 0.0\text{ V}$ ;  $V_{EE} = -5.0\text{ V}$  (Note 9)

| Symbol                               | Characteristic  | 0°C                       |                              |                              | 25°C                      |                              |                              | 85°C                      |                              |                              | Unit |
|--------------------------------------|---|---------------------------|------------------------------|------------------------------|---------------------------|------------------------------|------------------------------|---------------------------|------------------------------|------------------------------|------|
|                                      |   | Min                       | Typ                          | Max                          | Min                       | Typ                          | Max                          | Min                       | Typ                          | Max                          |      |
| $f_{\text{COUNT}}$                   | Maximum Count Frequency   | 550                       | 650                          | –                            | 550                       | 650                          | –                            | 550                       | 650                          | –                            | MHz  |
| $t_{\text{PLH}}$<br>$t_{\text{PHL}}$ | Propagation Delay to Output<br>CLK to Q<br>MR to Q<br>CLK to COUT<br>CLK to CLOUT | 850<br>850<br>800<br>825  | 1150<br>1150<br>1150<br>1150 | 1450<br>1450<br>1300<br>1400 | 850<br>850<br>800<br>825  | 1150<br>1150<br>1150<br>1150 | 1450<br>1450<br>1300<br>1400 | 850<br>850<br>800<br>825  | 1150<br>1150<br>1150<br>1150 | 1450<br>1450<br>1300<br>1400 | ps   |
| $t_s$                                | Setup Time<br>S1, S2<br>D<br>CLIN<br>CIN  | 1000<br>800<br>150<br>800 | 650<br>400<br>0<br>400       | –<br>–<br>–<br>–             | 1000<br>800<br>150<br>800 | 650<br>400<br>0<br>400       | –<br>–<br>–<br>–             | 1000<br>800<br>150<br>800 | 650<br>400<br>0<br>400       | –<br>–<br>–<br>–             | ps   |
| $t_h$                                | Hold Time<br>S1, S2<br>D<br>CLIN<br>CIN   | 150<br>150<br>300<br>150  | –200<br>–250<br>0<br>–250    | –<br>–<br>–<br>–             | 150<br>150<br>300<br>150  | –200<br>–250<br>0<br>–250    | –<br>–<br>–<br>–             | 150<br>150<br>300<br>150  | –200<br>–250<br>0<br>–250    | –<br>–<br>–<br>–             | ps   |
| $t_{\text{RR}}$                      | Reset Recovery Time   | 1000                      | 700                          | –                            | 1000                      | 700                          | –                            | 1000                      | 700                          | –                            | ps   |
| $t_{\text{JITTER}}$                  | Random Clock Jitter   |                           | < 1                          |                              |                           | < 1                          |                              |                           | < 1                          |                              | ps   |
| $t_{\text{PW}}$                      | Minimum Pulse Width<br>CLK, MR  | 700                       | 400                          | –                            | 700                       | 400                          | –                            | 700                       | 400                          | –                            | ps   |
| $t_r$<br>$t_f$                       | Rise/Fall Times 20% - 80%   | 250                       | 425                          | 600                          | 250                       | 425                          | 600                          | 250                       | 425                          | 600                          | ps   |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

9. 10 Series:  $V_{EE}$  can vary  $-0.46\text{ V} / +0.06\text{ V}$ .  
100 Series:  $V_{EE}$  can vary  $-0.46\text{ V} / +0.8\text{ V}$ .

## APPLICATIONS INFORMATION

**Overview**

The MC10E/100E136 is a 6-bit synchronous, presettable, cascadable universal counter. Using the S1 and S2 control pins the user can select between preset, count up, count down and hold count. The master reset pin will reset the internal counter, and set the  $\overline{\text{COUT}}$ ,  $\overline{\text{CLOUT}}$ , and  $\overline{\text{CLIN}}$  flip-flops. Unlike previous 136 type counters the carry out outputs will go to a high state during the preset operation. In addition since the carry out outputs are registered they will not go low if terminal count is loaded into the register. The look-ahead-carry out output functions similarly.

Note from the schematic the use of the master information from the least significant bits for control of the two carry out functions. This architecture not only reduces the carry out delay, but is essential to incorporate the registered carry out functions. In addition to being faster, because these functions are registered the resulting carry out signals are stable and glitch free.

**Cascading Multiple E136 Devices**

Many applications require counters significantly larger than the 6 bits available with the E136. For these applications several E136 devices can be cascaded to increase the bit width of the counter to meet the needs of the application.

In the past cascading several 136 type universal counters necessarily impacted the maximum count frequency of the resulting counter chain. This performance impact was the

result of the terminal count signal of the lower order counters having to ripple through the entire counter chain. As a result past counters of this type were not widely used in large bit counter applications.

An alternative counter architecture similar to the E016 binary counter was implemented to alleviate the need to ripple propagate the terminal count signal. Unfortunately these types of counters require external gating for cascading designs of more than two devices. In addition to requiring additional components, these external gates limit the cascaded count frequency to a value less than the free running count frequency of a single counter. Although there is a performance impact with this type of architecture it is minor compared to the impact of the ripple propagate designs. As a result the E016 type counters have been used extensively in applications requiring very high speed, wide bit width synchronous counters.

ON Semiconductor has incorporated several improvements to past universal counter designs in the E136 universal counter. These enhancements make the E136 the unparalleled leader in its class. With the addition of look-ahead-carry features on the terminal count signal, very large counter chains can be designed which function at very nearly the same clock frequency as a single free running device. More importantly these counter chains require no external gating. Figure 1 below illustrates the interconnect scheme for using the look-ahead-carry features of the E136 counter.

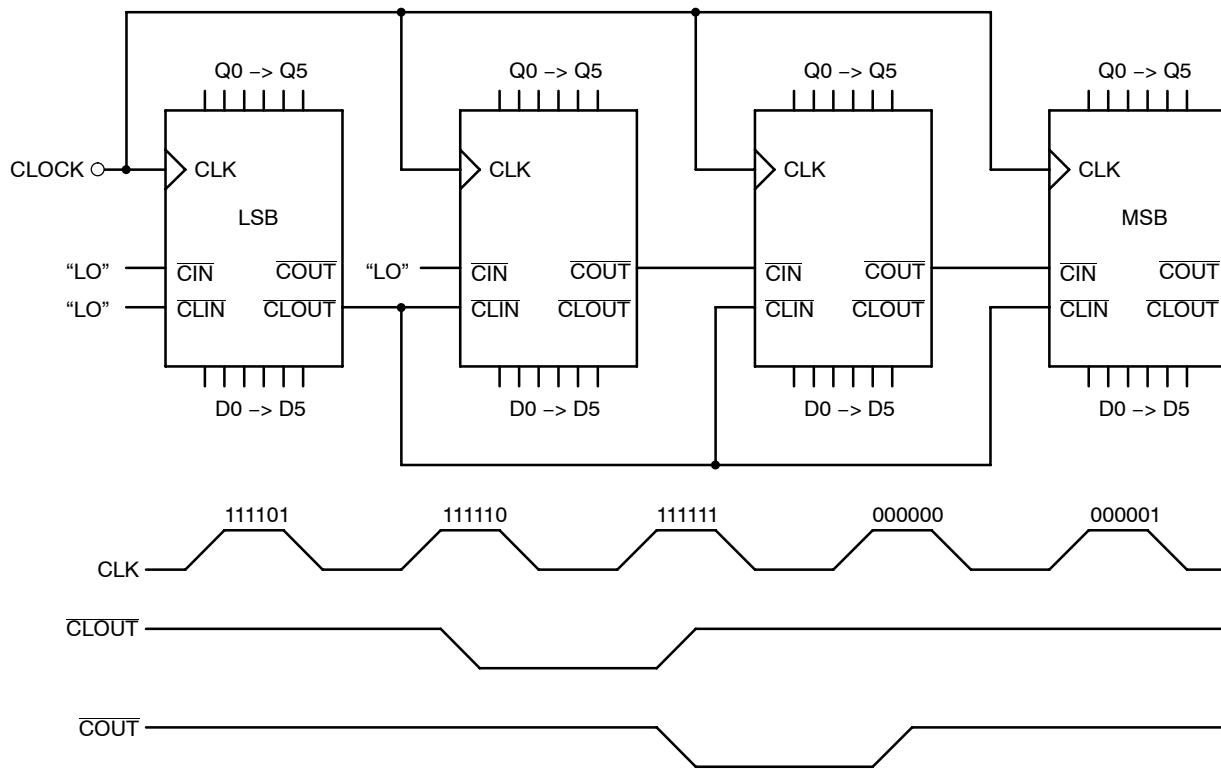


Figure 3. 24-bit Cascaded E136 Counter

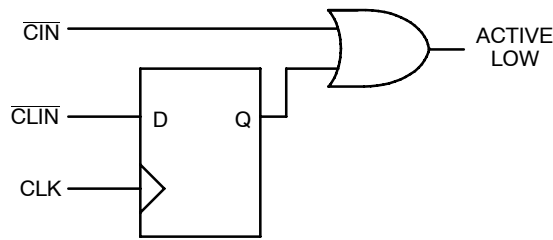


Figure 4. Look-Ahead-Carry Input Structure

Note from the waveforms that the look-ahead-carry output ( $\overline{\text{CLOUT}}$ ) pulses low one clock pulse before the counter reaches terminal count. Also note that both  $\overline{\text{CLOUT}}$  and the carry out pin ( $\overline{\text{COUT}}$ ) of the device pulse low for only one clock period. The input structure for look-ahead-carry in ( $\overline{\text{CLIN}}$ ) and carry in ( $\overline{\text{CIN}}$ ) is pictured in Figure 2.

The  $\overline{\text{CLIN}}$  input is registered and then ORed with the  $\overline{\text{CIN}}$  input. From the truth table one can see that both the  $\overline{\text{CIN}}$  and the  $\overline{\text{CLIN}}$  inputs must be in a LOW state for the E136 to be enabled to count (either count up or count down). The  $\overline{\text{CLIN}}$  inputs are driven by the  $\overline{\text{CLOUT}}$  output of the lowest order E136 and therefore are only asserted for a single clock period. Since the  $\overline{\text{CLIN}}$  input is registered it must be asserted one clock period prior to the  $\overline{\text{CIN}}$  input.

If the counter previous to a given counter is at terminal count its  $\overline{\text{COUT}}$  output and thus the  $\overline{\text{CIN}}$  input of the given counter will be in the "LOW" state. This signals the given counter that it will need to count one upon the next terminal count of the least significant counter (LSC). The  $\overline{\text{CLOUT}}$  output of the LSC will pulse low one clock period before it reaches terminal count. This  $\overline{\text{CLOUT}}$  signal will be clocked into the  $\overline{\text{CLIN}}$  input of the higher order counters on the following positive clock transition. Since both  $\overline{\text{CIN}}$  and  $\overline{\text{CLIN}}$  are in the LOW state the next clock pulse will cause the least significant counter to roll over and all higher order counters, if signaled by their  $\overline{\text{CIN}}$  inputs, to count by one.

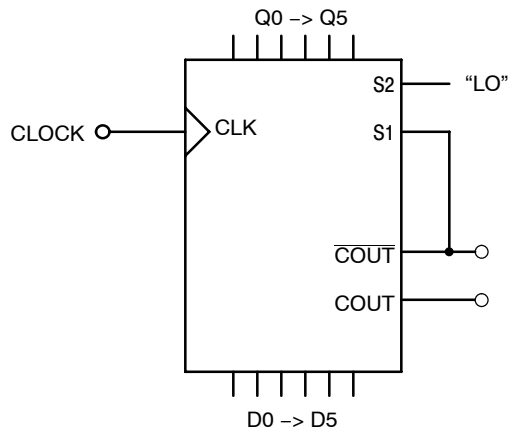


Figure 5. 6-bit Programmable Divider

During the clock pulse in which the higher order counter is counting by one the  $\overline{\text{CLIN}}$  is clocking in the high signal

presented by the  $\overline{\text{CLOUT}}$  of the LSC. The  $\overline{\text{CIN}}$ 's in the higher order counter will ripple propagate through the chain to update the count status for the next occurrence of terminal count on the LSC. This ripple propagation will not affect the count frequency as it has  $2^6-1$  or 63 clock pulses to ripple through without affecting the count operation of the chain.

The only limiting factor which could reduce the count frequency of the chain as compared to a free running single device will be the setup time of the  $\overline{\text{CLIN}}$  input. This limit will consist of the CLK to  $\overline{\text{CLOUT}}$  delay of the E136 plus the  $\overline{\text{CLIN}}$  setup time plus any path length differences between the  $\overline{\text{CLOUT}}$  output and the clock.

#### Programmable Divider

Using external feedback of the  $\overline{\text{COUT}}$  pin, the E136 can be configured as a programmable divider. Figure 3 illustrates the configuration for a 6-bit count down programmable divider. If for some reason a count up divider is preferred the  $\overline{\text{COUT}}$  signal is simply fed back to S2 rather than S1. Examination of the truth table for the E136 shows that when both S1 and S2 are LOW the counter will parallel load on the next positive transition of the clock. If the S2 input is low and the S1 input is high the counter will be in the count down mode and will count towards an all zero state upon successive clock pulses. Knowing this and the operation of the  $\overline{\text{COUT}}$  output it becomes a trivial matter to build programmable dividers.

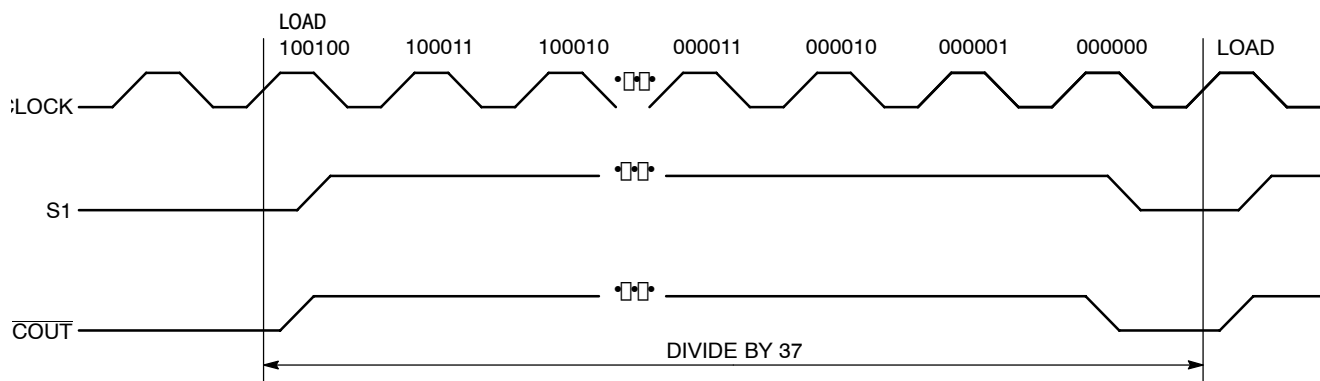
For a programmable divider one wants to load a predesignated number into the counter and count to terminal count. Upon terminal count the counter should automatically reload the divide number. With the architecture shown in Figure 3 when the counter reaches terminal count the  $\overline{\text{COUT}}$  output and thus the S1 input will go LOW, this combined with the low on S2 will cause the counter to load the inputs present on D0-D5. Upon loading the divide value into the counter  $\overline{\text{COUT}}$  will go HIGH as the counter is no longer at terminal count thereby placing the counter back into the count mode.

Table 10. Preset Inputs Versus Divide Ratio

| Divide Ratio | Preset Data Inputs |    |    |    |    |    |
|--------------|--------------------|----|----|----|----|----|
|              | D5                 | D4 | D3 | D2 | D1 | D0 |
| 2            | L                  | L  | L  | L  | L  | H  |
| 3            | L                  | L  | L  | L  | H  | L  |
| 4            | L                  | L  | L  | L  | H  | H  |
| 5            | L                  | L  | L  | H  | L  | L  |
| •            | •                  | •  | •  | •  | •  | •  |
| •            | •                  | •  | •  | •  | •  | •  |
| 36           | H                  | L  | L  | L  | H  | H  |
| 37           | H                  | L  | L  | H  | L  | L  |
| 38           | H                  | L  | L  | H  | L  | H  |
| •            | •                  | •  | •  | •  | •  | •  |
| •            | •                  | •  | •  | •  | •  | •  |
| 62           | H                  | H  | H  | H  | L  | H  |
| 63           | H                  | H  | H  | H  | H  | L  |
| 64           | H                  | H  | H  | H  | H  | H  |



## MC10E136, MC100E136

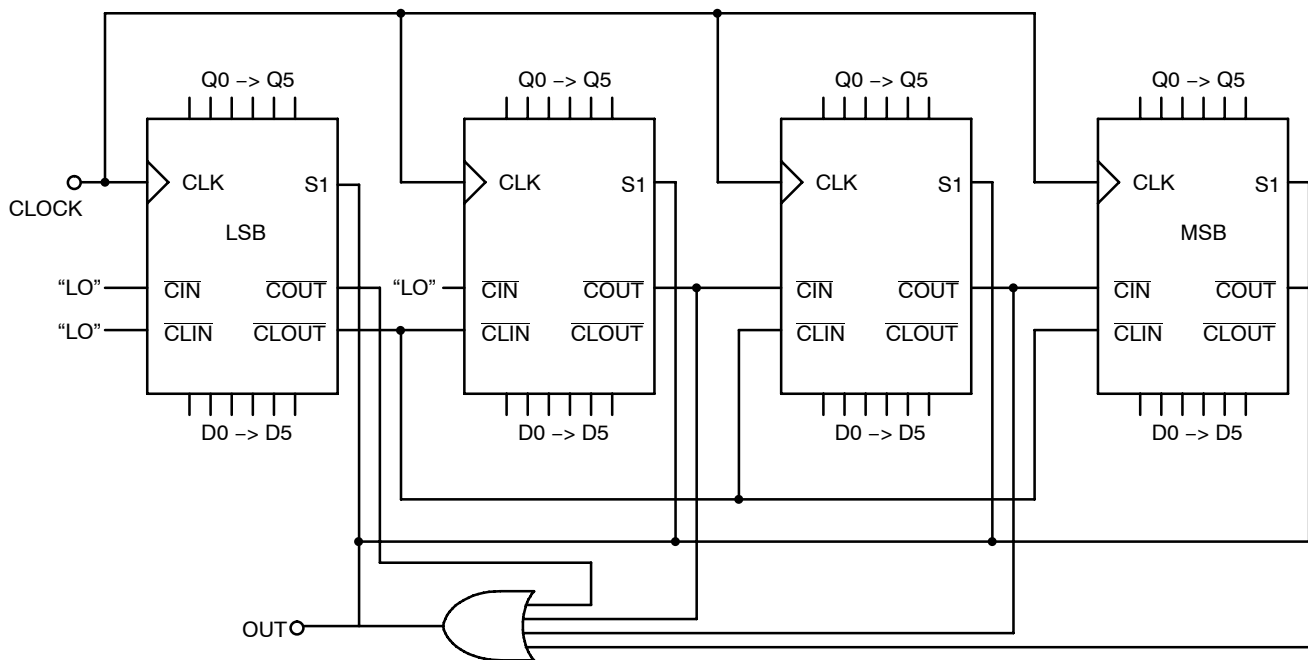


### Figure 6. Programmable Divider Waveforms

The exercise of building a programmable divider then becomes simply determining what value to load into the counter to accomplish the desired division. Since the load operation requires a clock pulse, to divide by N, N-1 must be loaded into the counter. A single E136 device is capable of divide ratios of 2 to 64 inclusive, Table 1 outlines the load values for the various divide ratios. Figure 4 presents the waveforms resulting from a divide by 37 operation. Note that the availability of the COUT complementary output COUT allows the user to choose the polarity of the divide by output.

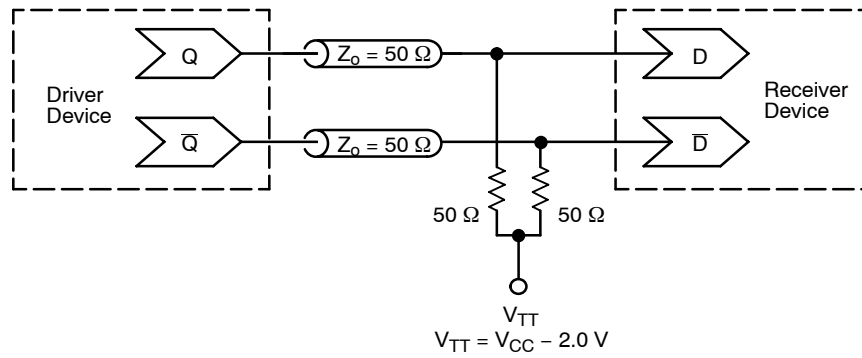
For single device programmable counters the E016 counter is probably a better choice than the E136. The E016 has an internal feedback to control the reloading of the counter, this not only simplifies board design but also will result in a faster maximum count frequency.

For programmable dividers of larger than 8 bits the superiority of the E016 diminishes, and in fact for very wide dividers the E136 will provide the capability of a faster count frequency. This potential is a result of the cascading features mentioned previously in this document. Figure 5 shows the architecture of a 24-bit programmable divider implemented using E136 counters. Note the need for one external gate to control the loading of the entire counter chain. An ideal device for the external gating of this architecture would be the 4-input OR function in the 8-lead SOIC ECLinPS Lite™ family. However the final decision as to what device to use for the external gating requires a balancing of performance needs, cost and available board space. Note that because of the need for external gating the maximum count frequency of a given sized programmable divider will be less than that of a single cascaded counter.



### Figure 7. 24-bit Programmable Divider Architecture

## MC10E136, MC100E136



**Figure 8. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note AND8020/D – Termination of ECL Logic Devices.)

### ORDERING INFORMATION

| Device         | Package              | Shipping <sup>†</sup> |
|----------------|----------------------|-----------------------|
| MC10E136FN     | PLCC-28              | 37 Units / Rail       |
| MC10E136FNG    | PLCC-28<br>(Pb-Free) | 37 Units / Rail       |
| MC10E136FNR2   | PLCC-28              | 500 / Tape & Reel     |
| MC10E136FNR2G  | PLCC-28<br>(Pb-Free) | 500 / Tape & Reel     |
| MC100E136FN    | PLCC-28              | 37 Units / Rail       |
| MC100E136FNG   | PLCC-28<br>(Pb-Free) | 37 Units / Rail       |
| MC100E136FNR2  | PLCC-28              | 500 / Tape & Reel     |
| MC100E136FNR2G | PLCC-28<br>(Pb-Free) | 500 / Tape & Reel     |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

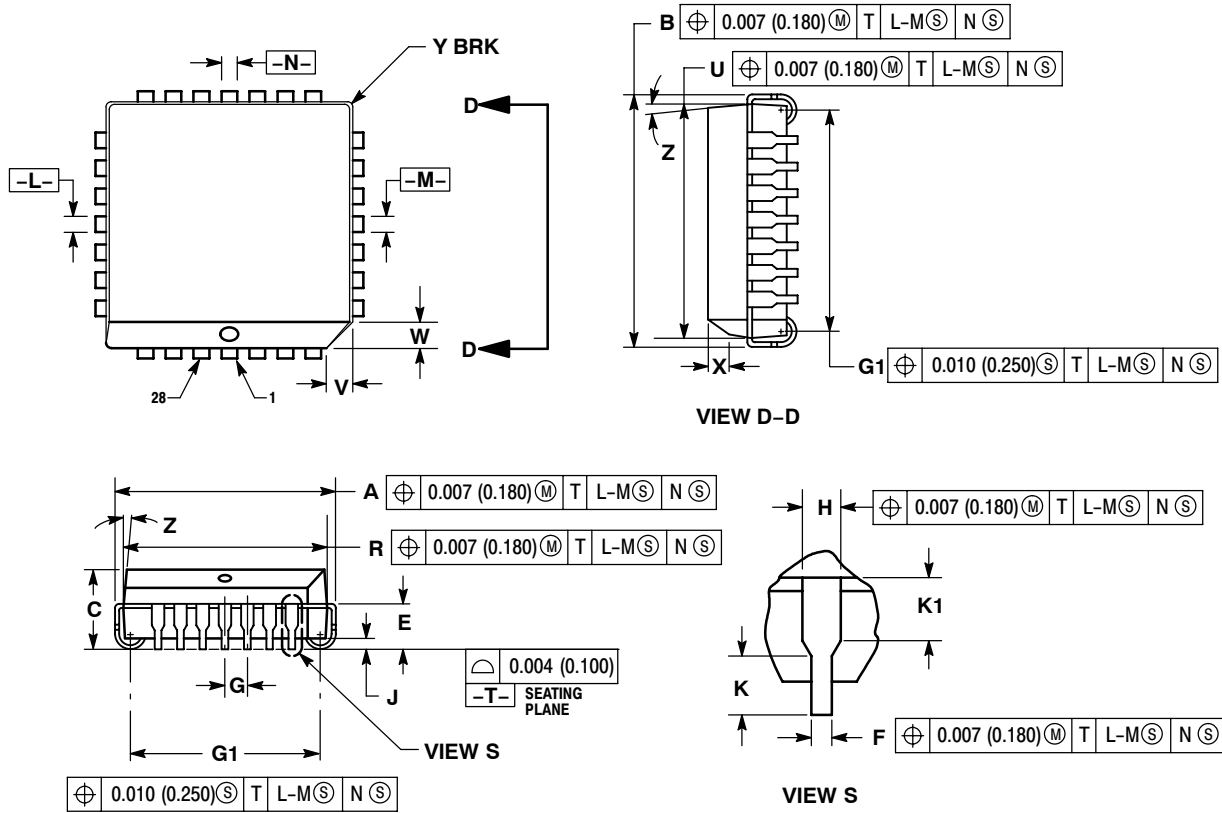
### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

# MC10E136, MC100E136


## PACKAGE DIMENSIONS

PLCC-28  
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PLASTIC PLCC PACKAGE  
CASE 776-02  
ISSUE E



# MC10E136, MC100E136

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