NCV5106A, NCV5106B

High Voltage, High and Low Side Driver

The NCV5106 is a high voltage gate driver IC providing two outputs for direct drive of 2 N−channel power MOSFETs or IGBTs arranged in a half−bridge configuration version B (version B on demand only) or any other high−side + low−side configuration version A.

It uses the bootstrap technique to ensure a proper drive of the high−side power switch. The driver works with 2 independent inputs.

Features

- High Voltage Range: Up to 600 V
- dV/dt Immunity ±50 V/nsec
- Negative Current Injection Characterized Over the Temperature Range
- Gate Drive Supply Range from 10 V to 20 V
- High and Low Drive Outputs
- Output Source / Sink Current Capability 250 mA / 500 mA
- 3.3 V and 5 V Input Logic Compatible
- Up to V_{CC} Swing on Input Pins
- Extended Allowable Negative Bridge Pin Voltage Swing to −10 V for Signal Propagation
- Matched Propagation Delays Between Both Channels
- Outputs in Phase with the Inputs
- Independent Logic Inputs to Accommodate All Topologies (Version A)
- Cross Conduction Protection with 100 ns Internal Fixed Dead Time (Version B − on demand only)
- Under V_{CC} LockOut (UVLO) for Both Channels
- Pin−to−Pin Compatible with Industry Standards
- These are Pb−Free Devices

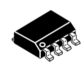
Typical Applications

- Half−Bridge Power Converters
- Any Complementary Drive Converters (Asymmetrical Half−Bridge, Active Clamp) (A Version Only).
- Full−Bridge Converters

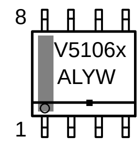
ON Semiconductor®

www.onsemi.com

MARKING DIAGRAMS

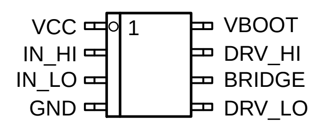


SOIC−8
D SUFFIX
CASE 751



V5106x	= Specific Device Code
x	= A or B version
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

PINOUT INFORMATION



SOIC−8

ORDERING INFORMATION

See detailed ordering and shipping information on page 16 of this data sheet.

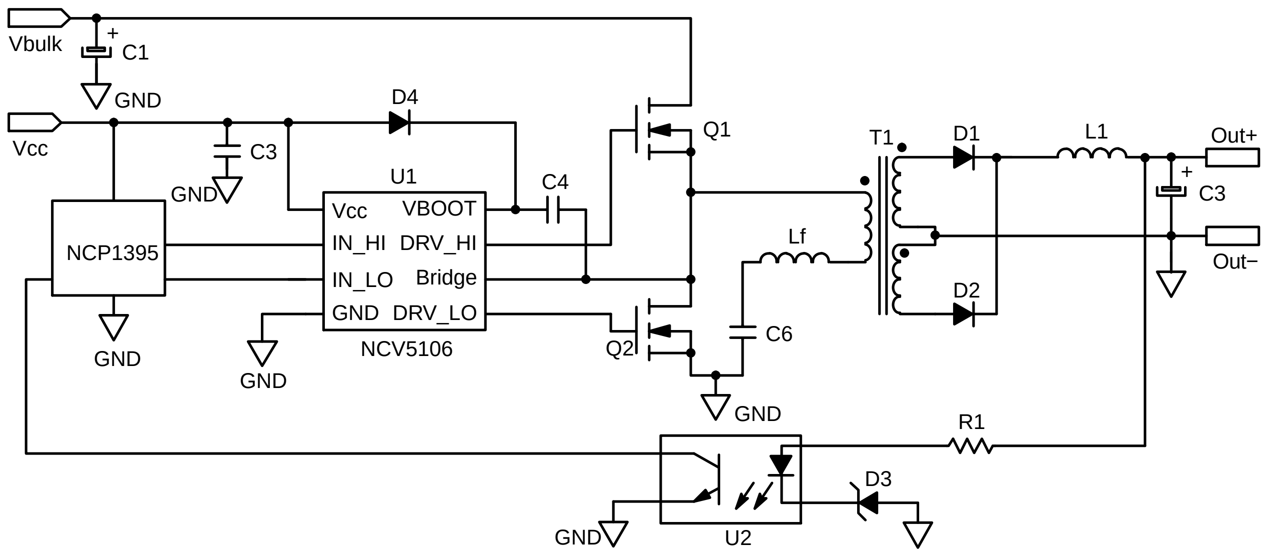


Figure 1. Typical Application Resonant Converter (LLC type)

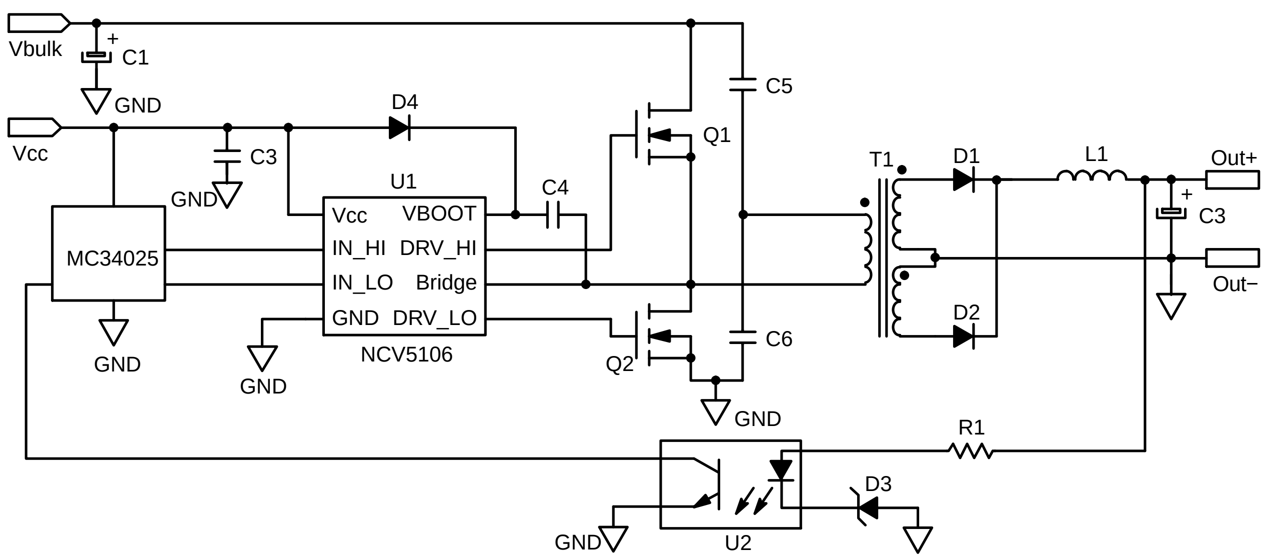


Figure 2. Typical Application Half Bridge Converter

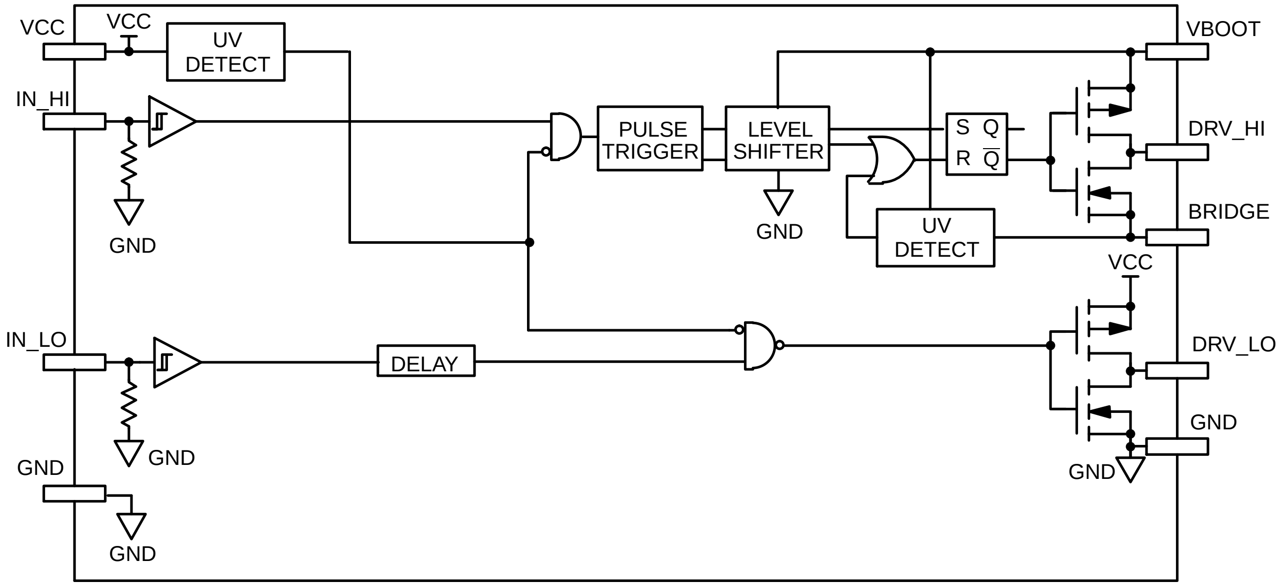


Figure 3. Detailed Block Diagram: Version A

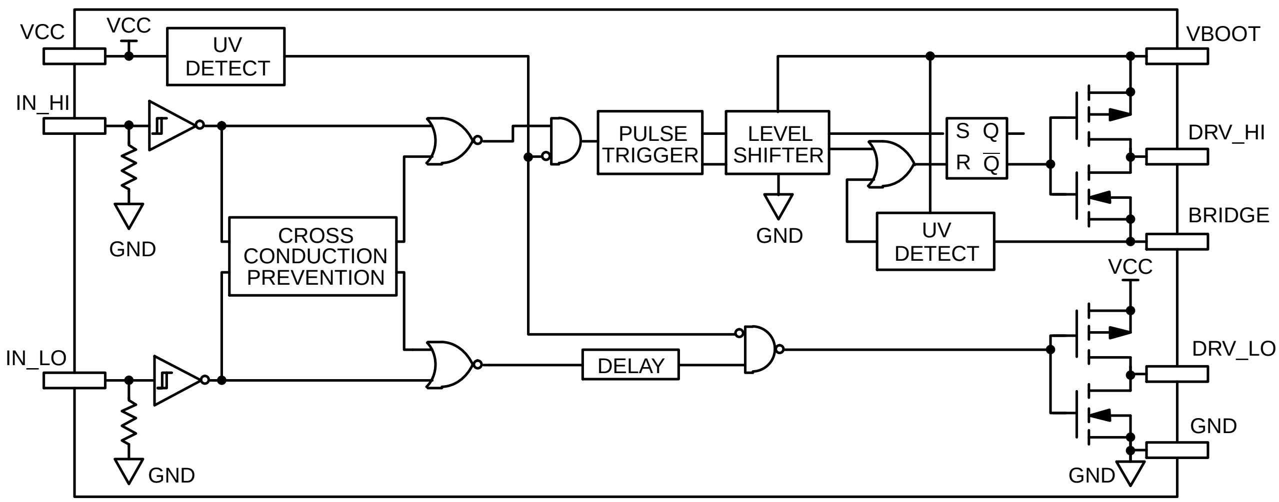


Figure 4. Detailed Block Diagram: Version B

PIN DESCRIPTION

Pin Name	Description
IN_HI	Logic Input for High Side Driver Output in Phase
IN_LO	Logic Input for Low Side Driver Output in Phase
GND	Ground
DRV_LO	Low Side Gate Drive Output
V_{CC}	Low Side and Main Power Supply
V_{BOOT}	Bootstrap Power Supply
DRV_HI	High Side Gate Drive Output
BRIDGE	Bootstrap Return or High Side Floating Supply Return
NC	Removed for creepage distance (DFN package only)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
V_{CC}	Main power supply voltage	−0.3 to 20	V
$V_{CC\_transient}$	Main transient power supply voltage: IV_{CC_max} = 5 mA during 10 ms	23	V
V_{BRIDGE}	VHV: High Voltage BRIDGE pin	−1 to 600	V
V_{BRIDGE}	Allowable Negative Bridge Pin Voltage for IN_LO Signal Propagation to DRV_LO (see characterization curves for detailed results)	−10	V
V_{BOOT}–V_{BRIDGE}	VHV: Floating supply voltage	−0.3 to 20	V
V_{DRV_HI}	VHV: High side output voltage	V_{BRIDGE} − 0.3 to V_{BOOT} + 0.3	V
V_{DRV_LO}	Low side output voltage	−0.3 to V_{CC} + 0.3	V
dV_{BRIDGE}/dt	Allowable output slew rate	50	V/ns
V_{IN_XX}	Inputs IN_HI, IN_LO	−1.0 to V_{CC} + 0.3	V
	ESD Capability: − HBM Model (all pins) − CDM Model	 750 1000	 V V
	Latch up capability per JEDEC JESD78		
$R_{\theta JA}$	Power dissipation and Thermal characteristics SO−8: Thermal Resistance, Junction−to−Air	 178	°C/W
T_{ST}	Storage Temperature Range	−55 to +150	°C
T_{J_max}	Maximum Operating Junction Temperature	+150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTIC (V_{CC} = V_{boot} = 15 V, V_{GND} = V_{bridge}, −40°C < T_J < 125°C, Outputs loaded with 1 nF)

Rating	Symbol	T_J −40°C to 125°C Min	Typ	Max	Units
OUTPUT SECTION					
Output high short circuit pulsed current V_{DRV} = 0 V, PW ≤ 10 μs (Note 1)	$I_{DRVsource}$	−	250	−	mA
Output low short circuit pulsed current V_{DRV} = V_{CC}, PW ≤ 10 μs (Note 1)	$I_{DRVsink}$	−	500	−	mA
Output resistor (Typical value @ 25°C) Source	R_{OH}	−	30	60	Ω
Output resistor (Typical value @ 25°C) Sink	R_{OL}	−	10	20	Ω
High level output voltage, V_{BIAS}−V_{DRV_XX} @ I_{DRV_XX} = 20 mA	V_{DRV_H}	−	0.7	1.6	V
Low level output voltage V_{DRV_XX} @ I_{DRV_XX} = 20 mA	V_{DRV_L}	−	0.2	0.6	V
DYNAMIC OUTPUT SECTION					
Turn−on propagation delay (Vbridge = 0 V)	t_{ON}	−	100	170	ns
Turn−off propagation delay (Vbridge = 0 V or 50 V) (Note 2)	t_{OFF}	−	100	170	ns
Output voltage rise time (from 10% to 90% @ V_{CC} = 15 V) with 1 nF load	tr	−	85	160	ns
Output voltage fall time (from 90% to 10% @V_{CC} = 15 V) with 1 nF load	tf	−	35	75	ns
Propagation delay matching between the High side and the Low side @ 25°C (Note 3)	Δt	−	20	35	ns
Internal fixed dead time (only valid for B version) (Note 4)	DT	65	100	190	ns
Minimum input width that changes the output	t_{PW1}	−	−	50	ns
Maximum input width that does not change the output	t_{PW2}	15	−	−	ns
INPUT SECTION					
Low level input voltage threshold	V_{IN}	−	−	0.8	V
Input pull−down resistor (V_{IN} < 0.5 V)	R_{IN}	−	200	−	kΩ
High level input voltage threshold	V_{IN}	2.3	−	−	V
Logic “1” input bias current @ V_{IN_XX} = 5 V @ 25°C	I_{IN+}	−	5	25	μA
Logic “0” input bias current @ V_{IN_XX} = 0 V @ 25°C	I_{IN-}	−	−	2.0	μA
SUPPLY SECTION					
V_{CC} UV Start−up voltage threshold	V_{CC}_stup	8.0	8.9	9.9	V
V_{CC} UV Shut−down voltage threshold	V_{CC}_shtdwn	7.3	8.2	9.1	V
Hysteresis on V_{CC}	V_{CC}_hyst	0.3	0.7	−	V
Vboot Start−up voltage threshold reference to bridge pin (Vboot_stup = Vboot − Vbridge)	Vboot_stup	8.0	8.9	9.9	V
Vboot UV Shut−down voltage threshold	Vboot_shtdwn	7.3	8.2	9.1	V
Hysteresis on Vboot	Vboot_shtdwn	0.3	0.7	−	V
Leakage current on high voltage pins to GND (V_{BOOT} = V_{BRIDGE} = DRV_HI = 600 V)	I_{HV_LEAK}	−	5	40	μA
Consumption in active mode (V_{CC} = Vboot, fsw = 100 kHz and 1 nF load on both driver outputs)	ICC1	−	4	5	mA
Consumption in inhibition mode (V_{CC} = Vboot)	ICC2	−	250	400	μA
V_{CC} current consumption in inhibition mode	ICC3	−	200	−	μA
Vboot current consumption in inhibition mode	ICC4	−	50	−	μA

1. Parameter guaranteed by design.
2. Turn−off propagation delay @ Vbridge = 600 V is guaranteed by design.
3. See characterization curve for Δt parameters variation on the full range temperature.
4. Version B integrates a dead time in order to prevent any cross conduction between DRV_HI and DRV_LO. See timing diagram of Figure 10.
5. Timing diagram definition see: Figure 7, Figure 8 and Figure 9.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

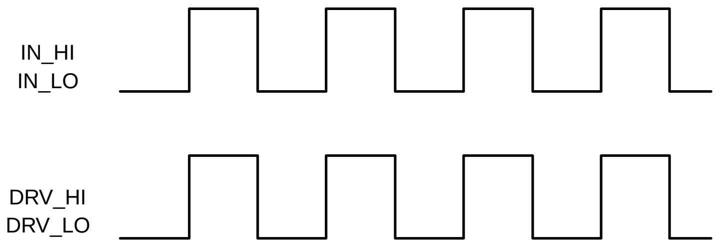


Figure 5. Input/Output Timing Diagram (A Version)

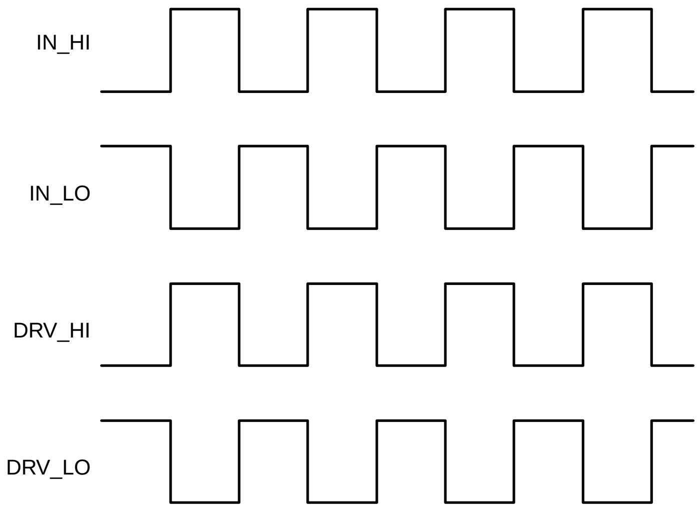


Figure 6. Input/Output Timing Diagram (B Version)

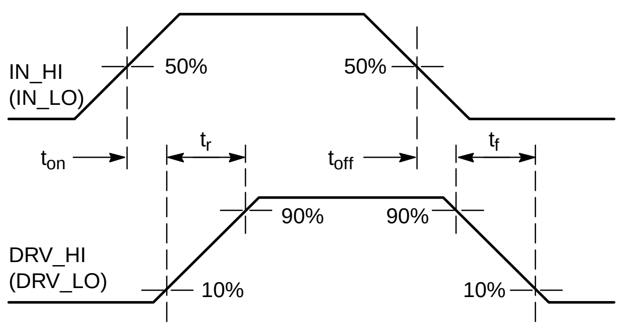


Figure 7. Propagation Delay and Rise / Fall Time Definition

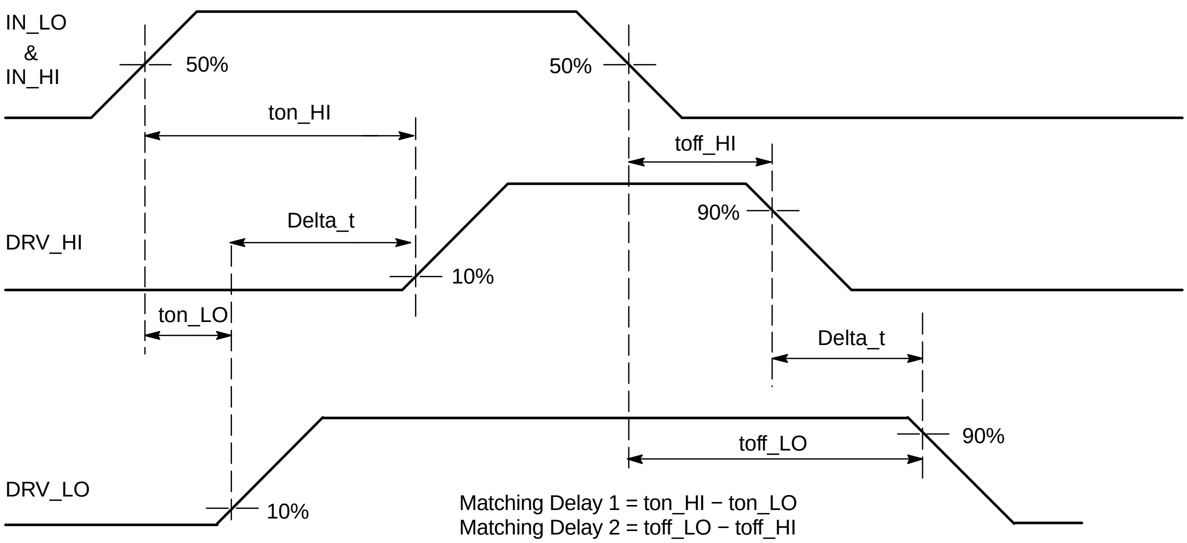


Figure 8. Matching Propagation Delay (A Version)

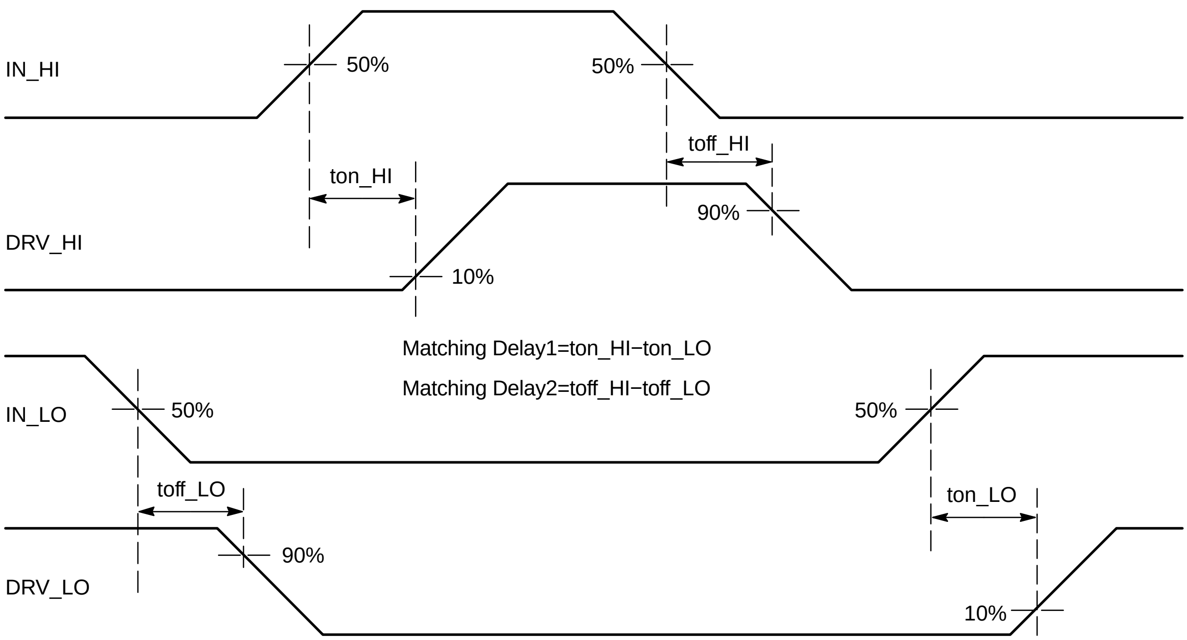


Figure 9. Matching Propagation Delay (B Version)

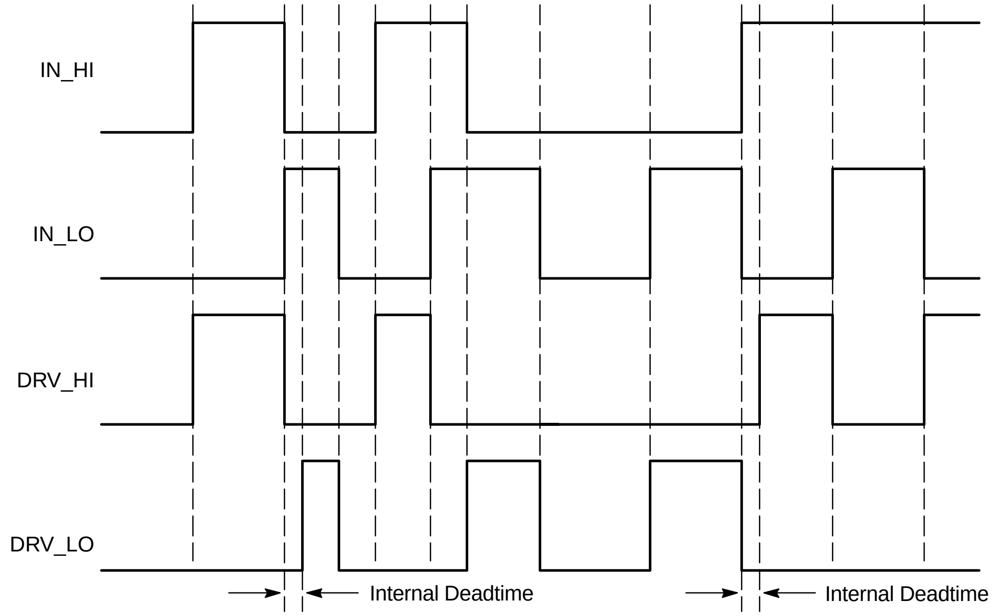


Figure 10. Input/Output Cross Conduction Output Protection Timing Diagram (B Version)

CHARACTERIZATION CURVES

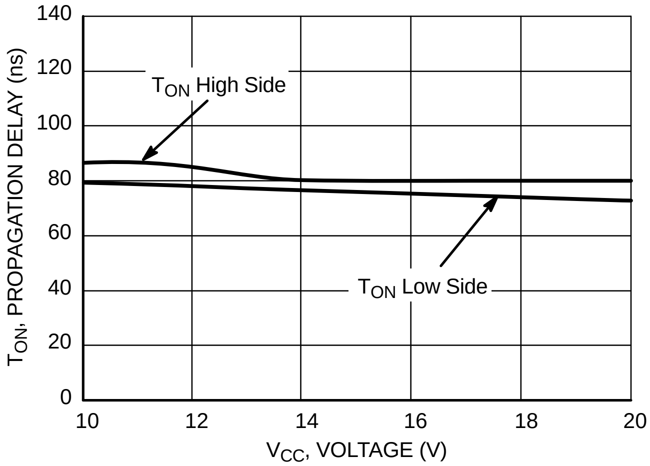


Figure 11. Turn ON Propagation Delay vs. Supply Voltage (V_{CC} = V_{BOOT})

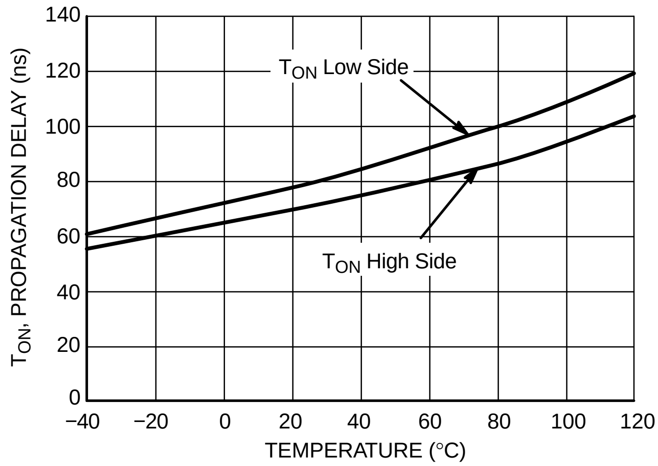


Figure 12. Turn ON Propagation Delay vs. Temperature

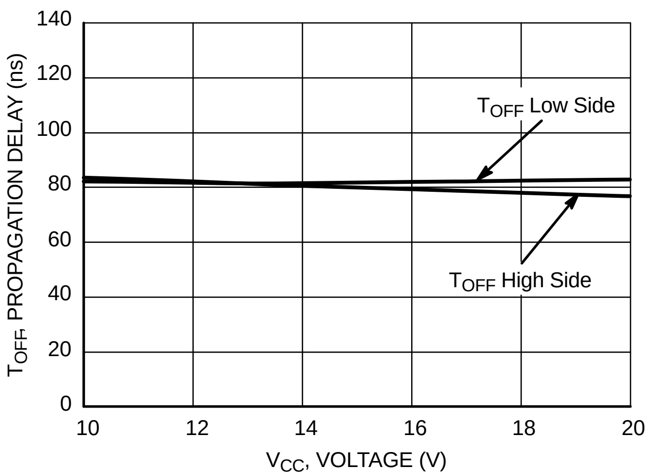


Figure 13. Turn OFF Propagation Delay vs. Supply Voltage (V_{CC} = V_{BOOT})

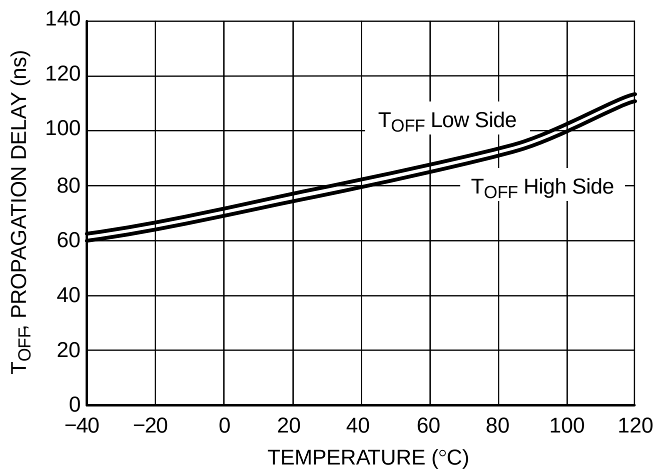


Figure 14. Turn OFF Propagation Delay vs. Temperature

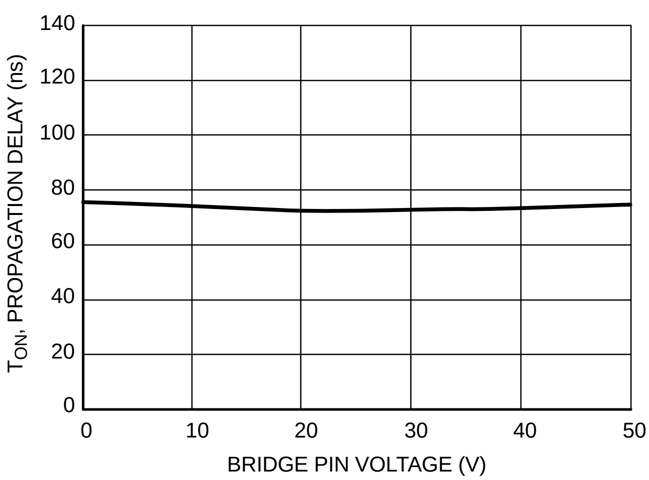


Figure 15. High Side Turn ON Propagation Delay vs. VBRIDGE Voltage

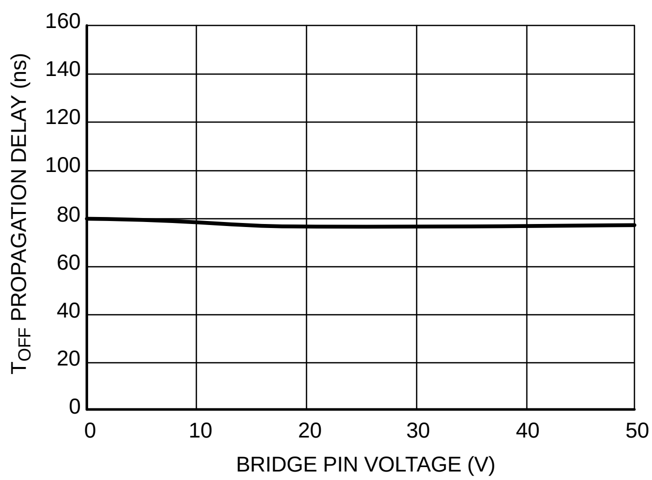


Figure 16. High Side Turn OFF Propagation Delay vs. VBRIDGE Voltage

CHARACTERIZATION CURVES

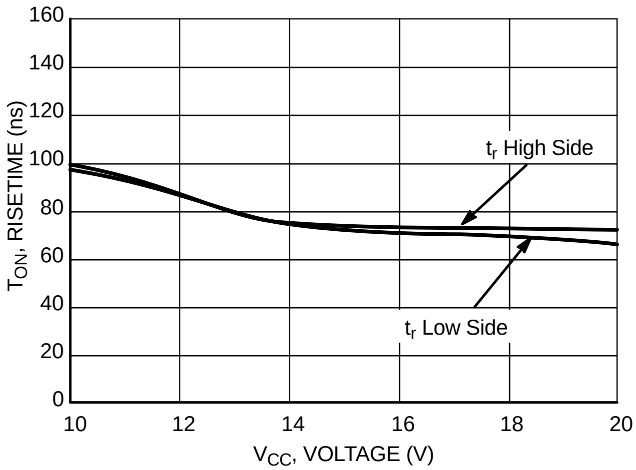


Figure 17. Turn ON Risetime vs. Supply Voltage (V_{CC} = V_{BOOT})

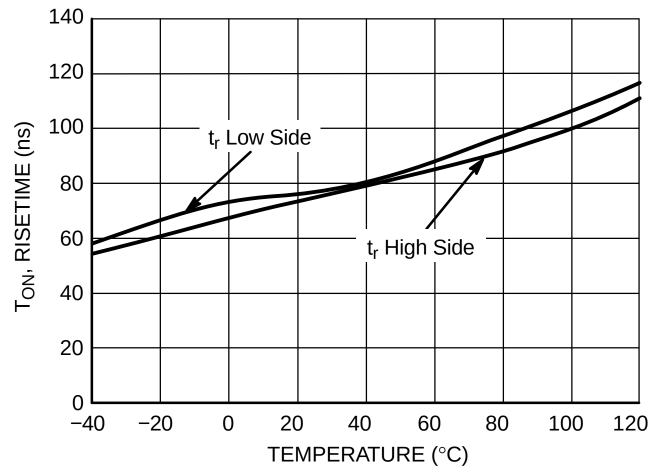


Figure 18. Turn ON Risetime vs. Temperature

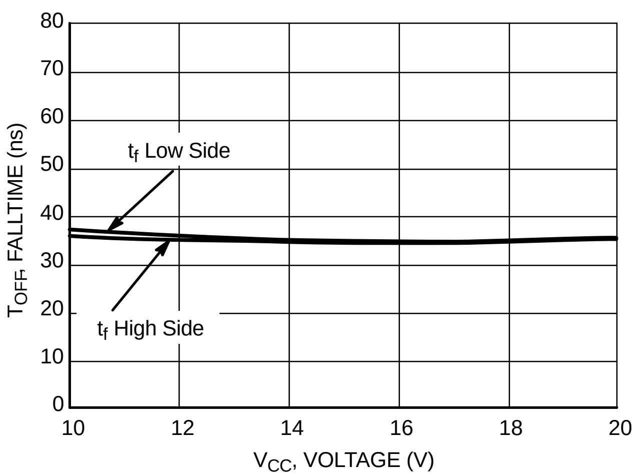


Figure 19. Turn OFF Falltime vs. Supply Voltage (V_{CC} = V_{BOOT})

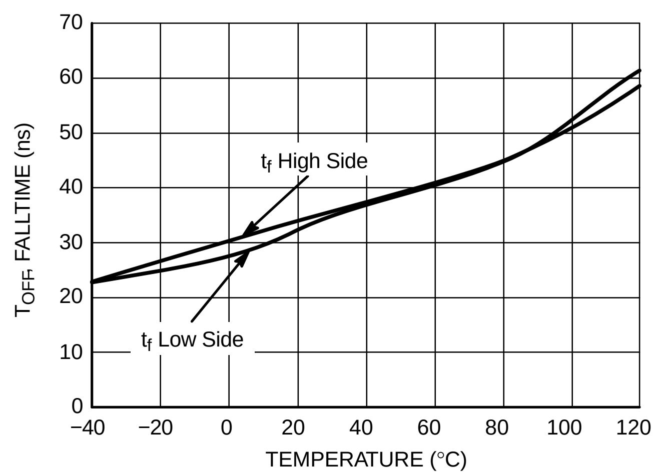


Figure 20. Turn OFF Falltime vs. Temperature

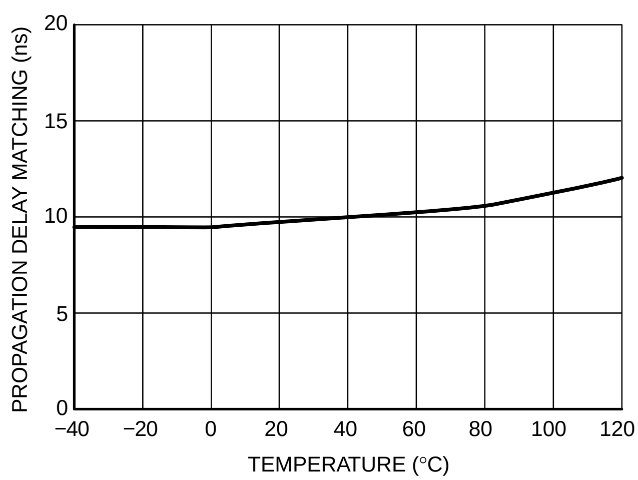


Figure 21. Propagation Delay Matching Between High Side and Low Side Driver vs. Temperature

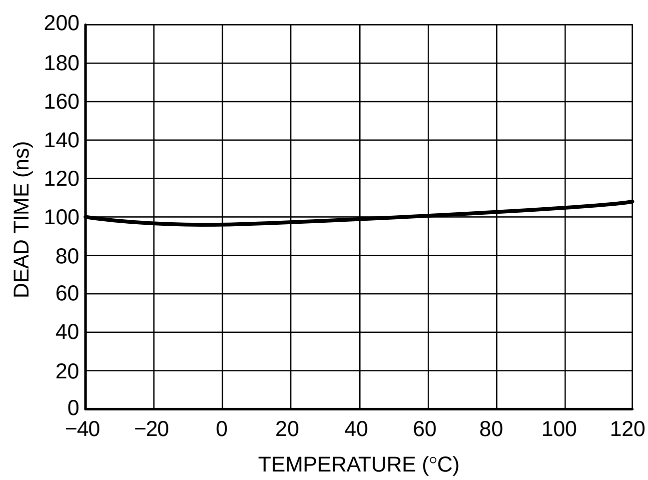


Figure 22. Dead Time vs. Temperature

CHARACTERIZATION CURVES

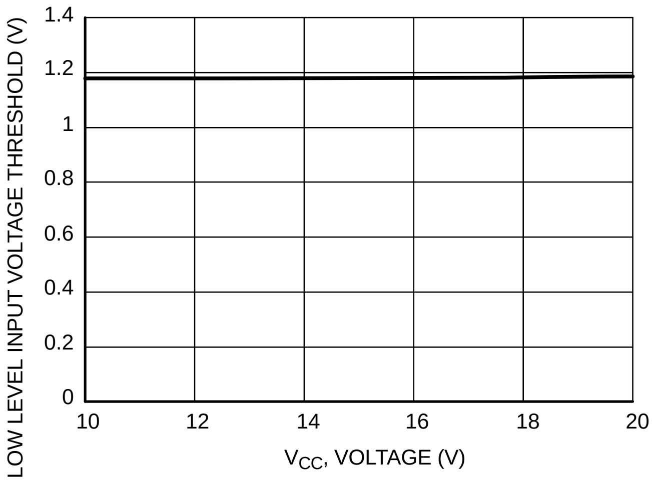


Figure 23. Low Level Input Voltage Threshold vs. Supply Voltage ($V_{CC} = V_{BOOT}$)

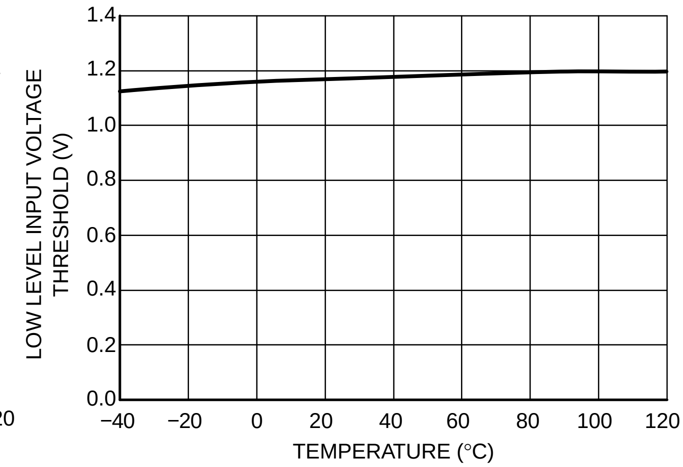


Figure 24. Low Level Input Voltage Threshold vs. Temperature

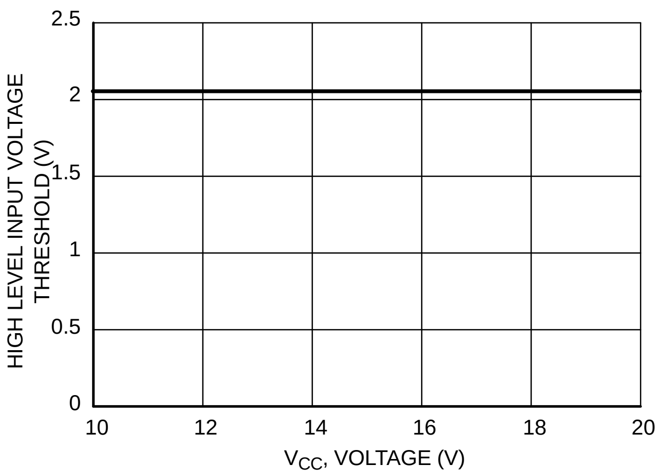


Figure 25. High Level Input Voltage Threshold vs. Supply Voltage ($V_{CC} = V_{BOOT}$)

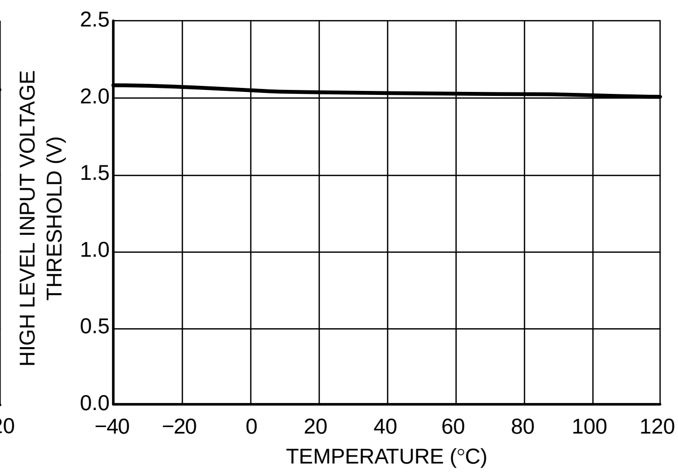


Figure 26. High Level Input Voltage Threshold vs. Temperature

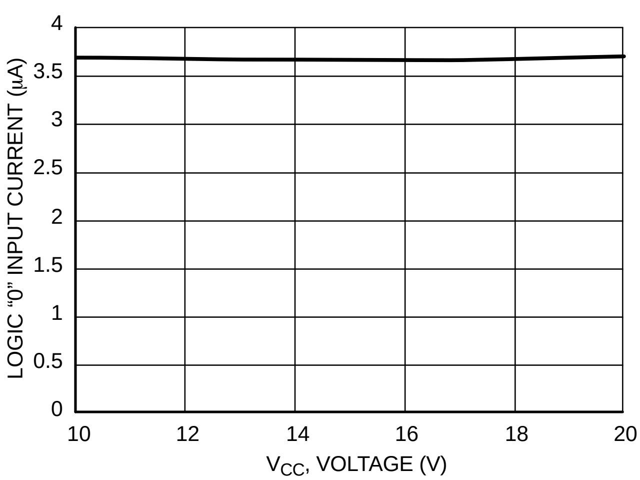


Figure 27. Logic “0” Input Current vs. Supply Voltage ($V_{CC} = V_{BOOT}$)

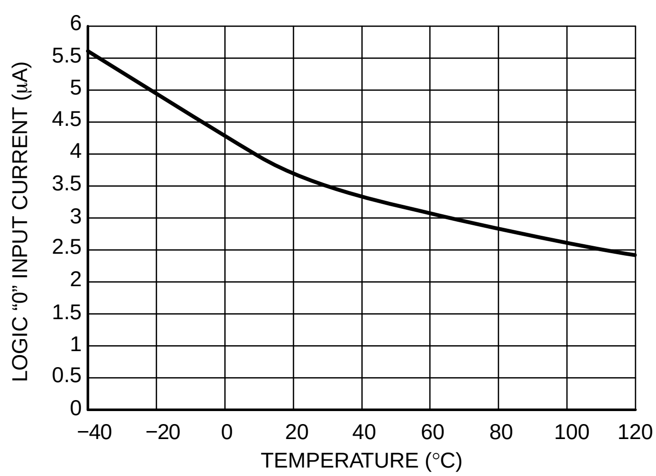


Figure 28. Logic “0” Input Current vs. Temperature

CHARACTERIZATION CURVES

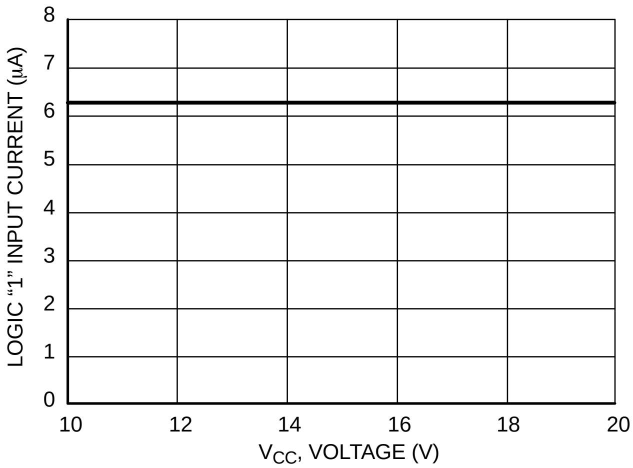


Figure 29. Logic “1” Input Current vs. Supply Voltage (V_{CC} = V_{BOOT})

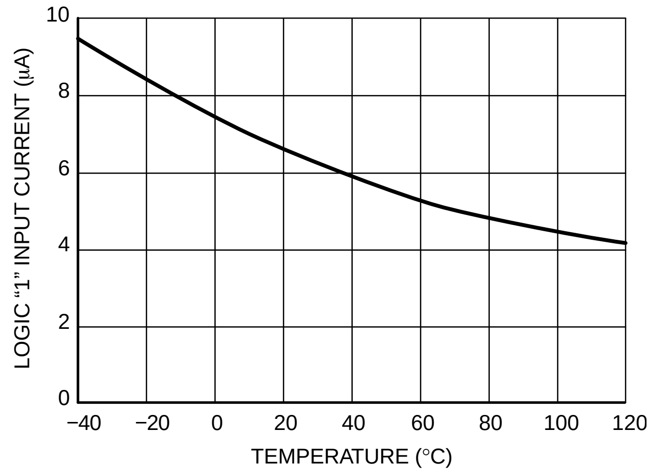


Figure 30. Logic “1” Input Current vs. Temperature

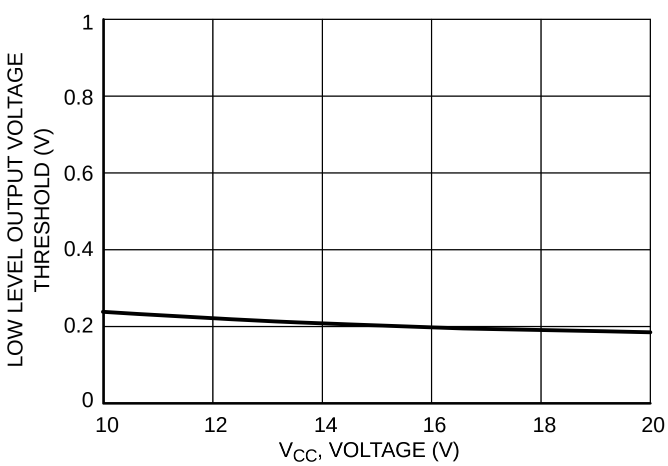


Figure 31. Low Level Output Voltage vs. Supply Voltage (V_{CC} = V_{BOOT})

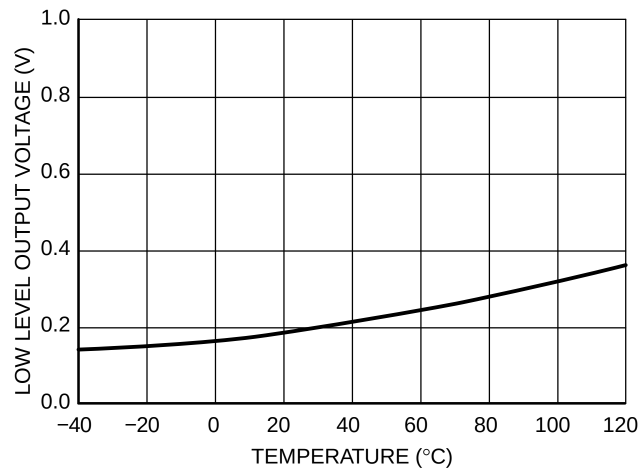


Figure 32. Low Level Output Voltage vs. Temperature

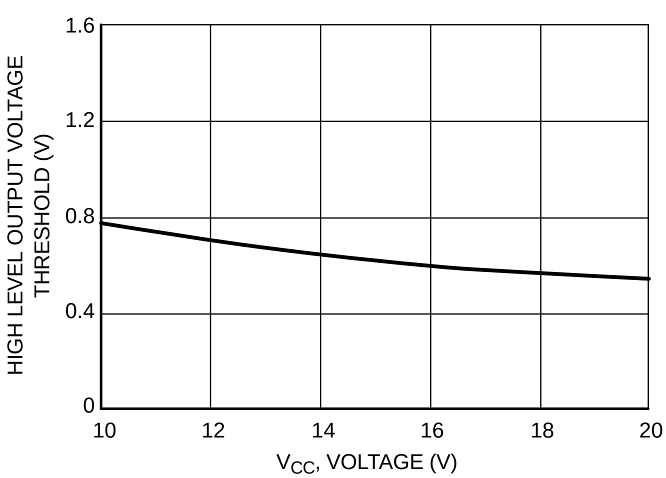


Figure 33. High Level Output Voltage vs. Supply Voltage (V_{CC} = V_{BOOT})

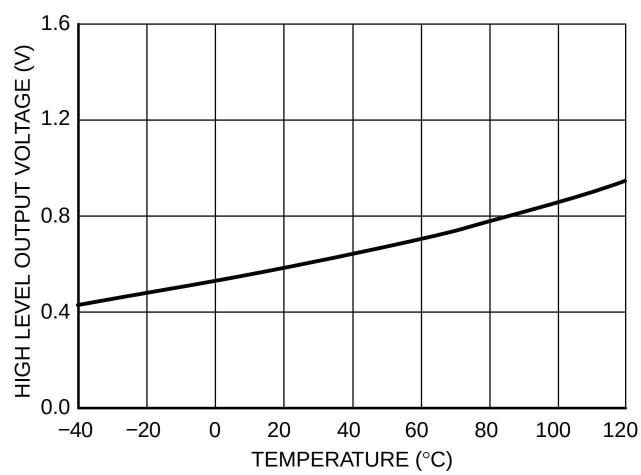


Figure 34. High Level Output Voltage vs. Temperature

CHARACTERIZATION CURVES

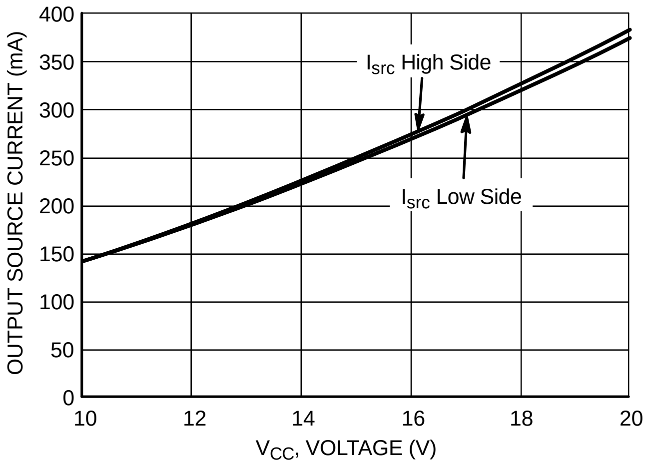


Figure 35. Output Source Current vs. Supply Voltage ($V_{CC} = V_{BOOT}$)

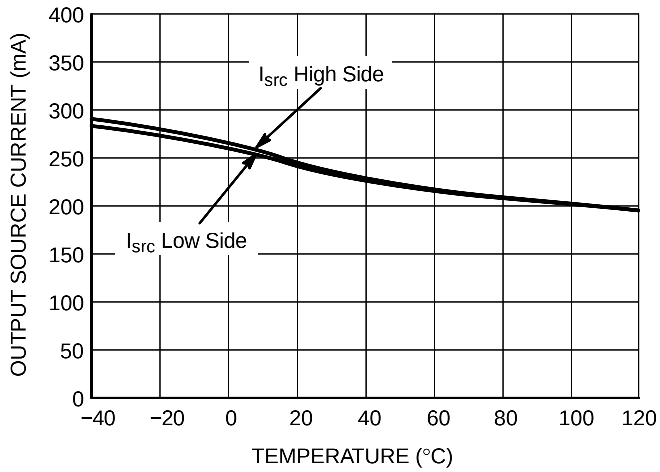


Figure 36. Output Source Current vs. Temperature

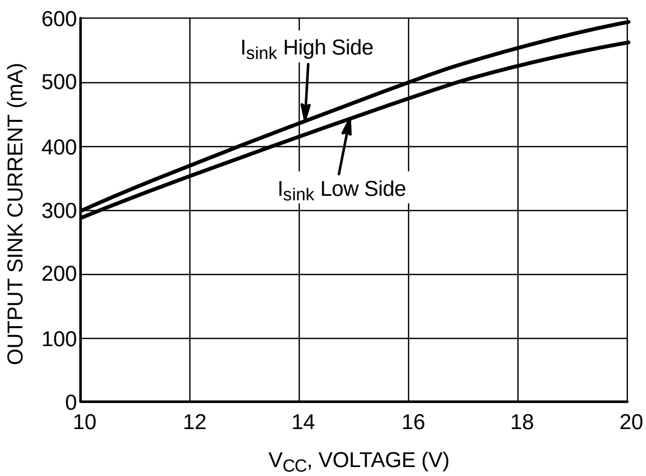


Figure 37. Output Sink Current vs. Supply Voltage ($V_{CC} = V_{BOOT}$)

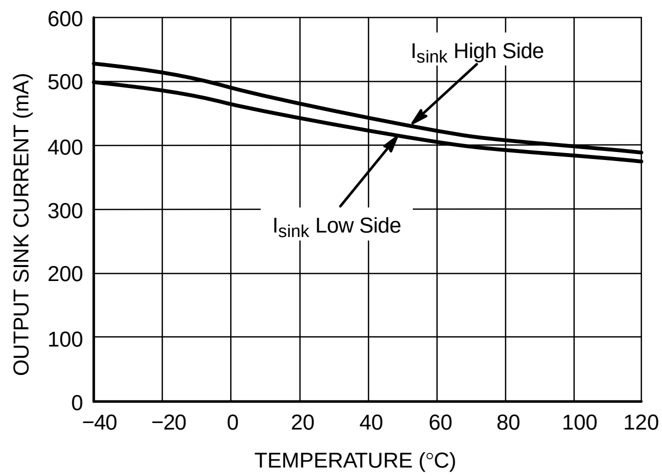


Figure 38. Output Sink Current vs. Temperature

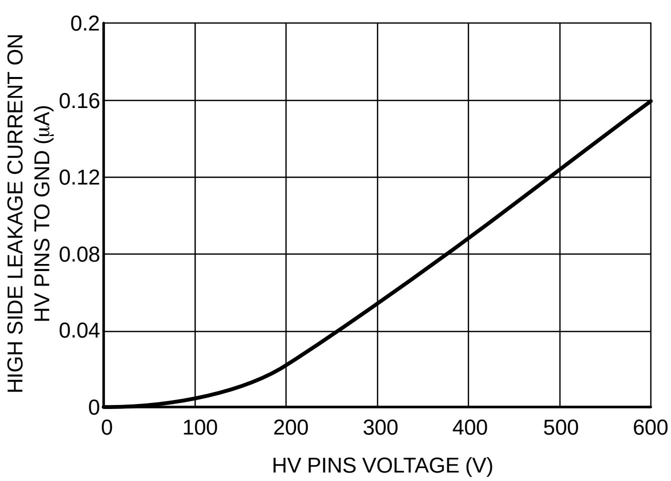


Figure 39. Leakage Current on High Voltage Pins (600 V) to Ground vs. V_{BRIDGE} Voltage ($V_{BRIGDE} = V_{BOOT} = V_{DRV\_HI}$)

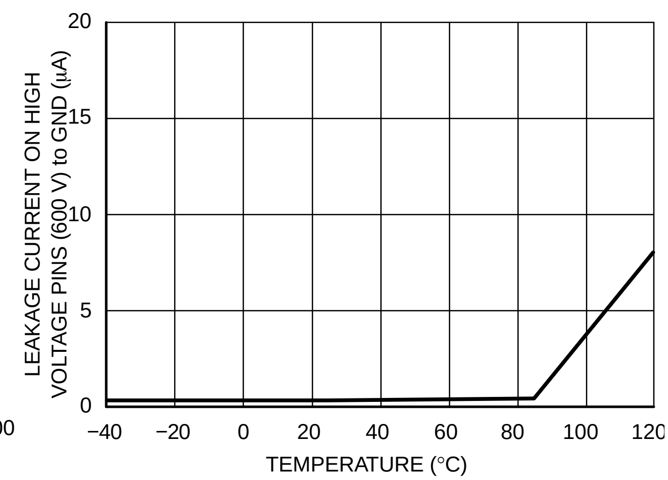


Figure 40. Leakage Current on High Voltage Pins (600 V) to Ground vs. Temperature (VBRIDGE = $V_{BOOT} = V_{DRV\_HI}$ = 600 V)

CHARACTERIZATION CURVES

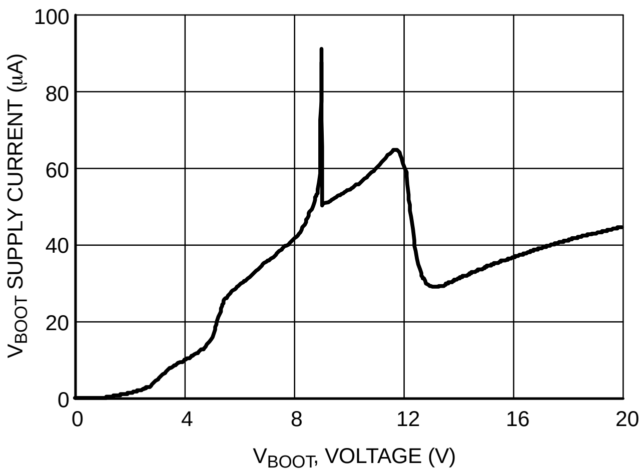


Figure 41. V_{BOOT} Supply Current vs. Bootstrap Supply Voltage

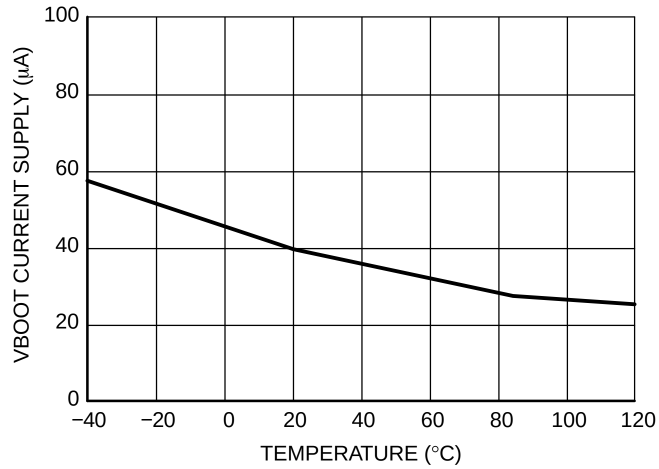


Figure 42. V_{BOOT} Supply Current vs. Temperature

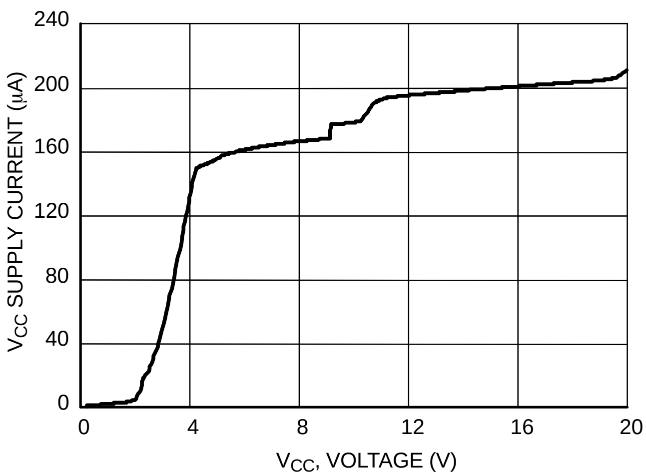


Figure 43. V_{CC} Supply Current vs. V_{CC} Supply Voltage

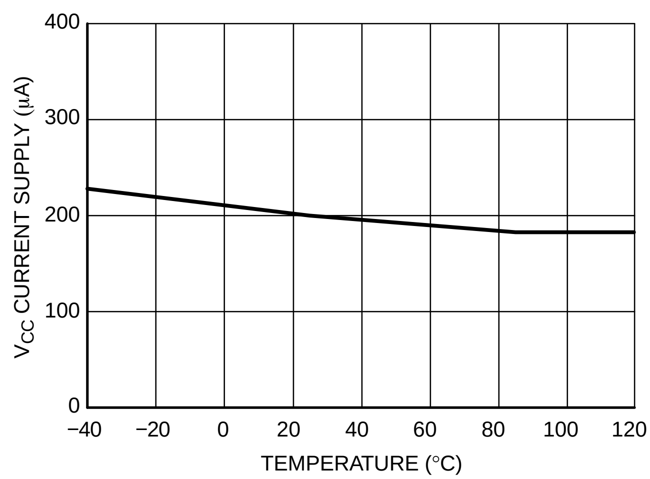


Figure 44. V_{CC} Supply Current vs. Temperature

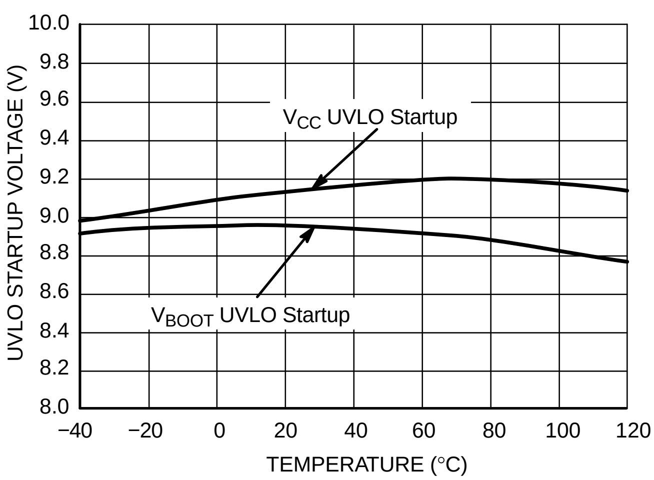


Figure 45. UVLO Startup Voltage vs. Temperature

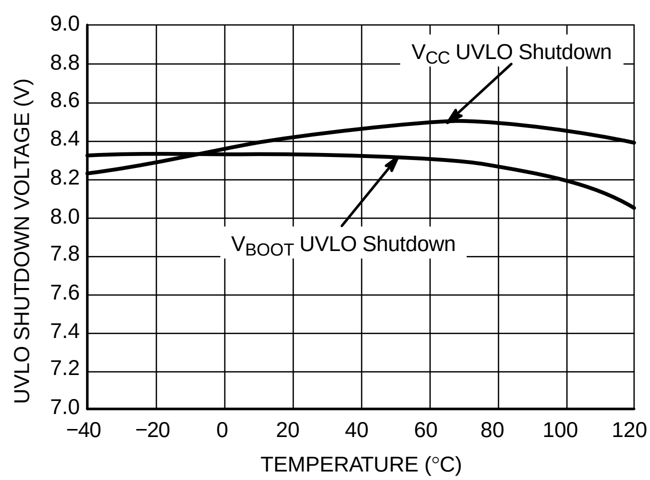


Figure 46. UVLO Shutdown Voltage vs. Temperature

CHARACTERIZATION CURVES

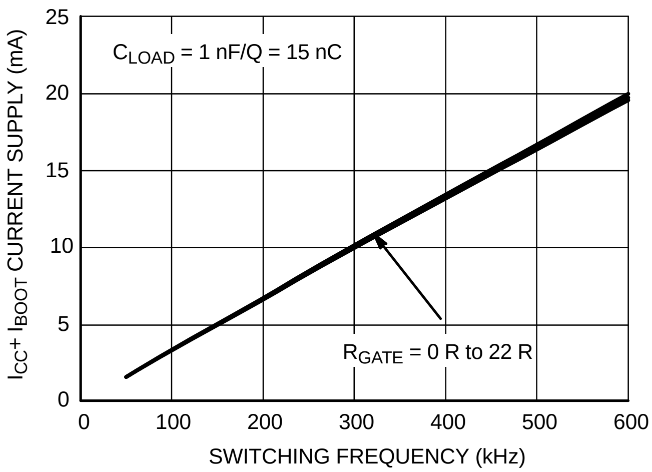


Figure 47. I_{CC1} Consumption vs. Switching Frequency with 15 nC Load on Each Driver @ V_{CC} = 15 V

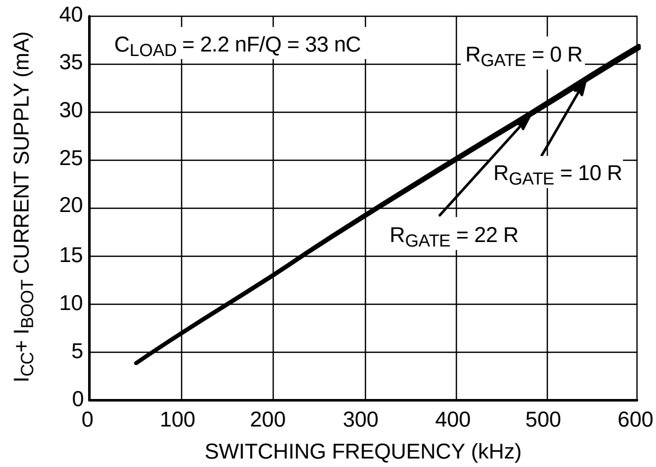


Figure 48. I_{CC1} Consumption vs. Switching Frequency with 33 nC Load on Each Driver @ V_{CC} = 15 V

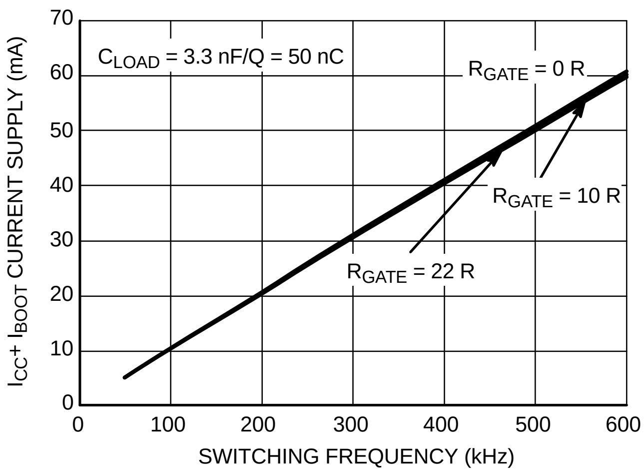


Figure 49. I_{CC1} Consumption vs. Switching Frequency with 50 nC Load on Each Driver @ V_{CC} = 15 V

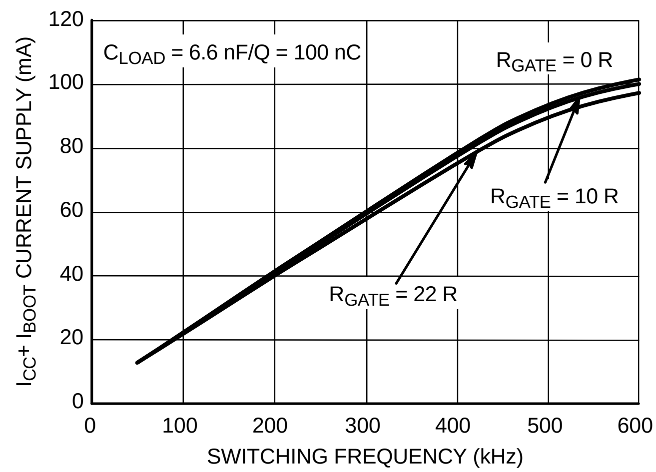


Figure 50. I_{CC1} Consumption vs. Switching Frequency with 100 nC Load on Each Driver @ V_{CC} = 15 V

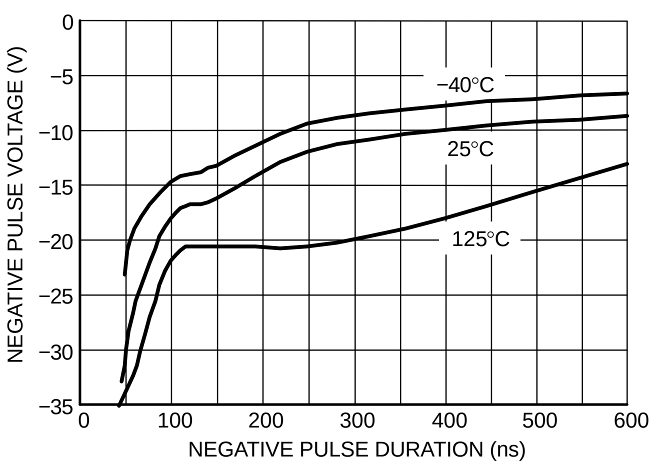


Figure 51. NCV5106A, Negative Voltage Safe Operating Area on the Bridge Pin

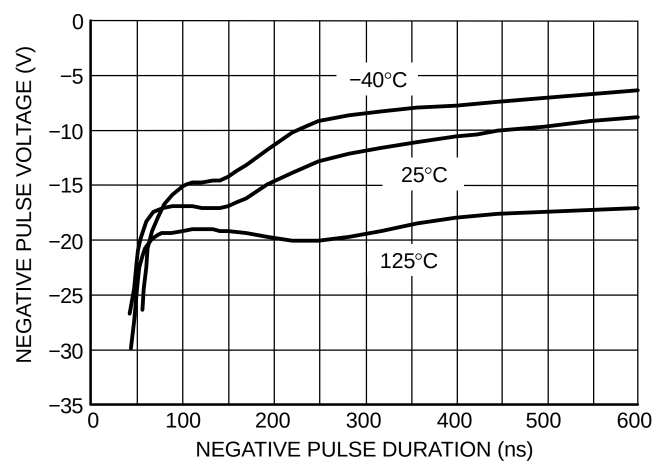


Figure 52. NCV5106B, Negative Voltage Safe Operating Area on the Bridge Pin

APPLICATION INFORMATION

Negative Voltage Safe Operating Area

When the driver is used in a half bridge configuration, it is possible to see negative voltage appearing on the bridge pin (pin 6) during the power MOSFETs transitions. When the high−side MOSFET is switched off, the body diode of the low−side MOSFET starts to conduct. The negative voltage applied to the bridge pin thus corresponds to the forward voltage of the body diode. However, as pcb copper tracks and wire bonding introduce stray elements (inductance and capacitor), the maximum negative voltage of the bridge pin will combine the forward voltage and the oscillations created by the parasitic elements. As any CMOS device, the deep negative voltage of a selected pin can inject carriers into the substrate, leading to an erratic behavior of the concerned component. ON Semiconductor provides characterization data of its half−bridge driver to show the maximum negative voltage the driver can safely operate with. To prevent the negative injection, it is the designer duty to verify that the amount of negative voltage pertinent to his/her application does not exceed the characterization curve we provide, including some safety margin.

In order to estimate the maximum negative voltage accepted by the driver, this parameter has been characterized over full the temperature range of the component. A test fixture has been developed in which we purposely negatively bias the bridge pin during the freewheel period of a buck converter. When the upper gate voltage shows signs of an erratic behavior, we consider the limit has been reached.

Figure 51 (or 52), illustrates the negative voltage safe operating area. Its interpretation is as follows: assume a negative 10 V pulse featuring a 100 ns width is applied on the bridge pin, the driver will work correctly over the whole die temperature range. Should the pulse swing to −20 V, keeping the same width of 100 ns, the driver will not work properly or will be damaged for temperatures below 125°C.

Summary:

- If the negative pulse characteristic (negative voltage level & pulse width) is above the curves the driver runs in safe operating area.
- If the negative pulse characteristic (negative voltage level & pulse width) is below one or all curves the driver will NOT run in safe operating area.

Note, each curve of the Figure 51 (or 52) represents the negative voltage and width level where the driver starts to fail at the corresponding die temperature.

If in the application the bridge pin is too close of the safe operating limit, it is possible to limit the negative voltage to the bridge pin by inserting one resistor and one diode as follows:

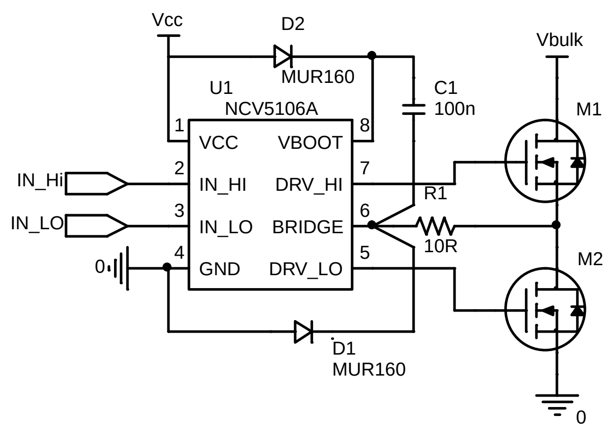


Figure 53. R1 and D1 Improves the Robustness of the Driver

R1 and D1 should be placed as close as possible of the driver. D1 should be connected directly between the bridge pin (pin 6) and the ground pin (pin 4). By this way the negative voltage applied to the bridge pin will be limited by D1 and R1 and will prevent any wrong behavior.

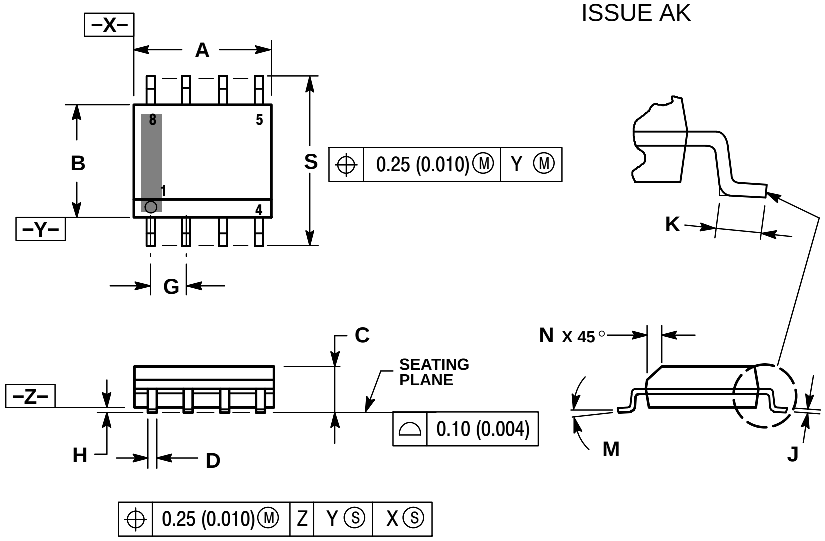
ORDERING INFORMATION

Device	Package	Shipping†
NCV5106ADR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCV5106BDR2G (On demand only, not released in production)	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

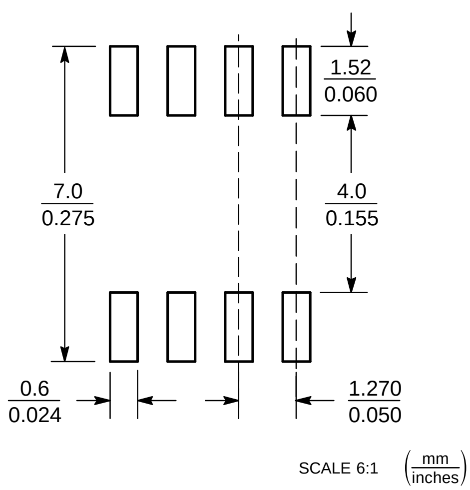
SOIC−8 NB
CASE 751−07
ISSUE AK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your loca Sales Representative

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001
Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
moschip.ru
moschip.ru_4
moschip.ru_6
moschip.ru_9