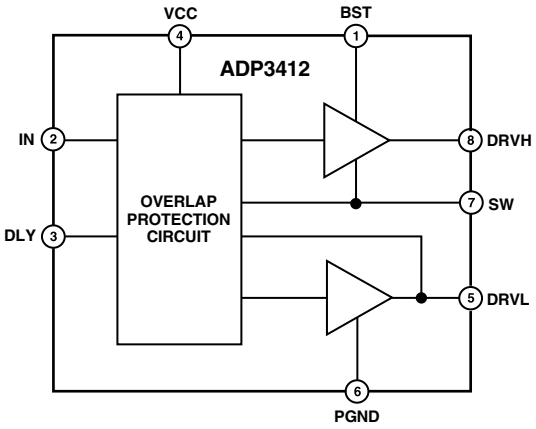
Dual MOSFET Driver with Bootstrapping

ADP3412

FEATURES
All-In-One Synchronous Buck Driver
Bootstrapped High-Side Drive
One PWM Signal Generates Both Drives
Programmable Transition Delay
Anticross-Conduction Protection Circuitry

APPLICATIONS
Multiphase Desktop CPU Supplies
Mobile Computing CPU Core Power Converters
Single-Supply Synchronous Buck Converters
Standard-to-Synchronous Converter Adaptations

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADP3412 is a dual MOSFET driver optimized for driving two N-channel MOSFETs which are the two switches in a nonisolated synchronous buck power converter. Each of the drivers is capable of driving a 3000 pF load with a 20 ns propagation delay and a 30 ns transition time. One of the drivers can be bootstrapped, and is designed to handle the high-voltage slew rate associated with "floating" high-side gate drivers. The ADP3412 includes overlapping drive protection (ODP) to prevent shoot-through current in the external MOSFETs.

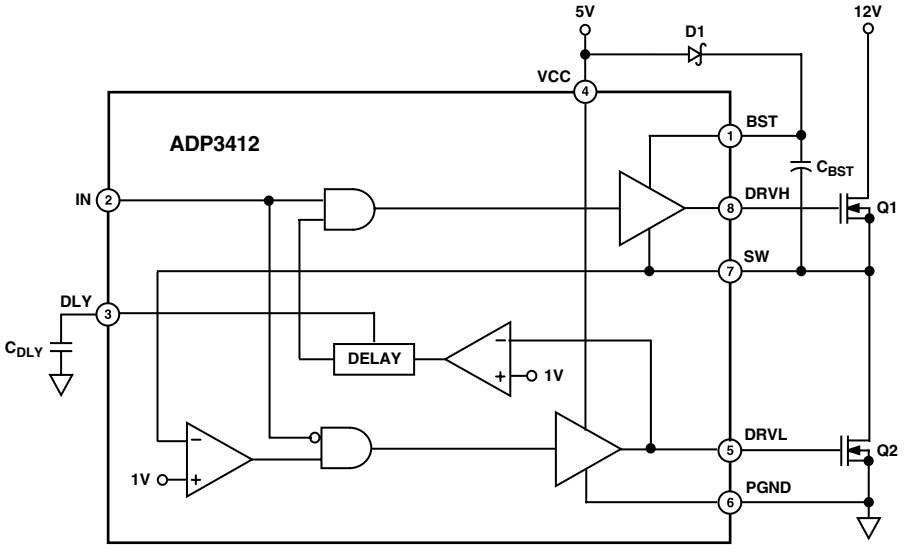


Figure 1. General Application Circuit

REV. 0

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ADP3412–SPECIFICATIONS[1] (T_A = 0°C to 70°C, VCC = 5 V, BST = 4 V to 26 V, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SUPPLY						
Supply Voltage Range	VCC		4.15	5.0	7.5	V
Quiescent Current	ICC_Q			1	2	mA
PWM INPUT						
Input Voltage High[2]			2.0			V
Input Voltage Low[2]					0.8	V
HIGH-SIDE DRIVER						
Output Resistance, Sourcing Current		$V_{BST} - V_{SW}$ = 4.6 V		2.5	5	Ω
Output Resistance, Sinking Current		$V_{BST} - V_{SW}$ = 4.6 V		2.5	5	Ω
Transition Times[3] (See Figure 2)	tr_{DRVH}, tf_{DRVH}	$V_{BST} - V_{SW}$ = 4.6 V, C_{LOAD} = 3 nF		20	35	ns
Propagation Delay[3, 4] (See Figure 2)	$tpdh_{DRVH}$	$V_{BST} - V_{SW}$ = 4.6 V	10	20	Note 5	ns
	$tpdl_{DRVH}$	$V_{BST} - V_{SW}$ = 4.6 V			25	ns
LOW-SIDE DRIVER						
Output Resistance, Sourcing Current		VCC = 4.6 V		2.5	5	Ω
Output Resistance, Sinking Current		VCC = 4.6 V		2.5	5	Ω
Transition Times[3] (See Figure 2)	tr_{DRVL}, tf_{DRVL}	VCC = 4.6 V, C_{LOAD} = 3 nF		20	35	ns
Propagation Delay[3, 4] (See Figure 2)	$tpdh_{DRVL}$	VCC = 4.6 V			30	ns
	$tpdl_{DRVL}$	VCC = 4.6 V			25	ns

NOTES
[1]All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.
[2]Logic inputs meet typical CMOS I/O conditions for source/sink current (~1 μA).
[3]AC specifications are guaranteed by characterization, but not production tested.
[4]For propagation delays, "tpdh" refers to the specified signal going high; "tpdl" refers to it going low.
[5]Maximum propagation delay = 40 ns + (1 ns/pF × C_{DLY}).

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

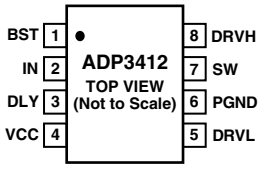
VCC . . . . . –0.3 V to +8 V
BST . . . . . –0.3 V to +30 V
BST to SW . . . . . –0.3 V to +8 V
SW . . . . . –5.0 V to +25 V
IN . . . . . –0.3 V to VCC + 0.3 V
Operating Ambient Temperature Range . . . . . 0°C to 70°C
Operating Junction Temperature Range . . . . . 0°C to 125°C
θ_{JA} . . . . . 155°C/W
θ_{JC} . . . . . 40°C/W
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . 300°C

*This is a stress rating only; operation beyond these limits can cause the device to be permanently damaged. Unless otherwise specified, all voltages are referenced to PGND.

PIN FUNCTION DESCRIPTIONS

Pin	Mnemonic	Function
1	BST	Floating Bootstrap Supply for the Upper MOSFET. A capacitor connected between BST and SW pins holds this bootstrapped voltage for the high-side MOSFET as it is switched. The capacitor should be chosen between 100 nF and 1 μF.
2	IN	TTL-level Input Signal, which has primary control of the drive outputs.
3	DLY	Low-High Transition Delay. A capacitor from this pin to ground programs the propagation delay from turn-off of the lower FET to turn-on of the upper FET. The formula for the low-high transition delay is DLY = C_{DLY} × (1 ns/pF) + 20 ns. The rise time for turn-on of the upper FET is not included in the formula.
4	VCC	Input Supply. This pin should be bypassed to PGND with ~1 μF ceramic capacitor.
5	DRVL	Synchronous Rectifier Drive. Output drive for the lower (synchronous rectifier) MOSFET.
6	PGND	Power Ground. Should be closely connected to the source of the lower MOSFET.
7	SW	This pin is connected to the buck-switching node, close to the upper MOSFET's source. It is the floating return for the upper MOSFET drive signal. It is also used to monitor the switched voltage to prevent turn-on of the lower MOSFET until the voltage is below ~1 V. Thus, according to operating conditions, the high-low transition delay is determined at this pin.
8	DRVH	Buck Drive. Output drive for the upper (buck) MOSFET.

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADP3412JR	0°C to 70°C	8-Lead Standard Small Outline Package (SOIC)	R-8

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP3412 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



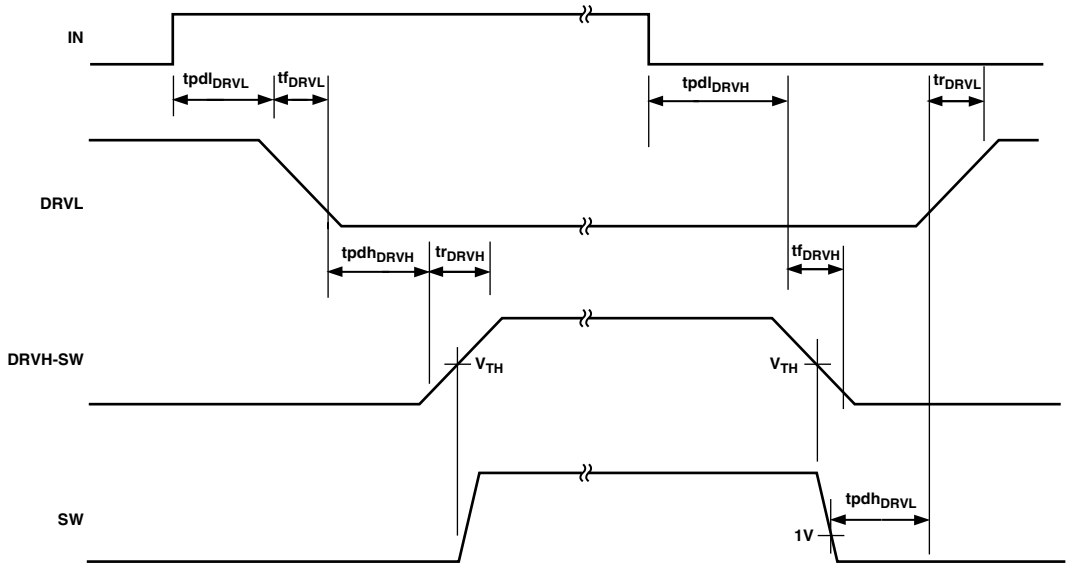
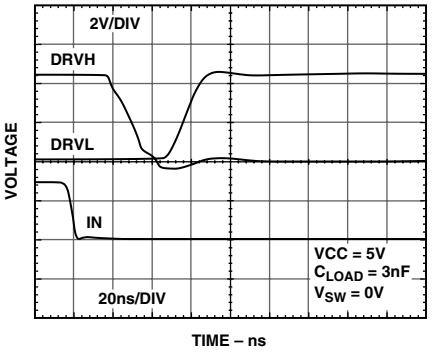
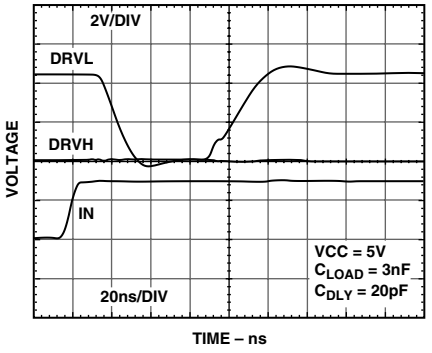


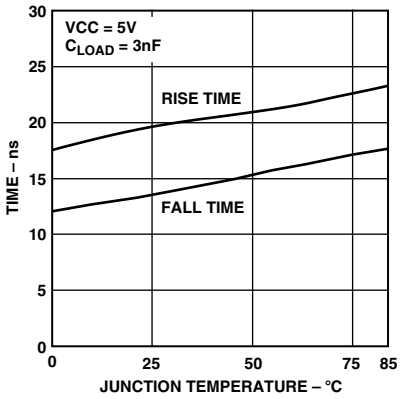
Figure 2. Nonoverlap Timing Diagram
(Timing Is Referenced to the 90% and 10% Points Unless Otherwise Noted)



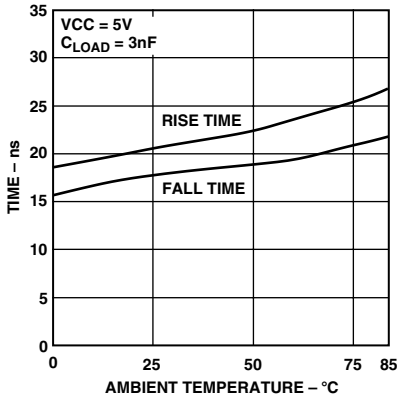
TPC 1. DRVH Fall and DRVL Rise Times



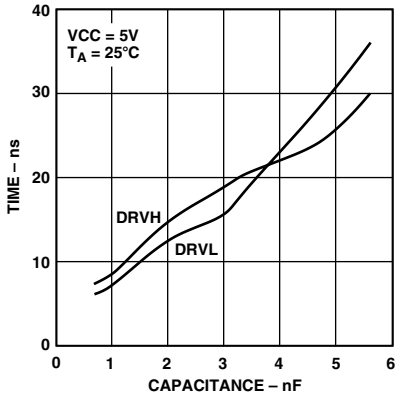
TPC 2. DRVL Fall and DRVH Rise Times



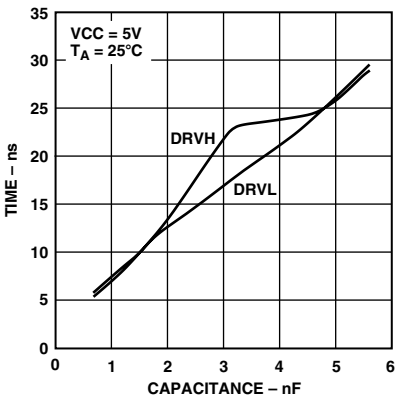
TPC 3. DRVH Rise and Fall Times vs. Temperature



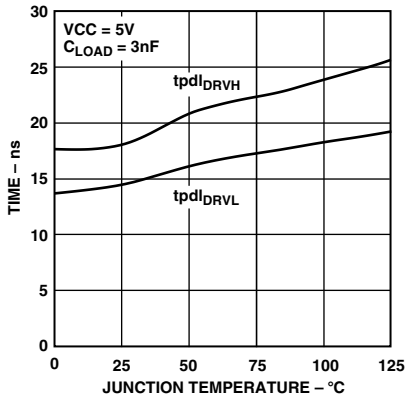
TPC 4. DRVL Rise and Fall Times vs. Temperature



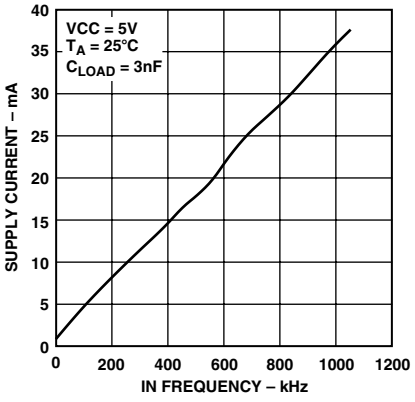
TPC 5. DRVH and DRVL Rise Times vs. Load Capacitance



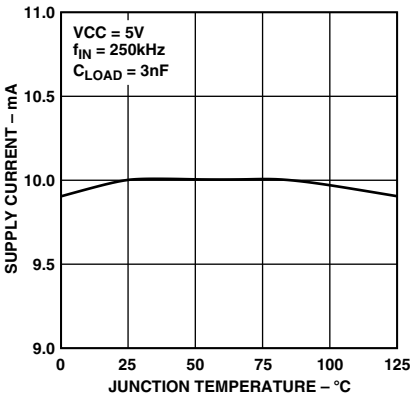
TPC 6. DRVH and DRVL Fall Times vs. Load Capacitance



TPC 7. Propagation Delay vs. Temperature



TPC 8. Supply Current vs. Frequency



TPC 9. Supply Current vs. Temperature

THEORY OF OPERATION

The ADP3412 is a dual MOSFET driver optimized for driving two N-channel MOSFETs in a synchronous buck converter topology. A single PWM input signal is all that is required to properly drive the high-side and the low-side FETs. Each driver is capable of driving a 3 nF load with only a 20 ns transition time.

A more detailed description of the ADP3412 and its features follows. Refer to the general application circuit in Figure 1.

Low-Side Driver

The low-side driver is designed to drive low-$R_{DS(ON)}$ N-channel MOSFETs. The maximum output resistance for the driver is 5 Ω for both sourcing and sinking gate current. The low output resistance allows the driver to have 20 ns rise and fall times into a 3 nF load. The bias to the low-side driver is internally connected to the VCC supply and PGND.

The driver's output is 180 degrees out of phase with the PWM input.

High-Side Driver

The high-side driver is designed to drive a floating low $R_{DS(ON)}$ N-channel MOSFET. The maximum output resistance for the driver is 5 Ω for both sourcing and sinking gate current. The low output resistance allows the driver to have 20 ns rise and fall times into a 3 nF load. The bias voltage for the high-side driver is developed by an external bootstrap supply circuit, which is connected between the BST and SW pins.

The bootstrap circuit comprises a diode, D1, and bootstrap capacitor, C_{BST}. When the ADP3412 is starting up, the SW pin is at ground, so the bootstrap capacitor will charge up to VCC through D1. When the PWM input goes high, the high-side driver will begin to turn ON the high-side MOSFET, Q1, by pulling charge out of C_{BST}. As Q1 turns ON, the SW pin will rise up to V_{IN}, forcing the BST pin to $V_{IN} + V_{C(BST)}$, which is enough gate-to-source voltage to hold Q1 ON. To complete the cycle, Q1 is switched OFF by pulling the gate down to the voltage at the SW pin. When the low-side MOSFET, Q2, turns ON, the SW pin is pulled to ground. This allows the bootstrap capacitor to charge up to VCC again. The high-side driver's output is in phase with the PWM input.

Overlap Protection Circuit

The Overlap Protection Circuit (OPC) prevents both of the main power switches, Q1 and Q2, from being ON at the same time. This is done to prevent shoot-through currents from flowing through both power switches and the associated losses that can occur during their ON-OFF transitions. The Overlap Protection Circuit accomplishes this by adaptively controlling the delay from Q1's turn OFF to Q2's turn ON, and by externally setting the delay from Q2's turn OFF to Q1's turn ON.

To prevent the overlap of the gate drives during Q1's turn OFF and Q2's turn ON, the overlap circuit monitors the voltage at the SW pin. When the PWM input signal goes low, Q1 will begin to turn OFF (after a propagation delay), but before Q2 can turn ON, the overlap protection circuit waits for the voltage at the SW pin to fall from V_{IN} to 1 V. Once the voltage on the SW pin has fallen to 1 V, Q2 will begin turn ON. By waiting for the voltage on the SW pin to reach 1 V, the overlap protection circuit ensures that Q1 is OFF before Q2 turns on, regardless of variations in temperature, supply voltage, gate charge, and drive current.

To prevent the overlap of the gate drives during Q2's turn OFF and Q1's turn ON, the overlap circuit provides a programmable delay that is set by a capacitor on the DLY pin. When the PWM input signal goes high, Q2 will begin to turn OFF (after a propagation delay), but before Q1 can turn ON the overlap protection circuit waits for the voltage at DRVL to drop to around 10% of VCC. Once the voltage at DRVL has reached the 10% point, the overlap protection circuit will wait for a 20 ns typical propagation delay plus an additional delay based on the external capacitor, C_{DLY}. The delay capacitor adds an additional 1 ns/pF of delay. Once the programmable delay period has expired, Q1 will begin turn ON. The delay allows time for current to commutate from the body diode of Q2 to an external Schottky diode, which allows turnoff losses to be reduced. Although not as foolproof as the adaptive delay, the programmable delay adds a safety margin to account for variations in size, gate charge, and internal delay of the external power MOSFETs.

APPLICATION INFORMATION

Supply Capacitor Selection

For the supply input (VCC) of the ADP3412, a local bypass capacitor is recommended to reduce the noise and to supply some of the peak currents drawn. Use a 1 µF, low ESR capacitor. Multilayer ceramic chip (MLCC) capacitors provide the best combination of low ESR and small size and can be obtained from the following vendors:

Murata	GRM235Y5V106Z16	www.murata.com
Taiyo-Yuden	EMK325F106ZF	www.t-yuden.com
Tokin	C23Y5V1C106ZP	www.tokin.com

Keep the ceramic capacitor as close as possible to the ADP3412.

Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor (C_{BST}) and a Schottky diode, as shown in Figure 1. Selection of these components can be done after the high-side MOSFET has been chosen.

The bootstrap capacitor must have a voltage rating that is able to handle the maximum battery voltage plus 5 volts. A minimum 50 V rating is recommended. The capacitance is determined using the following equation:

$$C_{BST} = \frac{Q_{GATE}}{\Delta V_{BST}}$$

where, Q_{GATE} is the total gate charge of the high-side MOSFET, and ΔV_{BST} is the voltage droop allowed on the high-side MOSFET drive. For example, the IRF7811 has a total gate charge of about 20 nC. For an allowed droop of 200 mV, the required bootstrap capacitance is 100 nF. A good quality ceramic capacitor should be used.

A Schottky diode is recommended for the bootstrap diode due to its low forward drop, which maximizes the drive available for the high-side MOSFET. The bootstrap diode must have a minimum 40 V rating to withstand the maximum battery voltage plus 5 V. The average forward current can be estimated by:

$$I_{F(AVG)} \approx Q_{GATE} \times f_{MAX}$$

where f_{MAX} is the maximum switching frequency of the controller. The peak surge current rating should be checked in-circuit, since this is dependent on the source impedance of the 5 V supply, and the ESR of C_{BST}.

Delay Capacitor Selection

The delay capacitor, C_{DLY}, is used to add an additional delay when the low-side FET drive turns off and when the high-side drive starts to turn on. The delay capacitor adds 1 ns/pF of additional time to the 20 ns of fixed delay.

If a delay capacitor is required, look for a good quality ceramic capacitor with an NPO or COG dielectric, or for a good quality mica capacitor. Both types of capacitors are available in the 1 pF to 100 pF range and have excellent temperature and leakage characteristics.

Printed Circuit Board Layout Considerations

Use the following general guidelines when designing printed circuit boards:

1. Trace out the high-current paths and use short, wide traces to make these connections.
2. Connect the PGND pin of the ADP3412 as close as possible to the source of the lower MOSFET.
3. The VCC bypass capacitor should be located as close as possible to VCC and PGND pins.

Typical Application Circuits

The circuit in Figure 3 shows how two drivers can be combined with the ADP3160 to form a total power conversion solution for $V_{CC(CORE)}$ generation in a high-current GOA computer. Figure 4 gives CPU a similar application circuit for a 35 A processor.

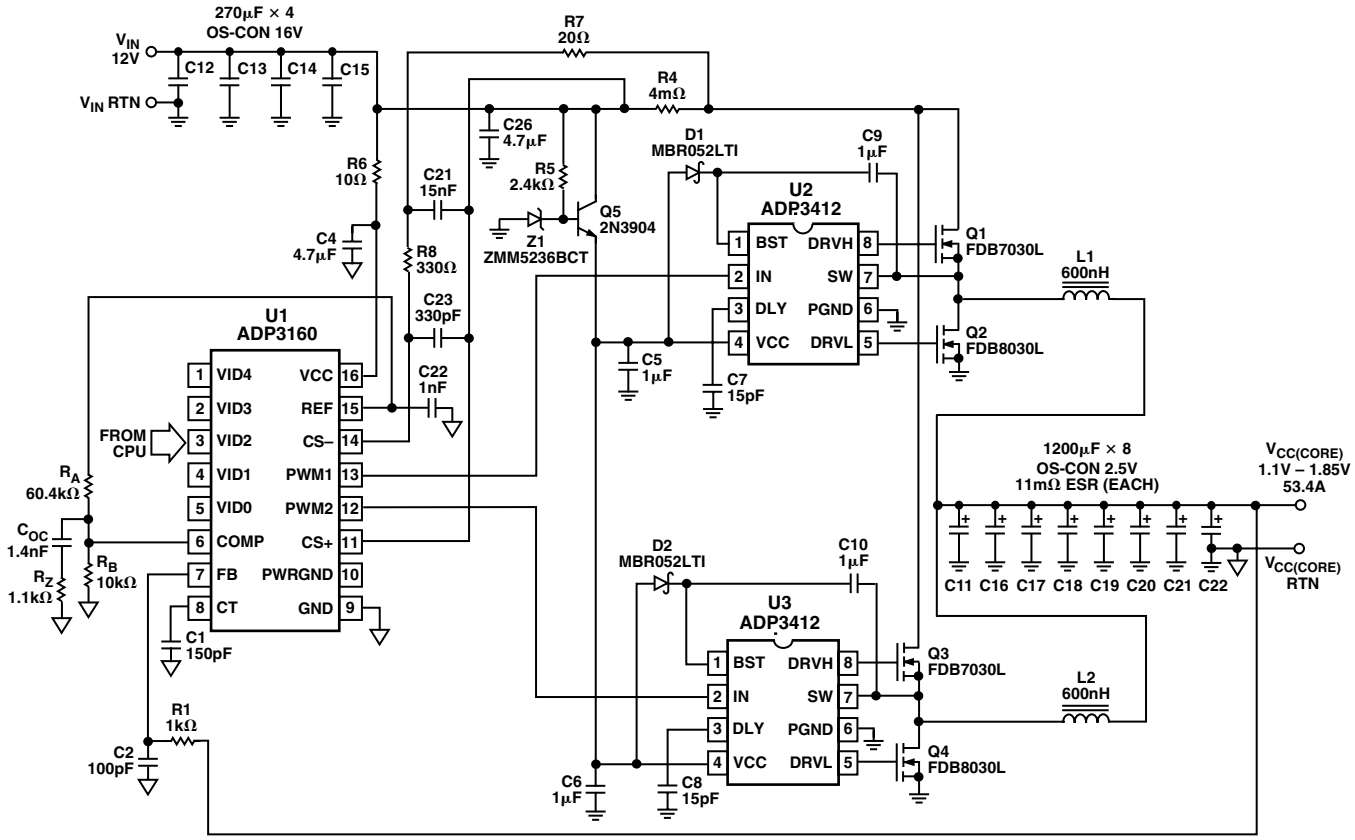


Figure 3. 53.4 A Intel CPU Supply Circuit

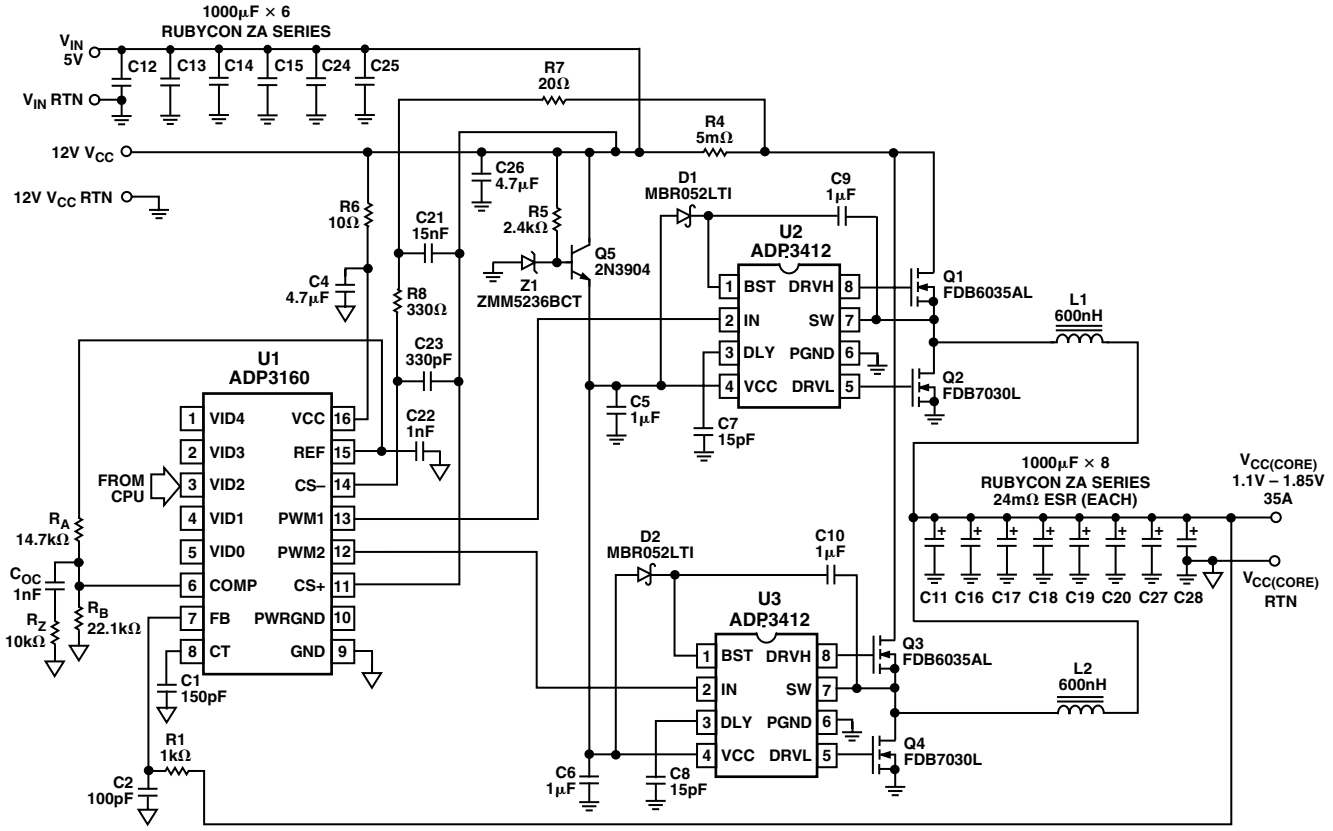
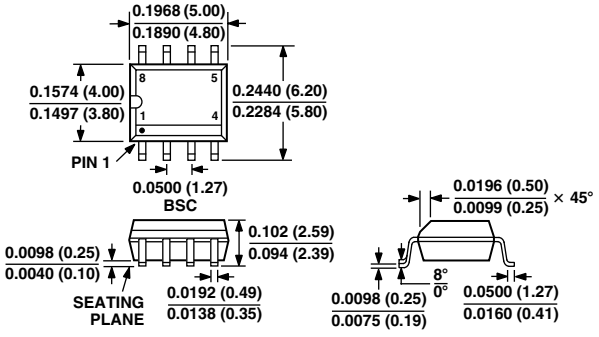


Figure 4. 35 A Athlon CPU Supply Circuit

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead Small Outline Package
(R-8)



C01023–2.5–9/00 (rev. 0)

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