TYN20X-800T

SCR

23 July 2018 Product data sheet

1. General description

Planar passivated Silicon Controlled Rectifier (SCR) in a SOT186A (TO-220F) "full pack" plastic package intended for use in applications requiring very high inrush current capability, high thermal cycling performance and high junction temperature capability ($T_{j(max)}$ = 150 °C).

2. Features and benefits

- High bidirectional blocking voltage capability
- High junction operating temperature capability
- High thermal cycling performance
- Isolated package
- Planar passivated for voltage ruggedness and reliability
- Very high current surge capability

3. Applications

- Capacitive Discharge Ignition (CDI)
- Crowbar protection
- Inrush protection
- Motor control
- Voltage regulation

4. Quick reference data

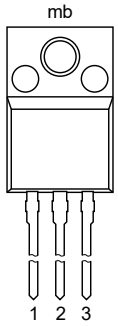
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RRM}	repetitive peak reverse voltage			-	-	800	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_h \leq$ 75 °C; Fig. 1		-	-	12.7	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_h \leq$ 75 °C; Fig. 2; Fig. 3		-	-	20	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)}$ = 25 °C; t_p = 10 ms; Fig. 4; Fig. 5		-	-	210	A
		half sine wave; $T_{j(init)}$ = 25 °C; t_p = 8.3 ms		-	-	231	A
T_j	junction temperature			-	-	150	°C
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 7		-	4.5	32	mA
Dynamic characteristics							

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 402 V; T_j = 150 °C; exponential waveform; gate open circuit		1000	-	-	V/µs
		V_{DM} = 536 V; T_j = 150 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit		500	-	-	V/µs

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode	 **TO-220F (SOT186A)**	
2	A	anode		
3	G	gate		
mb	n.c.	mounting base; isolated		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
TYN20X-800T	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"	SOT186A

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7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	800	V
V_{RRM}	repetitive peak reverse voltage			-	800	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_h \leq 75$ °C; Fig. 1		-	12.7	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_h \leq 75$ °C; Fig. 2; Fig. 3		-	20	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25$ °C; $t_p = 10$ ms; Fig. 4; Fig. 5		-	210	A
		half sine wave; $T_{j(init)} = 25$ °C; $t_p = 8.3$ ms		-	231	A
I^2t	I^2t for fusing	$t_p = 10$ ms; sine-wave pulse		-	220.5	A²s
dI_T/dt	rate of rise of on-state current	$I_G = 70$ mA		-	100	A/µs
I_{GM}	peak gate current			-	5	A
V_{RGM}	peak reverse gate voltage			-	5	V
P_{GM}	peak gate power			-	20	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	1	W
T_{stg}	storage temperature			-40	150	°C
T_j	junction temperature			-	150	°C

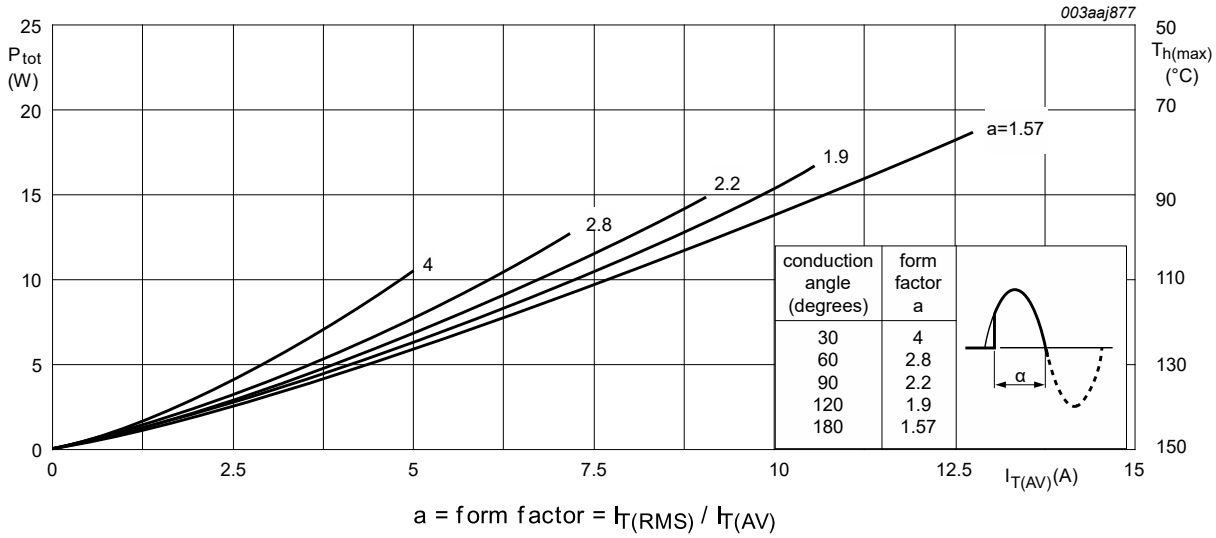

Fig. 1. Total power dissipation as a function of average on-state current; maximum values

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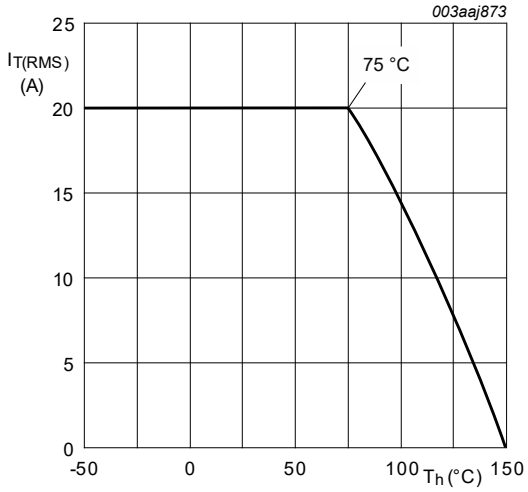
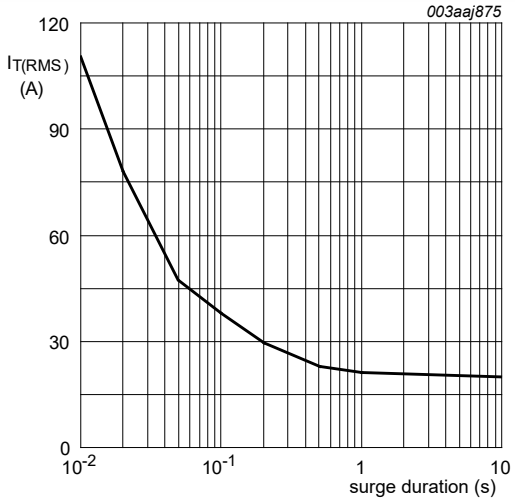
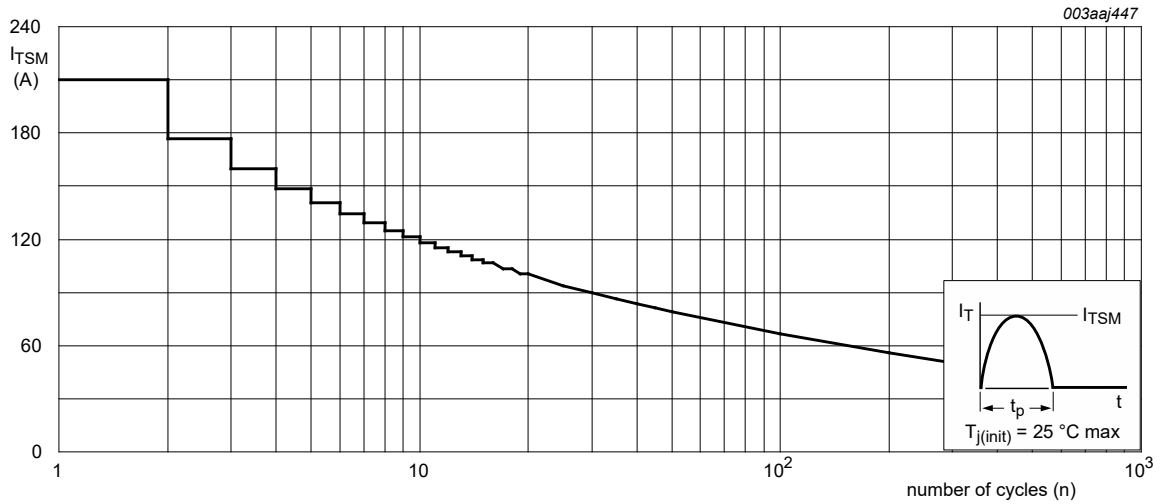


Fig. 2. RMS on-state current as a function of heatsink temperature; maximum values



f = 50 Hz; T_h = 75 °C

Fig. 3. RMS on-state current as a function of surge duration; maximum values



f = 50 Hz

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

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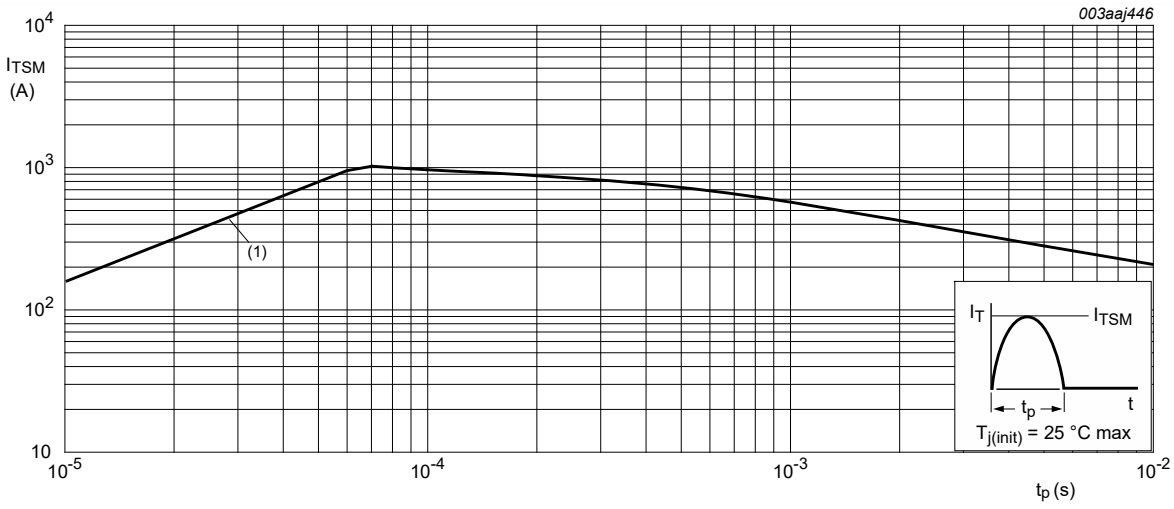

$t_p \leq 10$ ms; (1) dI_T / dt limit

Fig. 5. Non-repetitive peak on-state current as a function of pulse width for sinusoidal currents; maximum values

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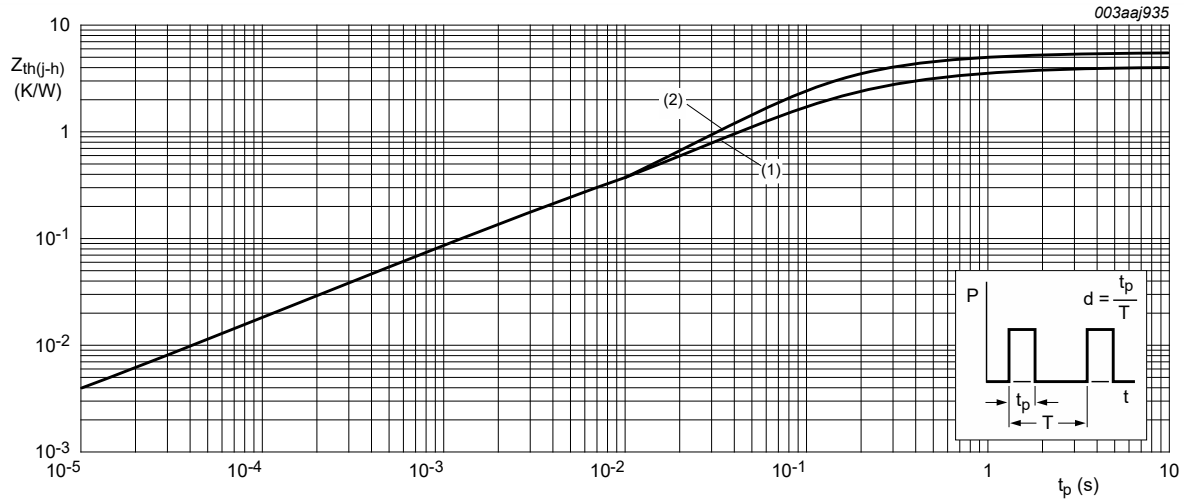
8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	with heatsink compound; Fig. 6		-	-	4	K/W
		without heatsink compound; Fig. 6		-	-	5.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	in free air		-	55	-	K/W



(1) with heatsink compound
(2) without heatsink compound

Fig. 6. Transient thermal impedance from junction to heatsink as a function of pulse width

9. Isolation characteristics

Table 6. Isolation characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	from all terminals to external heatsink; sinusoidal waveform; clean and dust free; 50 Hz ≤ f ≤ 60 Hz; RH ≤ 65 %; T_h = 25 °C		-	-	2500	V
C_{isol}	isolation capacitance	from anode to external heatsink; f = 1 MHz; T_h = 25 °C		-	10	-	pF

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10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 7		-	4.5	32	mA
I_L	latching current	V_D = 12 V; I_G = 0.1 A; T_j = 25 °C; Fig. 8		-	21	60	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 9		-	16	40	mA
V_T	on-state voltage	I_T = 32 A; T_j = 25 °C; Fig. 10		-	1.2	1.5	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 11		-	0.7	1.3	V
		V_D = 400 V; I_T = 0.1 A; T_j = 150 °C; Fig. 11		0.2	0.4	-	V
I_D	off-state current	V_D = 800 V; T_j = 150 °C		-	0.2	1	mA
I_R	reverse current	V_R = 800 V; T_j = 150 °C		-	0.2	1	mA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 402 V; T_j = 150 °C; exponential waveform; gate open circuit		1000	-	-	V/µs
		V_{DM} = 536 V; T_j = 150 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit		500	-	-	V/µs
t_{gt}	gate-controlled turn-on time	I_{TM} = 40 A; V_D = 800 V; I_G = 100 mA; dI_G/dt = 5 A/µs; T_j = 25 °C		-	2	-	µs
t_q	commutated turn-off time	V_{DM} = 536 V; T_j = 125 °C; I_{TM} = 20 A; V_R = 25 V; $(dI_T/dt)_M$ = 30 A/µs; dV_D/dt = 50 V/µs; $R_{GK(ext)}$ = 100 Ω; (V_{DM} = 67% of V_{DRM})		-	70	-	µs

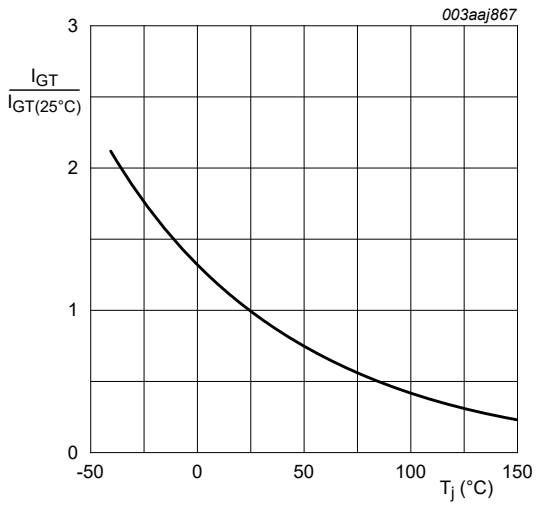

Fig. 7. Normalized gate trigger current as a function of junction temperature

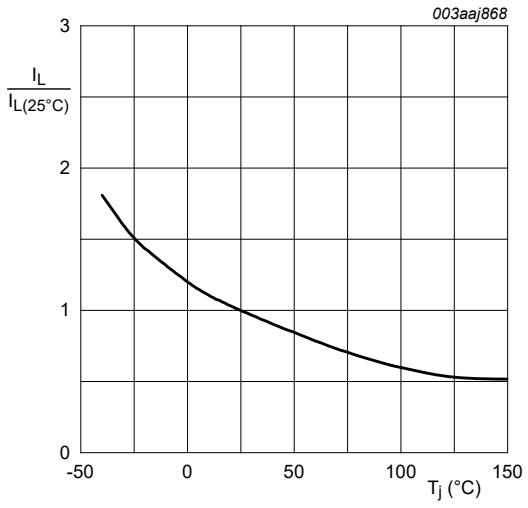

Fig. 8. Normalized latching current as a function of junction temperature

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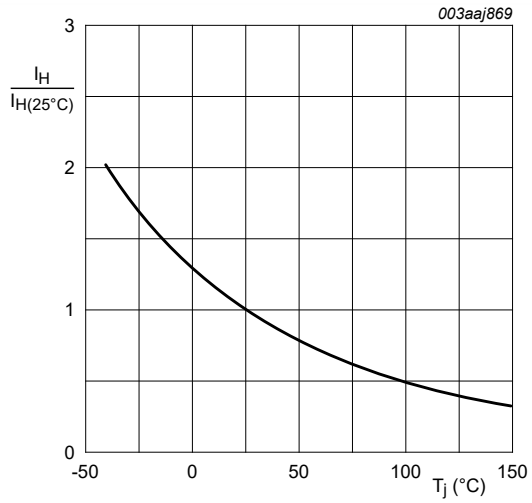
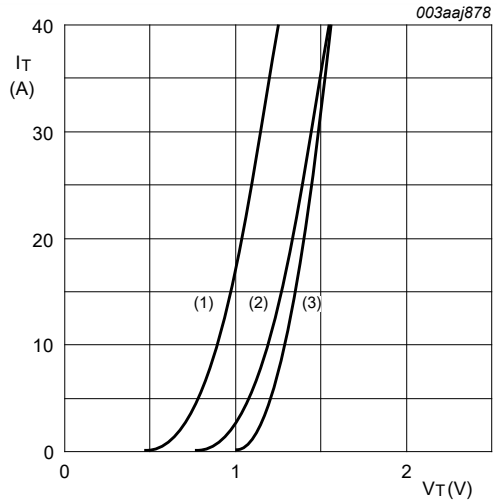


Fig. 9. Normalized holding current as a function of junction temperature



V_o = 1.0485 V; R_s = 0.0133 Ω
(1) T_j = 150 °C; typical values
(2) T_j = 150 °C; maximum values
(3) T_j = 25 °C; maximum values

Fig. 10. On-state current as a function of on-state voltage

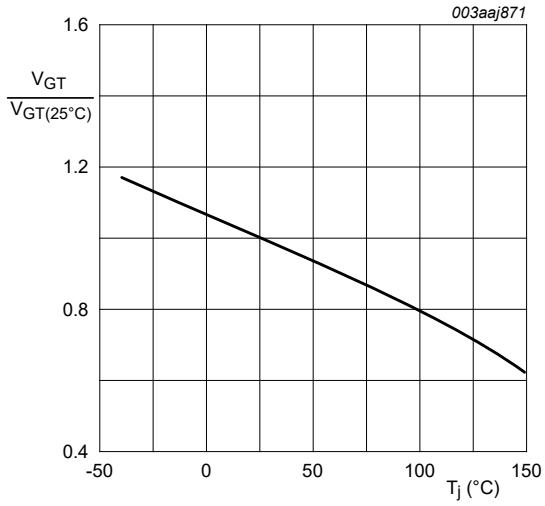


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

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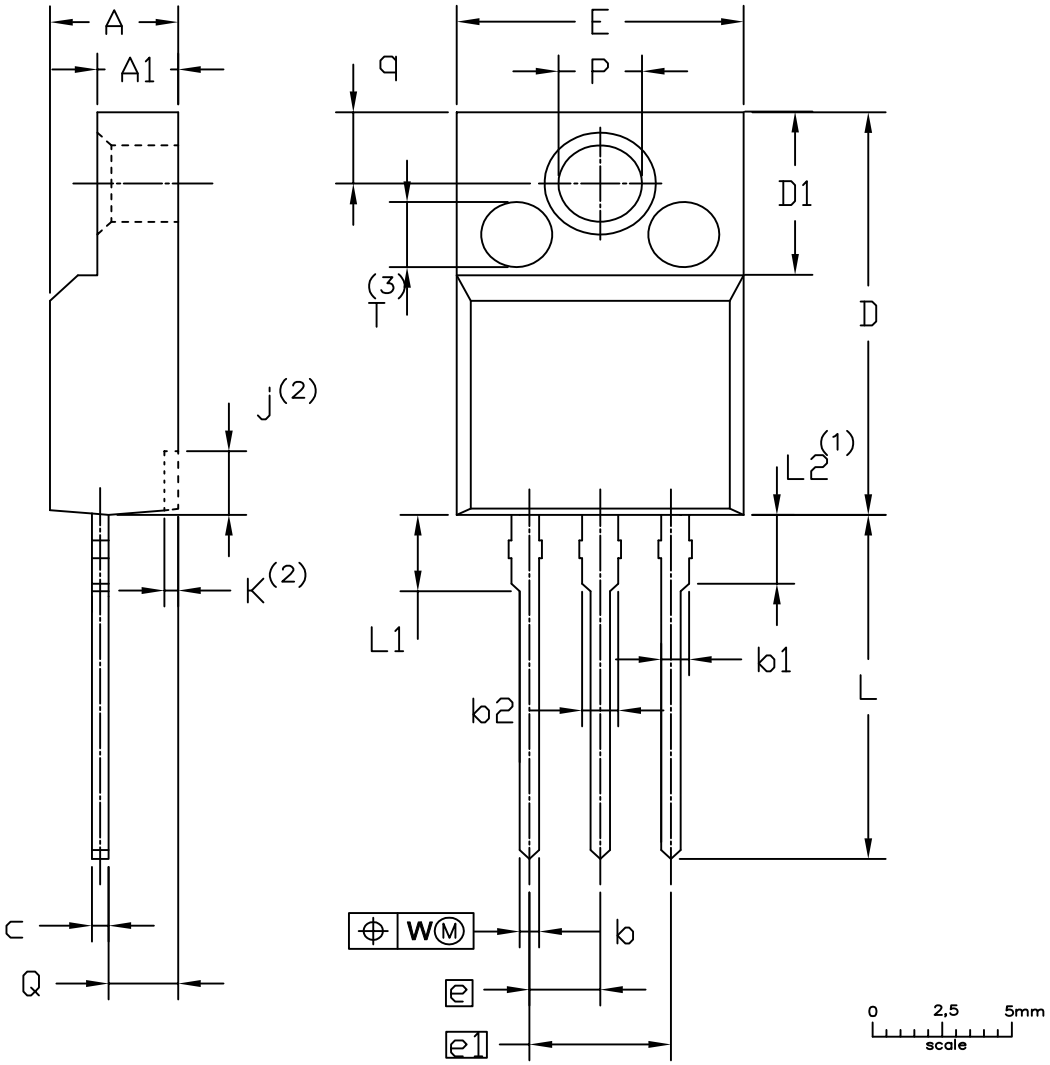
11. Package outline

Plastic single−ended package; isolated heatsink mounted; 1 mounting hole; 3−lead TO−220 "full pack" SOT186A



UNIT	A	A_1	b	b_1	b_2	c	D	D_1	E	e	e_1	j(2)	K(2)	L	L_1	L_2(1) max.	P	Q	q	W	T(3)
mm	4.6	2.9	0.9	1.1	1.4	0.7	15.8	6.5	10.3	2.54	5.08	2.7	0.6	14.4	3.30	3	3.2	2.6	3.0	0.4	2.5
	4.0	2.5	0.7	0.9	1.0	0.4	15.2	6.3	9.7			1.7	0.4	13.5	2.79		3.0	2.3	2.6		

Notes
1. Terminal dimensions within this zone are uncotrolled
2. Dot lines area designs may vary
3. Eject pin mark is for reference only

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT186A		3 LEADS TO220F				2013−11−14

Fig. 12. Package outline TO-220F (SOT186A)

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Document status [1][2]	Product status [3]	Definition
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