CAT24C32

32-Kb I^{2}C CMOS Serial EEPROM

Description

The CAT24C32 is a 32−Kb CMOS Serial EEPROM devices, internally organized as 4096 words of 8 bits each.

It features a 32−byte page write buffer and supports the Standard (100 kHz), Fast (400 kHz) and Fast−Plus (1 MHz) I^{2}C protocol.

External address pins make it possible to address up to eight CAT24C32 devices on the same bus.

Features

- Supports Standard, Fast and Fast−Plus I^{2}C Protocol
- 1.7 V to 5.5 V Supply Voltage Range
- 32−Byte Page Write Buffer
- Hardware Write Protection for Entire Memory
- Schmitt Triggers and Noise Suppression Filters on I^{2}C Bus Inputs (SCL and SDA)
- Low Power CMOS Technology
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Industrial and Extended Temperature Range
- PDIP, SOIC, TSSOP, TDFN, UDFN 8−lead, TSOP 5−lead, and WLCSP 5−ball Packages
- This Device is Pb−Free, Halogen Free/BFR Free, and RoHS Compliant

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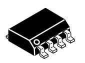
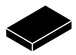
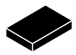


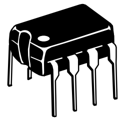
SOIC−8
W SUFFIX
CASE 751BD



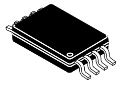
UDFN−8
HU4 SUFFIX
CASE 517AZ



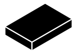
TDFN−8*
VP2 SUFFIX
CASE 511AK



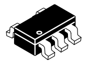
PDIP−8
L SUFFIX
CASE 646AA



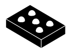
TSSOP−8
Y SUFFIX
CASE 948AL



UDFN−8*
HU3 SUFFIX
CASE 517AX

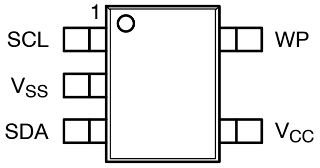


TSOP−5
TS SUFFIX
CASE 483

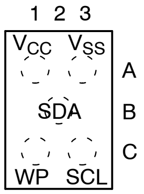


WLCSP−5**
C5A SUFFIX
CASE 567GN

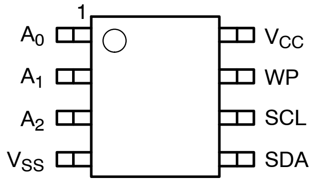
PIN CONFIGURATIONS



TSOP−5 (TS)



WLCSP−5 (C5A)**



PDIP (L), SOIC (W), TSSOP (Y), TDFN (VP2)*, UDFN (HU3*, HU4)

(Top Views)

For the location of Pin 1, please consult the corresponding package drawing.

* Not recommended for new designs

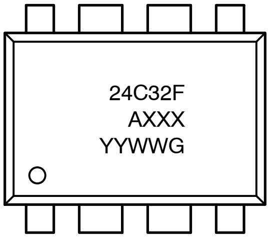
** Preliminary, please contact factory for availability.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 17 of this data sheet.

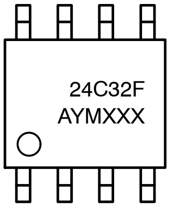
DEVICE MARKINGS

(PDIP−8)



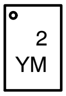
24C32F = Specific Device Code
A = Assembly Location
XXX = Last Three Digits of Assembly Lot Number
YY = Production Year (Last Two Digits)
WW = Production Week (Two Digits)
G = Pd−Free designator

(SOIC−8)



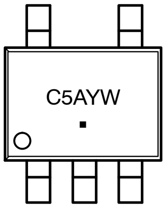
24C32F = Specific Device Code
A = Assembly Location
Y = Production Year (Last Digit)
M = Production Month (1−9, O, N, D)
XXX = Last Three Digits of Assembly Lot Number

(WLCSP−5)



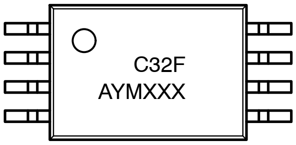
2 = Specific Device Code
Y = Production Year (Last Digit)
M = Production Month (1−9, O, N, D)

(TSOP−5)



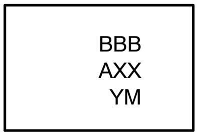
C5 = Specific Device Code
A = Assembly Location
YW = Date Code (two digits)
▪ = Pb−Free Package

(TSSOP−8)



C32F = Specific Device Code
A = Assembly Location
Y = Production Year (Last Digit)
M = Production Month (1−9, O, N, D)
XXX = Last Three Digits of Assembly Lot Number

(UDFN−8 and TDFN−8)



BBB = C5U = CAT24C32HU4
BBB = C5V = CAT24C32HU3
BBB = C5T = CAT24C32VP2
A = Assembly Location
XX = Last Two Digits of Assembly Lot Number
Y = Production Year (Last Digit)
M = Production Month (1−9, O, N, D)

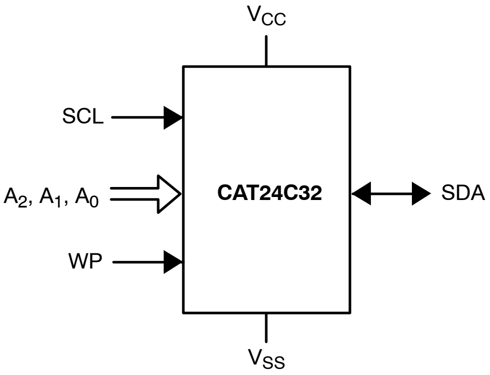


Figure 1. Functional Symbol

PIN FUNCTION

Pin Name	Function
A0, A1, A2	Device Address
SDA	Serial Data
SCL	Serial Clock
WP	Write Protect
V_{CC}	Power Supply
V_{SS}	Ground

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Storage Temperature	–65 to +150	°C
Voltage on any Pin with Respect to Ground (Note 1)	–0.5 to +6.5	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The DC input voltage on any pin should not be lower than −0.5 V or higher than V_{CC} + 0.5 V. During transitions, the voltage on any pin may undershoot to no less than −1.5 V or overshoot to no more than V_{CC} + 1.5 V, for periods of less than 20 ns.

Table 2. RELIABILITY CHARACTERISTICS (Note 2)

Symbol	Parameter	Min	Units
N_{END} (Note 3)	Endurance	1,000,000	Program/Erase Cycles
T_{DR}	Data Retention	100	Years

2. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.
3. Page Mode, V_{CC} = 5 V, 25°C.

Table 3. D.C. OPERATING CHARACTERISTICS

(V_{CC} = 1.8 V to 5.5 V, T_A = −40°C to +125°C and V_{CC} = 1.7 V to 5.5 V, T_A = −40°C to +85°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions		Min	Max	Units
I_{CCR}	Read Current	Read, f_{SCL} = 400 kHz			1	mA
I_{CCW}	Write Current	Write, f_{SCL} = 400 kHz			2	mA
I_{SB}	Standby Current	All I/O Pins at GND or V_{CC}	T_A = −40°C to +85°C V_{CC} ≤ 3.3 V		1	μA
			T_A = −40°C to +85°C V_{CC} > 3.3 V		3	
			T_A = −40°C to +125°C		5	
I_L	I/O Pin Leakage	Pin at GND or V_{CC}			2	μA
V_{IL}	Input Low Voltage			−0.5	V_{CC} x 0.3	V
V_{IH}	Input High Voltage			V_{CC} x 0.7	V_{CC} + 0.5	V
V_{OL1}	Output Low Voltage	V_{CC} < 2.5 V, I_{OL} = 3.0 mA			0.4	V
V_{OL2}	Output Low Voltage	V_{CC} < 2.5 V, I_{OL} = 1.0 mA			0.2	V

Table 4. PIN IMPEDANCE CHARACTERISTICS

(V_{CC} = 1.8 V to 5.5 V, T_A = −40°C to +125°C and V_{CC} = 1.7 V to 5.5 V, T_A = −40°C to +85°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Max	Units
C_{IN} (Note 4)	SDA I/O Pin Capacitance	V_{IN} = 0 V, T_A = 25°C, f = 1.0 MHz	8	pF
C_{IN} (Note 4)	Input Capacitance (other pins)	V_{IN} = 0 V, T_A = 25°C, f = 1.0 MHz	6	pF
I_{WP} (Note 5)	WP Input Current	V_{IN} < V_{IH}, V_{CC} = 5.5 V	130	μA
		V_{IN} < V_{IH}, V_{CC} = 3.3 V	120	
		V_{IN} < V_{IH}, V_{CC} = 1.7 V	80	
		V_{IN} > V_{IH}	2	
I_A (Note 5)	Address Input Current (A0, A1, A2) Product Rev F	V_{IN} < V_{IH}, V_{CC} = 5.5 V	50	μA
		V_{IN} < V_{IH}, V_{CC} = 3.3 V	35	
		V_{IN} < V_{IH}, V_{CC} = 1.7 V	25	
		V_{IN} > V_{IH}	2	

4. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.
5. When not driven, the WP, A0, A1 and A2 pins are pulled down to GND internally. For improved noise immunity, the internal pull−down is relatively strong; therefore the external driver must be able to supply the pull−down current when attempting to drive the input HIGH. To conserve power, as the input level exceeds the trip point of the CMOS input buffer (~ 0.5 x V_{CC}), the strong pull−down reverts to a weak current source.

Table 5. A.C. CHARACTERISTICS

(V_{CC} = 1.8 V to 5.5 V, T_A = −40°C to +125°C and V_{CC} = 1.7 V to 5.5 V, T_A = −40°C to +85°C.) (Note 6)

Symbol	Parameter	Standard V_{CC} = 1.7 V – 5.5 V		Fast V_{CC} = 1.7 V – 5.5 V		Fast−Plus (Note 9) V_{CC} = 2.5 V – 5.5 V T_A = −40°C to +85°C		Units
		Min	Max	Min	Max	Min	Max	
F_{SCL}	Clock Frequency		100		400		1,000	kHz
$t_{HD:STA}$	START Condition Hold Time	4		0.6		0.25		μs
t_{LOW}	Low Period of SCL Clock	4.7		1.3		0.45		μs
t_{HIGH}	High Period of SCL Clock	4		0.6		0.40		μs
$t_{SU:STA}$	START Condition Setup Time	4.7		0.6		0.25		μs
$t_{HD:DAT}$	Data In Hold Time	0		0		0		μs
$t_{SU:DAT}$	Data In Setup Time	250		100		50		ns
t_R (Note 7)	SDA and SCL Rise Time		1,000		300		100	ns
t_F (Note 7)	SDA and SCL Fall Time		300		300		100	ns
$t_{SU:STO}$	STOP Condition Setup Time	4		0.6		0.25		μs
t_{BUF}	Bus Free Time Between STOP and START	4.7		1.3		0.5		μs
t_{AA}	SCL Low to Data Out Valid		3.5		0.9		0.40	μs
t_{DH}	Data Out Hold Time	100		100		50		ns
T_i (Note 7)	Noise Pulse Filtered at SCL and SDA Inputs		100		100		100	ns
$t_{SU:WP}$	WP Setup Time	0		0		0		μs
$t_{HD:WP}$	WP Hold Time	2.5		2.5		1		μs
t_{WR}	Write Cycle Time		5		5		5	ms
t_{PU} (Notes 7, 8)	Power−up to Ready Mode		1		1	0.1	1	ms

6. Test conditions according to “A.C. Test Conditions” table.
7. Tested initially and after a design or process change that affects this parameter.
8. t_{PU} is the delay between the time V_{CC} is stable and the device is ready to accept commands.
9. Fast−Plus (1 MHz) speed class available for product revision “F”. The die revision “F” is identified by letter “F” or a dedicated marking code on top of the package.

Table 6. A.C. TEST CONDITIONS

Input Drive Levels	0.2 x V_{CC} to 0.8 x V_{CC}
Input Rise and Fall Time	≤ 50 ns
Input Reference Levels	0.3 x V_{CC}, 0.7 x V_{CC}
Output Reference Level	0.5 x V_{CC}
Output Test Load	Current Source I_{OL} = 3 mA (V_{CC} ≥ 2.5 V); I_{OL} = 1 mA (V_{CC} < 2.5 V); C_L = 100 pF

Power−On Reset (POR)

Each CAT24C32 incorporates Power−On Reset (POR) circuitry which protects the internal logic against powering up in the wrong state. The device will power up into Standby mode after V_{CC} exceeds the POR trigger level and will power down into Reset mode when V_{CC} drops below the POR trigger level. This bi−directional POR behavior protects the device against ‘brown−out’ failure following a temporary loss of power.

Pin Description

SCL: The Serial Clock input pin accepts the clock signal generated by the Master.

SDA: The Serial Data I/O pin accepts input data and delivers output data. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.

A_0, A_1 and A_2: The Address inputs set the device address that must be matched by the corresponding Slave address bits. The Address inputs are hard−wired HIGH or LOW allowing for up to eight devices to be used (cascaded) on the same bus. When left floating, these pins are pulled LOW internally.

WP: When pulled HIGH, the Write Protect input pin inhibits all write operations. When left floating, this pin is pulled LOW internally.

Functional Description

The CAT24C32 supports the Inter−Integrated Circuit (I^2C) Bus protocol. The protocol relies on the use of a Master device, which provides the clock and directs bus traffic, and Slave devices which execute requests. The CAT24C32 operates as a Slave device. Both Master and Slave can transmit or receive, but only the Master can assign those roles.

I^2C Bus Protocol

The 2−wire I^2C bus consists of two lines, SCL and SDA, connected to the V_{CC} supply via pull−up resistors. The Master provides the clock to the SCL line, and either the Master or the Slaves drive the SDA line. A ‘0’ is transmitted by pulling a line LOW and a ‘1’ by letting it stay HIGH. Data transfer may be initiated only when the bus is not busy (see A.C. Characteristics). During data transfer, SDA must remain stable while SCL is HIGH.

START/STOP Condition

An SDA transition while SCL is HIGH creates a START or STOP condition (Figure 2). The START consists of a HIGH to LOW SDA transition, while SCL is HIGH. Absent the START, a Slave will not respond to the Master. The STOP completes all commands, and consists of a LOW to HIGH SDA transition, while SCL is HIGH.

Device Addressing

The Master addresses a Slave by creating a START condition and then broadcasting an 8−bit Slave address. For the CAT24C32, the first four bits of the Slave address are set to 1010 (Ah); the next three bits, A_2, A_1 and A_0, must match the logic state of the similarly named input pins. The R/W bit tells the Slave whether the Master intends to read (1) or write (0) data (Figure 3).

Acknowledge

During the 9th clock cycle following every byte sent to the bus, the transmitter releases the SDA line, allowing the receiver to respond. The receiver then either acknowledges (ACK) by pulling SDA LOW, or does not acknowledge (NoACK) by letting SDA stay HIGH (Figure 4). Bus timing is illustrated in Figure 5.

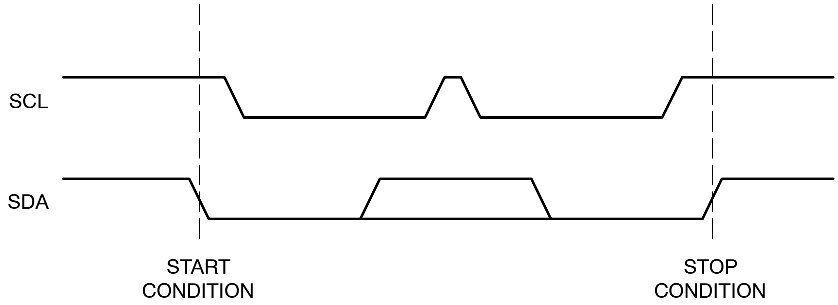


Figure 2. Start/Stop Timing

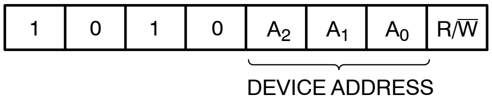


Figure 3. Slave Address Bits

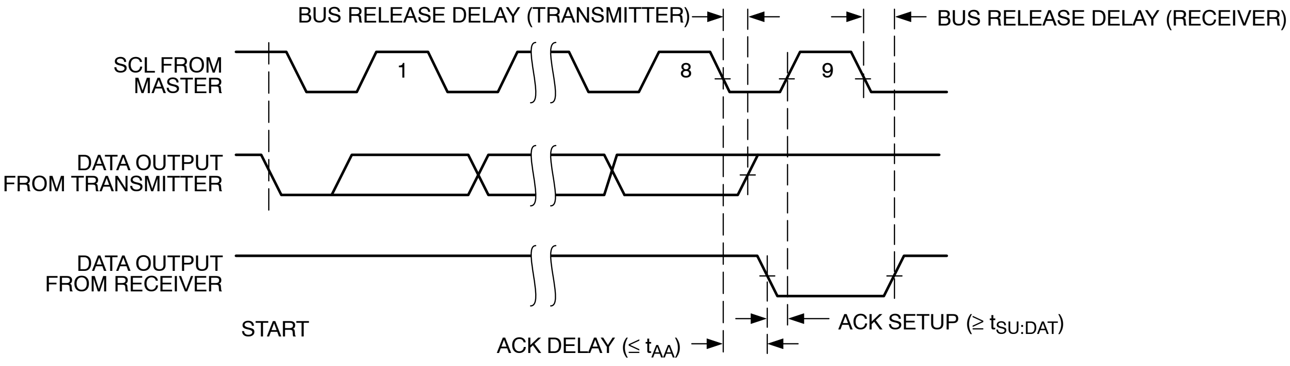


Figure 4. Acknowledge Timing

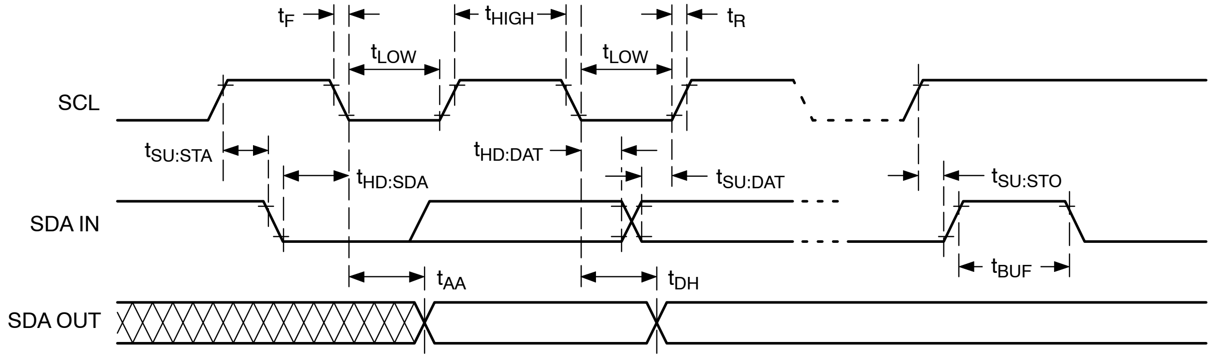


Figure 5. Bus Timing

WRITE OPERATIONS

Byte Write

To write data to memory, the Master creates a START condition on the bus and then broadcasts a Slave address with the R/$\overline{W}$ bit set to ‘0’. The Master then sends two address bytes and a data byte and concludes the session by creating a STOP condition on the bus. The Slave responds with ACK after every byte sent by the Master (Figure 6). The STOP starts the internal Write cycle, and while this operation is in progress (t_{WR}), the SDA output is tri−stated and the Slave does not acknowledge the Master (Figure 7).

Page Write

The Byte Write operation can be expanded to Page Write, by sending more than one data byte to the Slave before issuing the STOP condition (Figure 8). Up to 32 distinct data bytes can be loaded into the internal Page Write Buffer starting at the address provided by the Master. The page address is latched, and as long as the Master keeps sending data, the internal byte address is incremented up to the end of page, where it then wraps around (within the page). New data can therefore replace data loaded earlier. Following the STOP, data loaded during the Page Write session will be written to memory in a single internal Write cycle (t_{WR}).

Acknowledge Polling

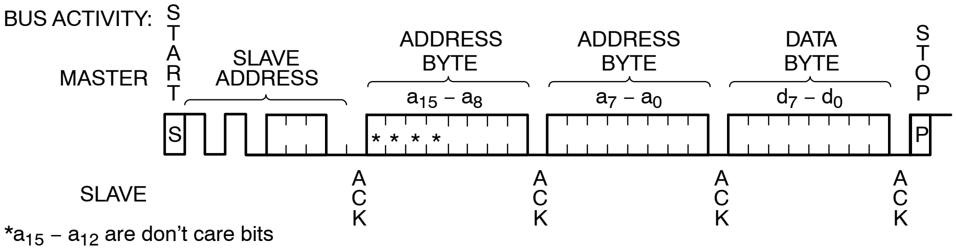
As soon (and as long) as internal Write is in progress, the Slave will not acknowledge the Master. This feature enables the Master to immediately follow−up with a new Read or Write request, rather than wait for the maximum specified Write time (t_{WR}) to elapse. Upon receiving a NoACK response from the Slave, the Master simply repeats the request until the Slave responds with ACK.

Hardware Write Protection

With the WP pin held HIGH, the entire memory is protected against Write operations. If the WP pin is left floating or is grounded, it has no impact on the Write operation. The state of the WP pin is strobed on the last falling edge of SCL immediately preceding the 1st data byte (Figure 9). If the WP pin is HIGH during the strobe interval, the Slave will not acknowledge the data byte and the Write request will be rejected.

Delivery State

The CAT24C32 is shipped erased, i.e., all bytes are FFh.



*$a_{15} – a_{12}$ are don’t care bits

Figure 6. Byte Write Sequence

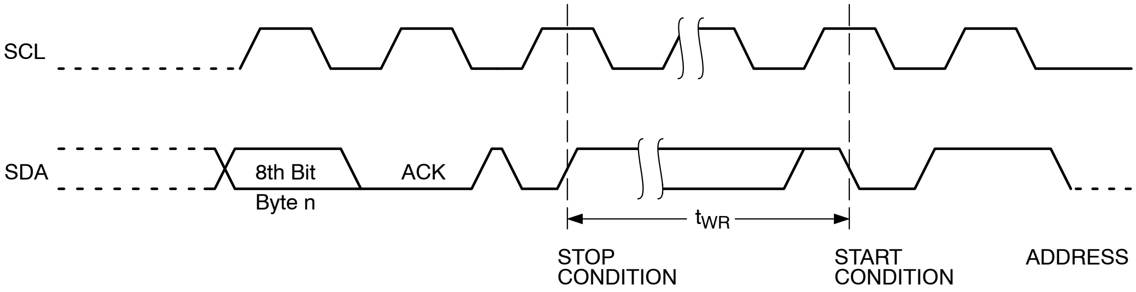
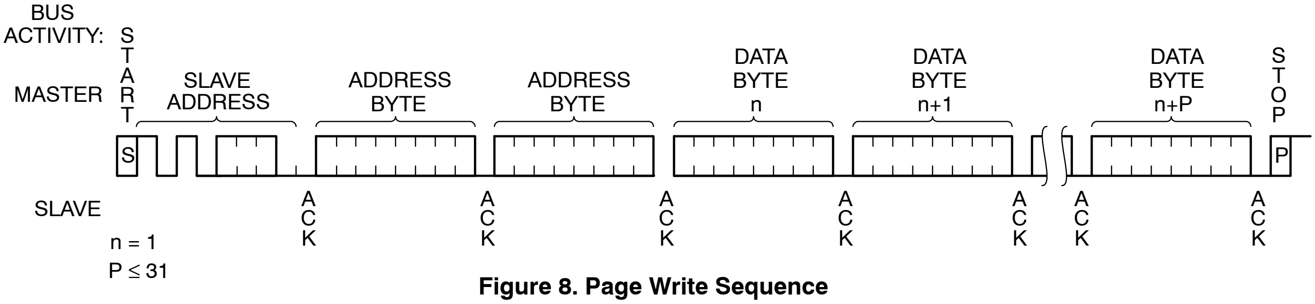


Figure 7. Write Cycle Timing



n = 1
P ≤ 31

Figure 8. Page Write Sequence

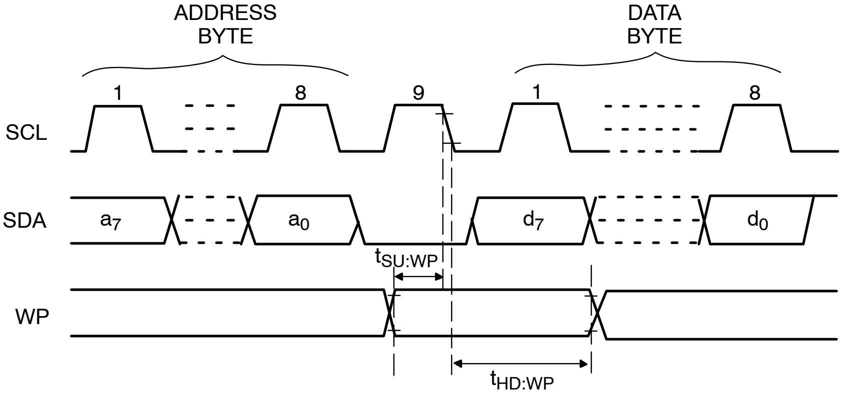


Figure 9. WP Timing

READ OPERATIONS

Immediate Read

To read data from memory, the Master creates a START condition on the bus and then broadcasts a Slave address with the R/$\overline{W}$ bit set to '1'. The Slave responds with ACK and starts shifting out data residing at the current address. After receiving the data, the Master responds with NoACK and terminates the session by creating a STOP condition on the bus (Figure 10). The Slave then returns to Standby mode.

Selective Read

To read data residing at a specific address, the selected address must first be loaded into the internal address register. This is done by starting a Byte Write sequence, whereby the Master creates a START condition, then broadcasts a Slave address with the R/$\overline{W}$ bit set to '0' and then sends two address bytes to the Slave. Rather than completing the Byte Write sequence by sending data, the Master then creates a START condition and broadcasts a Slave address with the R/$\overline{W}$ bit set to '1'. The Slave responds with ACK after every byte sent by the Master and then sends out data residing at the selected address. After receiving the data, the Master responds with NoACK and then terminates the session by creating a STOP condition on the bus (Figure 11).

Sequential Read

If, after receiving data sent by the Slave, the Master responds with ACK, then the Slave will continue transmitting until the Master responds with NoACK followed by STOP (Figure 12). During Sequential Read the internal byte address is automatically incremented up to the end of memory, where it then wraps around to the beginning of memory.

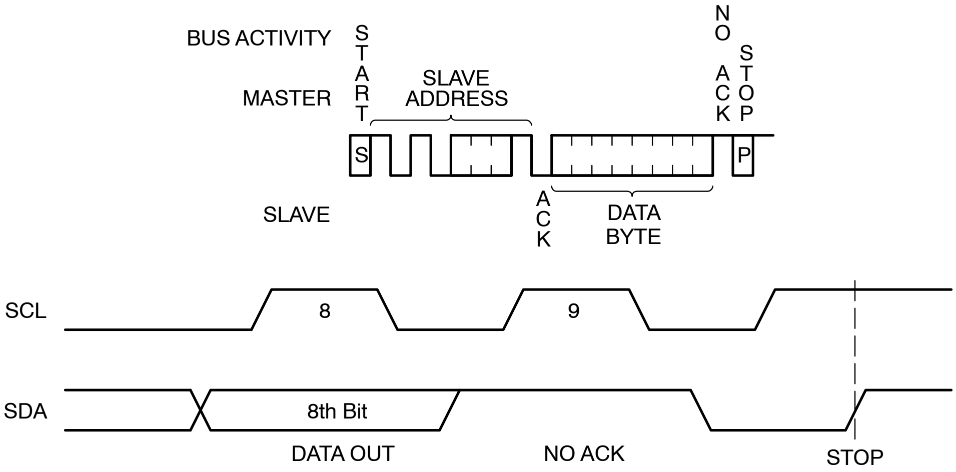


Figure 10. Immediate Read Sequence and Timing

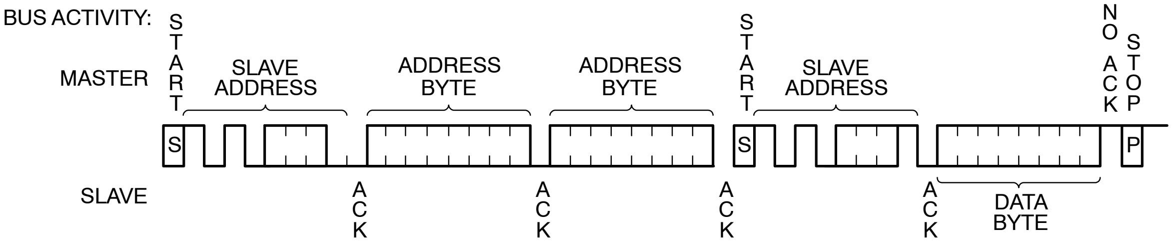


Figure 11. Selective Read Sequence

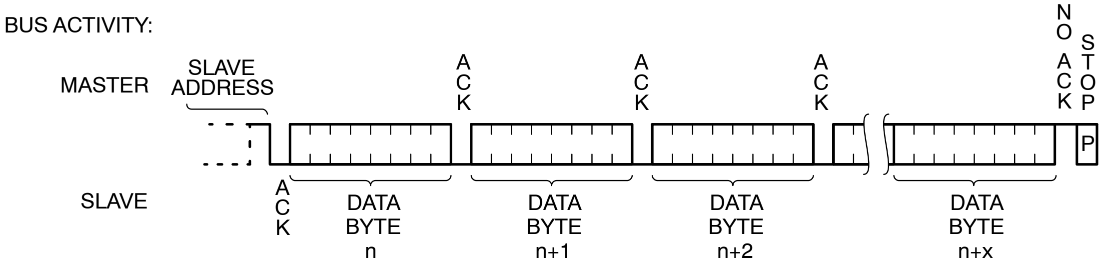
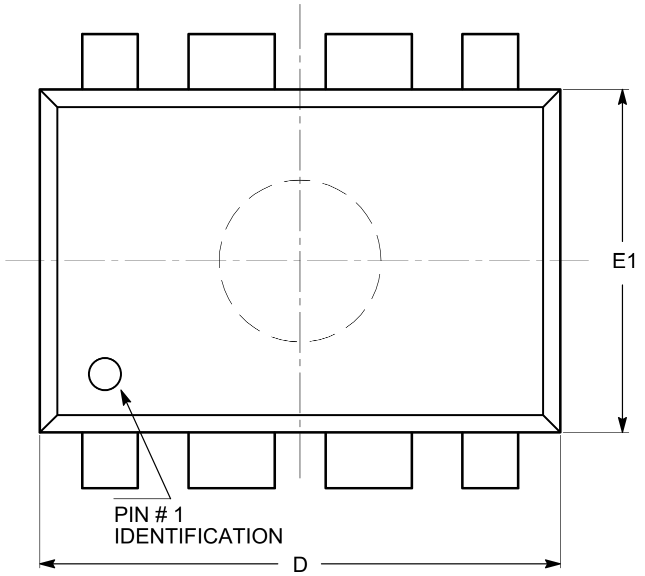


Figure 12. Sequential Read Sequence

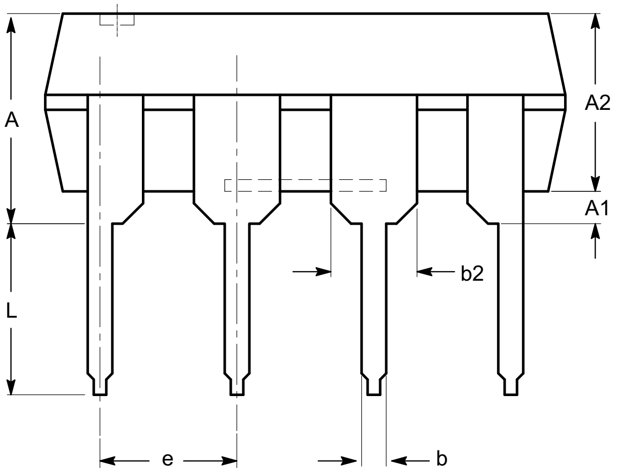
PACKAGE DIMENSIONS

PDIP−8, 300 mils
CASE 646AA−01
ISSUE A

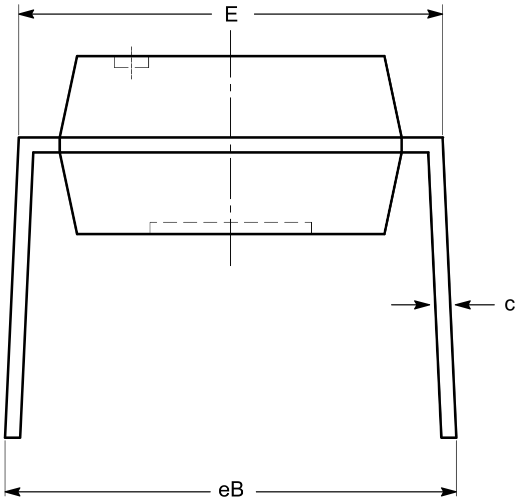


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.36	0.46	0.56
b2	1.14	1.52	1.78
c	0.20	0.25	0.36
D	9.02	9.27	10.16
E	7.62	7.87	8.25
E1	6.10	6.35	7.11
e	2.54 BSC		
eB	7.87		10.92
L	2.92	3.30	3.80



SIDE VIEW



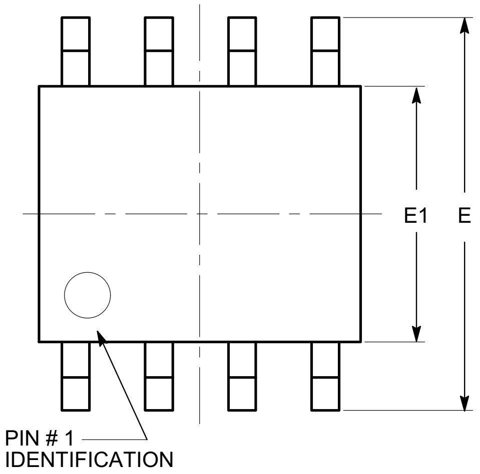
END VIEW

Notes:

(1) All dimensions are in millimeters.
(2) Complies with JEDEC MS-001.

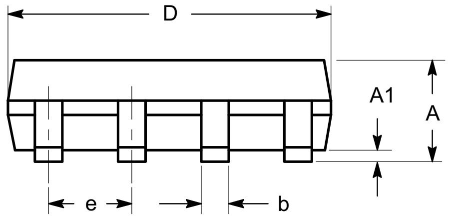
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD−01
ISSUE O

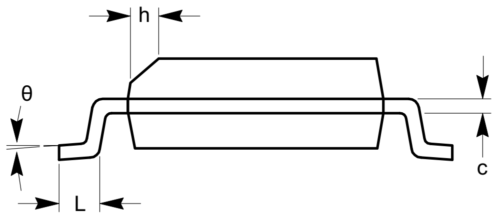


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW



END VIEW

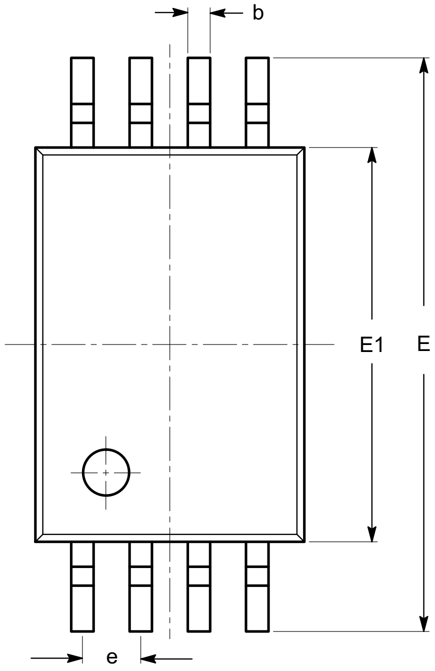
Notes:

(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

PACKAGE DIMENSIONS

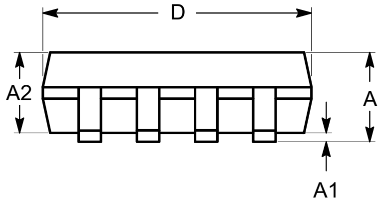
TSSOP8, 4.4x3

CASE 948AL−01
ISSUE O

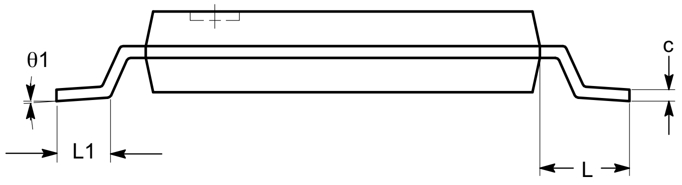


SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
θ	0º		8º

TOP VIEW



SIDE VIEW



END VIEW

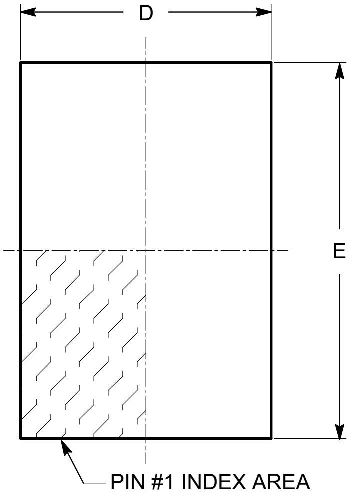
Notes:

(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

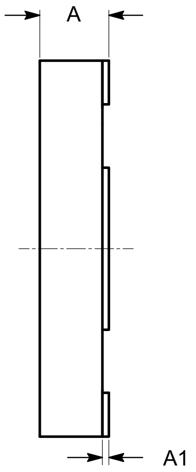
PACKAGE DIMENSIONS

UDFN8, 2x3 EXTENDED PAD

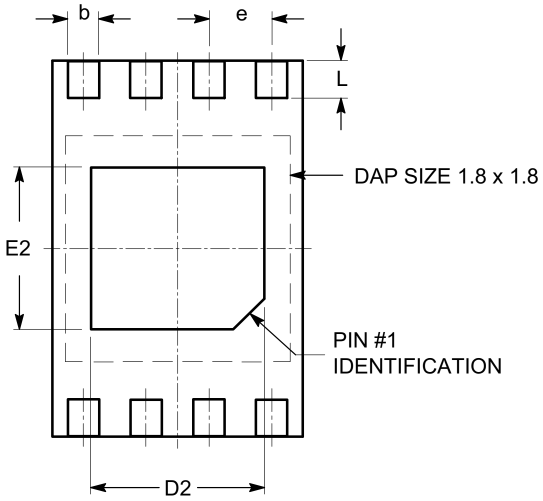
CASE 517AZ−01
ISSUE O



TOP VIEW



SIDE VIEW

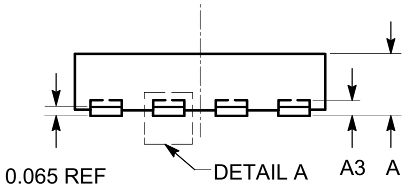


BOTTOM VIEW

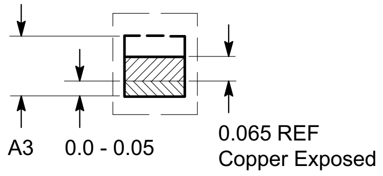
SYMBOL	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0.00	0.02	0.05
A3	0.127 REF		
b	0.20	0.25	0.30
D	1.95	2.00	2.05
D2	1.35	1.40	1.45
E	2.95	3.00	3.05
E2	1.25	1.30	1.35
e	0.50 REF		
L	0.25	0.30	0.35

Notes:

(1) All dimensions are in millimeters.
(2) Refer JEDEC MO-236/MO-252.



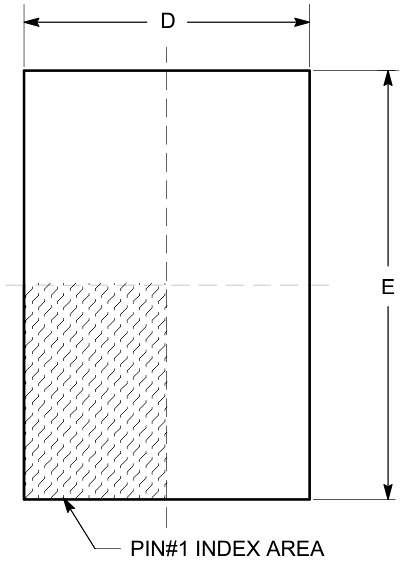
FRONT VIEW



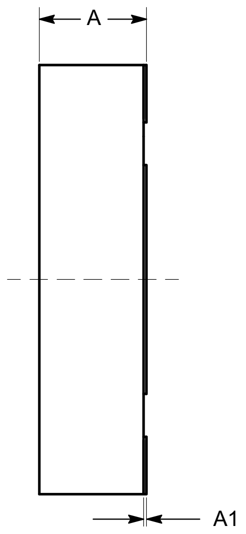
DETAIL A

PACKAGE DIMENSIONS

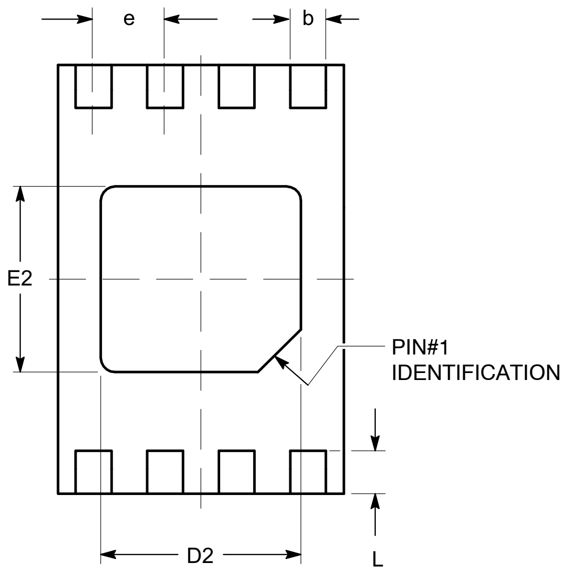
TDFN8, 2x3
CASE 511AK−01
ISSUE A



TOP VIEW



SIDE VIEW

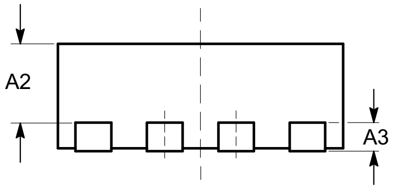


BOTTOM VIEW

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.45	0.55	0.65
A3	0.20 REF		
b	0.20	0.25	0.30
D	1.90	2.00	2.10
D2	1.30	1.40	1.50
E	2.90	3.00	3.10
E2	1.20	1.30	1.40
e	0.50 TYP		
L	0.20	0.30	0.40

Notes:

(1) All dimensions are in millimeters.
(2) Complies with JEDEC MO-229.

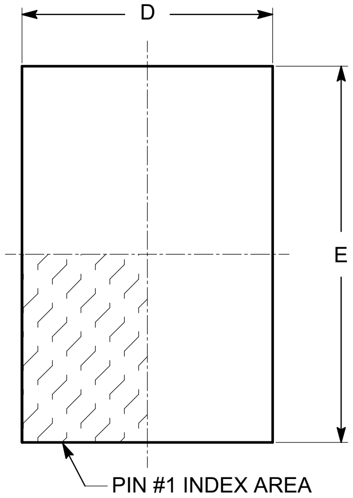


FRONT VIEW

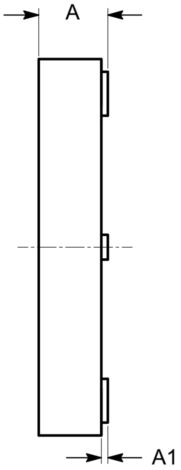
PACKAGE DIMENSIONS

UDFN8, 2x3

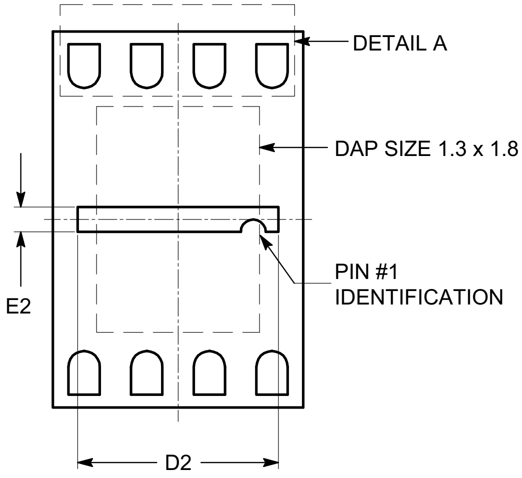
CASE 517AX−01
ISSUE O



TOP VIEW

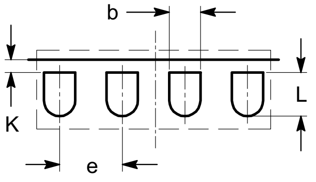


SIDE VIEW

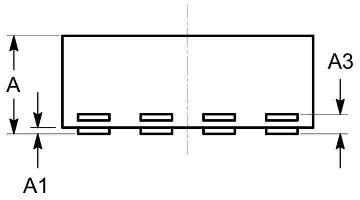


BOTTOM VIEW

SYMBOL	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0.00	0.02	0.05
A3		0.127 REF	
b	0.20	0.25	0.30
D	1.90	2.00	2.10
D2	1.50	1.60	1.70
E	2.90	3.00	3.10
E2	0.10	0.20	0.30
e		0.50 TYP	
K		0.10 REF	
L	0.30	0.35	0.40



DETAIL A



FRONT VIEW

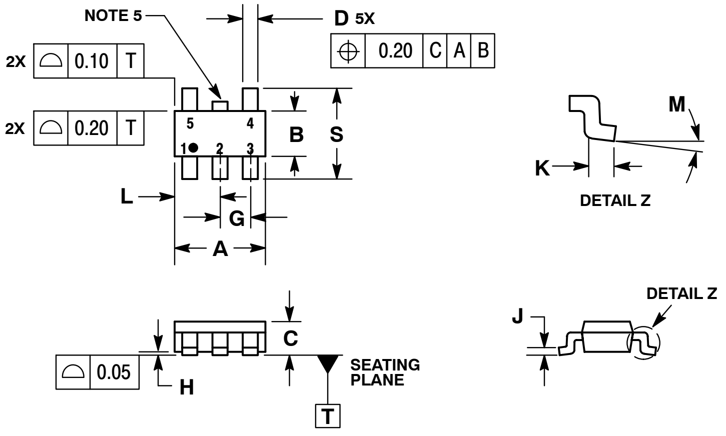
Notes:

(1) All dimensions are in millimeters.
(2) Complies with JEDEC MO-229.

PACKAGE DIMENSIONS

TSOP−5

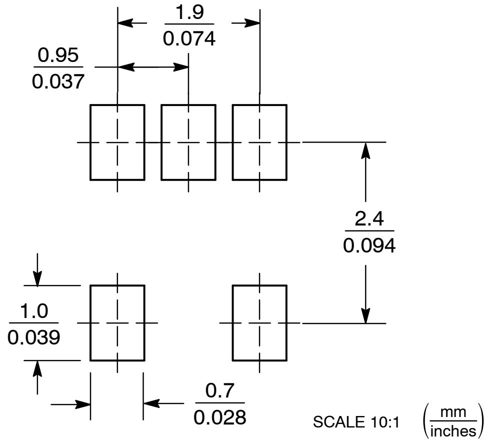
CASE 483−02
ISSUE H



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	3.00 BSC	
B	1.50 BSC	
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
L	1.25	1.55
M	0 °	10 °
S	2.50	3.00

SOLDERING FOOTPRINT*

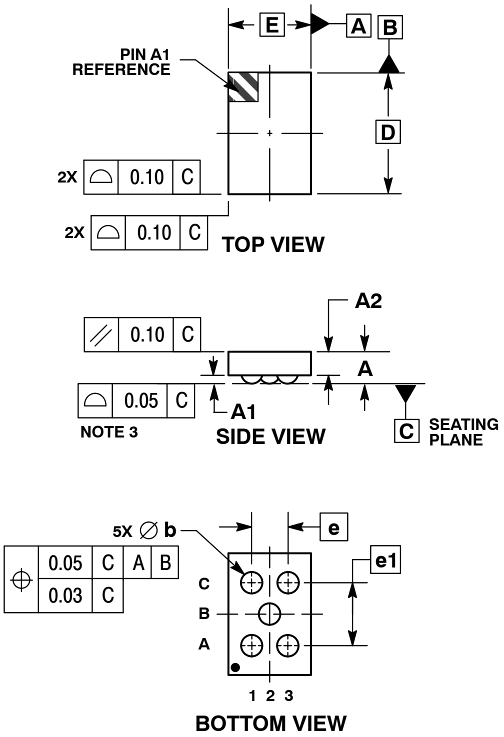


*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

WLCSP5, 1.34x0.91

CASE 567GN
ISSUE A

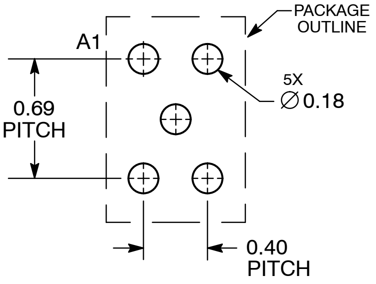


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. DIMENSION b IS MEASURED AT THE MAXIMUM BALL DIAMETER PARALLEL TO DATUM C.

	MILLIMETERS	
DIM	**MIN**	**MAX**
A	0.32	0.40
A1	0.08	0.12
A2	0.26 REF	
b	0.16	0.20
D	1.34 BSC	
E	0.91 BSC	
e	0.40 BSC	
e1	0.693 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Ordering Information

Device Order Number	Specific Device Marking*	Package Type	Temperature Range	Lead Finish	Shipping
CAT24C32HU3I−GT3	C5V	UDFN8	I = Industrial (−40°C to +85°C)	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT24C32HU4I−GT3	C5U	UDFN8	I = Industrial (−40°C to +85°C)	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT24C32HU4E−GT3	C5U	UDFN8	E = Extended (−40°C to +125°C)	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT24C32C5ATR**	2	WLCSP−5	I = Industrial (−40°C to +85°C)	N/A	Tape & Reel, 5,000 Units / Reel
CAT24C32LI−G	24C32F	PDIP−8	I = Industrial (−40°C to +85°C)	NiPdAu	Tube, 50 Units / Tube
CAT24C32LE−G	24C32F	PDIP−8	E = Extended (−40°C to +125°C)	NiPdAu	Tube, 50 Units / Tube
CAT24C32TSI−T3	C5	TSOP−5	I = Industrial (−40°C to +85°C)	Matte−Tin	Tape & Reel, 3,000 Units / Reel
CAT24C32VP2I−GT3	C5T	TDFN−8	I = Industrial (−40°C to +85°C)	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT24C32VP2E−GT3	C5T	TDFN−8	E = Extended (−40°C to +125°C)	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT24C32WI−G	24C32F	SOIC−8, JEDEC	I = Industrial (−40°C to +85°C)	NiPdAu	Tube, 100 Units / Tube
CAT24C32WE−G	24C32F	SOIC−8, JEDEC	E = Extended (−40°C to +125°C)	NiPdAu	Tube, 100 Units / Tube
CAT24C32WI−GT3	24C32F	SOIC−8, JEDEC	I = Industrial (−40°C to +85°C)	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT24C32WE−GT3	24C32F	SOIC−8, JEDEC	E = Extended (−40°C to +125°C)	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT24C32YI−G	C32F	TSSOP−8	I = Industrial (−40°C to +85°C)	NiPdAu	Tube, 100 Units / Tube
CAT24C32YE−G	C32F	TSSOP−8	E = Extended (−40°C to +125°C)	NiPdAu	Tube, 100 Units / Tube
CAT24C32YI−GT3	C32F	TSSOP−8	I = Industrial (−40°C to +85°C)	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT24C32YE−GT3	C32F	TSSOP−8	E = Extended (−40°C to +125°C)	NiPdAu	Tape & Reel, 3,000 Units / Reel

* Marking for New Product (Rev F)

** Preliminary, please contact factory for availability.

10. All packages are RoHS−compliant (Lead−free, Halogen−free).
11. The standard lead finish is NiPdAu.
12. For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.
13. **The TDFN 2 x 3 x 0.75 mm (VP2) and UDFN 2 x 3 x 0.5 mm (HU3) are not recommended for new design. Please replace with UDFN 2 x 3 x 0.5 mm, extended pad (HU4).**
14. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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