

Features

- Ultra-low standby power
 - Typical standby current: 5.5 μ A
 - Maximum standby current: 16 μ A
- High speed: 45 ns / 55 ns
- Embedded error-correcting code (ECC) for single-bit error correction
- Wide voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V
- 1.0-V data retention
- Transistor-transistor logic (TTL) compatible inputs and outputs
- ERR pin to indicate 1-bit error detection and correction
- Easy memory expansion with \overline{CE}_1 and CE_2 features
- Available in Pb-free 119-ball PBGA package, 512 K × 32 bits SRAM

Functional Description

The CY62162G and CY62162GE devices are high performance CMOS MoBL SRAM organized as 512K words by 32-bits. Both CY62162G and CY62162GE are available with dual chip enables. CY62162GE includes an error indication pin that signals the host processor in the case of a single bit error-detection and correction event. It is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down

feature that reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99% when deselected (CE_1 HIGH or CE_2 LOW or \overline{B}_{A-D} HIGH). The input and output pins (I/O₀ through I/O₃₁) are placed in a high impedance state when deselected (CE_1 HIGH or CE_2 LOW) or outputs are disabled (OE HIGH) or the byte selects are disabled (\overline{B}_{A-D} HIGH).

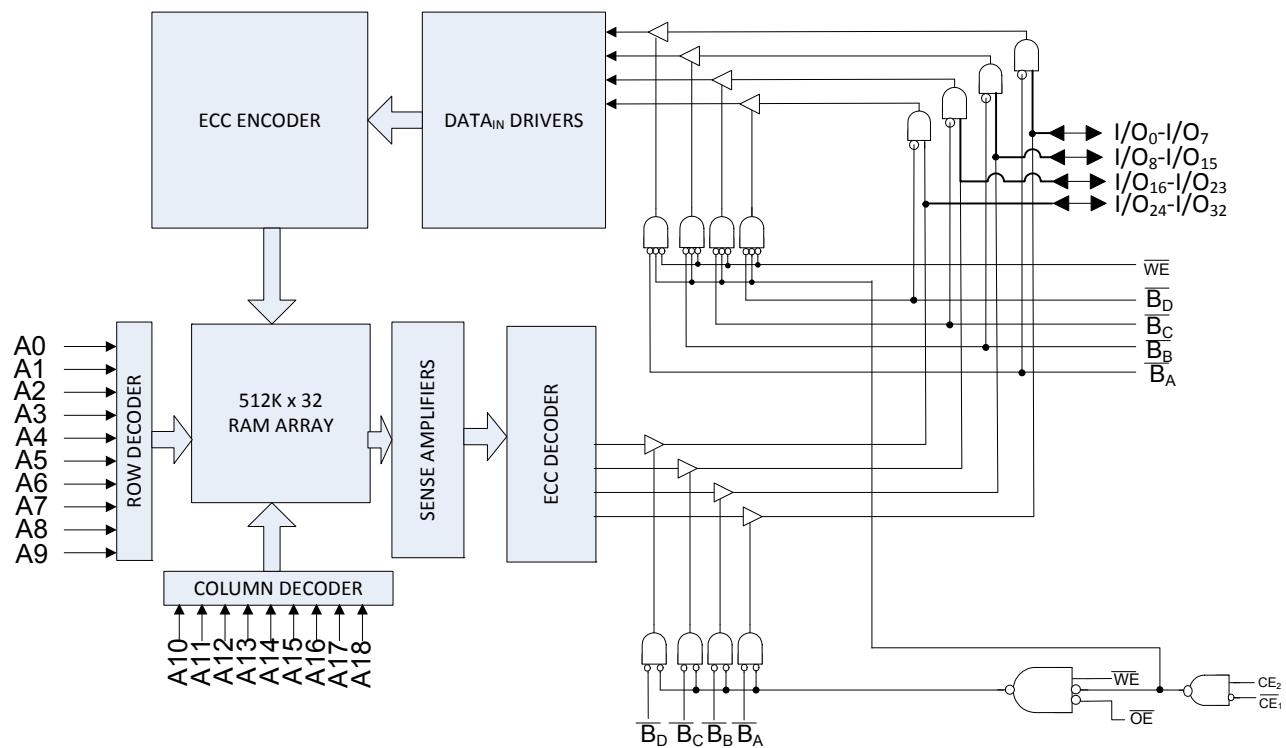
To write to the device, take chip enables (\overline{CE}_1 LOW, CE_2 HIGH) and write enable (WE) input LOW. If byte enable A (B_A) is LOW, then data from I/O pins (I/O₀ through I/O₇) is written into the location specified on the address pins (A₀ through A₁₈). If byte enable B (B_B) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₈). Likewise, \overline{B}_C and \overline{B}_D correspond with the I/O pins I/O₁₆ to I/O₂₃ and I/O₂₄ to I/O₃₁, respectively.

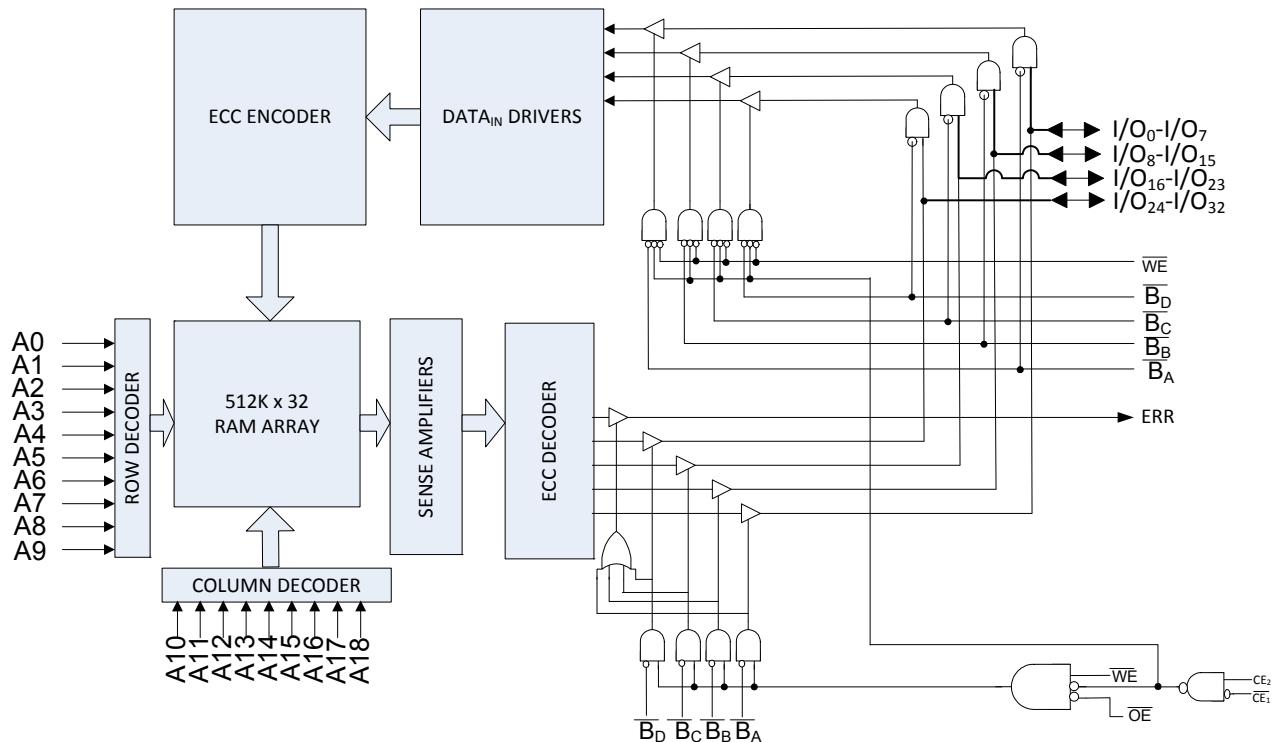
To read from the device, take chip enables (\overline{CE}_1 LOW, CE_2 HIGH), and output enable (OE) LOW while forcing the write enable (WE) HIGH. If the first byte enable (B_A) is LOW, then data from the memory location specified by the address pins appear on I/O₀ to I/O₇. If byte enable (B_B) is LOW, then data from memory appears on I/O₈ to I/O₁₅. Likewise, \overline{B}_C and \overline{B}_D correspond to the third and fourth bytes. During Read operation, in case of a single bit error detection and correction, ERR is asserted HIGH^[1]. See the [Truth Table – CY62162G / CY62162GE on page 15](#) for a complete description of read and write modes.

CY62162G and CY62162GE devices are available in a 119-ball PBGA package with center power and ground pinout.

Note

1. This device does not support automatic write-back on error detection.

Logic Block Diagram – CY62162G


Logic Block Diagram – CY62162GE


Contents

Pin Configurations	5
Product Portfolio	6
Maximum Ratings	7
Operating Range	7
Electrical Characteristics	7
Capacitance	8
Thermal Resistance	8
AC Test Loads and Waveforms	8
Data Retention Characteristics	9
Data Retention Waveform	9
Switching Characteristics	10
Switching Waveforms	11
Truth Table – CY62162G / CY62162GE	15
ERR Output – CY62162GE	15
Ordering Information	16
Ordering Code Definitions	16
Package Diagram	17
Acronyms	18
Document Conventions	18
Units of Measure	18
Document History Page	19
Sales, Solutions, and Legal Information	20
Worldwide Sales and Design Support	20
Products	20
PSoC® Solutions	20
Cypress Developer Community	20
Technical Support	20

Pin Configurations

Figure 1. 119-ball FBGA pinout [2]
CY62162G (512 K × 32)

	1	2	3	4	5	6	7
A	I/O ₁₆	A ₄	A ₃	A ₂	A ₁	A ₀	I/O ₀
B	I/O ₁₇	A ₁₈	A ₁₇	CE ₁	A ₁₆	A ₁₅	I/O ₁
C	I/O ₁₈	̄B _c	CE ₂	NC	NC	̄B _a	I/O ₂
D	I/O ₁₉	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₃
E	I/O ₂₀	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	I/O ₄
F	I/O ₂₁	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₅
G	I/O ₂₂	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	I/O ₆
H	I/O ₂₃	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₇
J	NC	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	NC
K	I/O ₂₄	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₈
L	I/O ₂₅	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	I/O ₉
M	I/O ₂₆	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₁₀
N	I/O ₂₇	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	I/O ₁₁
P	I/O ₂₈	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₁₂
R	I/O ₂₉	A ₁₄	̄B _d	NC	B _b	A ₁₃	I/O ₁₃
T	I/O ₃₀	A ₁₂	A ₁₁	̄WE	A ₁₀	A ₉	I/O ₁₄
U	I/O ₃₁	A ₈	A ₇	̄OE	A ₆	A ₅	I/O ₁₅

Figure 2. 119-ball FBGA pinout [2, 3]
CY62162GE (512 K × 32)

	1	2	3	4	5	6	7
A	I/O ₁₆	A ₄	A ₃	A ₂	A ₁	A ₀	I/O ₀
B	I/O ₁₇	A ₁₈	A ₁₇	CE ₁	A ₁₆	A ₁₅	I/O ₁
C	I/O ₁₈	̄B _c	CE ₂	NC	NC	̄B _a	I/O ₂
D	I/O ₁₉	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₃
E	I/O ₂₀	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	I/O ₄
F	I/O ₂₁	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₅
G	I/O ₂₂	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	I/O ₆
H	I/O ₂₃	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₇
J	ERR	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	NC
K	I/O ₂₄	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₈
L	I/O ₂₅	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	I/O ₉
M	I/O ₂₆	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₁₀
N	I/O ₂₇	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	I/O ₁₁
P	I/O ₂₈	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₁₂
R	I/O ₂₉	A ₁₄	̄B _d	NC	B _b	A ₁₃	I/O ₁₃
T	I/O ₃₀	A ₁₂	A ₁₁	̄WE	A ₁₀	A ₉	I/O ₁₄
U	I/O ₃₁	A ₈	A ₇	̄OE	A ₆	A ₅	I/O ₁₅

Note

2. NC pins are not connected internally to the die.
3. ERR is an Output pin. If not used, this pin should be left floating.

Product Portfolio

Product	Features and Options (see the Pin Configurations Section)	Range	V _{CC} Range (V)	Speed (ns)	Power Dissipation			
					Operating I _{CC} , (mA)		Standby, I _{SB2} (µA)	
					f = f _{max}			
					Typ ^[4]	Max	Typ ^[4]	Max
CY62162G(E)18	Dual Chip Enable Optional Error indication on ERR pinout	Industrial	1.65 V–2.2 V	55	29	32	7	26
CY62162G(E)30			2.2 V–3.6 V	45	29	36	5.5	16

Note

4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for V_{CC} range of 2.2 V–3.6 V), T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature -65°C to $+150^{\circ}\text{C}$

Ambient temperature

with power applied -55°C to $+125^{\circ}\text{C}$

Supply voltage to ground potential -0.5 V to $V_{\text{CC}} + 0.5\text{ V}$

DC voltage applied to outputs
in high Z State^[6] -0.5 V to $V_{\text{CC}} + 0.5\text{ V}$

DC input voltage^[6] -0.5 V to $V_{\text{CC}} + 0.5\text{ V}$

Output current into outputs (LOW) 20 mA

Static discharge voltage
(per MIL-STD-883, method 3015) $> 2001\text{ V}$

Latch-up current $> 140\text{ mA}$

Operating Range

Device	Range	Ambient Temperature	$V_{\text{CC}}^{[7]}$
CY62162G	Industrial	-40°C to $+85^{\circ}\text{C}$	1.65 V to 2.2 V, 2.2 V to 3.6 V

Electrical Characteristics

Over the Operating Range

Parameter	Description		Test Conditions		Min	Typ ^[8]	Max	Unit
V_{OH}	Output HIGH voltage	1.65 V to 2.2 V	$V_{\text{CC}} = \text{Min}$, $I_{\text{OH}} = -0.1\text{ mA}$		1.4	—	—	V
		2.2 V to 2.7 V	$V_{\text{CC}} = \text{Min}$, $I_{\text{OH}} = -1.0\text{ mA}$		2.0	—	—	
		2.7 V to 3.6 V	$V_{\text{CC}} = \text{Min}$, $I_{\text{OH}} = -4.0\text{ mA}$		2.2	—	—	
V_{OL}	Output LOW voltage	1.65 V to 2.2 V	$V_{\text{CC}} = \text{Min}$, $I_{\text{OL}} = 0.1\text{ mA}$		—	—	0.2	V
		2.2 V to 2.7 V	$V_{\text{CC}} = \text{Min}$, $I_{\text{OL}} = 2\text{ mA}$		—	—	0.4	
		2.7 V to 3.6 V	$V_{\text{CC}} = \text{Min}$, $I_{\text{OL}} = 8\text{ mA}$		—	—	0.4	
V_{IH}	Input HIGH voltage	1.65 V to 2.2 V	—		1.4	—	$V_{\text{CC}} + 0.2$	V
		2.2 V to 2.7 V	—		2.0	—	$V_{\text{CC}} + 0.3$	
		2.7 V to 3.6 V	—		2.0	—	$V_{\text{CC}} + 0.3$	
V_{IL}	Input LOW voltage ^[6]	1.65 V to 2.2 V	—		-0.2	—	0.4	mA
		2.2 V to 2.7 V	—		-0.3	—	0.6	
		2.7 V to 3.6 V	—		-0.3	—	0.8	
I_{IX}	Input leakage current		$\text{GND} \leq V_{\text{IN}} \leq V_{\text{CC}}$		-1.0	—	+1.0	μA
I_{OZ}	Output leakage current		$\text{GND} \leq V_{\text{OUT}} \leq V_{\text{CC}}$, Output disabled		-1.0	—	+1.0	
I_{CC}	V_{CC} operating supply current	$f = 22.22\text{ MHz}$ (45 ns)	$V_{\text{CC}} = V_{\text{CC(max)}}$		—	29.0	36.0	mA
		$f = 18.18\text{ MHz}$ (55 ns)	$I_{\text{OUT}} = 0\text{ mA}$		—	29.0	32.0	
		$f = 1\text{ MHz}$	CMOS levels		—	7.0	9.0	
$I_{\text{SB1}}^{[9]}$	Automatic power down current – CMOS inputs; $V_{\text{CC}} = 2.2$ to 3.6 V		$\overline{CE}_1 \geq V_{\text{CC}} - 0.2\text{ V}$ or $\overline{CE}_2 \leq 0.2\text{ V}$ or $\overline{B}_{\text{A-D}} \geq V_{\text{CC}} - 0.2\text{ V}$,		—	5.5	16.0	μA
	Automatic power down current – CMOS inputs; $V_{\text{CC}} = 1.65$ to 2.2 V		$V_{\text{IN}} \geq V_{\text{CC}} - 0.2\text{ V}$, $V_{\text{IN}} \leq 0.2\text{ V}$, $f = f_{\text{max}}$ (address and data only), $f = 0$ (OE, and WE), $V_{\text{CC}} = V_{\text{CC(max)}}$		—	7.0	26.0	
$I_{\text{SB2}}^{[9]}$	Automatic power down current – CMOS inputs; $V_{\text{CC}} = 2.2$ to 3.6 V		$\overline{CE}_1 \geq V_{\text{CC}} - 0.2\text{ V}$ or $\overline{CE}_2 \leq 0.2\text{ V}$ or $\overline{B}_{\text{A-D}} \geq V_{\text{CC}} - 0.2\text{ V}$,		—	5.5	16.0	μA
	Automatic power down current – CMOS inputs; $V_{\text{CC}} = 1.65$ to 2.2 V		$V_{\text{IN}} \geq V_{\text{CC}} - 0.2\text{ V}$ or $V_{\text{IN}} \leq 0.2\text{ V}$, $f = 0$, $V_{\text{CC}} = V_{\text{CC(max)}}$		—	7.0	26.0	

Notes

- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{\text{CC}} = 1.8\text{ V}$ (for V_{CC} range of 1.65 V–2.2 V), $V_{\text{CC}} = 3\text{ V}$ (for V_{CC} range of 2.2 V–3.6 V), $T_A = 25^{\circ}\text{C}$.
- $V_{\text{IL(min)}} = -2.0\text{ V}$ and $V_{\text{IH(max)}} = V_{\text{CC}} + 2\text{ V}$ for pulse durations of less than 2 ns.
- Full device AC operation assumes a 100- μs ramp time from 0 to V_{CC} (min) and 200- μs wait time after V_{CC} stabilizes to its operational value.
- Indicates the value for the center of distribution at 3.0 V, 25 °C and not 100% tested.
- Chip enables (\overline{CE}_1 and \overline{CE}_2) must be tied to CMOS levels to meet the $I_{\text{SB1}}/I_{\text{SB2}}/I_{\text{CCDR}}$ spec. Other inputs can be left floating.

Capacitance

Parameter ^[10]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = V_{CC(\text{typ})}$	10	pF
C_{OUT}	Output capacitance			

Thermal Resistance

Parameter ^[10]	Description	Test Conditions	119-ball BGA	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3×4.5 inch, 2-layer printed circuit board	20.92	$^\circ\text{C/W}$
Θ_{JC}	Thermal resistance (junction to case)		15.84	

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms

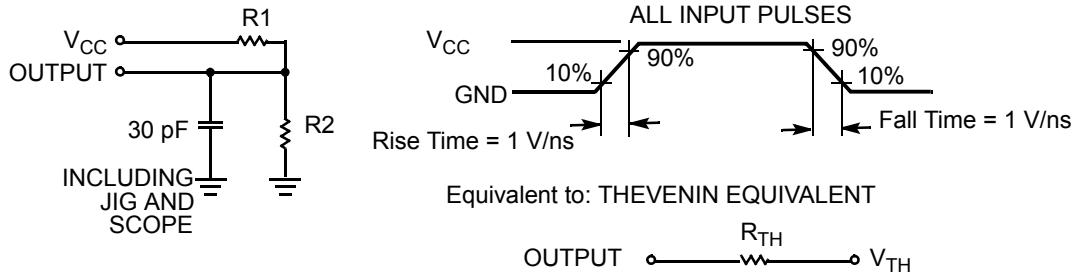


Table 1. AC Test Loads

Parameter	1.8 V	2.5 V	3.0 V	Unit
R1	13500	16667	1103	Ω
R2	10800	15385	1554	
R_{TH}	6000	8000	645	
V_{TH}	0.8	1.2	1.75	V

Note

10. Tested initially and after any design or process changes that may affect these parameters.

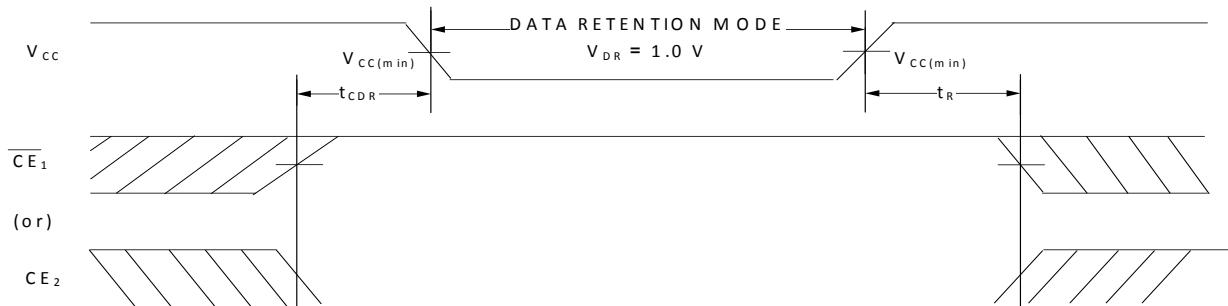
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ [11]	Max	Unit
V_{DR}	V_{CC} for data retention		1.0	—	—	V
I_{CCDR} [12, 13]	Data retention current	1.0 V $\leq V_{CC} \leq$ 2.2 V, $\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or $\overline{B}_{A-D} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	—	7.0	26.0	μA
		2.2 V $< V_{CC} \leq$ 3.6 V, $\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or $\overline{B}_{A-D} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	—	5.5	16.0	
t_{CDR} [14]	Chip deselect to data retention time	—	0	—	—	ns
t_R [14, 15]	Operation recovery time	—	45 / 55	—	—	ns

Data Retention Waveform

Figure 4. Data Retention Waveform



Notes

11. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = 1.8$ V for the range 1.7 V to 2.2 V; 3 V for the range 2.2 V to 3.6 V, $T_A = 25$ °C.

12. Only chip enables (\overline{CE}_1 and CE_2) and all byte enables (\overline{B}_{A-D}) need to be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

13. \overline{B}_{A-D} is the AND of \overline{B}_A , \overline{B}_B , \overline{B}_C and \overline{B}_D . Chip is deselected by either disabling the chip enable signals or by disabling all byte enables together.

14. These parameters are guaranteed by design and are not tested.

15. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(\min)} \geq 100$ μ s or stable at $V_{CC(\min)} \geq 100$ μ s.

Switching Characteristics

Over the Operating Range

Parameter [16, 17]	Description	45 ns		55 ns		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read cycle time	45.0	—	55.0	—	ns
t_{AA}	Address to data/ERR valid	—	45.0	—	55.0	
t_{OHA}	Data/ERR hold from address change	10	—	10.0	—	
t_{ACE}	\overline{CE}_1 LOW and CE_2 HIGH to data/ERR valid	—	45.0	—	55.0	
t_{DOE}	\overline{OE} LOW to data/ERR valid	—	22.0	—	25.0	
t_{LZOE}	\overline{OE} LOW to low Z [17, 18]	5.0	—	5.0	—	
t_{HZOE}	\overline{OE} HIGH to high Z [17, 18, 19]	—	18.0	—	18.0	
t_{LZCE}	\overline{CE}_1 LOW and CE_2 HIGH to low Z [17, 18]	10.0	—	10.0	—	
t_{HZCE}	\overline{CE}_1 HIGH and CE_2 LOW to high Z [17, 18, 19]	—	18.0	—	18.0	
t_{PU}	\overline{CE}_1 LOW and CE_2 HIGH to power-up [20]	0	—	0	—	
t_{PD}	\overline{CE}_1 HIGH and CE_2 LOW to power-down [20]	—	45.0	—	55.0	
t_{DBE}	Byte enable LOW to data valid	—	45.0	—	55.0	
t_{LZBE}	Byte enable LOW to low Z [17]	5.0	—	5.0	—	
t_{HZBE}	Byte enable HIGH to high Z [17, 19]	—	18.0	—	18.0	
Write Cycle [21, 22]						
t_{WC}	Write cycle time	45.0	—	55.0	—	ns
t_{SCE}	\overline{CE}_1 LOW and CE_2 HIGH to write end	35.0	—	40.0	—	
t_{AW}	Address setup to write end	35.0	—	40.0	—	
t_{HA}	Address hold from write end	0	—	0	—	
t_{SA}	Address setup to write start	0	—	0	—	
t_{PWE}	\overline{WE} pulse width	35.0	—	40.0	—	
t_{BW}	Byte enable LOW to write end	35.0	—	40.0	—	
t_{SD}	Data setup to write end	25.0	—	25.0	—	
t_{HD}	Data hold from write end	0	—	0	—	
t_{HZWE}	\overline{WE} LOW to high Z [17, 19, 18]	—	18.0	—	20.0	
t_{LZWE}	\overline{WE} HIGH to low Z [17, 18]	10.0	—	10.0	—	

Notes

16. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1 V/ns, timing reference levels of V_{TH} , input pulse levels of 0 to $V_{CC(ty)}$, and output loading of the specified I_{OL}/I_{OH} as shown in [Table 1 on page 8](#).
17. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
18. Tested initially and after any design or process changes that may affect these parameters.
19. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
20. These parameters are guaranteed by design and are not tested.
21. The internal write time of the memory is defined by the overlap of \overline{CE} and \overline{WE} LOW. Chip enable must be active and \overline{WE} and byte enables must be LOW to initiate a write, and the transition of any of these signals terminate the write. The input data setup and hold timing are referenced to the leading edge of the signal that terminates the write.
22. The minimum write cycle pulse width for Write Cycle No. 2 (\overline{WE} Controlled, \overline{OE} LOW) should be equal to sum of t_{HZWE} and t_{SD} .

Switching Waveforms

Figure 5. Read Cycle No. 1 of CY62162G (Address Transition Controlled) [23, 24]

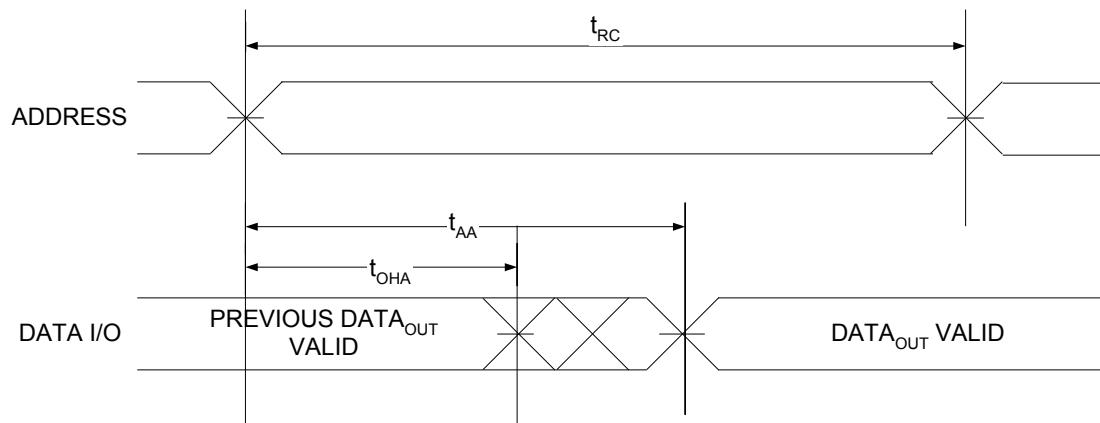
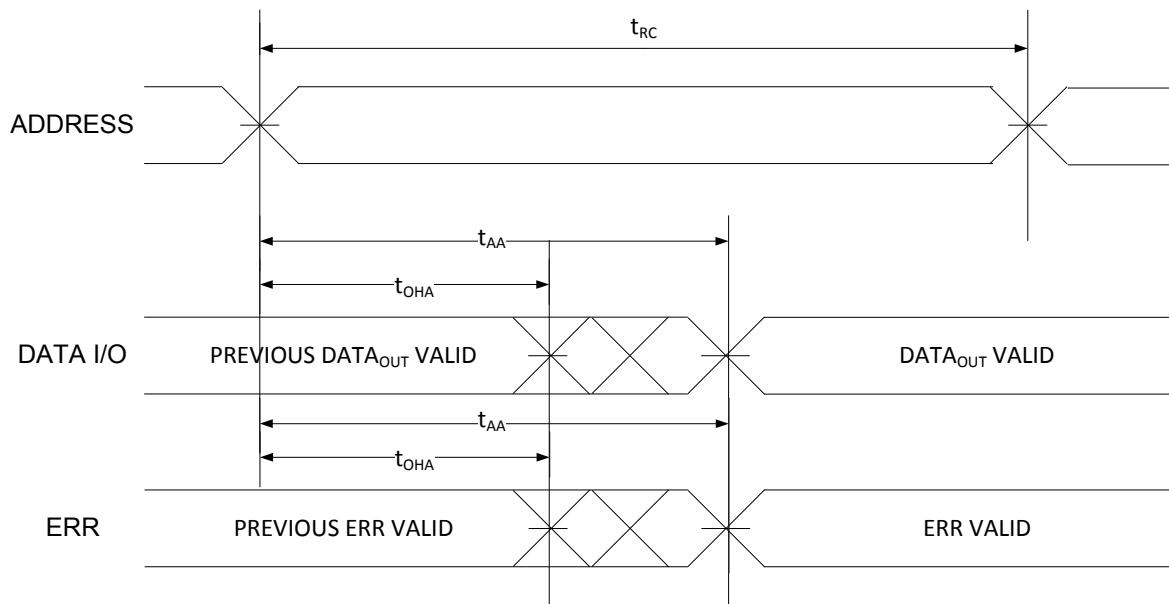


Figure 6. Read Cycle No. 1 of CY62162GE (Address Transition Controlled) [23, 24]

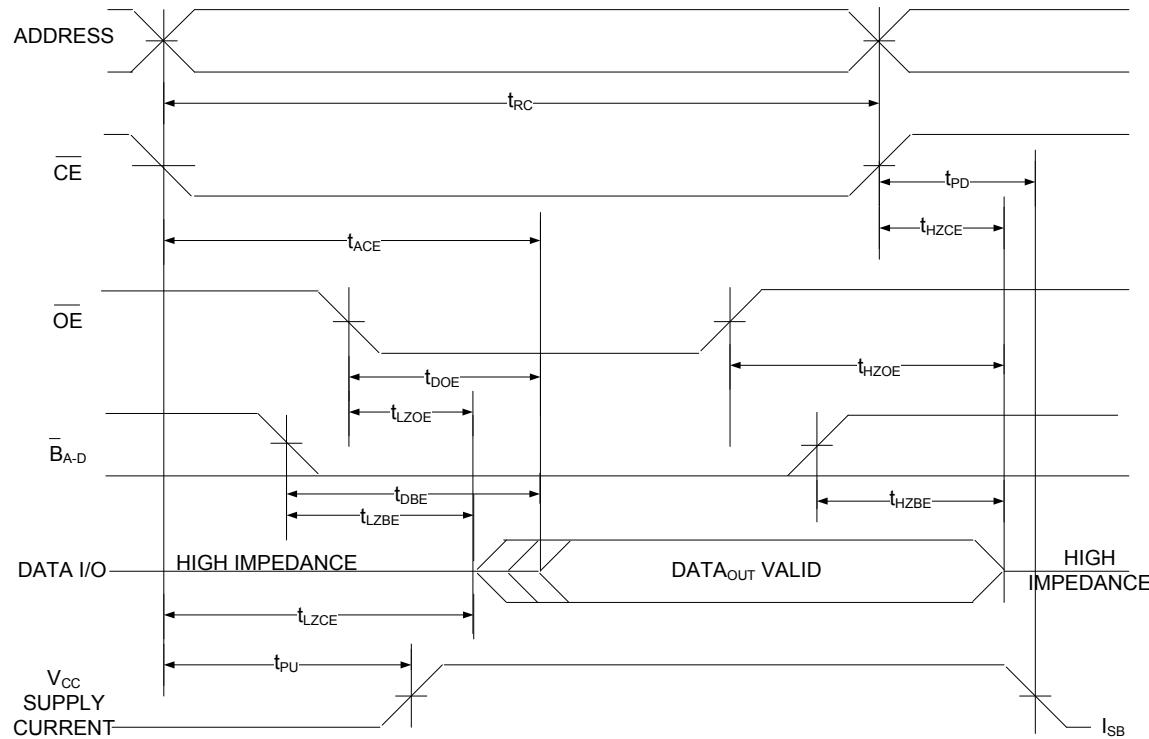


Notes

23. Device is continuously selected. $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IL}$.
 24. WE is HIGH for read cycle.

Switching Waveforms (continued)

Figure 7. Read Cycle No. 2 (\overline{OE} Controlled) [25, 26, 27]

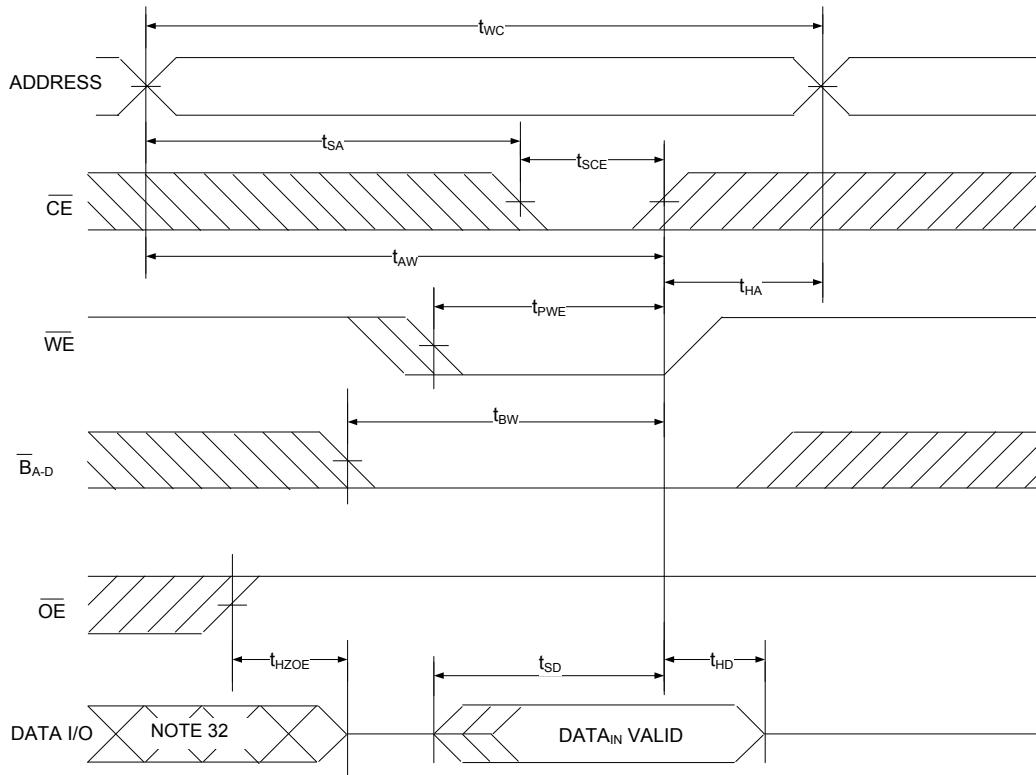


Notes

25. WE is HIGH for read cycle.
26. Address valid before or similar to \overline{CE} transition LOW.
27. \overline{CE} refers to a combination of \overline{CE}_1 and CE_2 . \overline{CE} is LOW when \overline{CE}_1 is LOW and CE_2 is HIGH. \overline{CE} is HIGH when \overline{CE}_1 is HIGH or CE_2 is LOW.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 1 (CE Controlled) [28, 29, 30, 31]



Notes

28. The internal write time of the memory is defined by the overlap of \overline{CE} and \overline{WE} LOW. Chip enable must be active and \overline{WE} and byte enables must be LOW to initiate a write, and the transition of any of these signals terminate the write. The input data setup and hold timing are referenced to the leading edge of the signal that terminates the write.
29. Data I/O is high impedance if \overline{OE} or \overline{B}_A , \overline{B}_B , \overline{B}_C , $\overline{B}_D = V_{IH}$.
30. If \overline{CE} goes HIGH simultaneously with \overline{WE} going HIGH, the output remains in a high impedance state.
31. \overline{CE} refers to a combination of \overline{CE}_1 and CE_2 . \overline{CE} is LOW when \overline{CE}_1 is LOW and CE_2 is HIGH. \overline{CE} is HIGH when \overline{CE}_1 is HIGH or CE_2 is LOW.
32. During this period the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 2 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) [33, 34, 35]

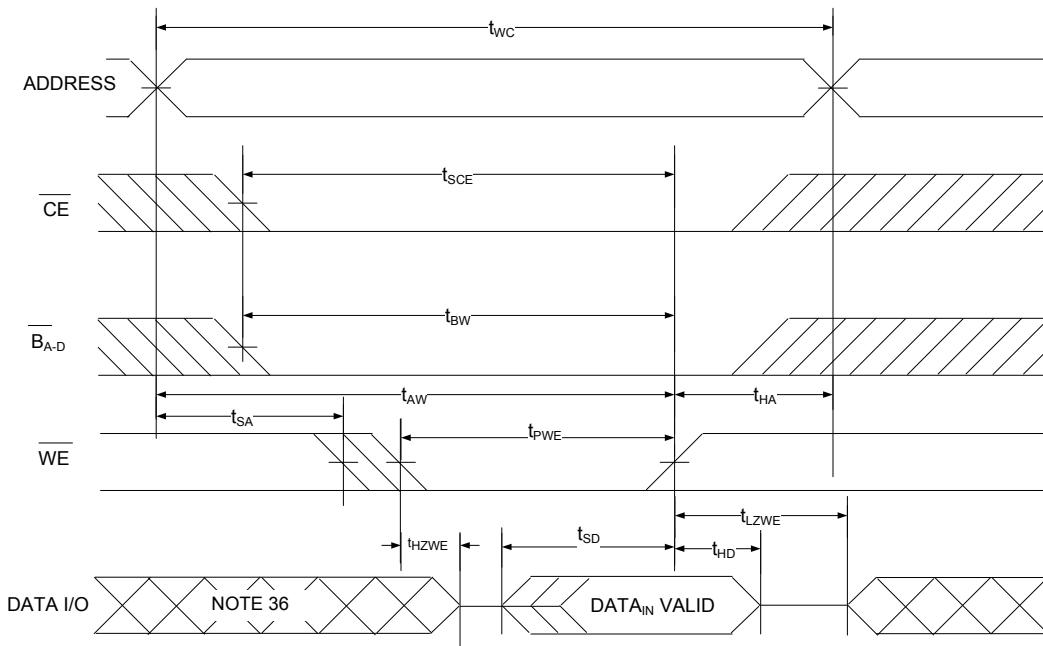
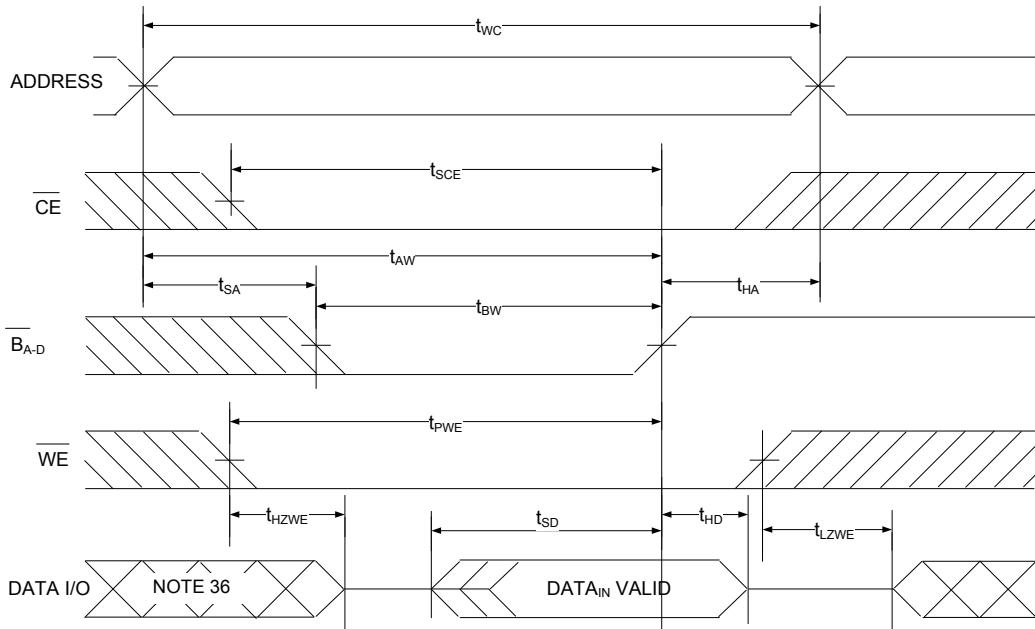


Figure 10. Write Cycle No. 3 ($\overline{\text{B}_A}$, $\overline{\text{B}_B}$, $\overline{\text{B}_C}$, $\overline{\text{B}_D}$ Controlled, $\overline{\text{OE}}$ LOW) [33, 34]



Notes

33. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high impedance state.

34. $\overline{\text{CE}}$ refers to a combination of $\overline{\text{CE}}_1$ and $\overline{\text{CE}}_2$. $\overline{\text{CE}}$ is LOW when $\overline{\text{CE}}_1$ is LOW and $\overline{\text{CE}}_2$ is HIGH. $\overline{\text{CE}}$ is HIGH when $\overline{\text{CE}}_1$ is HIGH or $\overline{\text{CE}}_2$ is LOW.

35. The minimum write cycle pulse width should be equal to the sum of t_{HZWE} and t_{SD} .

36. During this period the I/Os are in output state and input signals should not be applied.

Truth Table – CY62162G / CY62162GE

CE^[37]	OE	WE	\bar{B}_A	\bar{B}_B	\bar{B}_C	\bar{B}_D	I/O₀–I/O₇	I/O₈–I/O₁₅	I/O₁₆–I/O₂₃	I/O₂₄–I/O₃₁	Mode	Power
H	X	X	X ^[38]	X ^[38]	X ^[38]	X ^[38]	High Z	High Z	High Z	High Z	Standby	(I _{SB})
X ^[38]	X	X	H	H	H	H	High Z	High Z	High Z	High Z	Standby	(I _{SB})
L	L	H	L	L	L	L	Data out	Data out	Data out	Data out	Read all bits	(I _{CC})
L	L	H	L	H	H	H	Data out	High Z	High Z	High Z	Read byte A bits only	(I _{CC})
L	L	H	H	L	H	H	High Z	Data out	High Z	High Z	Read byte B bits only	(I _{CC})
L	L	H	H	H	L	H	High Z	High Z	Data out	High Z	Read byte C bits only	(I _{CC})
L	L	H	H	H	H	L	High Z	High Z	High Z	Data out	Read byte D bits only	(I _{CC})
L	X	L	L	L	L	L	Data in	Data in	Data in	Data in	Write all bits	(I _{CC})
L	X	L	L	H	H	H	Data in	High Z	High Z	High Z	Write byte A bits only	(I _{CC})
L	X	L	H	L	H	H	High Z	Data in	High Z	High Z	Write byte B bits only	(I _{CC})
L	X	L	H	H	L	H	High Z	High Z	Data in	High Z	Write byte C bits only	(I _{CC})
L	X	L	H	H	H	L	High Z	High Z	High Z	Data in	Write byte D bits only	(I _{CC})
L	H	H	X ^[38]	X ^[38]	X ^[38]	X ^[38]	High Z	High Z	High Z	High Z	Selected, outputs disabled	(I _{CC})

ERR Output – CY62162GE

Output^[39]	Mode
0	Read Operation, no single bit error in the stored data.
1	Read Operation, single bit error detected and corrected.
Z	Device deselected / Outputs disabled / Write Operation.

Note

37. \overline{CE} refers to a combination of \overline{CE}_1 and CE_2 . \overline{CE} is LOW when \overline{CE}_1 is LOW and CE_2 is HIGH. \overline{CE} is HIGH when \overline{CE}_1 is HIGH or CE_2 is LOW.

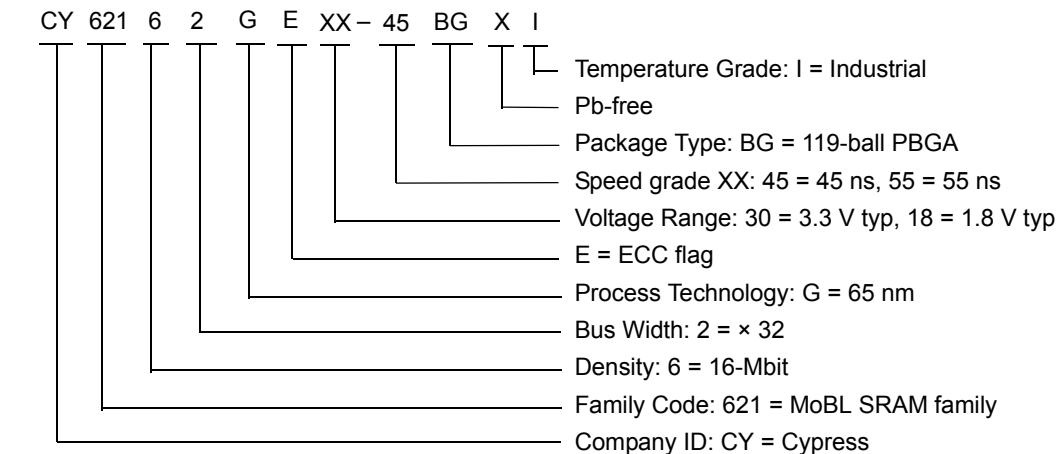
38. 'X' refers to V_{IL} or V_{IH} . For CMOS voltage levels refer to I_{SB2} test conditions in [Electrical Characteristics on page 7](#). Chip enables (\overline{CE}_1 and CE_2) and all Byte Enables (B_{A-D}) must be in CMOS voltage levels to meet the I_{SB2}/I_{CCDR} spec.

39. ERR is an Output pin. If not used, this pin should be left floating.

Ordering Information

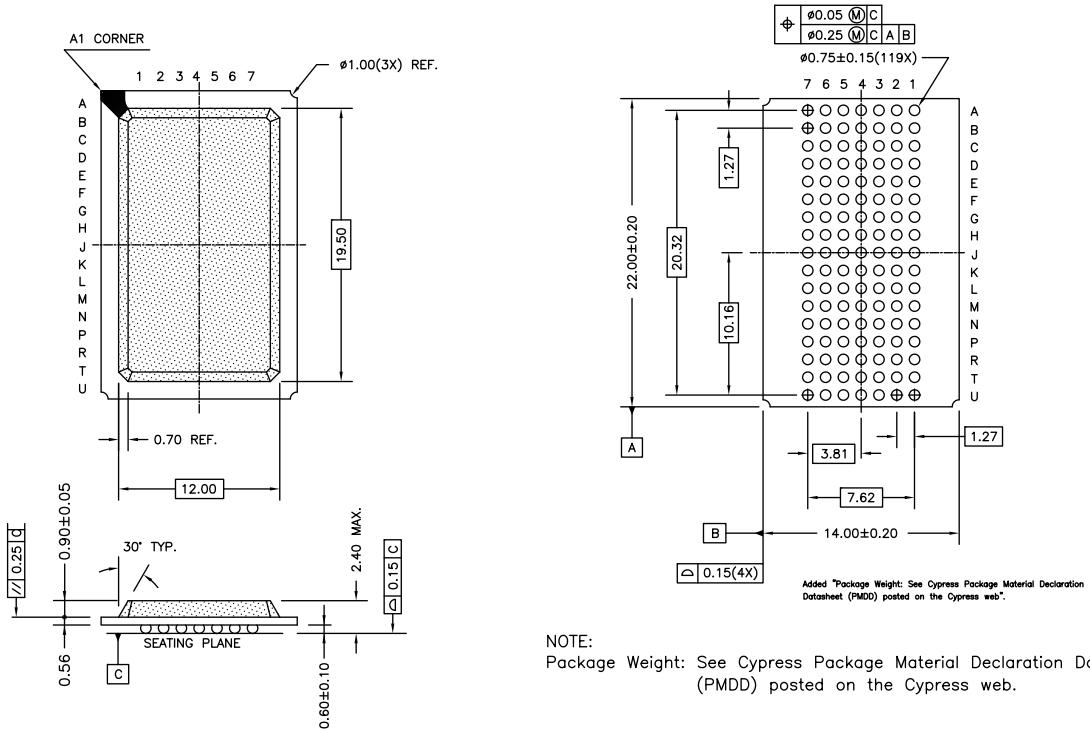
Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type (All Pb-free)	Operating Range
45	2.2 V–3.6 V	CY62162G30-45BGXI	51-85115	119-ball PBGA (14 × 22 × 2.4 mm)	Industrial
55	1.65 V–2.2 V	CY62162G18-55BGXI			Industrial

Ordering Code Definitions



Package Diagram

Figure 11. 119-ball PBGA (14 x 22 x 2.4 mm) BG119 Package Outline, 51-85115



NOTE:
Package Weight: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85115 *D

Acronyms

Acronym	Description
CE	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
FBGA	Fine-Pitch Ball Grid Array
I/O	Input/Output
OE	Output Enable
SRAM	Static Random Access Memory
WE	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
mA	milliampere
MHz	megahertz
mm	millimeter
µA	microampere
µs	microsecond
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62162G/CY62162GE MoBL®, 16-Mbit (512 K × 32) Static RAM with Error-Correcting Code (ECC)
Document Number: 001-81598

Revision	ECN	Orig. of Change	Submission Date	Description of Change
*C	4863821	NILE	07/31/2015	Changed status from Preliminary to Final.
*D	6012120	AESATMP9	01/03/2018	Updated logo and copyright.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Arm® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6 MCU](#)

Cypress Developer Community

[Community](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2012-2018. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. No computing device can be absolutely secure. Therefore, despite security measures implemented in Cypress hardware or software products, Cypress does not assume any liability arising out of any security breach, such as unauthorized access to or use of a Cypress product. In addition, the products described in these materials may contain design defects or errors known as errata which may cause the product to deviate from published specifications. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.

Данный компонент на территории Российской Федерации**Вы можете приобрести в компании MosChip.**

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

<http://moschip.ru/get-element>

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибуторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ Р В 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru
moschip.ru_4

moschip.ru_6
moschip.ru_9