

## Features

- Gain Control in 20-dB Steps
- Very Low I/Q Amplitude and Phase Errors
- High Input P1dB
- Small and Optimized Package for High Reliability and Performance

## Applications

- Infrastructure Digital Communication Systems
- GSM/Cellular Transceivers
- ISM Band Transceivers

## Benefits

- Fully Integrated Device with Reduced External Component Count

Electrostatic sensitive device.  
Observe precautions for handling.



## 65 - 300 MHz SiGe IF Receiver/ Demodulator

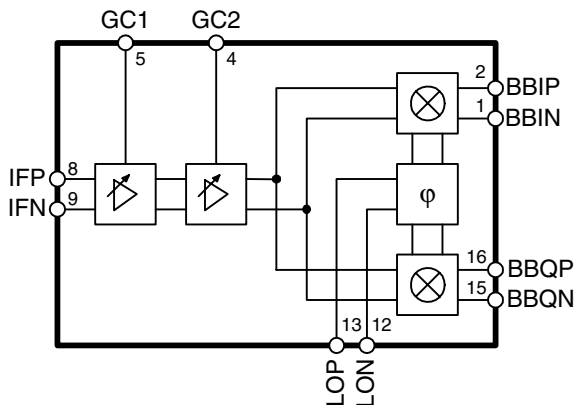
### ATR0797



## Description

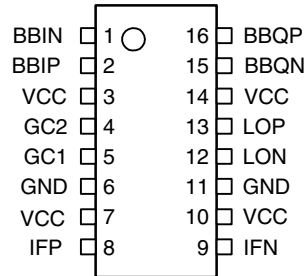
The ATR0797 is a multi-purpose demodulator RFIC. The silicon monolithic integrated circuit is designed with Atmel's advanced SiGe technology. This demodulator is capable of both quadrature demodulation or direct IF output. Features include switchable gain control on a frequency range from 65 MHz to 300 MHz. The device performs a very low amplitude as well as phase error and allows high input P1dB. The ATR0797 targets a variety of system applications for communications including 3G wireless.

**Figure 1.** Block Diagram



## Pin Configuration

**Figure 2.** Pinning



## Pin Description

| Pin | Symbol | Function                                                   |
|-----|--------|------------------------------------------------------------|
| 1   | BBIN   | Baseband I-axis negative output, self biasing              |
| 2   | BBIP   | Baseband I-axis positive output, self biasing              |
| 3   | VCC    | 5 V power supply                                           |
| 4   | GC2    | Gain control input, stage 2, 5 V CMOS levels               |
| 5   | GC1    | Gain control input, stage 1, 5 V CMOS levels               |
| 6   | GND    | Ground                                                     |
| 7   | VCC    | 5 V power supply                                           |
| 8   | IFP    | IF positive input, self biasing, AC-coupled                |
| 9   | IFN    | IF negative input, self biasing, AC-coupled                |
| 10  | VCC    | 5 V power supply                                           |
| 11  | GND    | Ground                                                     |
| 12  | LON    | Local oscillator, negative input, self biasing, AC-coupled |
| 13  | LOP    | Local oscillator, positive input, self biasing, AC-coupled |
| 14  | VCC    | 5 V power supply                                           |
| 15  | BBQN   | Baseband Q-axis negative output, self biasing              |
| 16  | BBQP   | Baseband Q-axis positive output, self biasing              |

## Product Description

Atmel's ATR0797 is a variable gain I-Q demodulator designed for use in receiver IF sections, that are typically existing in superheterodyne RF architectures.

The ATR0797 has two gain stages that are independent of each other. These gain stages are broadband differential amplifiers each with a digital control pin to set the gain. Since the amplifiers have approximately the same gain, setting GC1 high and GC2 low results in approximately the same gain as setting GC1 low and GC2 high. Former setting offers better noise figures.

The IF input is a differential input that has internal bias circuitry to set the common mode voltage. The use of blocking capacitors to facilitate AC coupling is highly recommended to avoid changing the common mode voltage. Either input may be driven single ended if the other input is connected to ground through an AC short such as a 1000 pF capacitor. This typically results in slightly lower input P1dB.

The two matched mixers are configured with the quadrature LO generator to provide in-phase and quadrature baseband outputs.

The LO and IF ports offer a differential 50  $\Omega$  impedance. The passives at these ports (parallel L-R network) and the package itself adds inductance that tends to degrade return loss.

The ATR0797 features immunity from changes in LO power. The gain features change by less than 0.6 dB over a 6 dB range of LO power. Also note the excellent I/Q balance, which typically falls within 0.1 dB and 1 degree from 65 MHz to 300 MHz, and varies less than 0.05 dB and 0.5 degree over temperature (-40°C to +85°C).

The frequency response of the IF and LO ports is dominated by the L-R network on the input. When de-embedded, the gain and P1dB response is within 0.5 dB from 65 MHz to 300 MHz.

The figures in the datasheet illustrate a typical ATR0797's performance with respect to temperature. Note that these numbers include the effect of the R-L network in the IF port.

Evaluation board design and equipment constraints:

Please take into account that the evaluation board uses baluns on the I/Q outputs, and these baluns limit the low frequency response of the device. For true baseband operation, the baluns should be removed, and the differential signals used directly.

The 27 pF capacitor on the evaluation board is appropriate for lower frequencies.

## Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

All voltages are referred to GND.

| Parameters            | Symbol    | Value       | Unit |
|-----------------------|-----------|-------------|------|
| Supply voltage        | $V_{CC}$  | 5.5         | V    |
| LO input              | LOP, LON  | 10          | dBm  |
| IF input              | IFN, IFP  | 10          | V    |
| Operating temperature | $T_{OP}$  | -40 to +85  | °C   |
| Storage temperature   | $T_{stg}$ | -65 to +150 | °C   |

Note: The device may not survive all maximums applied simultaneously.

## Thermal Resistance

| Parameters       | Symbol     | Value | Unit |
|------------------|------------|-------|------|
| Junction ambient | $R_{thJA}$ | 35    | K/W  |

## Electrical Characteristics

Test conditions:  $V_{CC} = 5\text{ V}$ ,  $T_{amb} = 25^\circ\text{C}$ , LO input: 0 dBm at 200 MHz

IF input: at 200.1 MHz, GC1 = 0, GC2 = 0; 0 dBm

IF input: at 200.1 MHz, GC1 = 1, GC2 = 0; -20 dBm

IF input: at 200.1 MHz, GC1 = 1, GC2 = 1; -40 dBm

| No.      | Parameters                               | Test Conditions                                               | Pin             | Symbol   | Min. | Typ.      | Max. | Unit | Type <sup>(1)</sup> |
|----------|------------------------------------------|---------------------------------------------------------------|-----------------|----------|------|-----------|------|------|---------------------|
| <b>1</b> | <b>IF Input (I/Q Mixing to Baseband)</b> |                                                               |                 |          |      |           |      |      |                     |
| 1.1      | Frequency range                          |                                                               | 8-9             | f        | 65   | 120 - 220 | 300  | MHz  | B                   |
| 1.2      | IF input return loss                     | 50 $\Omega$ nominal differential input <sup>(2)</sup>         | 8-9             | RL       |      | 20        |      | dB   | D                   |
| 1.3      | IF input common mode voltage             | Internally generated                                          | 8, 9            | $V_{CH}$ |      | 2         |      | V    |                     |
| 1.4      | Gain                                     | Gain set = high;<br>GC1 = GC2 = 1                             | 2-1,<br>16-15   | G        | 32   | 35        | 38   | dB   | A                   |
| 1.5      | Input P1dB                               |                                                               | 1, 2,<br>15, 16 | P1dB     | -29  | -27       |      | dBm  | C                   |
| 1.6      | DSB Noise figure                         |                                                               | 2-1,<br>16-15   | NF       |      | 11        |      | dB   | D                   |
| 1.7      | Gain                                     | Gain set = medium;<br>GC1 = 1; GC2 = 0 or<br>GC1 = 0; GC2 = 1 | 2-1,<br>16-15   | G        | 12   | 15        | 17   | dB   | A                   |
| 1.8      | Input P1dB                               |                                                               | 1, 2,<br>15, 16 | P1dB     | -8   | -6        |      | dBm  | C                   |
| 1.9      | DSB Noise figure                         |                                                               | 2-1,<br>16-15   | NF       |      | 14.5      |      | dB   | D                   |

- Notes:
1. Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter
  2. The parasitic inductance of the package, the board, and L5, L6 must be matched out at the center frequency with a series capacitor to achieve 20 dB of port match.
  3. The parasitic inductance of the package must be matched out to reach 20 dB port match above 100 MHz.

## Electrical Characteristics (Continued)

Test conditions:  $V_{CC} = 5\text{ V}$ ,  $T_{amb} = 25^{\circ}\text{C}$ , LO input: 0 dBm at 200 MHz

IF input: at 200.1 MHz, GC1 = 0, GC2 = 0; 0 dBm

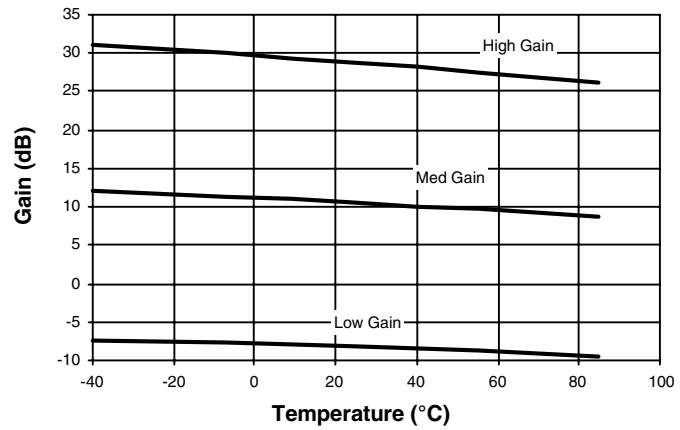
IF input: at 200.1 MHz, GC1 = 1, GC2 = 0; -20 dBm

IF input: at 200.1 MHz, GC1 = 1, GC2 = 1; -40 dBm

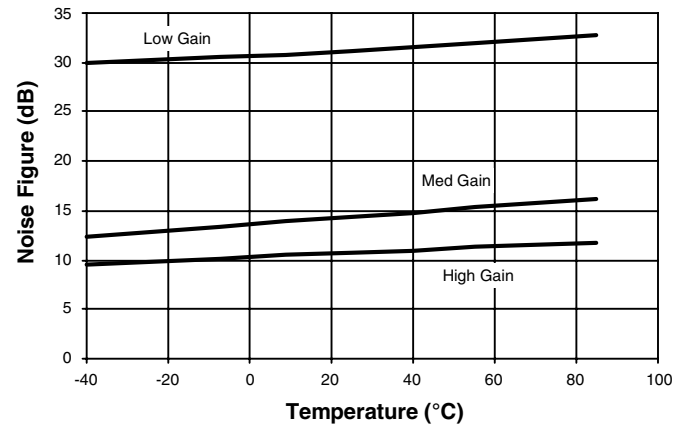
| No.  | Parameters                             | Test Conditions                                 | Pin             | Symbol              | Min.                  | Typ. | Max.                  | Unit | Type <sup>(1)</sup> |
|------|----------------------------------------|-------------------------------------------------|-----------------|---------------------|-----------------------|------|-----------------------|------|---------------------|
| 1.10 | Gain                                   | Gain set = low;<br>GC1 = GC2 = 0                | 2-1,<br>16-15   | G                   | -7                    | -4   | -2                    | dB   | A                   |
| 1.11 | Input P1dB                             |                                                 | 1, 2,<br>15, 16 | P1dB                | 12                    | 14   |                       | dBm  | C                   |
| 1.12 | DSB Noise figure                       |                                                 | 2-1,<br>16-15   | NF                  |                       | 31   |                       | dB   | D                   |
| 2    | I/Q Output                             |                                                 |                 |                     |                       |      |                       |      |                     |
| 2.1  | I/Q output frequency range             |                                                 | 1, 2,<br>15, 16 | f <sub>I/Q</sub>    | DC                    |      | 500                   | MHz  | D                   |
| 2.2  | I/Q output amplitude error             |                                                 | 2-1,<br>16-15   |                     | -0.2                  |      | +0.2                  | dB   | A                   |
| 2.3  | I/Q phase error                        |                                                 | 2-1,<br>16-15   |                     | -2                    |      | +2                    | deg  | A                   |
| 2.4  | I/Q output common mode voltage         |                                                 | 1, 2,<br>15, 16 |                     |                       | 2.5  |                       | V    | A                   |
| 2.5  | I/Q output differential offset voltage |                                                 | 2-1,<br>16-15   | V <sub>offset</sub> | -100                  |      | +100                  | mV   | A                   |
| 2.6  | I/Q output return loss                 | 50 Ω nominal differential output <sup>(3)</sup> | 1, 2,<br>15, 16 | RL <sub>I/Q</sub>   |                       | 20   |                       | dB   | D                   |
| 3    | LO input                               |                                                 |                 |                     |                       |      |                       |      |                     |
| 3.1  | LO input level                         |                                                 | 13-12           | P <sub>LO</sub>     | -3                    | 0    | +3                    | dBm  | D                   |
| 3.2  | Return loss                            |                                                 | 13-12           | RL <sub>LO</sub>    |                       | 20   |                       | dB   | D                   |
| 3.3  | LO frequency range                     |                                                 | 13-12           | RL <sub>LO</sub>    | 65                    |      | 300                   | MHz  | D                   |
| 4    | Miscellaneous                          |                                                 |                 |                     |                       |      |                       |      |                     |
| 4.1  | Supply voltage                         |                                                 | 3, 7,<br>10, 14 | V <sub>CC</sub>     | 4.75                  | 5    | 5.25                  | V    | A                   |
| 4.2  | Supply current                         |                                                 | 3, 7,<br>10, 14 | I <sub>CC</sub>     |                       | 195  |                       | mA   | A                   |
| 4.3  | GC1, GC2 logic level low               |                                                 | 4, 5            | V <sub>IL</sub>     | 0                     |      | 0.3 × V <sub>CC</sub> | V    | D                   |
| 4.4  | GC1, GC2 logic level high              |                                                 | 4, 5            | V <sub>IH</sub>     | 0.7 × V <sub>CC</sub> |      | V <sub>CC</sub>       | V    | D                   |
| 4.5  | GC1, GC2 input impedance               |                                                 | 4, 5            | Z                   | 40                    |      |                       | kΩ   | D                   |

- Notes: 1. Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter  
2. The parasitic inductance of the package, the board, and L5, L6 must be matched out at the center frequency with a series capacitor to achieve 20 dB of port match.  
3. The parasitic inductance of the package must be matched out to reach 20 dB port match above 100 MHz.

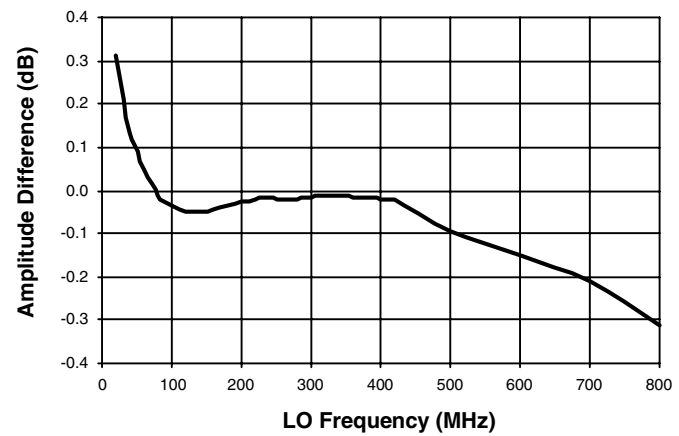
**Figure 3. Gain versus Temperature**



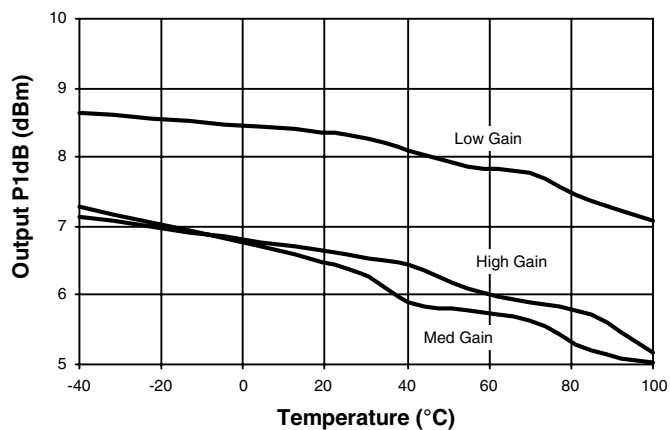
**Figure 4. Noise Figure versus Temperature**



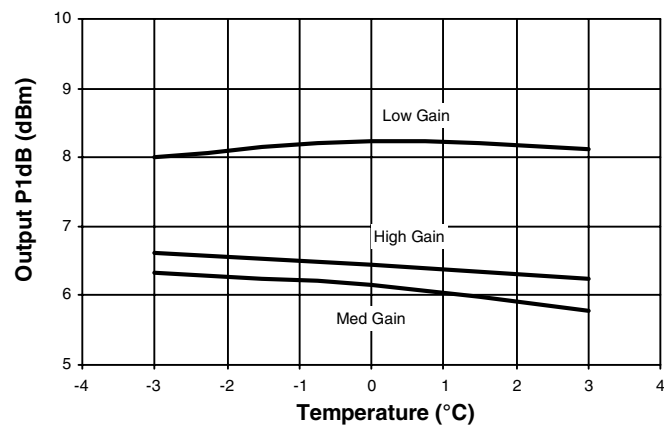
**Figure 5. Amplitude Difference versus LO Frequency**



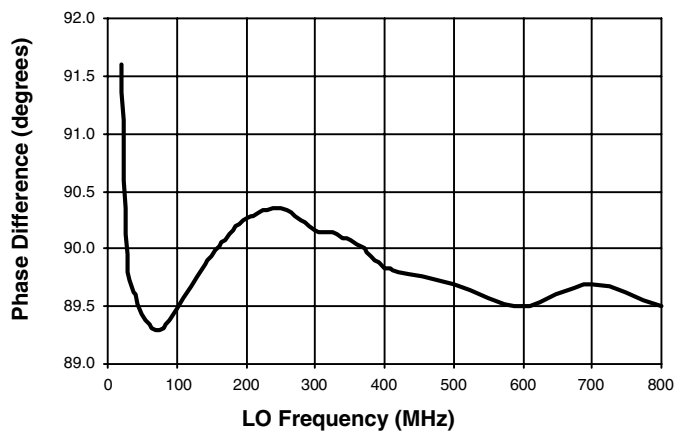
**Figure 6.** Output P1dB versus Temperature



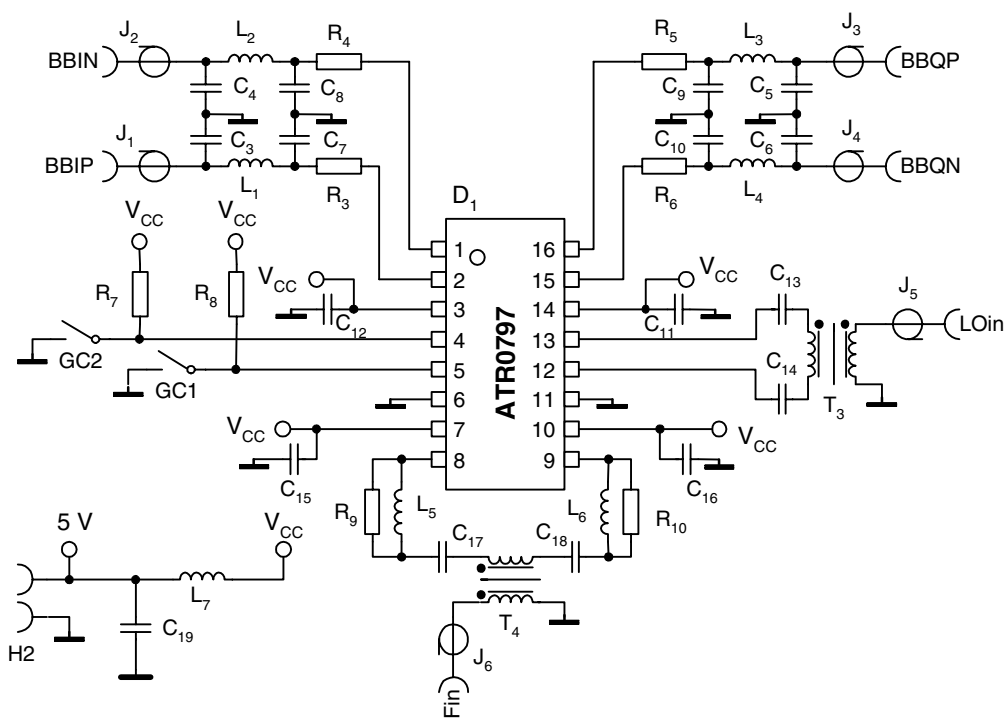
**Figure 7.** Output P1dB versus LO Power



**Figure 8.** Phase Difference versus LO Frequency



**Figure 9. Demo Test Board Schematic**



### Table 1. Bill of Materials

| Component                | Reference                                                                                                                              | Vendor              | Part Number  | Value  | Size/Package |
|--------------------------|----------------------------------------------------------------------------------------------------------------------------------------|---------------------|--------------|--------|--------------|
| IF Demodulator           | D <sub>1</sub>                                                                                                                         | Atmel               | ATR0797      |        | PSSO16       |
| SMA end launch connector | J <sub>1</sub> , J <sub>2</sub> , J <sub>3</sub> , J <sub>4</sub> , J <sub>5</sub> , J <sub>6</sub>                                    | Johnson Components™ | 742-0711-841 |        |              |
| Transformer              | T <sub>3</sub> , T <sub>4</sub>                                                                                                        | Mini-Circuits®      | TC1-1        |        |              |
| Supply bypass capacitor  | C <sub>19</sub>                                                                                                                        |                     |              | 1 μF   | 1206         |
| Resistor                 | R <sub>7</sub> , R <sub>8</sub>                                                                                                        |                     |              | 1 kΩ   | 0402         |
| Capacitor                | C <sub>11</sub> , C <sub>12</sub> , C <sub>16</sub>                                                                                    |                     |              | 22 pF  | 0402         |
| Inductor                 | L <sub>1</sub> , L <sub>2</sub> , L <sub>3</sub> , L <sub>4</sub> , L <sub>7</sub>                                                     | Würth Elektronik®   | 74476401     | 1 μH   | 1210         |
| Capacitor                | C <sub>13</sub> , C <sub>14</sub> , C <sub>17</sub> , C <sub>18</sub>                                                                  |                     |              | 68 pF  | 0402         |
| Resistor                 | R <sub>3</sub> , R <sub>4</sub> , R <sub>5</sub> , R <sub>6</sub>                                                                      |                     |              | 0 Ω    | 0402         |
| Capacitor                | C <sub>3</sub> , C <sub>4</sub> , C <sub>5</sub> , C <sub>6</sub> , C <sub>7</sub> , C <sub>8</sub> , C <sub>9</sub> , C <sub>10</sub> |                     |              | 820 pF | 0402         |
| Resistor                 | R <sub>9</sub> , R <sub>10</sub>                                                                                                       |                     |              | 51 Ω   | 0402         |
| Inductor                 | L <sub>5</sub> , L <sub>6</sub>                                                                                                        |                     |              | 10 nH  | 0402         |
| Capacitor                | C <sub>15</sub>                                                                                                                        |                     |              | 100 pF | 0402         |

Figure 10. Demo Test Board (Fully Assembled PCB)

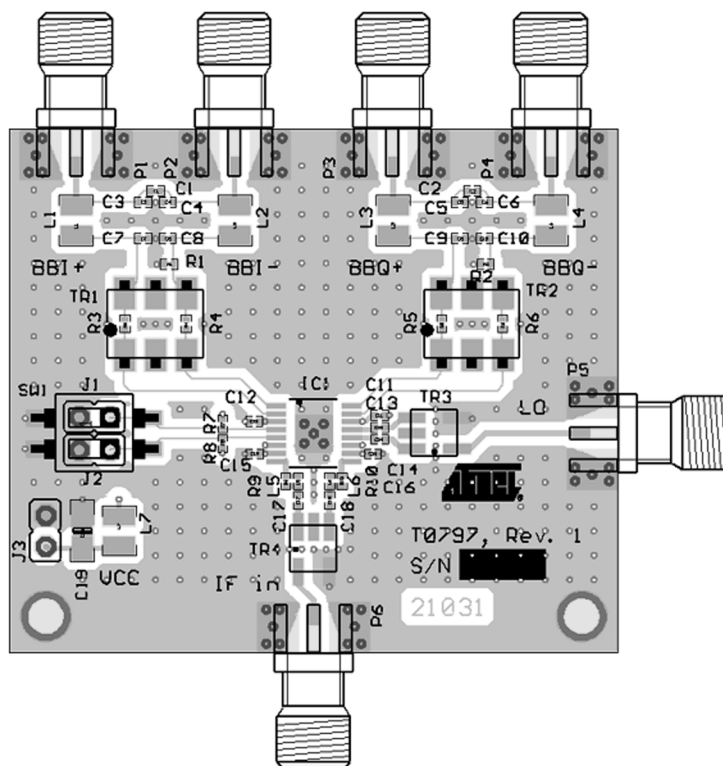
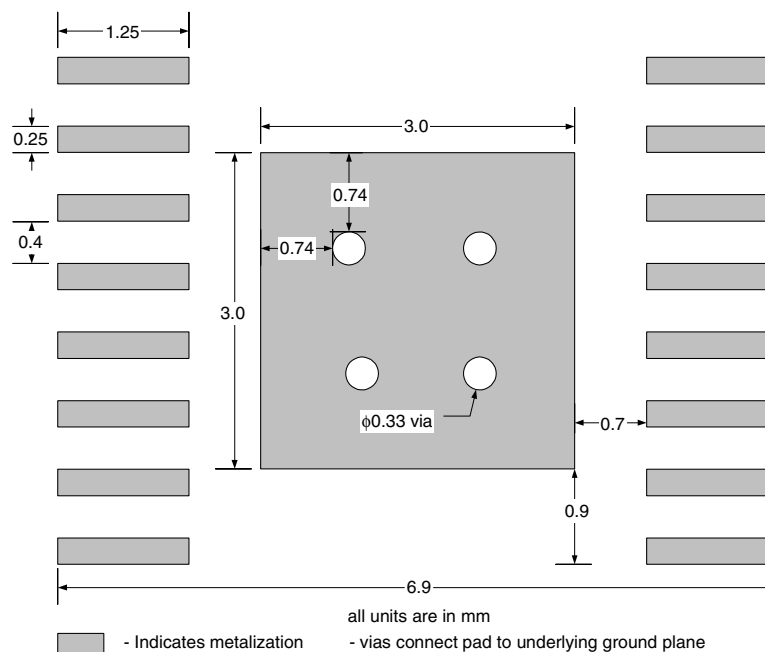


Figure 11. Recommended Package Footprint

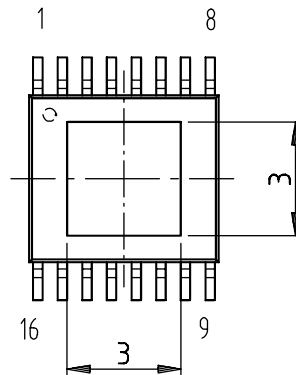


Remark: Heatslug must be soldered to GND.  
 In order to avoid soldering problems, plugging of the vias under the heatslug is recommended. Only ground signal traces are allowed directly under the package.

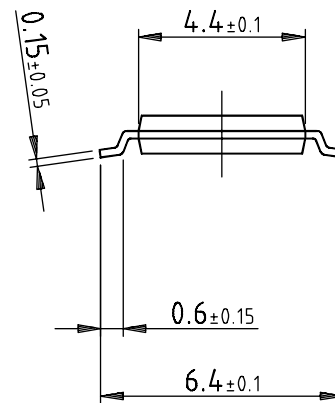
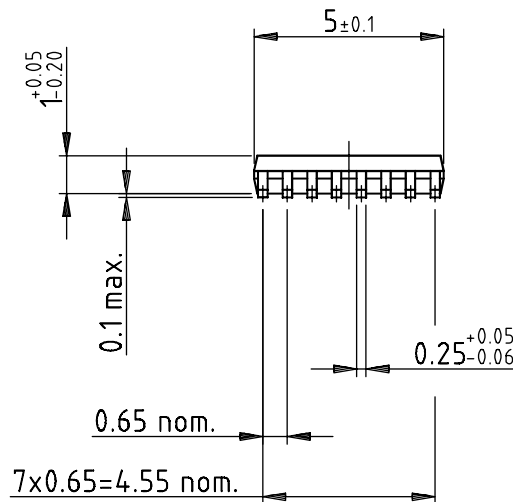
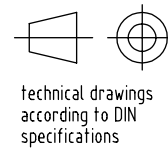
## Ordering Information

| Extended Type Number | Package | Remarks   |
|----------------------|---------|-----------|
| ATR0797-6CPH         | PSSO16  | Lead free |

## Package Information



Package: PSSO16  
( acc. JEDEC SMALL OUTLINE No. MO-153 )  
Dimensions in mm



Drawing-No.: 6.543-5079.01-4  
Issue: 2; 01.03.02



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