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FDMC8296

June 2014

N-Channel Power Trench[®] MOSFET 30V, 18A, $8.0m\Omega$

Features

- Max $r_{DS(on)}$ = 8.0m Ω at V_{GS} = 10V, I_D = 12A
- Max $r_{DS(on)}$ = 13.0m Ω at V_{GS} = 4.5V, I_D = 10A
- High performance trench technology for extremely low r_{DS(on)}
- Termination is Lead-free and RoHS Compliant

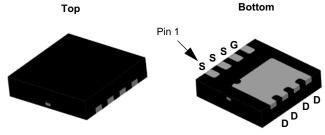


General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench® process that has been especially tailored to minimize the on-state resistance. This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

Application

- DC DC Buck Converter
- Notebook battery power management
- Load switch in Notebook





MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Paramet		Ratings	Units	
V_{DS}	Drain to Source Voltage			30	V
V_{GS}	Gate to Source Voltage			±20	V
	Drain Current -Continuous	T _C = 25°C		18	
-Continuous		T _A = 25°C	(Note 1a)	12	A
	-Pulsed			52	
Eas	Single Pulse Avalanche Energy		(Note 3)	72	mJ
Б	Power Dissipation	T _C = 25°C		27	w
P_{D}	Power Dissipation	T _A = 25°C	(Note 1a)	2.3	VV
T _{J, TSTG}	Operating and Storage Junction Temperate	ure Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	4.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a	53	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC8296	FDMC8296	MLP 3.3X3.3	13 "	12 mm	3000 units

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	cteristics					
BV_DSS	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I _D = 250μA, referenced to 25°C		17		mV/°C
lano	Zero Gate Voltage Drain Current	V _{DS} = 24V,			1	μА
IDSS	Zero Gate Voltage Brain Gurrent	$V_{GS} = 0V$, $T_J = 125^{\circ}C$			250	μΛ
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$			±100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	1.0	1.9	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 250μA, referenced to 25°C		-6		mV/°C
r _{DS(on)} Static Dra		V _{GS} = 10V, I _D = 12A		6.5	8.0	
	Static Drain to Source On Resistance	$V_{GS} = 4.5V, I_D = 10A$		9.5	13.0	mΩ
		$V_{GS} = 10V, I_D = 12A, T_J = 125^{\circ}C$		9.0	12.8	
9 _{FS}	Forward Transconductance	$V_{DD} = 5V$, $I_D = 12A$		44		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V = 45V V = 0V	1038	1385	pF
Coss	Output Capacitance	V _{DS} = 15V, V _{GS} = 0V, f = 1MHz	513	685	pF
C _{rss}	Reverse Transfer Capacitance	1 - 11/11/2	87	135	pF
R_q	Gate Resistance	f = 1MHz	0.9		Ω

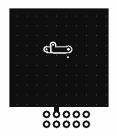
Switching Characteristics

t _{d(on)}	Turn-On Delay Time		9	18	ns
t _r	Rise Time	$V_{DD} = 15V, I_{D} = 12A,$ $V_{GS} = 10V, R_{GEN} = 6\Omega$	3	10	ns
t _{d(off)}	Turn-Off Delay Time	VGS - 10V, NGEN - 052	19	35	ns
t _f	Fall Time		2	10	ns
0	Total Gate Charge	V _{GS} = 0V to 10V	16	23	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0V \text{ to } 4.5V$ $V_{DD} = 15V,$	7.6	10.6	nC
Q_{gs}	Total Gate Charge	I _D = 12A	3		nC
Q _{gd}	Gate to Drain "Miller" Charge		2.5		nC

Drain-Source Diode Characteristics

V _{SD} Source to Drain Diode Forward Voltage	Source to Drain Diede, Ferward Voltage	$V_{GS} = 0V, I_S = 12A$ (Note 2)		0.82	1.3	W
	$V_{GS} = 0V, I_S = 1.9A$ (Note 2)		0.73	1.2	V	
t _{rr}	Reverse Recovery Time	I _E = 12A, di/dt = 100A/μs		25	45	ns
Q _{rr}	Reverse Recovery Charge	1F - 12A, αι/αι - 100A/μS		9	18	nC

^{1.} R_{0,1A} is determined with the device mounted on a 1in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{0,1C} is guaranteed by design while R_{0,CA} is determined by the user's board design.



a. 53 °C/W when mounted on a 1 in² pad of 2 oz copper



b.125 °C/W when mounted on a minimum pad of 2 oz copper

^{2.} Pulse Test: Pulse Width < 300μ s, Duty cycle < 2.0%. 3. E_{AS} of 72 mJ is based on starting T = 25 C, L = 1 mH, I_{AS} = 12 A, V_{DD} = 27 V, V_{GS} = 10 V. 100% test at L = 3 mH, I_{AS} = 5.7 A.

Typical Characteristics T_J = 25°C unless otherwise noted

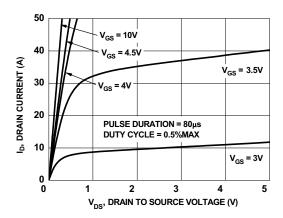


Figure 1. On-Region Characteristics

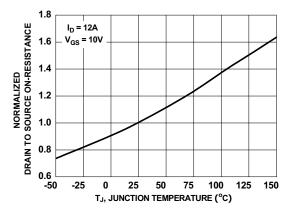


Figure 3. Normalized On-Resistance vs. Junction Temperature

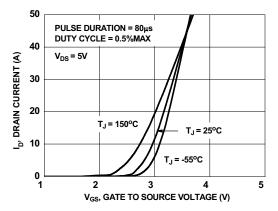


Figure 5. Transfer Characteristics

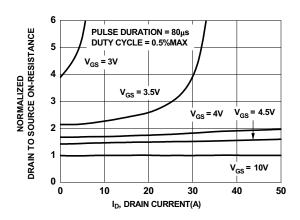


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

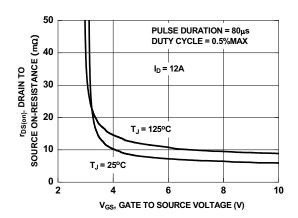


Figure 4. On-Resistance vs. Gate to Source Voltage

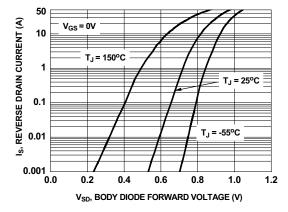


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics $T_J = 25$ °C unless otherwise noted

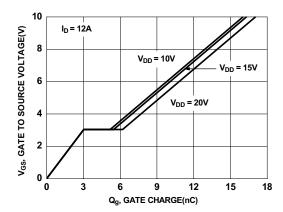


Figure 7. Gate Charge Characteristics

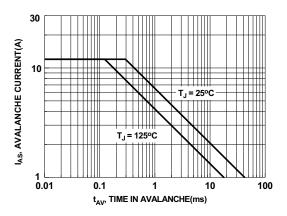


Figure 9. Unclamped Inductive Switching Capability

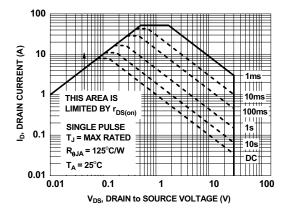


Figure 11. Forward Bias Safe Operating Area

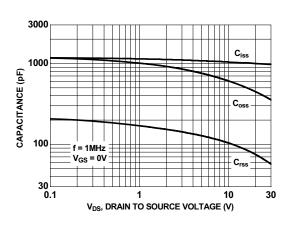


Figure 8. Capacitance vs.Drain to Source Voltage

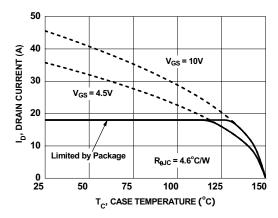


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

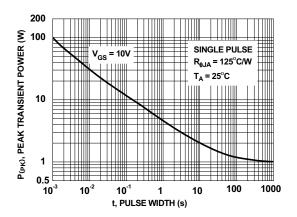


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25°C unless otherwise noted

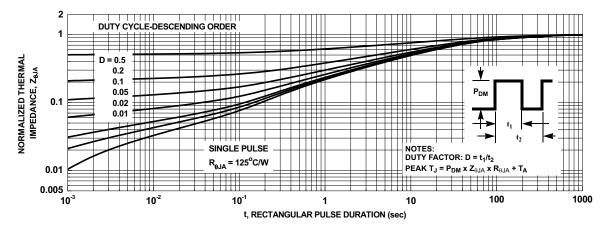
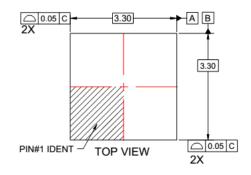
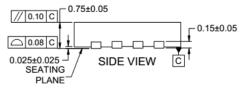
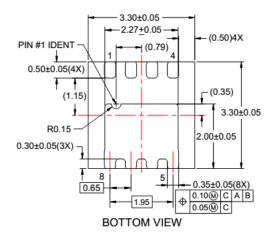


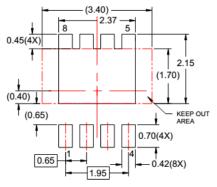
Figure 13. Transient Thermal Response Curve

Dimensional Outline and Pad Layout









RECOMMENDED LAND PATTERN

NOTES:

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- E. DRAWING FILENAME: MKT-MLP08Srev3.



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Rev. 168

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