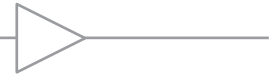


COMLINEAR[®] CLC1011, CLC2011, CLC4011

Low Power, Low Cost, Rail-to-Rail I/O Amplifiers



FEATURES

- 136 μ A supply current
- 4.9MHz bandwidth
- Output swings to within 20mV of either rail
- Input voltage range exceeds the rail by >250mV
- 5.3V/ μ s slew rate
- 21nV/ $\sqrt{\text{Hz}}$ input voltage noise
- 16mA output current
- Fully specified at 2.7V and 5V supplies
- CLC1011: Pb-free SOT23-5, SC70-5, SOIC-8
- CLC2011: Pb-free SOIC-8, MSOP-8
- CLC4011: Pb-free SOIC-14, TSSOP-14

APPLICATIONS

- Portable/battery-powered applications
- PCMCIA, USB
- Mobile communications, cell phones, pagers
- ADC buffer
- Active filters
- Portable test instruments
- Notebooks and PDA's
- Signal conditioning
- Medical Equipment
- Portable medical instrumentation

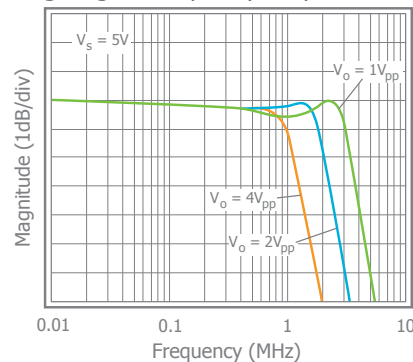
General Description

The COMLINEAR CLC1011 (single), CLC2011 (dual), and CLC4011 (quad) are ultra-low cost, low power, voltage feedback amplifiers. At 2.7V, the CLCx011 family uses only 136 μ A of supply current per amplifier and are designed to operate from a supply range of 2.5V to 5.5V (± 1.25 to ± 2.75). The input voltage range exceeds the negative and positive rails.

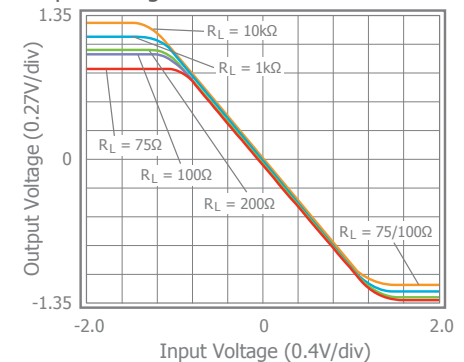
The CLCx011 family of amplifiers offer high bipolar performance at a low CMOS prices. They offer superior dynamic performance with 4.9MHz small signal bandwidths and 5.3V/ μ s slew rates. The combination of low power, high bandwidth, and rail-to-rail performance make the CLCx011 amplifiers well suited for battery-powered communication/computing systems.

Typical Performance Examples

Large Signal Frequency Response



Output Swing vs. Load



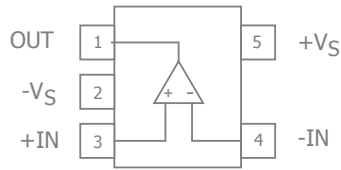
Ordering Information

| Part Number | Package | Pb-Free | RoHS Compliant | Operating Temperature Range | Packaging Method |
|----------------|----------|---------|----------------|-----------------------------|------------------|
| CLC1011ISC5X* | SC70-5 | Yes | Yes | -40°C to +85°C | Reel |
| CLC1011IST5X* | SOT23-5 | Yes | Yes | -40°C to +85°C | Reel |
| CLC2011ISO8X | SOIC-8 | Yes | Yes | -40°C to +85°C | Reel |
| CLC2011IMP8X* | MSOP-8 | Yes | Yes | -40°C to +85°C | Reel |
| CLC4011ISO14X* | SOIC-14 | Yes | Yes | -40°C to +85°C | Reel |
| CLC4011ITP14X* | TSSOP-14 | Yes | Yes | -40°C to +85°C | Reel |

Moisture sensitivity level for all parts is MSL-1. *Advance Information - Future Products.



CLC1011 Pin Configuration



CLC1011 Pin Assignments

| Pin No. | Pin Name | Description |
|---------|----------|-----------------|
| 1 | OUT | Output |
| 2 | -VS | Negative supply |
| 3 | +IN | Positive input |
| 4 | -IN | Negative input |
| 5 | +VS | Positive supply |

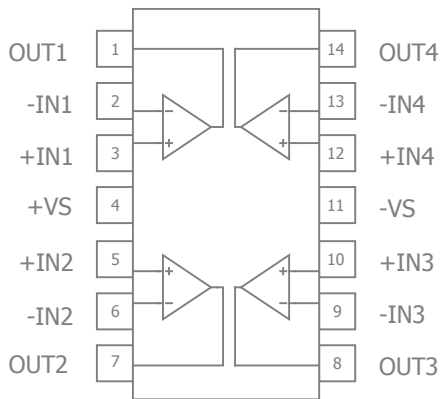
CLC2011 Pin Configuration



CLC2011 Pin Configuration

| Pin No. | Pin Name | Description |
|---------|----------|---------------------------|
| 1 | OUT1 | Output, channel 1 |
| 2 | -IN1 | Negative input, channel 1 |
| 3 | +IN1 | Positive input, channel 1 |
| 4 | -VS | Negative supply |
| 5 | +IN2 | Positive input, channel 2 |
| 6 | -IN2 | Negative input, channel 2 |
| 7 | OUT2 | Output, channel 2 |
| 8 | +VS | Positive supply |

CLC4011 Pin Configuration



CLC4011 Pin Configuration

| Pin No. | Pin Name | Description |
|---------|----------|---------------------------|
| 1 | OUT1 | Output, channel 1 |
| 2 | -IN1 | Negative input, channel 1 |
| 3 | +IN1 | Positive input, channel 1 |
| 4 | +VS | Positive supply |
| 5 | +IN2 | Positive input, channel 2 |
| 6 | -IN2 | Negative input, channel 2 |
| 7 | OUT2 | Output, channel 2 |
| 8 | OUT3 | Output, channel 3 |
| 9 | -IN3 | Negative input, channel 3 |
| 10 | +IN3 | Positive input, channel 3 |
| 11 | -VS | Negative supply |
| 12 | +IN4 | Positive input, channel 4 |
| 13 | -IN4 | Negative input, channel 4 |
| 14 | OUT4 | Output, channel 4 |



Absolute Maximum Ratings

The safety of the device is not guaranteed when it is operated above the "Absolute Maximum Ratings". The device should not be operated at these "absolute" limits. Adhere to the "Recommended Operating Conditions" for proper device function. The information contained in the Electrical Characteristics tables and Typical Performance plots reflect the operating conditions noted on the tables and plots.

| Parameter | Min | Max | Unit |
|---------------------------|---------------|---------------|------|
| Supply Voltage | 0 | 6 | V |
| Input Voltage Range | $-V_S - 0.5V$ | $+V_S + 0.5V$ | V |
| Continuous Output Current | -40 | 40 | mA |

Reliability Information

| Parameter | Min | Typ | Max | Unit |
|-----------------------------------|-----|-----|-----|------|
| Junction Temperature | | | 175 | °C |
| Storage Temperature Range | -65 | | 150 | °C |
| Lead Temperature (Soldering, 10s) | | | 260 | °C |
| Package Thermal Resistance | | | | |
| 5-Lead SC70 | | TBD | | °C/W |
| 5-Lead SOT23 | | 221 | | °C/W |
| 6-Lead SOT23 | | 177 | | °C/W |
| 8-Lead SOIC | | 100 | | °C/W |
| 8-Lead MSOP | | 139 | | °C/W |
| 14-Lead TSSOP | | TBD | | °C/W |

Notes:

Package thermal resistance (θ_{JA}), JEDEC standard, multi-layer test boards, still air.

ESD Protection

| Product | SC70-5 | SOT23-5 | SOIC-8 | MSOP-8 | SOIC-14 | TSSOP-14 |
|----------------------------|--------|---------|--------|--------|---------|----------|
| Human Body Model (HBM) | TBD | TBD | 2kV | TBD | TBD | TBD |
| Charged Device Model (CDM) | TBD | TBD | 2kV | TBD | TBD | TBD |

Recommended Operating Conditions

| Parameter | Min | Typ | Max | Unit |
|-----------------------------|-----|-----|-----|------|
| Operating Temperature Range | -40 | | +85 | °C |
| Supply Voltage Range | 2.5 | | 5.5 | V |



Electrical Characteristics at +2.7V

$T_A = 25^\circ\text{C}$, $V_S = +2.7\text{V}$, $R_f = R_g = 5\text{k}\Omega$, $R_L = 10\text{k}\Omega$ to $V_S/2$, $G = 2$; unless otherwise noted.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---------------------------|---|---|-----|---------------|-----|------------------------------|
| Frequency Domain Response | | | | | | |
| $UGBW_{SS}$ | Unity Gain -3dB Bandwidth | $G = +1$, $V_{OUT} = 0.02V_{pp}$ | | 4.9 | | MHz |
| BW_{SS} | -3dB Bandwidth | $G = +2$, $V_{OUT} = 0.2V_{pp}$ | | 3.2 | | MHz |
| BW_{LS} | Large Signal Bandwidth | $G = +2$, $V_{OUT} = 2V_{pp}$ | | 1.4 | | MHz |
| GBWP | Gain Bandwidth Product | $G = +11$, $V_{OUT} = 0.2V_{pp}$ | | 2.5 | | MHz |
| Time Domain Response | | | | | | |
| t_R, t_F | Rise and Fall Time | $V_{OUT} = 1\text{V}$ step; (10% to 90%) | | 163 | | ns |
| t_S | Settling Time to 0.1% | $V_{OUT} = 1\text{V}$ step | | 500 | | ns |
| OS | Overshoot | $V_{OUT} = 1\text{V}$ step | | <1 | | % |
| SR | Slew Rate | 1V step | | 5.3 | | V/ μs |
| Distortion/Noise Response | | | | | | |
| HD2 | 2nd Harmonic Distortion | $V_{OUT} = 1V_{pp}$, 10kHz | | -72 | | dBc |
| HD3 | 3rd Harmonic Distortion | $V_{OUT} = 1V_{pp}$, 10kHz | | -72 | | dBc |
| THD | Total Harmonic Distortion | $V_{OUT} = 1V_{pp}$, 10kHz | | 0.03 | | % |
| e_n | Input Voltage Noise | > 10kHz | | 21 | | nV/ $\sqrt{\text{Hz}}$ |
| X_{TALK} | Crosstalk | Channel to Channel, $V_{OUT} = 2V_{pp}$, 10kHz | | 82 | | dB |
| | | Channel to Channel, $V_{OUT} = 2V_{pp}$, 50kHz | | 74 | | dB |
| DC Performance | | | | | | |
| V_{IO} | Input Offset Voltage | | | 0.5 | | mV |
| dV_{IO} | Average Drift | | | 5 | | $\mu\text{V}/^\circ\text{C}$ |
| I_b | Input Bias Current | | | 90 | | nA |
| dI_b | Average Drift | | | 32 | | $\text{pA}/^\circ\text{C}$ |
| PSRR | Power Supply Rejection Ratio ⁽¹⁾ | DC | 55 | 83 | | dB |
| A_{OL} | Open-Loop Gain | $V_{OUT} = V_S / 2$ | | 90 | | dB |
| I_S | Supply Current | per channel | | 136 | | μA |
| Input Characteristics | | | | | | |
| R_{IN} | Input Resistance | Non-inverting | | 12 | | M Ω |
| C_{IN} | Input Capacitance | | | 2 | | pF |
| CMIR | Common Mode Input Range | | | -0.25 to 2.95 | | V |
| CMRR | Common Mode Rejection Ratio | DC | | 81 | | dB |
| Output Characteristics | | | | | | |
| V_{OUT} | Output Voltage Swing | $R_L = 10\text{k}\Omega$ to $V_S / 2$ | | 0.02 to 2.68 | | V |
| | | $R_L = 1\text{k}\Omega$ to $V_S / 2$ | | 0.05 to 2.63 | | V |
| | | $R_L = 200\Omega$ to $V_S / 2$ | | 0.11 to 2.52 | | V |
| I_{OUT} | Output Current | | | ± 30 | | mA |

Notes:

- 100% tested at 25°C



Electrical Characteristics at +5V

$T_A = 25^\circ\text{C}$, $V_S = +5\text{V}$, $R_f = R_g = 5\text{k}\Omega$, $R_L = 10\text{k}\Omega$ to $V_S/2$, $G = 2$; unless otherwise noted.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---------------------------|---|--|--------------|---------------|-----|------------------------------|
| Frequency Domain Response | | | | | | |
| $UGBW_{SS}$ | Unity Gain -3dB Bandwidth | $G = +1$, $V_{OUT} = 0.02V_{pp}$ | | 4.3 | | MHz |
| BW_{SS} | -3dB Bandwidth | $G = +2$, $V_{OUT} = 0.2V_{pp}$ | | 3.0 | | MHz |
| BW_{LS} | Large Signal Bandwidth | $G = +2$, $V_{OUT} = 2V_{pp}$ | | 2.3 | | MHz |
| GBWP | Gain Bandwidth Product | $G = +11$, $V_{OUT} = 0.2V_{pp}$ | | 2.5 | | MHz |
| Time Domain Response | | | | | | |
| t_R, t_F | Rise and Fall Time | $V_{OUT} = 1\text{V}$ step; (10% to 90%) | | 110 | | ns |
| t_S | Settling Time to 0.1% | $V_{OUT} = 2\text{V}$ step | | 470 | | ns |
| OS | Overshoot | $V_{OUT} = 1\text{V}$ step | | <1 | | % |
| SR | Slew Rate | 2V step | | 9 | | V/ μs |
| Distortion/Noise Response | | | | | | |
| HD2 | 2nd Harmonic Distortion | $V_{OUT} = 1V_{pp}$, 10kHz | | -73 | | dBc |
| HD3 | 3rd Harmonic Distortion | $V_{OUT} = 1V_{pp}$, 10kHz | | -75 | | dBc |
| THD | Total Harmonic Distortion | $V_{OUT} = 1V_{pp}$, 10kHz | | 0.03 | | % |
| e_n | Input Voltage Noise | > 10kHz | | 22 | | nV/ $\sqrt{\text{Hz}}$ |
| X_{TALK} | Crosstalk | Channel to Channel, $V_{OUT} = 2V_{pp}$, 10kHz | | 82 | | dB |
| | | Channel to Channel, $V_{OUT} = 2V_{pp}$, 50kHz | | 74 | | dB |
| DC Performance | | | | | | |
| V_{IO} | Input Offset Voltage ⁽¹⁾ | | -8 | 1.5 | 8 | mV |
| dV_{IO} | Average Drift | | | 15 | | $\mu\text{V}/^\circ\text{C}$ |
| I_b | Input Bias Current ⁽¹⁾ | | | 90 | 450 | nA |
| dI_b | Average Drift | | | 40 | | $\text{pA}/^\circ\text{C}$ |
| PSRR | Power Supply Rejection Ratio ⁽¹⁾ | DC | 55 | 85 | | dB |
| A_{OL} | Open-Loop Gain | $V_{OUT} = V_S / 2$ | | 80 | | dB |
| I_S | Supply Current ⁽¹⁾ | per channel | | 160 | 235 | μA |
| Input Characteristics | | | | | | |
| R_{IN} | Input Resistance | Non-inverting | | 12 | | M Ω |
| C_{IN} | Input Capacitance | | | 2 | | pF |
| CMIR | Common Mode Input Range | | | -0.25 to 5.25 | | V |
| CMRR | Common Mode Rejection Ratio ⁽¹⁾ | DC | 58 | 80 | | dB |
| Output Characteristics | | | | | | |
| V_{OUT} | Output Voltage Swing | $R_L = 10\text{k}\Omega$ to $V_S / 2$ ⁽¹⁾ | 0.08 to 4.92 | 0.04 to 4.96 | | V |
| | | $R_L = 1\text{k}\Omega$ to $V_S / 2$ | | 0.07 to 4.9 | | V |
| | | $R_L = 200\Omega$ to $V_S / 2$ | | 0.14 to 4.67 | | V |
| I_{OUT} | Output Current | | | ± 35 | | mA |

Notes:

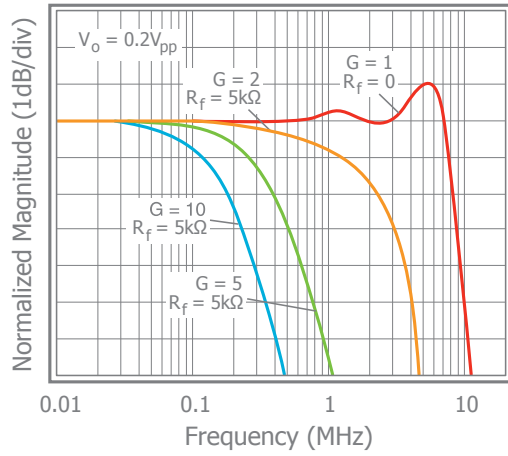
- 100% tested at 25°C



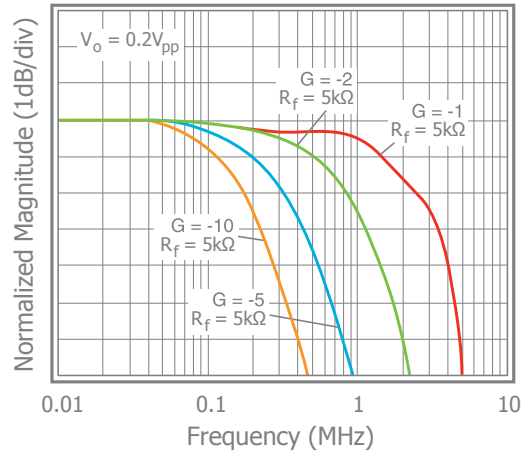
Typical Performance Characteristics

$T_A = 25^\circ\text{C}$, $V_S = +2.7\text{V}$, $R_f = R_g = 5\text{k}\Omega$, $R_L = 10\text{k}\Omega$ to $V_S/2$, $G = 2$; unless otherwise noted.

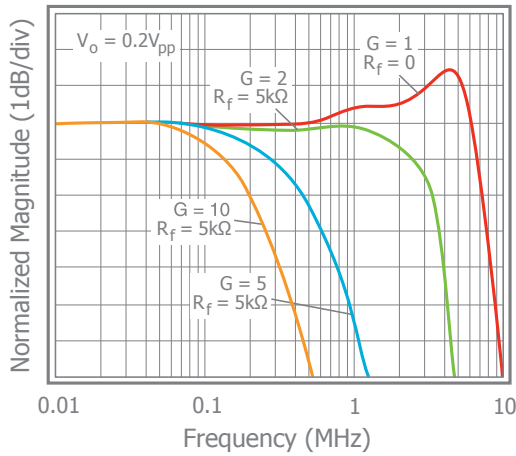
Non-Inverting Frequency Response at $V_S = 5\text{V}$



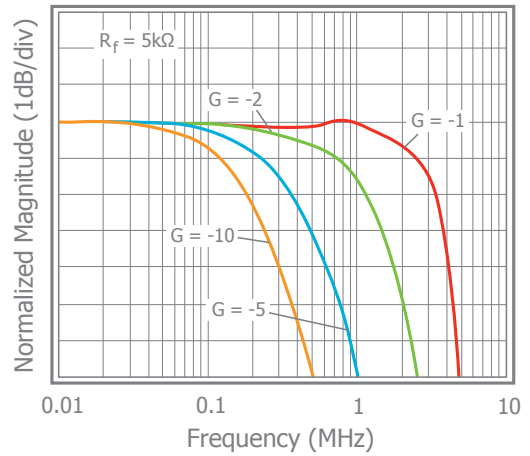
Inverting Frequency Response at $V_S = 5\text{V}$



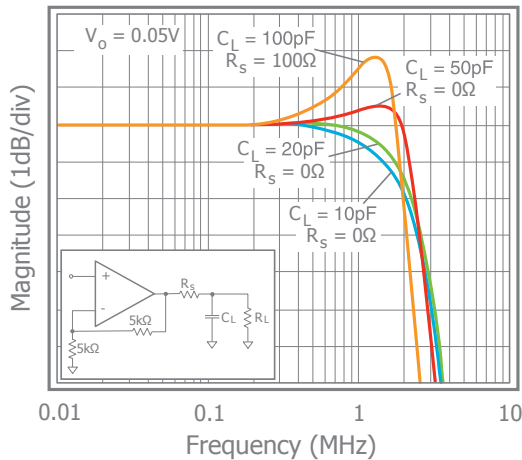
Non-Inverting Frequency Response



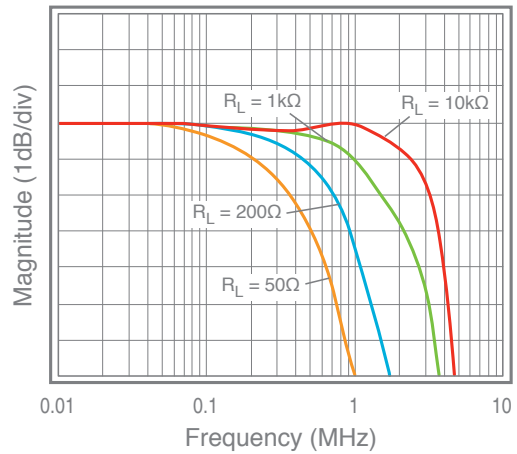
Inverting Frequency Response



Frequency Response vs. C_L



Frequency Response vs. R_L

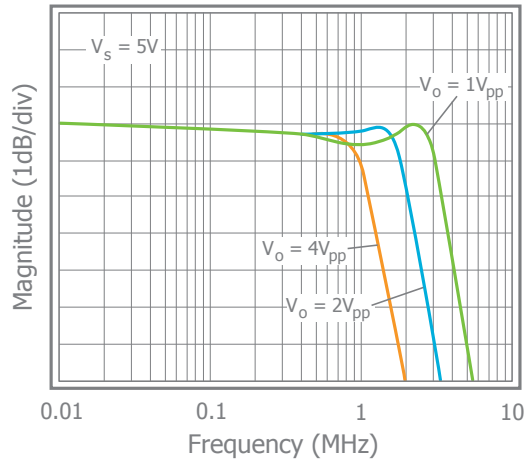




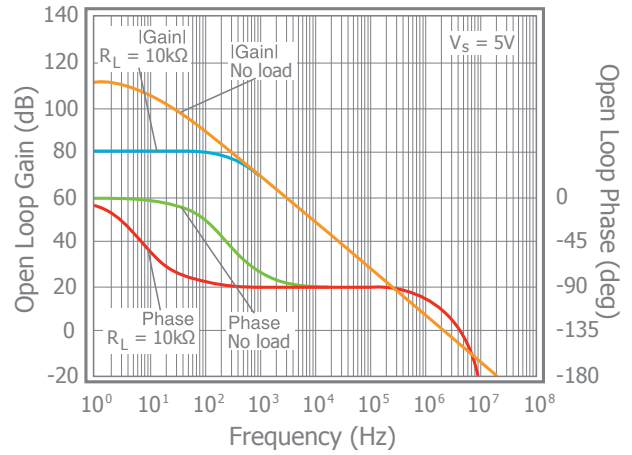
Typical Performance Characteristics

$T_A = 25^\circ\text{C}$, $V_S = +2.7\text{V}$, $R_f = R_g = 5\text{k}\Omega$, $R_L = 10\text{k}\Omega$ to $V_S/2$, $G = 2$; unless otherwise noted.

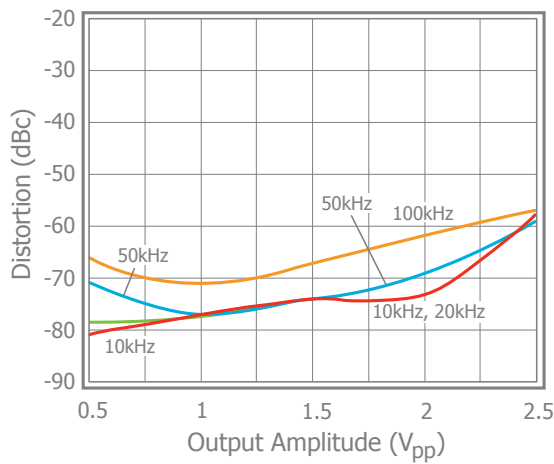
Frequency Response vs. V_{OUT}



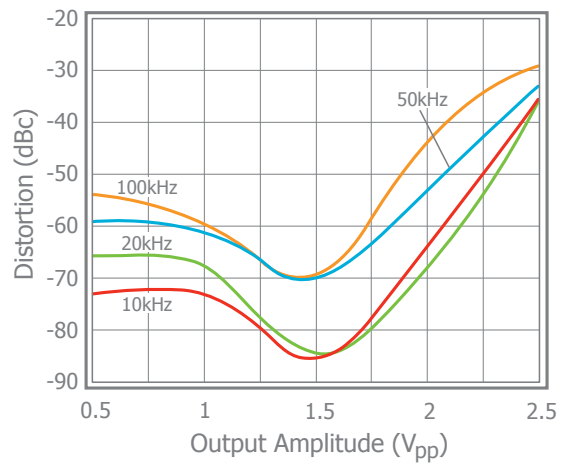
Open Loop Gain & Phase vs. Frequency



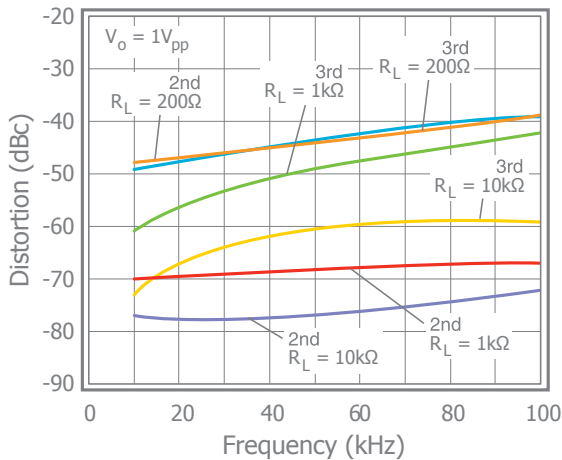
2nd Harmonic Distortion vs. V_{OUT}



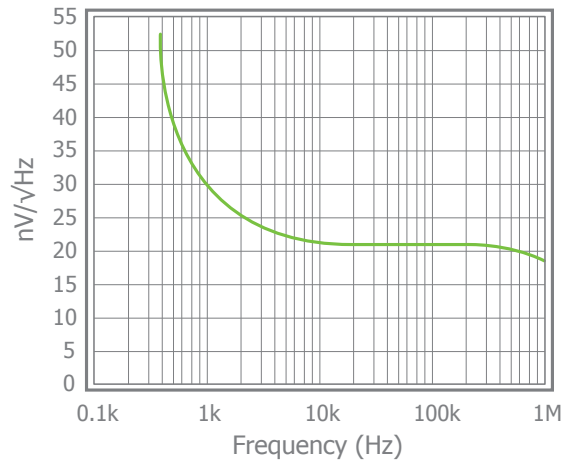
3rd Harmonic Distortion vs. V_{OUT}



2nd & 3rd Harmonic Distortion



Input Voltage Noise

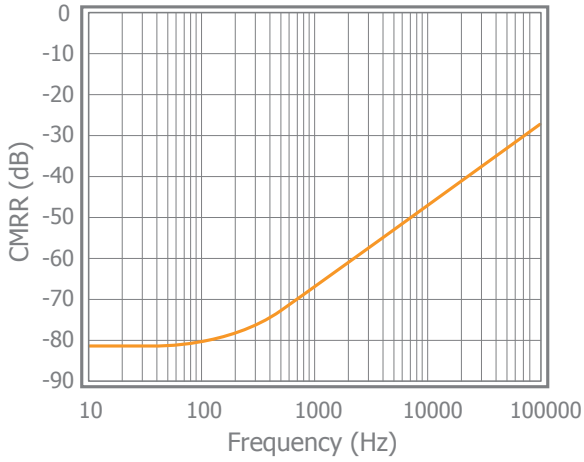




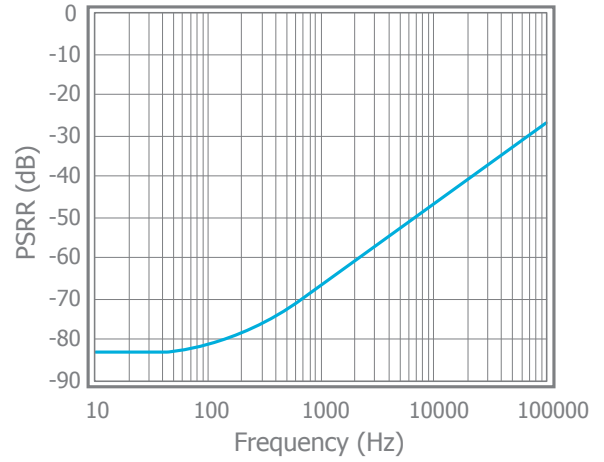
Typical Performance Characteristics - Continued

$T_A = 25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_f = R_g = 150\Omega$, $R_L = 150\Omega$, $G = 2$; unless otherwise noted.

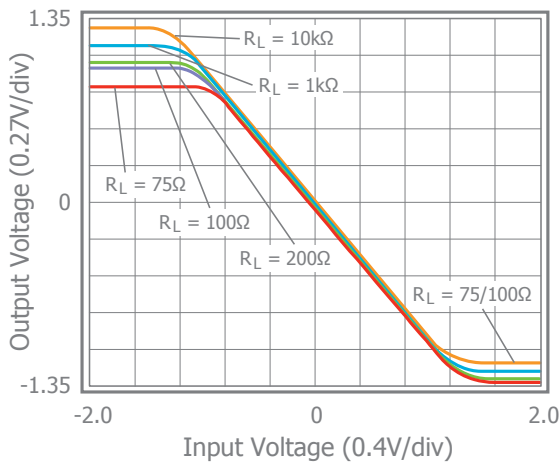
CMRR



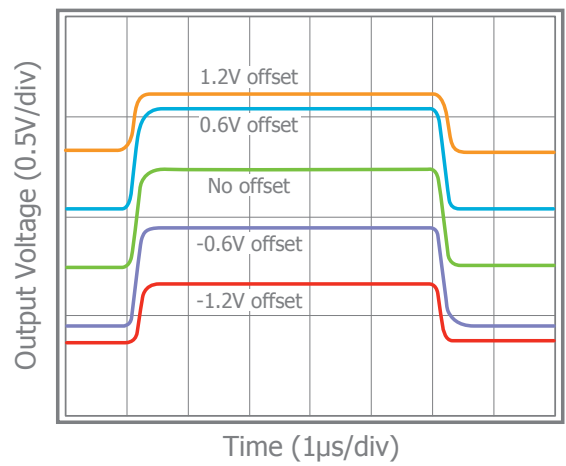
PSRR



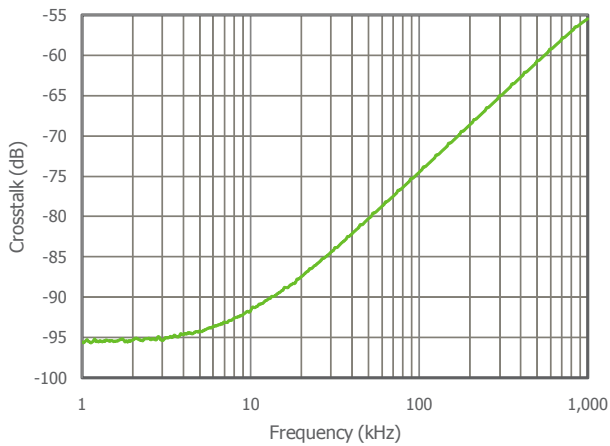
Output Swing vs. Load



Pulse Response vs. Common Mode Voltage



Crosstalk vs. Frequency





Application Information

General Description

The CLCx011 family of amplifiers are single supply, general purpose, voltage-feedback amplifiers. They are fabricated on a complimentary bipolar process, feature a rail-to-rail input and output, and are unity gain stable.

Basic Operation

Figures 1, 2, and 3 illustrate typical circuit configurations for non-inverting, inverting, and unity gain topologies for dual supply applications. They show the recommended bypass capacitor values and overall closed loop gain equations. Figure 4 shows the typical non-inverting gain circuit for single supply applications.

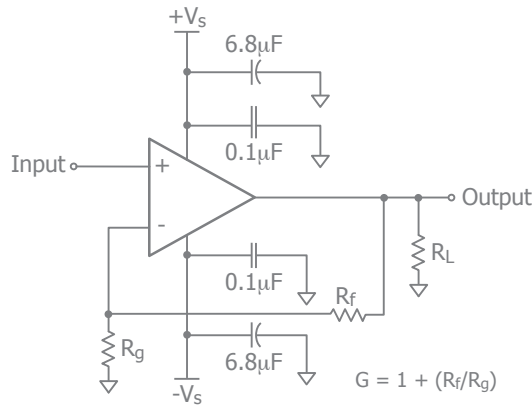


Figure 1. Typical Non-Inverting Gain Circuit

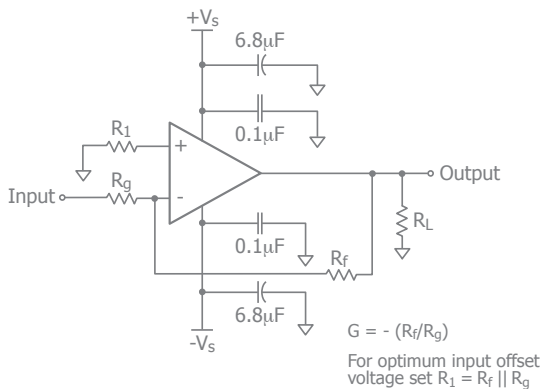


Figure 2. Typical Inverting Gain Circuit

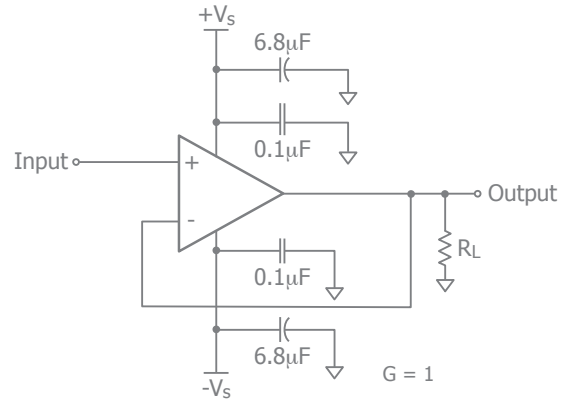


Figure 3. Unity Gain Circuit

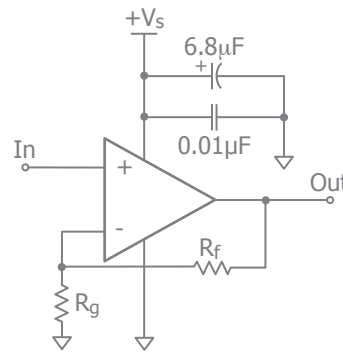


Figure 4. Single Supply Non-Inverting Gain Circuit

Power Dissipation

Power dissipation should not be a factor when operating under the stated 10k ohm load condition. However, applications with low impedance, DC coupled loads should be analyzed to ensure that maximum allowed junction temperature is not exceeded. Guidelines listed below can be used to verify that the particular application will not cause the device to operate beyond its intended operating range.

Maximum power levels are set by the absolute maximum junction rating of 150°C. To calculate the junction temperature, the package thermal resistance value Θ_{JA} (Θ_{JA}) is used along with the total die power dissipation.

$$T_{\text{Junction}} = T_{\text{Ambient}} + (\Theta_{JA} \times P_D)$$

Where T_{Ambient} is the temperature of the working environment.



In order to determine P_D , the power dissipated in the load needs to be subtracted from the total power delivered by the supplies.

$$P_D = P_{\text{supply}} - P_{\text{load}}$$

Supply power is calculated by the standard power equation.

$$P_{\text{supply}} = V_{\text{supply}} \times I_{\text{RMS supply}}$$

$$V_{\text{supply}} = V_{S+} - V_{S-}$$

Power delivered to a purely resistive load is:

$$P_{\text{load}} = ((V_{\text{LOAD}})_{\text{RMS}}^2) / R_{\text{load eff}}$$

The effective load resistor ($R_{\text{load eff}}$) will need to include the effect of the feedback network. For instance,

$R_{\text{load eff}}$ in figure 3 would be calculated as:

$$R_L \parallel (R_f + R_g)$$

These measurements are basic and are relatively easy to perform with standard lab equipment. For design purposes however, prior knowledge of actual signal levels and load impedance is needed to determine the dissipated power. Here, P_D can be found from

$$P_D = P_{\text{Quiescent}} + P_{\text{Dynamic}} - P_{\text{Load}}$$

Quiescent power can be derived from the specified I_S values along with known supply voltage, V_{Supply} . Load power can be calculated as above with the desired signal amplitudes using:

$$(V_{\text{LOAD}})_{\text{RMS}} = V_{\text{PEAK}} / \sqrt{2}$$

$$(I_{\text{LOAD}})_{\text{RMS}} = (V_{\text{LOAD}})_{\text{RMS}} / R_{\text{load eff}}$$

The dynamic power is focused primarily within the output stage driving the load. This value can be calculated as:

$$P_{\text{DYNAMIC}} = (V_{S+} - V_{\text{LOAD}})_{\text{RMS}} \times (I_{\text{LOAD}})_{\text{RMS}}$$

Assuming the load is referenced in the middle of the power rails or $V_{\text{supply}}/2$.

Figure 4 shows the maximum safe power dissipation in the package vs. the ambient temperature for the packages available.

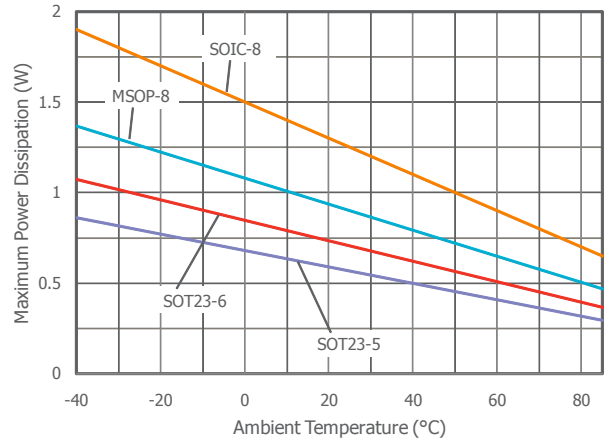


Figure 4. Maximum Power Derating

Input Common Mode Voltage

The common mode input range extends to 250mV below ground and to 250mV above V_s , in single supply operation. Exceeding these values will not cause phase reversal. However, if the input voltage exceeds the rails by more than 0.5V, the input ESD devices will begin to conduct. The output will stay at the rail during this overdrive condition. If the absolute maximum input voltage (700mV beyond either rail) is exceeded, externally limit the input current to $\pm 5\text{mA}$ as shown in Figure 5.

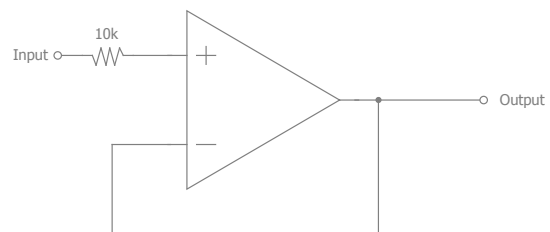


Figure 5. Circuit for Input Current Protection

Driving Capacitive Loads

Increased phase delay at the output due to capacitive loading can cause ringing, peaking in the frequency response, and possible unstable behavior. Use a series resistance, R_S , between the amplifier and the load to help improve stability and settling performance. Refer to Figure 6.

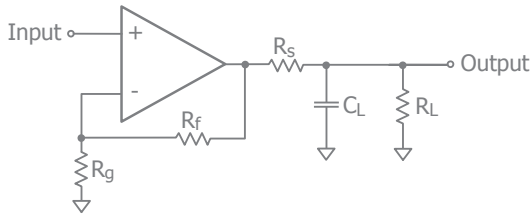


Figure 6. Addition of R_S for Driving Capacitive Loads

Table 1 provides the recommended R_S for various capacitive loads. The recommended R_S values result in approximately <1dB peaking in the frequency response. The Frequency Response vs. C_L plot, on page 6, illustrates the response of the CLCx011.

| C_L (pF) | R_S (Ω) | -3dB BW (kHz) |
|------------|--------------------|---------------|
| 10pF | 0 | 2.2 |
| 20pF | 0 | 2.4 |
| 50pF | 0 | 2.5 |
| 100pF | 100 | 2 |

Table 1: Recommended R_S vs. C_L

For a given load capacitance, adjust R_S to optimize the tradeoff between settling time and bandwidth. In general, reducing R_S will increase bandwidth at the expense of additional overshoot and ringing.

Overdrive Recovery

An overdrive condition is defined as the point when either one of the inputs or the output exceed their specified voltage range. Overdrive recovery is the time needed for the amplifier to return to its normal or linear operating point. The recovery time varies, based on whether the input or output is overdriven and by how much the range is exceeded. The CLCx011 will typically recover in less than 50ns from an overdrive condition. Figure 7 shows the CLC1011 in an overdriven condition.

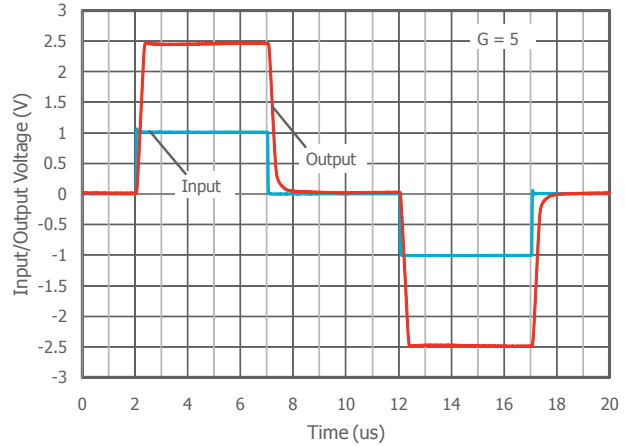


Figure 7. Overdrive Recovery

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. CADEKA has evaluation boards to use as a guide for high frequency layout and as an aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 6.8 μ F and 0.1 μ F ceramic capacitors for power supply decoupling
- Place the 6.8 μ F capacitor within 0.75 inches of the power pin
- Place the 0.1 μ F capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts below for more information.

Evaluation Board Information

The following evaluation boards are available to aid in the testing and layout of these devices:

| Evaluation Board | Products |
|------------------|------------------|
| CEB011 | CLC1011 in SC70 |
| CEB002 | CLC1011 in SOT23 |
| CEB006 | CLC2011 in SOIC |
| CEB010 | CLC2011 in MSOP |
| CEB018 | CLC4011 in SOIC |
| CEB017 | CLC4011 in TSSOP |



Evaluation Board Schematics

Evaluation board schematics and layouts are shown in Figures 8-14. These evaluation boards are built for dual-supply operation. Follow these steps to use the board in a single-supply application:

1. Short -Vs to ground.
2. Use C3 and C4, if the -Vs pin of the amplifier is not directly connected to the ground plane.

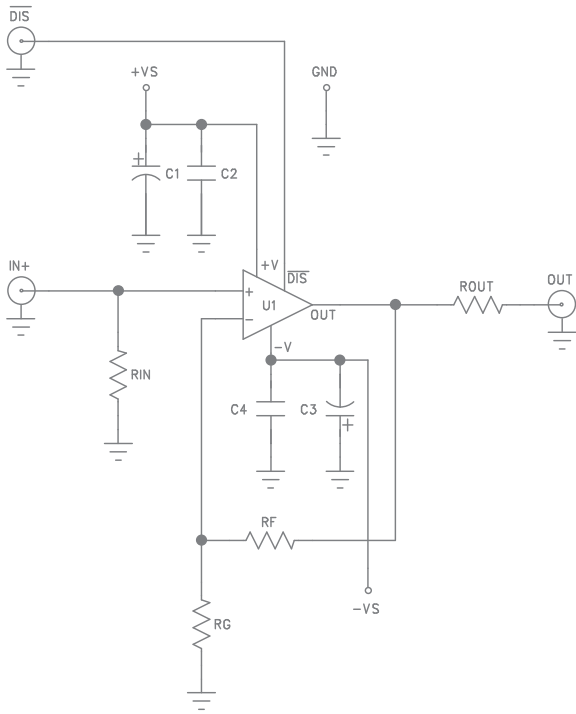


Figure 8. CEB002 & CEB011 Schematic

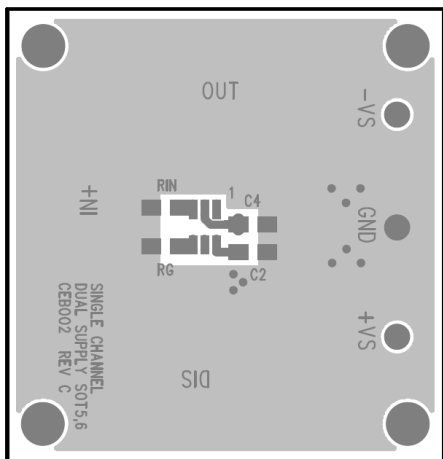


Figure 9. CEB002 Top View

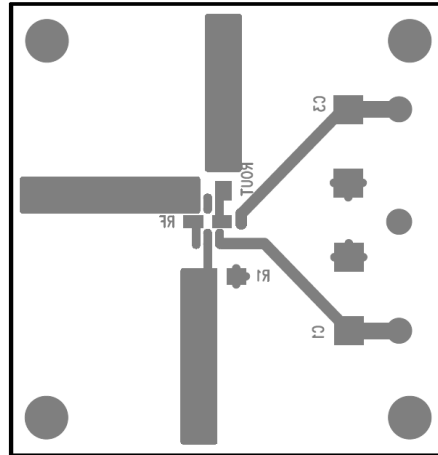


Figure 10. CEB002 Bottom View

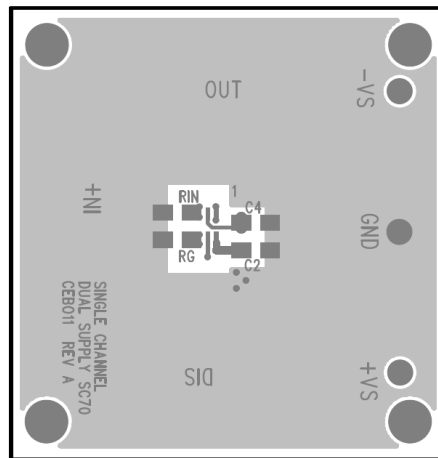


Figure 11. CEB011 Top View

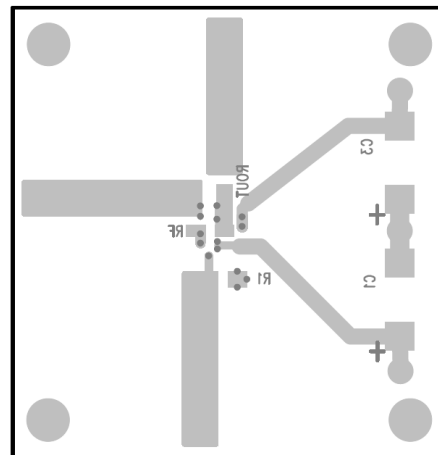


Figure 12. CEB011 Bottom View

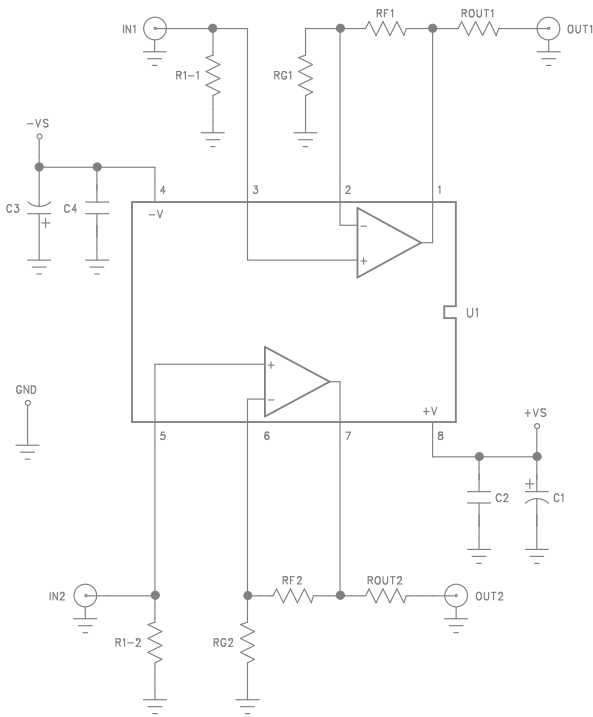


Figure 13. CEB006 & CEB010 Schematic

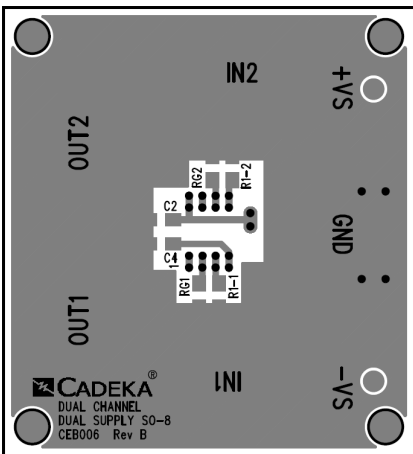


Figure 14. CEB006 Top View

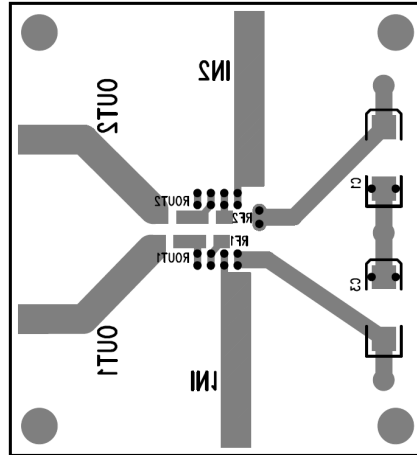


Figure 15. CEB006 Bottom View

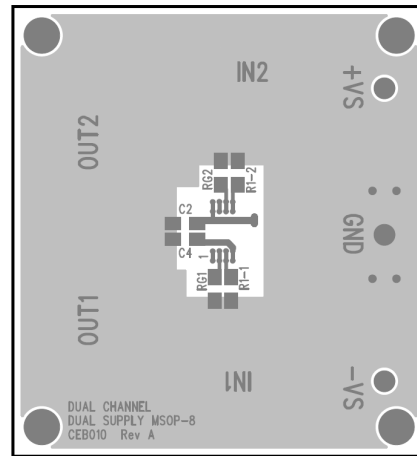


Figure 16. CEB010 Top View

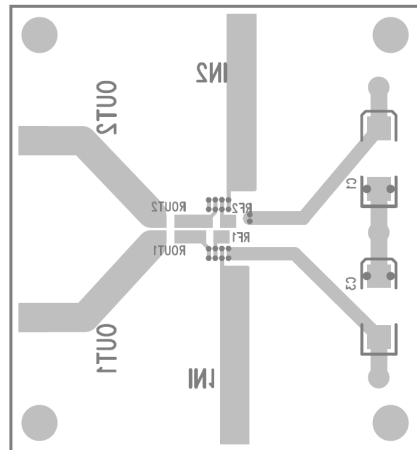


Figure 17. CEB010 Bottom View

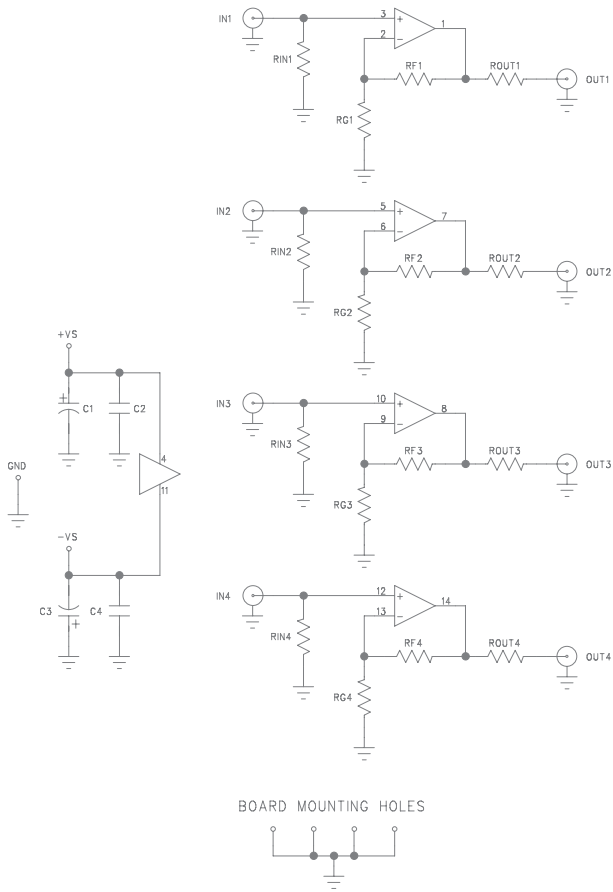


Figure 18. CEB018 & CEB017 Schematic

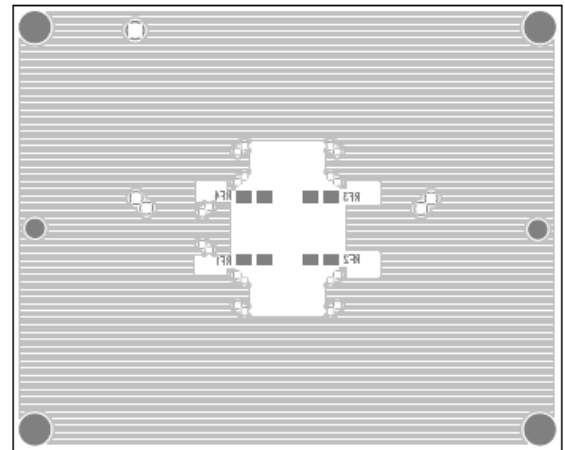


Figure 20. CEB018 Bottom View

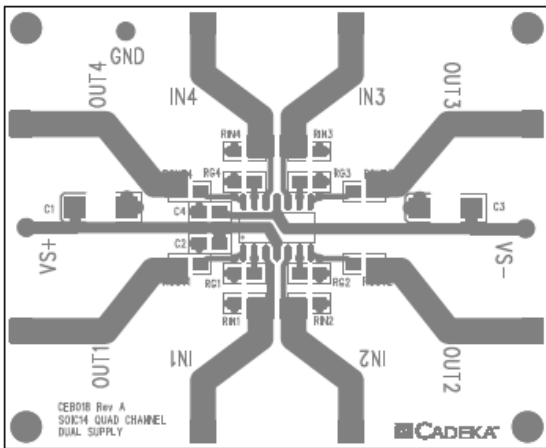
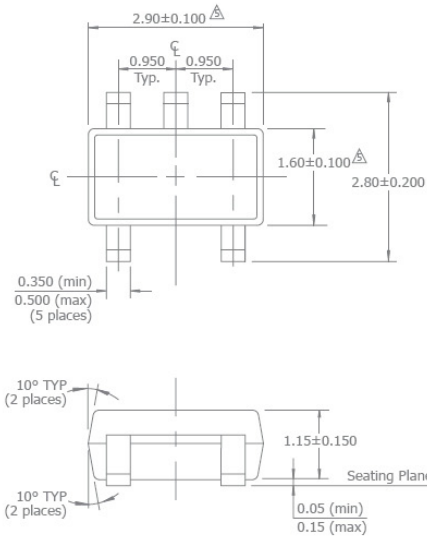


Figure 19. CEB018 Top View



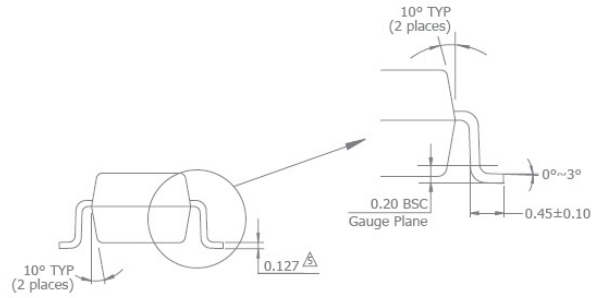
Mechanical Dimensions

SOT23-5 Package

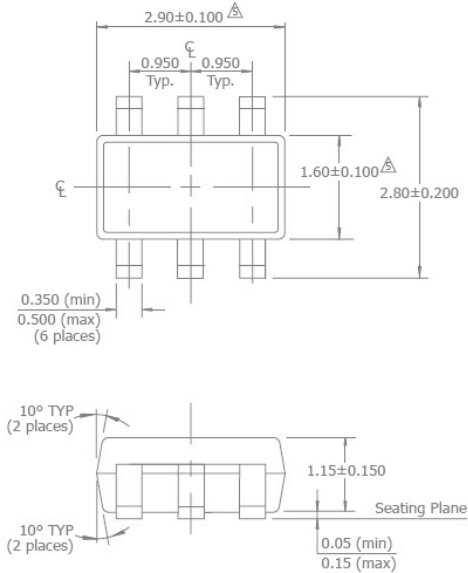


NOTES:

1. Dimensions and tolerances are as per ANSI Y14.5M-1982.
 2. Package surface to be matte finish VDI 11~13.
 3. Die is facing up for mold. Die is facing down for trim/form, ie. reverse trim/form.
 4. The footlength measuring is based on the gauge plane method.
- △ Dimension are exclusive of mold flash and gate burr.
 △ Dimension are exclusive of solder plating.

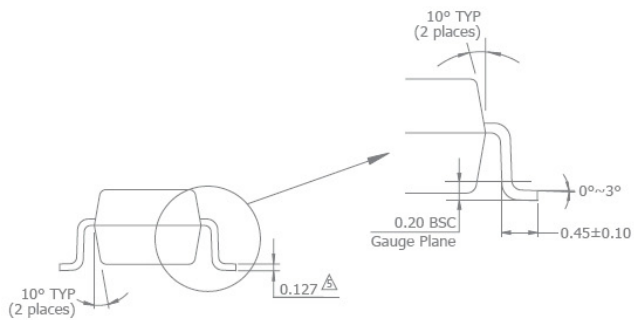


SOT23-6



NOTES:

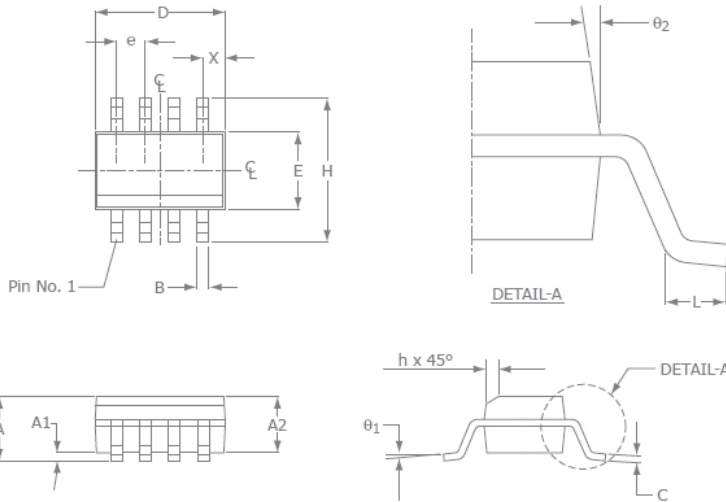
1. Dimensions and tolerances are as per ANSI Y14.5M-1982.
 2. Package surface to be matte finish VDI 11~13.
 3. Die is facing up for mold. Die is facing down for trim/form, ie. reverse trim/form.
 4. The footlength measuring is based on the gauge plane method.
- △ Dimension are exclusive of mold flash and gate burr.
 △ Dimension are exclusive of solder plating.





Mechanical Dimensions continued

SOIC-8 Package

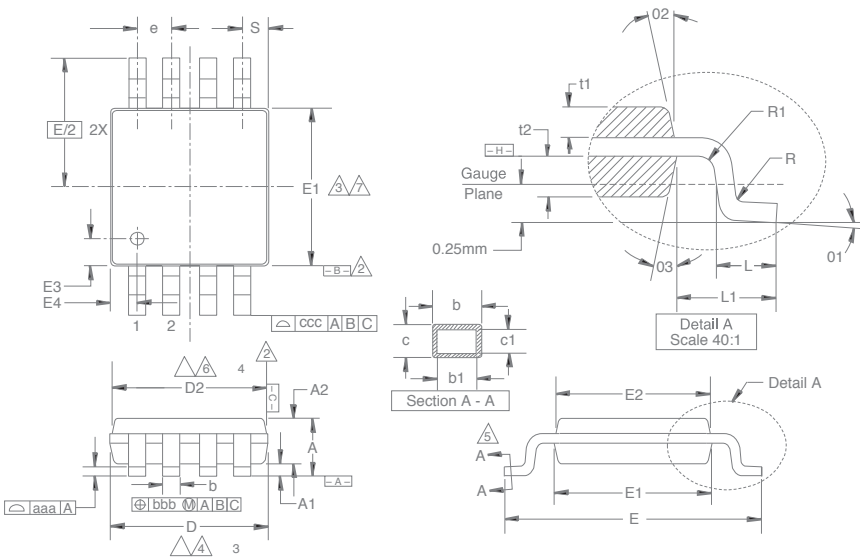


| SOIC-8 | | |
|------------|----------|------|
| SYMBOL | MIN | MAX |
| A1 | 0.10 | 0.25 |
| B | 0.36 | 0.48 |
| C | 0.19 | 0.25 |
| D | 4.80 | 4.98 |
| E | 3.81 | 3.99 |
| e | 1.27 BSC | |
| H | 5.80 | 6.20 |
| h | 0.25 | 0.5 |
| L | 0.41 | 1.27 |
| A | 1.37 | 1.73 |
| θ_1 | 0° | 8° |
| X | 0.55 ref | |
| θ_2 | 7° BSC | |

NOTE:

1. All dimensions are in millimeters.
2. Lead coplanarity should be 0 to 0.1mm (0.004") max.
3. Package surface finishing: VDI 24~27
4. All dimension excluding mold flashes.
5. The lead width, B to be determined at 0.1905mm from the lead tip.

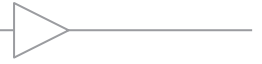
MSOP-8 Package



| Symbol | Min | Max |
|------------|-----------|-------------|
| A | 1.10 | - |
| A1 | 0.10 | ±0.05 |
| A2 | 0.86 | ±0.08 |
| D | 3.00 | ±0.10 |
| D2 | 2.95 | ±0.10 |
| E | 4.90 | ±0.15 |
| E1 | 3.00 | ±0.10 |
| E2 | 2.95 | ±0.10 |
| E3 | 0.51 | ±0.13 |
| E4 | 0.51 | ±0.13 |
| R | 0.15 | +0.15/-0.06 |
| R1 | 0.15 | +0.15/-0.06 |
| t1 | 0.31 | ±0.08 |
| t2 | 0.41 | ±0.08 |
| b | 0.33 | +0.07/-0.08 |
| b1 | 0.30 | ±0.05 |
| c | 0.18 | ±0.05 |
| c1 | 0.15 | +0.03/-0.02 |
| θ_1 | 3.0° | ±3.0° |
| θ_2 | 12.0° | ±3.0° |
| θ_3 | 12.0° | ±3.0° |
| L | 0.55 | ±0.15 |
| L1 | 0.95 BSC | - |
| aaa | 0.10 | - |
| bbb | 0.08 | - |
| ccc | 0.25 | - |
| e | 0.65 BSC | - |
| S | 0.525 BSC | - |

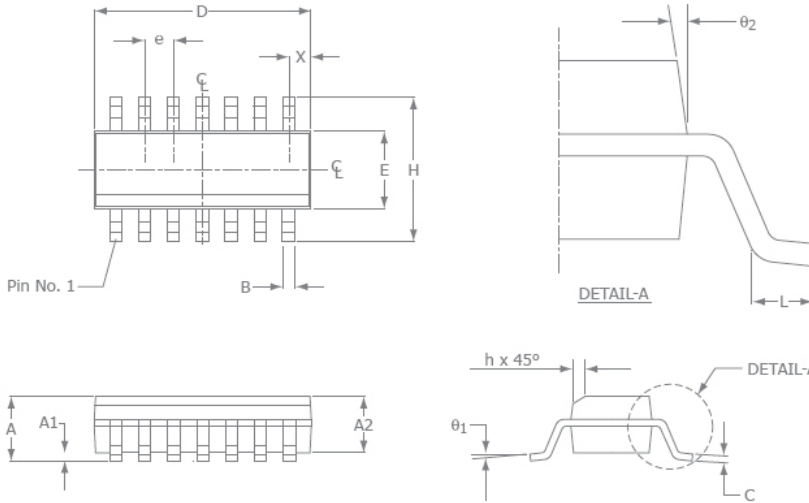
NOTE:

1. All dimensions are in millimeters (angle in degrees), unless otherwise specified.
- ▲ Datums \overline{B} and \overline{C} to be determined at datum plane \overline{H} .
- ▲ Dimensions "D" and "E1" are to be determined at datum \overline{H} .
- ▲ Dimensions "D2" and "E2" are for top package and dimensions "D" and "E1" are for bottom package.
- ▲ Cross sections A - A to be determined at 0.13 to 0.25mm from the leadtip.
- ▲ Dimension "D" and "D2" does not include mold flash, protrusion or gate burrs.
- ▲ Dimension "E1" and "E2" does not include interlead flash or protrusion.



Mechanical Dimensions continued

SOIC-14 Package

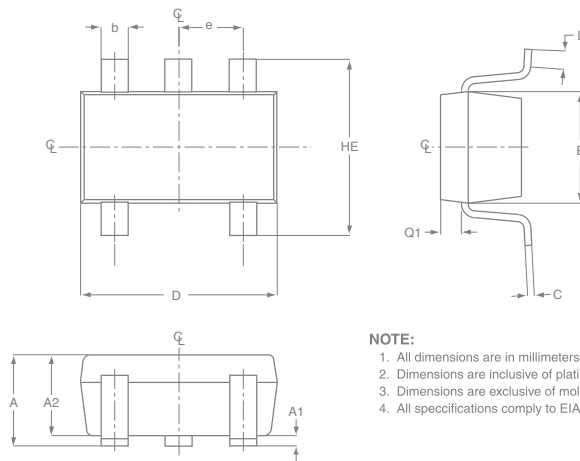


| SOIC-14 | | |
|----------------|----------|------|
| SYMBOL | MIN | MAX |
| A1 | 0.10 | 0.25 |
| B | 0.36 | 0.48 |
| C | 0.19 | 0.25 |
| D | 8.56 | 8.74 |
| E | 3.84 | 3.99 |
| e | 1.27 BSC | |
| H | 5.80 | 6.20 |
| h | 0.25 | 0.5 |
| L | 0.41 | 1.27 |
| A | 1.37 | 1.73 |
| θ ₁ | 0° | 8° |
| X | 0.51 ref | |
| θ ₂ | 7° BSC | |

NOTE:

1. All dimensions are in millimeters.
2. Lead coplanarity should be 0 to 0.1mm (0.004") max
3. Package surface finishing: VDI 24~27
4. All dimension excluding mold flashes.
5. The lead width, B to be determined at 0.1905mm from the lead tip.

SC70-5 Package



| Symbol | Min | Max |
|--------|----------|------|
| e | 0.65 BSC | |
| D | 1.80 | 2.20 |
| b | 0.15 | 0.30 |
| E | 1.15 | 1.35 |
| HE | 1.80 | 2.40 |
| Q1 | 0.10 | 0.40 |
| A2 | 0.80 | 1.00 |
| A1 | 0.00 | 0.10 |
| A | 0.80 | 1.10 |
| c | 0.10 | 0.18 |
| L | 1.10 | 0.30 |

NOTE:

1. All dimensions are in millimeters.
2. Dimensions are inclusive of plating.
3. Dimensions are exclusive of mold flashing and metal burr.
4. All specifications comply to EIAJ SC70.

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