



Logic Diagram

FEATURES:

- 32-Bit microprocessor
- RAD-PAK[®] radiation-hardened against natural space radiation
- Total dose hardness:
 - >100 Krad (Si), dependent upon space mission
- Single event effect:
 - $SEL_{TH} = 37-60 \text{ MeV/mg/cm}^2$
 - $SEU_{TH} = 3.4 \text{ MeV/mg/cm}^2$
 - SEU Cross section $1E-3 \text{ cm}^2/\text{bit}$
- Package:
 - 164 Pin RAD-PAK[®] quad flat pack
- 8, 16, 32-Bit data types
- 8 general purpose 32-Bit registers
- Hardware debugging support
- Very large address space:
 - 4 gigabyte physical
 - 64 terabyte Virtual
 - 4 gigabyte maximum segment size
- Integrated memory management unit
 - Virtual memory support
 - Four levels of protection
 - Fully compatible with 80C286
- Optimized for system development
 - Pipelined instructions
 - On-chip caches support address translation
 - 32 megabytes/sec bus bandwidth

DESCRIPTION:

Maxwell Technologies' 80386DX high performance 32-bit microprocessor features a greater than 100 krad (Si) total dose tolerance, dependent upon space mission. It is designed for very high performance and multitasking operating systems. The integrated memory management and protection architecture includes address translation registers, multitasking hardware and a protection mechanism to support operating systems. The 80386DX allows simultaneous running of multiple operations. In addition, the 80386DX is capable of execution at sustained rates of between 3 and 4 million instructions per second. It offers new testability and debugging features, including a self-test and direct access to the page translation cache.

Maxwell Technologies' patented RAD-PAK[®] packaging technology incorporates radiation shielding in the microcircuit package. It eliminates the need for box shielding while providing the required radiation shielding for a lifetime in orbit or space mission. In a GEO orbit, RAD-PAK provides greater than 100 krad (Si) radiation dose tolerance. This product is available with screening up to Class S.

TABLE 1. 80386DX PIN DESCRIPTION

| PIN | SYMBOL | DESCRIPTION |
|---|---|--------------------------------|
| 1-7, 9, 10, 12, 13, 16, 17, 20, 21, 24, 146-149, 152-154, 156-159, 161-163 | A16-A11, A9, A10, A7, A8, A5, A6, A3, A4, A2, A31-A28, A27-A25, A23-A22, A20-A18 | Address Bus |
| 8, 18, 19, 22, 23, 25, 28-30, 33, 36, 38-40, 47, 48, 65, 66, 68, 73, 76, 77, 82, 84, 86, 88, 103, 106, 107, 114, 125, 126, 129, 130, 133, 134, 145, 155, 160, 164 | NC | Not Connected |
| 11, 15, 27, 32, 35, 43, 51, 53, 55, 57, 61, 70, 92, 95, 100, 111, 118, 122, 138, 142, 151 | V _{SS} | Ground |
| 14, 26, 31, 34, 44, 50, 52, 54, 56, 58, 62, 69, 91, 96, 99, 110, 117, 137, 141, 150, | V _{CC} | Power Supply |
| 37 | INTR | Interrupt Request |
| 41 | NMI | Non-Maskable Interrupt Request |
| 42 | PEREQ | Processor Extension Request |
| 45 | ERROR | Error Status |
| 46 | RESET | Reset |
| 49 | BUSY | Busy Status |
| 59 | LOCK | Bus Lock |
| 60 | W/R | Write/ Read |
| 63 | M/I \bar{O} | Memory I/O |
| 64 | D/C | Data Control |
| 67, 71, 72, 74 | BE $\bar{2}$, BE $\bar{0}$, BE $\bar{3}$, BE $\bar{1}$ | Byte Enables |
| 78 | BS16 | Bus Size 16 |
| 75 | NA | Next Address |
| 79 | HOLD | Bus Hold Request |
| 80 | CLK2 | CPU Clock 2 |
| 81 | ADS | Address Status |
| 83 | READY | Bus Ready Input |
| 85, 87, 89, 90, 93, 94, 97, 98, 102, 104, 105, 108, 109, 112, 113, 115, 116, 119, 120, 121, 123, 124, 127, 128, 131, 132, 135, 136, 139, 140, 143, 144, | D1, D2, D4, D0, D6, D3, D8, D5, D7, D10, D9, D12, D11, D14, D13, D15, D16, D18, D17, D20, D22, D19, D24, D21, D25, D23, D27, D26, D29, D28, D31, D30, | Data Bus |
| 101 | HLDA | Bus Hold Acknowledge |

TABLE 2. 80386DX ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | MIN | MAX | UNIT |
|---------------------------------------|---------------|------|----------------|------|
| Supply Voltage with Respect to Ground | V_{SS} | -0.5 | 6.5 | V |
| Voltage on other pins | | -0.5 | $V_{CC} + 0.5$ | V |
| Thermal Impedance | Θ_{JC} | -- | 1.79 | °C/W |
| Operating Temperature Range (Ambient) | T_A | -55 | 125 | °C |
| Storage Temperature Range (Ambient) | T_S | -65 | 150 | °C |

TABLE 3. DELTA LIMITS

| PARAMETER | VARIATION |
|-----------|------------------------------------|
| I_{CC} | ±10% of specified value in Table 4 |
| I_{LI} | ±10% of specified value in Table 4 |
| I_{LO} | ±10% of specified value in Table 4 |

TABLE 4. 80386DX RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | MIN | MAX | UNIT |
|-----------------------------|-----------|----------------|------|------|
| Digital Supply Voltage | V_{CC} | 4.75 | 5.25 | V |
| Input Low Voltage | V_{IL} | -- | 0.8 | V |
| Input High Voltage | V_{IH} | 2.0 | -- | V |
| CLK2 Input Low Voltage | V_{ILC} | -- | 0.8 | V |
| CLK2 Input High Voltage | V_{IHC} | $V_{CC} - 0.8$ | -- | V |
| Operating Temperature Range | T_A | -55 | +125 | °C |

TABLE 5. 80386DX DC ELECTRICAL CHARACTERISTICS

($V_{CC} = +5V \pm 5\%$; $T_A = -55^\circ C$ TO $+125^\circ C$, UNLESS OTHERWISE SPECIFIED)

| PARAMETER | SYMBOL | CONDITION | MIN | MAX | UNIT |
|------------------------|----------|---|-----|------|---------|
| Input Leakage Current | I_{LI} | All pins except $\overline{BS16}$, \overline{PEREQ} , \overline{BUSY} , and \overline{ERROR} $0V \leq V_{IN} \leq V_{CC}$ | -15 | +15 | μA |
| Output Leakage Current | I_{LO} | $0.45V \leq V_{OUT} \leq V_{CC}$ | -15 | +15 | μA |
| Output Low Voltage | V_{OL} | $I_{OL} = 4 \text{ mA}$: A2 - A31, D0 - D31 | -- | 0.45 | V |
| | | $I_{OL} = 5 \text{ mA}$: BE0 - BE3, W/R, D/C, M/I/O, LOCK, ADS, HLDA | -- | 0.45 | |
| Output High Voltage | V_{OH} | $I_{OH} = 1 \text{ mA}$: A2 - A31, D0 - D31 | 2.4 | -- | V |
| | | $I_{OH} = 0.9 \text{ mA}$: BE0 - BE3, W/R, D/C, M/I/O, LOCK, ADS, HLDA | 2.4 | -- | |

TABLE 5. 80386DX DC ELECTRICAL CHARACTERISTICS

 $(V_{CC} = +5V \pm 5\%; T_A = -55^\circ C \text{ TO } +125^\circ C, \text{ UNLESS OTHERWISE SPECIFIED})$

| PARAMETER | SYMBOL | CONDITION | MIN | MAX | UNIT |
|---------------------------------------|-----------|-------------------------------------|-----|------|---------|
| Power Supply Current | I_{CC} | CLK2 = 32 MHz with 16 MHz Processor | -- | 460 | mA |
| | | CLK2 = 32 MHz with 20 MHz Processor | -- | 550 | |
| | | CLK2 = 32 MHz with 25 MHz Processor | -- | 680 | |
| Input Leakage Current | I_{IH} | PEREQ Pin ¹ | -- | 200 | μA |
| | I_{IL} | BS16, BUSY, ERROR Pins ² | -- | -400 | μA |
| CLK2 Capacitance ³ | C_{CLK} | $F_C = 1 \text{ MHz}$ | -- | 20 | pF |
| Input or I/O Capacitance ¹ | C_{IN} | $F_C = 1 \text{ MHz}$ | -- | 20 | pF |
| Output Capacitance ¹ | C_{OUT} | $F_C = 1 \text{ MHz}$ | -- | 25 | pF |

1. $V_{IH} = 2.4V$. PEREQ input has an internal pulldown resistor.
2. $V_{IL} = 0.45V$. BS16, BUSY and ERROR inputs have an internal pulldown resistor.
3. Guaranteed by design.

TABLE 6. 80386DX AC ELECTRICAL CHARACTERISTICS

 $(V_{CC} = +5V \pm 10\%; V_{PP} = V_{SS}; T_A = -55^\circ C \text{ TO } +125^\circ C, \text{ UNLESS OTHERWISE SPECIFIED})$

| PARAMETER | SYMBOL | CONDITION | MIN | MAX | UNIT | |
|-----------------------------|----------|------------------------|-----|-----|------|-----|
| Operating Frequency | -- | Half of CLK2 Frequency | | | MHz | |
| | | | -16 | 4 | | 16 |
| | | | -20 | 4 | | 20 |
| | | | -25 | 4 | | 25 |
| CLK2 Period | t_1 | | | | ns | |
| | | | -16 | 31 | | 125 |
| | | | -20 | 25 | | 125 |
| | | | -25 | 20 | | 125 |
| CLK2 High Time | t_{2a} | at 2V | | | ns | |
| | | | -16 | 9 | | -- |
| | | | -20 | 8 | | -- |
| | | | -25 | 7 | | -- |
| CLK2 High Time ¹ | t_{2b} | at $(V_{CC} - 0.8V)$ | | | ns | |
| | | | -16 | 5 | | -- |
| | | | -20 | 5 | | -- |
| | | | -25 | 4 | | -- |
| CLK2 Low Time | t_{3a} | at 2V | | | ns | |
| | | | -16 | 9 | | -- |
| | | | -20 | 8 | | -- |
| | | | -25 | 7 | | -- |
| CLK2 Low Time ¹ | t_{3b} | at $(V_{CC} - 0.8V)$ | | | ns | |
| | | | -16 | 7 | | -- |
| | | | -20 | 6 | | -- |
| | | | -25 | 5 | | -- |

TABLE 6. 80386DX AC ELECTRICAL CHARACTERISTICS
 ($V_{CC} = +5V \pm 10\%$; $V_{PP} = V_{SS}$; $T_A = -55^\circ C$ TO $+125^\circ C$, UNLESS OTHERWISE SPECIFIED)

| PARAMETER | SYMBOL | CONDITION | MIN | MAX | UNIT |
|---|----------|--|-----|-----|------|
| CLK2 Fall Time ¹ | t_4 | $(V_{CC} - 0.8V)$ to $0.8V$ | | | ns |
| -16 | | | -- | 8 | |
| -20 | | | -- | 8 | |
| -25 | | | -- | 7 | |
| CLK2 Rise Time ¹ | t_5 | $0.8V$ to $(V_{CC} - 0.8V)$ | | | ns |
| -16 | | | -- | 8 | |
| -20 | | | -- | 8 | |
| -25 | | | -- | 7 | |
| A2 - A31 Valid Delay | t_6 | $C_L = 120pF$ ($C_L = 50pF$ for 25 MHz) | | | ns |
| -16 | | | 4 | 36 | |
| -20 | | | 4 | 30 | |
| -25 | | | 4 | 21 | |
| A2 - A31 Float Delay ^{1,2} | t_7 | | | | ns |
| -16 | | | 4 | 40 | |
| -20 | | | 4 | 32 | |
| -25 | | | 4 | 30 | |
| BE0 - BE3, LOCK Valid Delay | t_8 | $C_L = 75pF$ ($C_L = 50pF$ for 25 MHz) | | | ns |
| -16 | | | 4 | 36 | |
| -20 | | | 4 | 30 | |
| -25 | | | 4 | 24 | |
| BE0 - BE3, LOCK Float Delay ^{1,2} | t_9 | | | | ns |
| -16 | | | 4 | 40 | |
| -20 | | | 4 | 32 | |
| -25 | | | 4 | 30 | |
| W/R, M/I \bar{O} , D/C and ADS Valid Delay | t_{10} | $C_L = 75pF$ ($C_L = 50pF$ for 25 MHz) | | | ns |
| -16 | | | 6 | 33 | |
| -20 | | | 6 | 28 | |
| -25 | | | 4 | 21 | |
| W/R, M/I \bar{O} , D/C and ADS Float Delay ^{1,2} | t_{11} | | | | ns |
| -16 | | | 6 | 35 | |
| -20 | | | 6 | 30 | |
| -25 | | | 4 | 30 | |
| D0 - D31 Valid Delay | t_{12} | $C_L = 120pF$ ($C_L = 50pF$ for 25 MHz) | | | ns |
| -16 | | | 4 | 48 | |
| -20 | | | 4 | 38 | |
| -25 | | | 7 | 27 | |
| D0 - D31 Float Delay ^{1,2} | t_{13} | | | | ns |
| -16 | | | 4 | 35 | |
| -20 | | | 4 | 27 | |
| -25 | | | 4 | 22 | |
| HLDA Valid Delay | t_{14} | $C_L = 75pF$ ($C_L = 50pF$ for 25 MHz) | | | ns |
| -16 | | | 6 | 323 | |
| -20 | | | 6 | 28 | |
| -25 | | | 4 | 22 | |

TABLE 6. 80386DX AC ELECTRICAL CHARACTERISTICS
 ($V_{CC} = +5V \pm 10\%$; $V_{PP} = V_{SS}$; $T_A = -55^\circ C$ TO $+125^\circ C$, UNLESS OTHERWISE SPECIFIED)

| PARAMETER | SYMBOL | CONDITION | MIN | MAX | UNIT |
|--|----------|-----------|----------------|----------------|------|
| N/A Setup Time -16 -20 -25 | t_{15} | | 11 9 7 | -- -- -- | ns |
| N/A Hold Time -16 -20 -25 | t_{16} | | 14 14 3 | -- -- -- | ns |
| BS16 Setup Time -16 -20 -25 | t_{17} | | 13 13 7 | -- -- -- | ns |
| BS16 Hold Time -16 -20 -25 | t_{18} | | 21 21 3 | -- -- -- | ns |
| READY Setup Time -16 -20 -25 | t_{19} | | 21 12 9 | -- -- -- | ns |
| READY Hold Time -16 -20 -25 | t_{20} | | 4 4 4 | -- -- -- | ns |
| D0 - D31 Read Setup Delay -16 -20 -25 | t_{21} | | 11 11 6 | -- -- -- | ns |
| D0 - D31 Read Hold Delay -16 -20 -25 | t_{22} | | 6 6 5 | -- -- -- | ns |
| HOLD Setup Time -16 -20 -25 | t_{23} | | 26 17 15 | -- -- -- | ns |
| HOLD Hold Time -16 -20 -25 | t_{24} | | 5 5 3 | -- -- -- | ns |
| RESET Setup Time -16 -20 -25 | t_{25} | | 10 10 10 | -- -- -- | ns |

TABLE 6. 80386DX AC ELECTRICAL CHARACTERISTICS
 ($V_{CC} = +5V \pm 10\%$; $V_{PP} = V_{SS}$; $T_A = -55^\circ C$ TO $+125^\circ C$, UNLESS OTHERWISE SPECIFIED)

| PARAMETER | SYMBOL | CONDITION | MIN | MAX | UNIT |
|---|----------|-----------|---------------|----------------|------|
| RESET Hold Time -16 -20 -25 | t_{26} | | 4 4 3 | -- -- -- | ns |
| NMI, INTR Setup Time ³ -16 -20 -25 | t_{27} | | 16 16 6 | -- -- -- | ns |
| NMI, INTR Hold Time ³ -16 -20 -25 | t_{28} | | 16 16 6 | -- -- -- | ns |
| REREQ, ERROR, BUSY Setup Time ³ -16 -20 -25 | t_{29} | | 16 14 6 | -- -- -- | ns |
| REREQ, ERROR, BUSY Hold Time ³ -16 -20 -25 | t_{30} | | 5 5 5 | -- -- -- | ns |

1. Guaranteed by design.
2. Float condition occurs when maximum when output current becomes less than ILO in magnitude.
3. These inputs are allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes, to assure recognition within a specific CLK2 period.

FIGURE 1. AC TEST LOADS



$C_L = 120$ pF on A2-A31, D0-D31
 $C_L = 75$ pF on BE0#-BE3#, W/R#, M/IO#, D/C#, ADS#,
 LOCK#, HLDA
 C_L includes all parasitic capacitances.

FIGURE 2. CLK2 TIMING

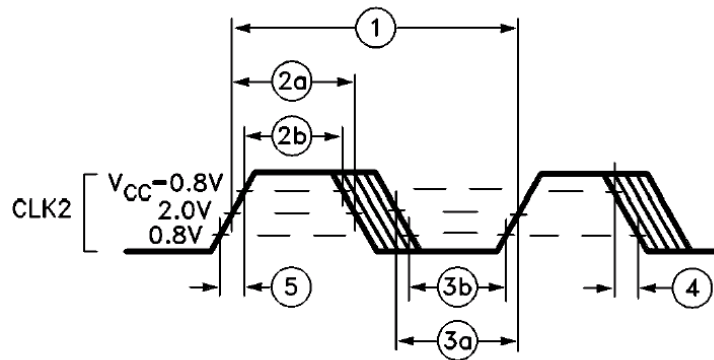


FIGURE 3. INPUT SETUP AND HOLD TIME



FIGURE 4. OUTPUT VALID DELAY TIMING

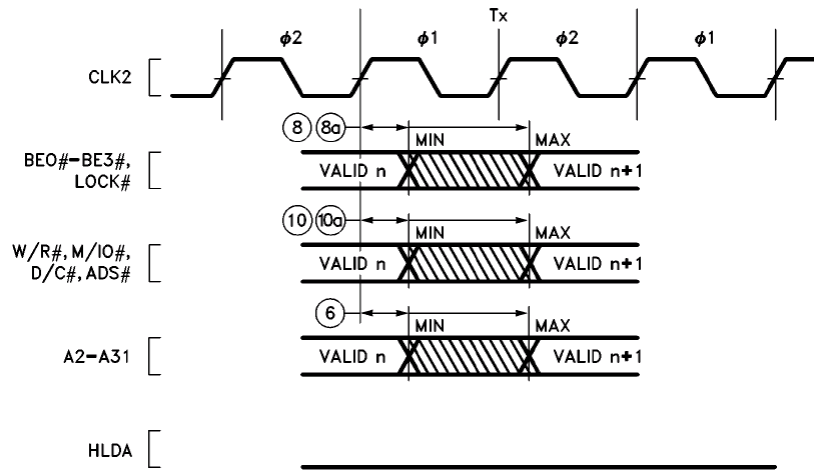


FIGURE 5. WRITE DATA VALID DELAY TIMING (25 MHz)

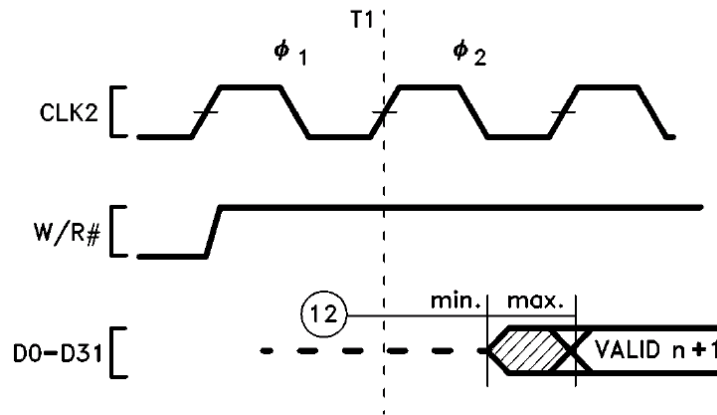


FIGURE 6. WRITE DATA HOLD TIMING (25 MHz)



FIGURE 7. WRITE DATA VALID DELAY TIMING (20 MHz)

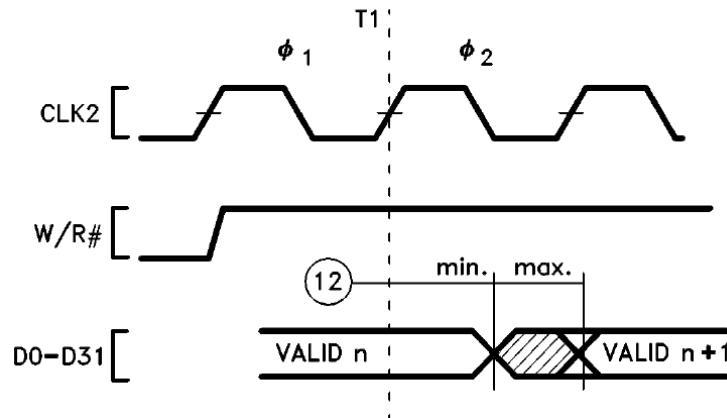


FIGURE 8. TYPICAL OUTPUT VALID DELAY VERSUS LOAD CAPACITANCE AT MAXIMUM OPERATING TEMPERATURE ($C_L = 120$ pF)



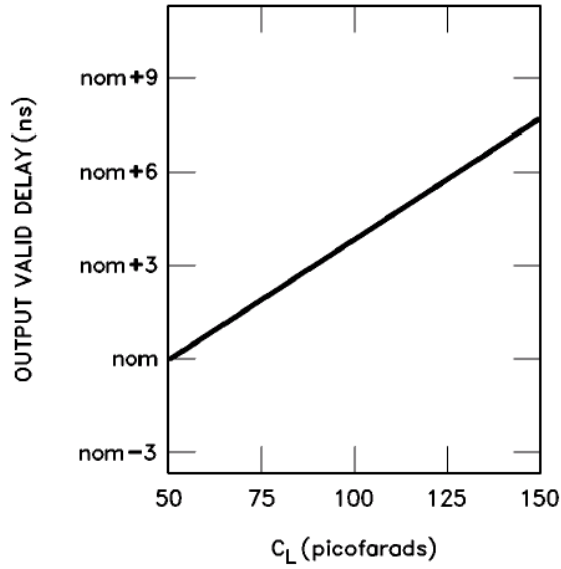
NOTE:
This graph will not be linear outside of the C_L range shown.

FIGURE 9. TYPICAL OUTPUT VALID DELAY VERSUS LOAD CAPACITANCE AT MAXIMUM OPERATING TEMPERATURE ($C_L = 75$ pF)



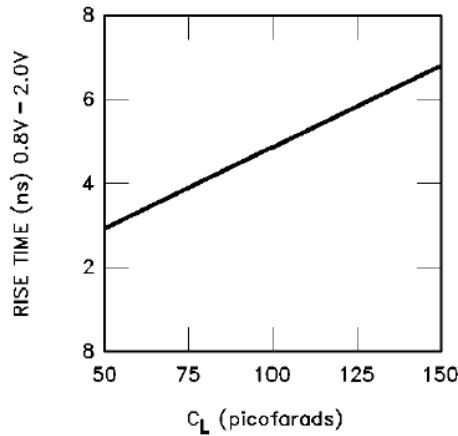
NOTE:
This graph will not be linear outside of the C_L range shown.

FIGURE 10. TYPICAL OUTPUT VALID DELAY VERSUS LOAD CAPACITANCE AT MAXIMUM OPERATING TEMPERATURE ($C_L = 50$ pF)



NOTE:
This graph will not be linear outside of the C_L range shown.

FIGURE 11. TYPICAL OUTPUT RISE TIME VERSUS LOAD CAPACITANCE AT MAXIMUM OPERATING TEMPERATURE



NOTE:
This graph will not be linear outside of the C_L range shown.

FIGURE 12. OUTPUT FLOAT DELAY AND HLDA AND DELAY TIMING



FIGURE 13. RESET SETUP AND HOLD TIMING, AND INTERNAL PHASE



The second internal processor phase following RESET high-to-low transition (provided t_{25} and t_{26} are met) is $\phi 2$.



164-PIN RAD-PAK[®] QUAD FLAT PACKAGE

| SYMBOL | DIMENSION | | |
|--------|-----------|-------|-------|
| | MIN | NOM | MAX |
| A | 0.118 | 0.132 | 0.146 |
| b | 0.007 | 0.008 | 0.013 |
| c | 0.004 | 0.006 | 0.009 |
| D | 1.138 | 1.150 | 1.167 |
| D1 | 1.000 BSC | | |
| e | 0.025 BSC | | |
| S1 | 0.013 | 0.071 | -- |
| F1 | 0.890 | 0.895 | 0.900 |
| F4 | 0.880 | 0.890 | 0.899 |
| L | 2.500 | 2.520 | 2.540 |
| L1 | 2.485 | 2.500 | 2.505 |
| L2 | 1.690 | 1.700 | 1.710 |
| A1 | 0.078 | 0.090 | 0.102 |
| N | 164 | | |

Q164-01

Note: All dimensions in inches

Important Notice:

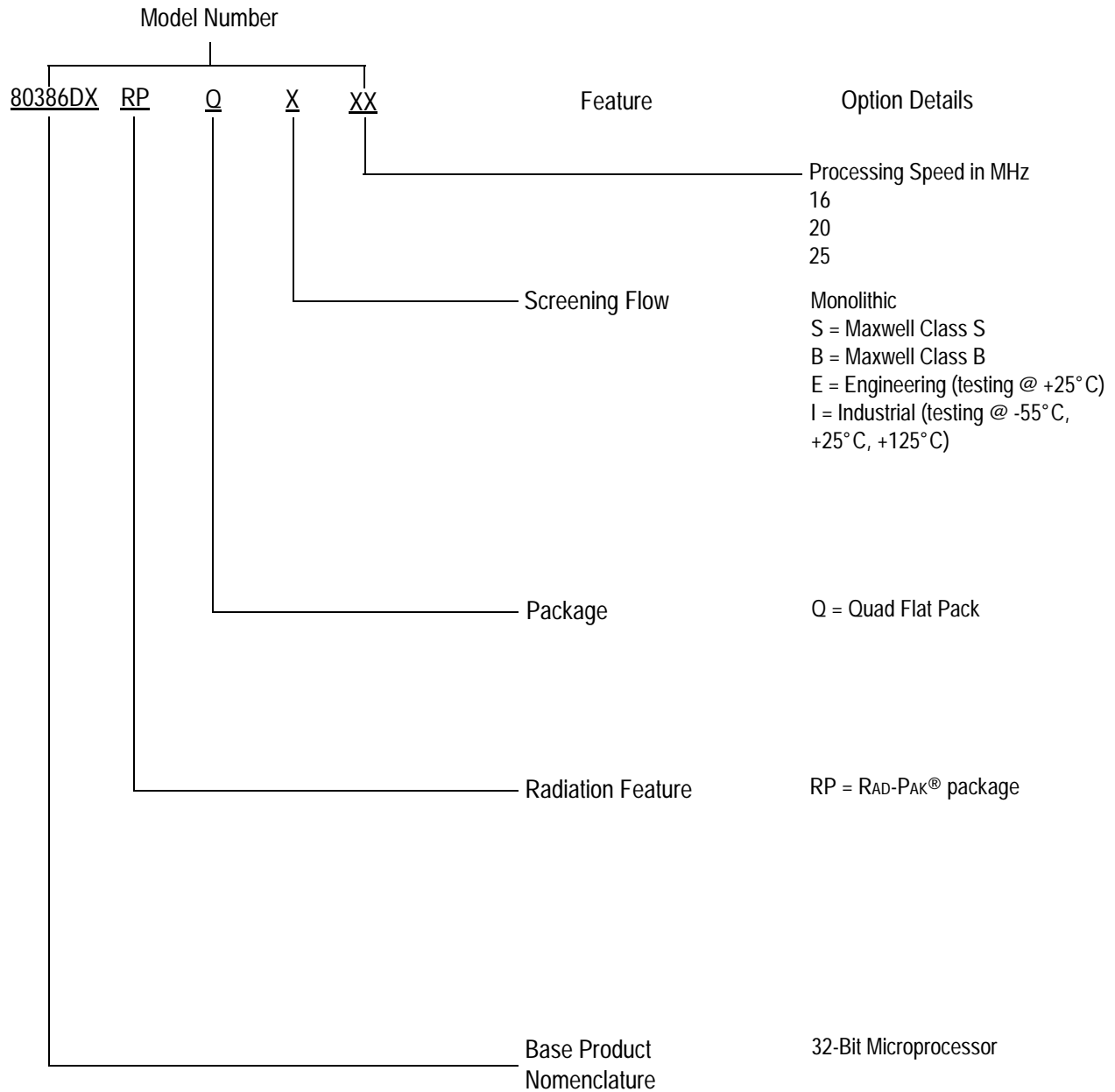
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