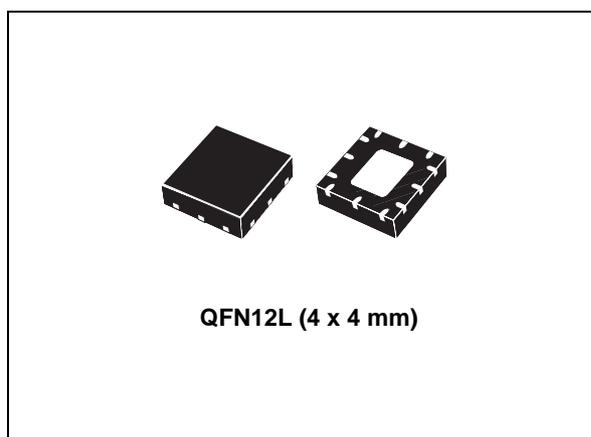


Dual synchronous rectification with reset or inhibit, 0.5 A, 1.5 MHz adjustable step-down switching regulator

Datasheet - production data



Description

The ST2S06A33 and ST2S06B are dual step-down DC-DC converters optimized for powering low-voltage digital cores in ODD applications and, generally, to replace high current linear solutions when the power dissipation may cause high heating of the application environment. It provides up to 0.5 A over an input voltage range of 2.5 V to 5.5 V.

A high switching frequency of 1.5 MHz allows the use of tiny surface-mount components as well as a resistor divider to set the output voltage value. Only an inductor and two capacitors are required. A low output ripple is guaranteed by the current mode PWM topology and the utilization of low ESR SMD ceramic capacitors. The devices are thermally protected and current-limited to prevent damage due to accidental short-circuit. The ST2S06A33 and ST2S06B are available in the QFN12L (4x4 mm) package.

Features

- Step-down current mode PWM (1.5 MHz) DC-DC converter
- Fixed or adjustable output voltage from 0.8 V
- 2% DC output voltage tolerance
- Synchronous rectification
- Reset function for A version
- Inhibit function for B version
- Internal soft start for startup current limitation and power ON delay of 50-100 μ s
- Typical efficiency: > 90%
- 0.5 A output current capability
- Non-switching quiescent current: max 1.2 mA over temperature range
- $R_{DS(ON)}$ 150 m Ω (typ.)
- Uses tiny capacitors and inductors
- Available in QFN12L (4x4 mm)

Table 1. Device summary

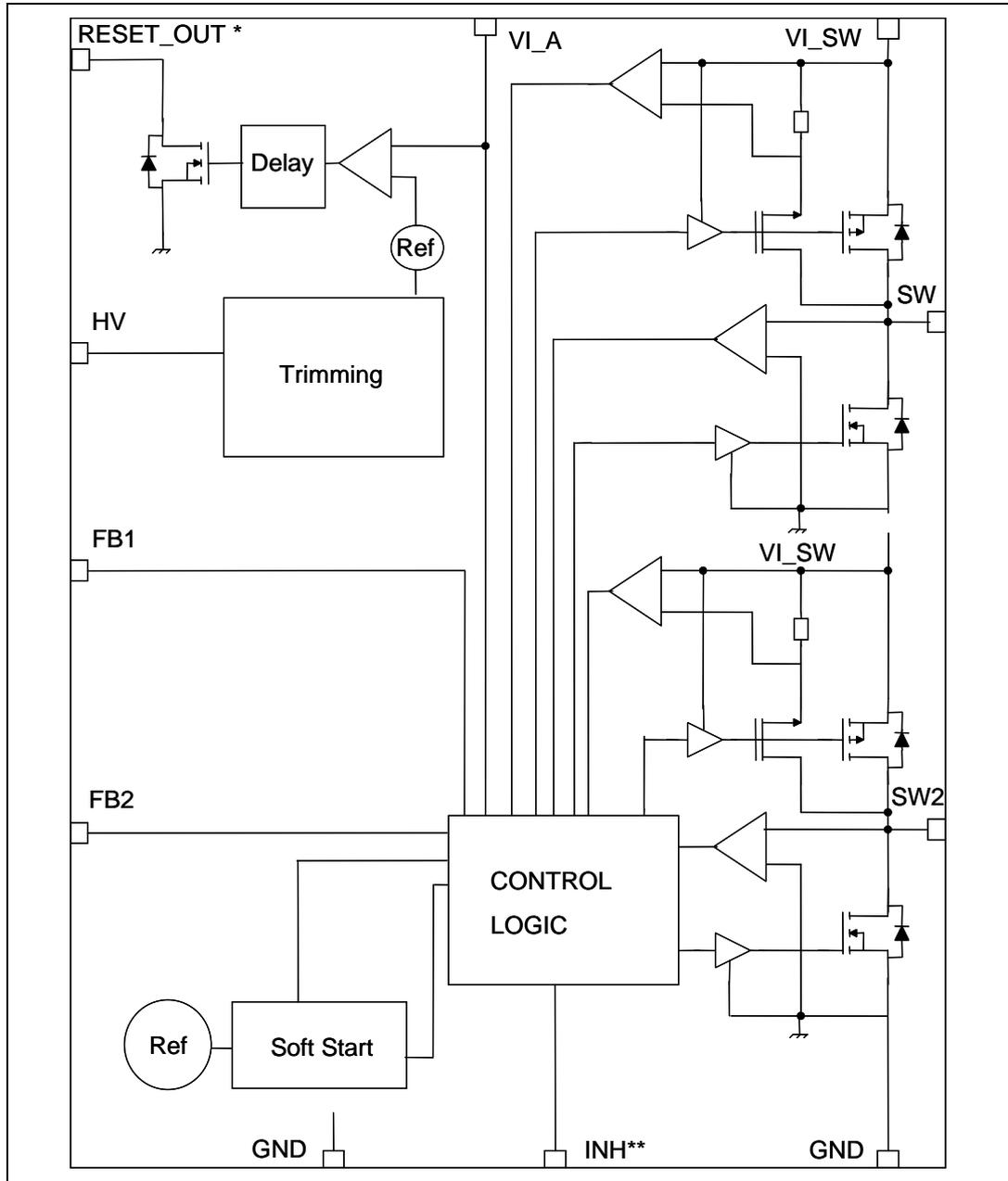
Order codes	Package	Packaging
ST2S06A33PQR	QFN12L (4 x 4 mm)	Tape and reel
ST2S06BPQR		

Contents

1	Schematic diagram	3
2	Pin configuration	4
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5	Typical performance characteristics	8
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1 Schematic diagram

Figure 1. Schematic diagram



* ST2S06A33

** ST2S06B

2 Pin configuration

Figure 2. Pin connections (top view)

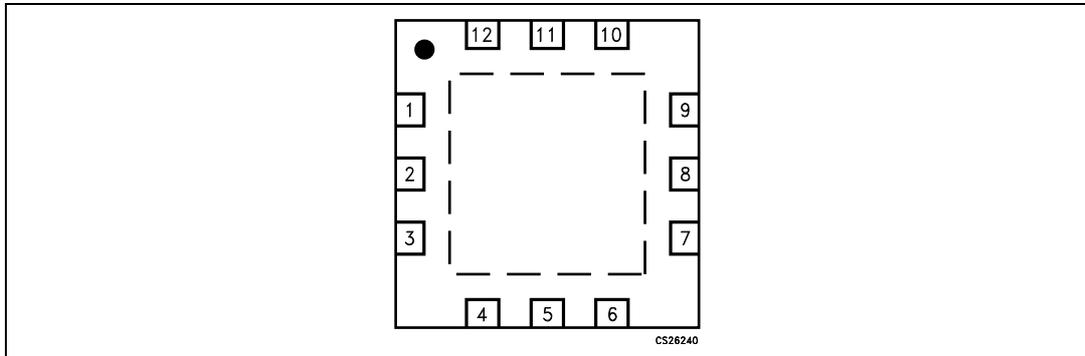


Table 2. Pin description

Pin n°	ST2S06A33	ST2S06B	Name and function
1	HV	HV	Programing pin. It must be floating or connected to GND.
2	FB2	FB2	Feedback voltage
3	GND2	GND2	Power ground
4	SW2	SW2	Switching pin
5	VIN_SW	VIN_SW	Power input voltage pin
6	SW1	SW1	Switching pin
7	GND1	GND1	Power ground
8	FB1/OUT1	FB1	Feedback voltage / output voltage
9	Reset_out	NC	Reset out pin
10	NC	INH	Inhibit pin
11	VIN_A	VIN_A	Supply for analog circuit
12	GND_A	GND_A	System ground

3 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN_SW}	Positive power supply voltage	-0.3 to 7	V
V_{IN_A}	Positive power supply voltage	-0.3 to 7	V
V_{INH}	Inhibit voltage	-0.3 to 7	V
SWITCH voltage	Max. voltage of output pin	-0.3 to 7	V
$V_{FB1,2}/V_{O1}$	Feedback voltage/output voltage	-0.3 to 2.5	V
V_{O1}	Output voltage (for $V_O > 1.6$ V)	-0.3 to 5	V
Current into VFB pin	Common mode input voltage	+1 to -1	mA
T_J	Max junction temperature	150	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{LEAD}	Lead temperature (soldering) 10 sec.	300	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case	10	°C/W
R_{thJA}	Thermal resistance junction-ambient	60	°C/W

Table 5. ESD performance

Symbol	Parameter	Test conditions	Value	Unit
ESD	ESD protection voltage	HBM-DH11C	4	kV

4 Electrical characteristics

$V_{IN_SW} = V_{IN_A} = 5\text{ V}$, $V_{O1} = 3.3\text{ V}$, $V_{O2} = 1.2\text{ V}$, $C_1 = 4.7\text{ }\mu\text{F}$, $C_2 = C_3 = 22\text{ }\mu\text{F}$, $L_1 = L_2 = 3.3\text{ }\mu\text{H}$, $T_J = -30\text{ to }125\text{ }^\circ\text{C}$ unless otherwise specified. Typical values are referred to $25\text{ }^\circ\text{C}$.

Table 6. Electrical characteristics for the ST2S06A33

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
OUT ₁	Output feedback pin		3.23	3.3	3.37	V
FB ₂	Feedback voltage		784	800	816	mV
I _{O1}	I _{O1} pin bias current	V _O = 3.5 V		15	20	μA
I _{FB2}	V _{FB} pin bias current	V _{FB} = 1 V			600	nA
I _Q	Quiescent current	V _{FB} = 1 V			1.2	mA
I _{O1,2}	Output current	V _{IN} = 4 to 5.5 V ⁽¹⁾		0.8		A
I _{MIN}	Minimum output current		1			mA
%V _{O1,2} /ΔV _{I_N}	Reference line regulation	4V < V _{IN} < 5.5 V		0.032		%V _O / V _{IN}
ΔV _{O1,2}	Reference load regulation	10mA < I _O < 0.5 A		5.5	15	mV
PWM f _S	PWM switching frequency ⁽¹⁾	V _{FB} = 0.7 V, T _A = 25°C	1.2	1.5	1.8	MHz
D _{MAX}	Maximum duty cycle	V _{FB} = 0.7 V, T _A = 25°C	85	94		%
I _{SWL}	Switching current limitation		1	1.2		A
I _{LKN}	NMOS leakage current	V _{FB} = 0.9 V, T _A = 25°C		0.1		μA
I _{LKP}	PMOS leakage current	V _{FB} = 0.9 V, T _A = 25°C		0.1		μA
R _{DSon-N}	NMOS switch on resistance	I _{SW} = 250 mA		0.15	0.3	W
R _{DSon-P}	PMOS switch on resistance	I _{SW} = 250 mA		0.2	0.4	W
η	Efficiency	I _O = 20 mA to 100 mA		75		%
		I _O = 100 mA to 0.5 A		90		%
T _{SHDN}	Thermal shut down ⁽²⁾		130	150		°C
T _{HYS}	Thermal shut down hysteresis ⁽²⁾			15		°C
ΔV _{O1,2} /ΔI _O	Load transient response ⁽²⁾	100 mA < I _O < 500 mA t _R = t _F => 100 ns, T _A = 25°C	-5		+5	%V _O
Reset section						
t _{DEL}	Delay time	T _A = 25°C	80	85		ms
V _{RES}	Reset in threshold measured on input pin	V _{IN_A} Rising	4.5	4.6	4.75	V
		V _{IN_A} Falling	4.12	4.2	4.28	

1. V_O = 90% of nominal value.

2. Guaranteed by design, but not tested in production.

$V_{IN_SW} = V_{IN_A} = 5\text{ V}$, $V_{O1,2} = 1.2\text{ V}$, $C_1 = 4.7\text{ }\mu\text{F}$, $C_2 = C_3 = 22\text{ }\mu\text{F}$, $L1 = L2 = 3.3\text{ }\mu\text{H}$,
 $T_J = -30\text{ to }125\text{ }^\circ\text{C}$ unless otherwise specified. Typical values are referred to $25\text{ }^\circ\text{C}$.

Table 7. Electrical characteristics for the ST2S06B

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$FB_{1,2}$	Feedback voltage		784	800	816	mV
$I_{FB1,2}$	V_{FB} pin bias current	$V_{FB} = 1\text{ V}$			600	nA
I_Q	Quiescent current	$V_{INH} > 1.2\text{ V}$, $V_{FB} = 1\text{ V}$			1	mA
		$V_{INH} < 0.4\text{ V}$			1	μA
$I_{O1,2}$	Output current	$V_{IN} = 2.5\text{ to }5.5\text{ V}^{(1)}$		0.8		A
I_{MIN}	Minimum output current		1			mA
V_{INH}	Inhibit threshold	$2.5\text{ V} < V_{IN} < 5\text{ V}$	1.2			V
		$2.5\text{ V} < V_{IN} < 5.5\text{ V}$	1.3			
		Device OFF			0.4	
$I_{INH1,2}$	Inhibit pin current				2	μA
$\%V_{O1,2}/\Delta V_{IN}$	Reference line regulation	$2.5\text{ V} < V_{IN} < 5.5\text{ V}$		0.032		$\%V_O/V_{IN}$
$\Delta V_{O1,2}$	Reference load regulation	$10\text{ mA} < I_O < 0.5\text{ A}$		5.5	15	mV
PWM f_S	PWM switching frequency ⁽¹⁾	$V_{FB} = 0.7\text{ V}$, $T_A = 25^\circ\text{C}$	1.2	1.5	1.8	MHz
D_{MAX}	Maximum duty cycle	$V_{FB} = 0.7\text{ V}$, $T_A = 25^\circ\text{C}$	85	94		%
I_{SWL}	Switching current limitation		1	1.2		A
I_{LKN}	NMOS leakage current	$V_{FB} = 0.9\text{ V}$, $T_A = 25^\circ\text{C}$		0.1		μA
I_{LKP}	PMOS leakage current	$V_{FB} = 0.9\text{ V}$, $T_A = 25^\circ\text{C}$		0.1		μA
R_{DSon-N}	NMOS switch on resistance	$I_{SW} = 250\text{ mA}$		0.15	0.3	W
R_{DSon-P}	PMOS switch on resistance	$I_{SW} = 250\text{ mA}$		0.2	0.4	W
η	Efficiency	$I_O = 20\text{ mA to }100\text{ mA}$		75		%
		$I_O = 100\text{ mA to }0.5\text{ A}$		90		%
T_{SHDN}	Thermal shut down ⁽²⁾		130	150		$^\circ\text{C}$
T_{HYS}	Thermal shut down hysteresis ⁽¹⁾			15		$^\circ\text{C}$
$\Delta V_{O1,2}/\Delta I_O$	Load transient response ⁽¹⁾	$100\text{ mA} < I_O < 500\text{ mA}$, $t_R = t_F = 1\text{ }\mu\text{s}$, $T_A = 25^\circ\text{C}$	-5		+5	$\%V_O$

1. $V_O = 90\%$ of nominal value.

2. Guaranteed by design, but not tested in production.

5 Typical performance characteristics

Figure 3. Feedback voltage 1 vs. temperature (ST2S06B)

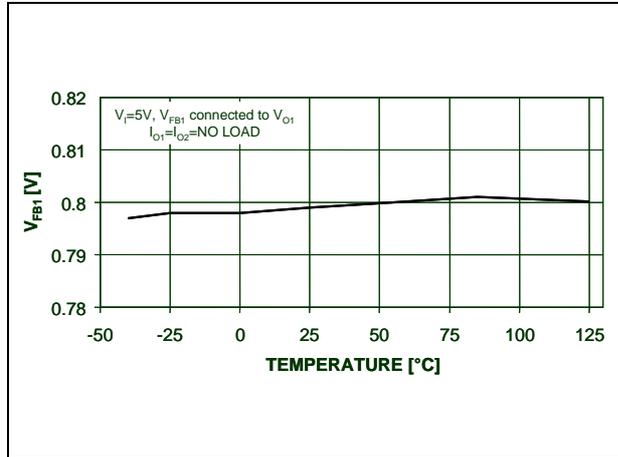


Figure 4. Feedback voltage 2 vs. temperature (ST2S06B)

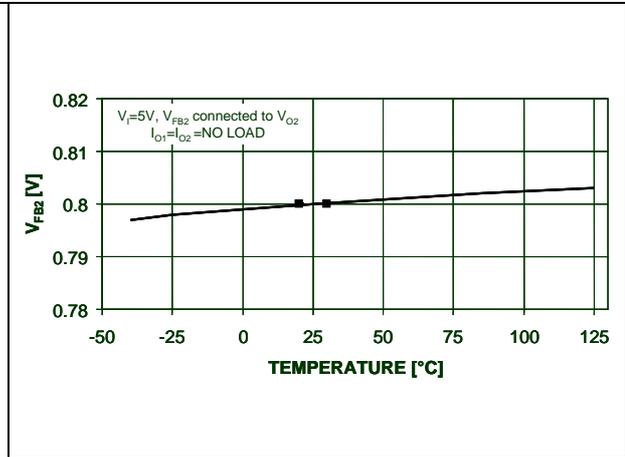


Figure 5. Efficiency vs. output current 1

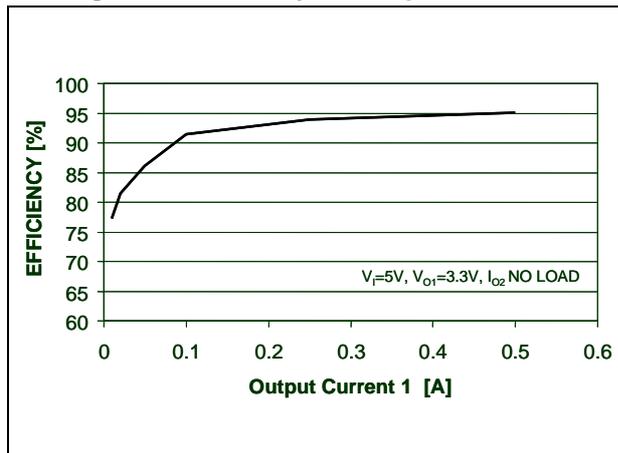


Figure 6. Efficiency vs. output current 2

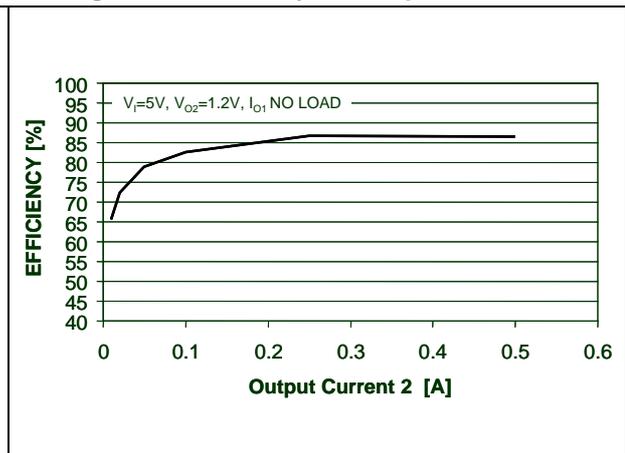


Figure 7. Switching frequency vs. temperature (ST2S06A33)

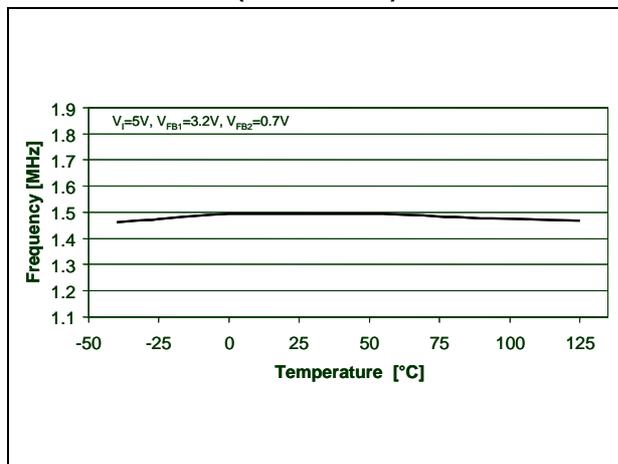


Figure 8. Duty cycle vs. temperature (ST2S06A33)

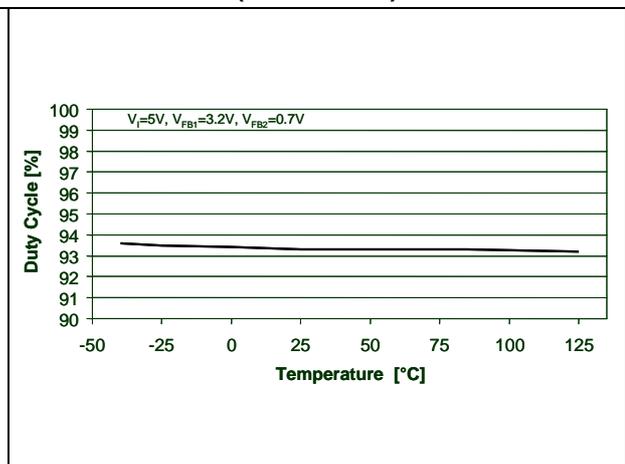


Figure 15. Delay time vs. temperature (ST2S06A33)

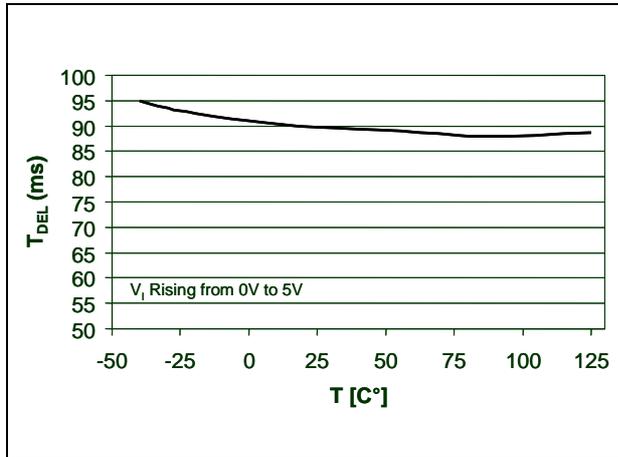


Figure 16. Reset in threshold vs. temperature (ST2S06A33)

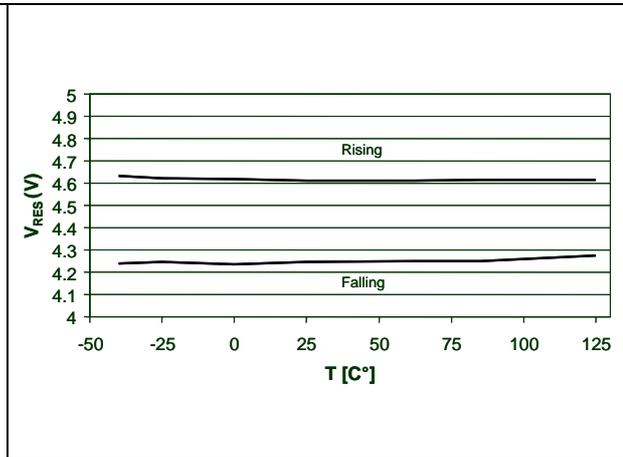


Figure 17. Load transient response (ST2S06A33)

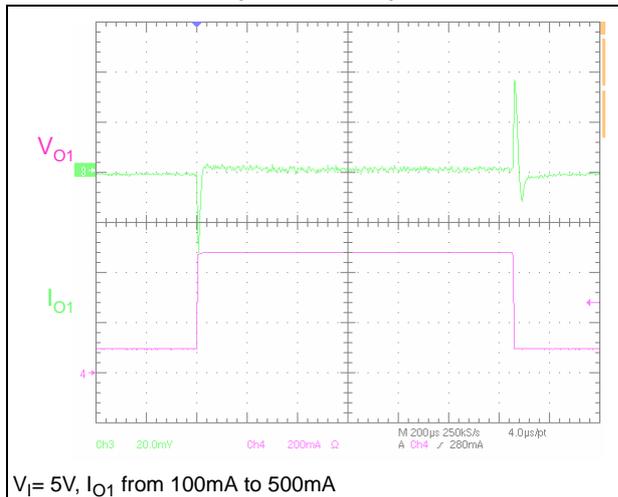


Figure 18. Startup transient (ST2S06A33)

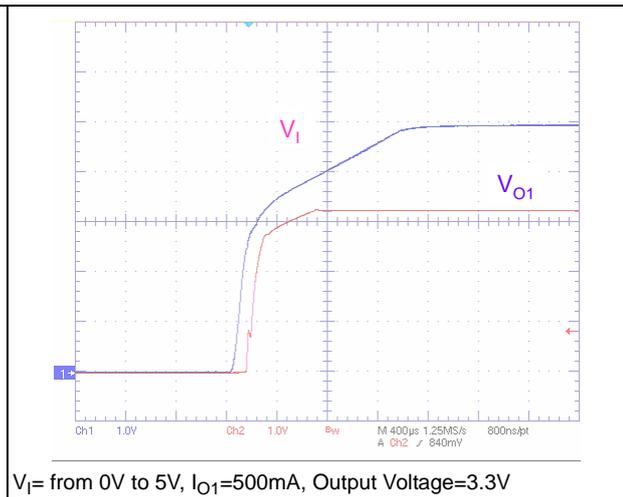


Figure 19. Startup transient (ST2S06B)

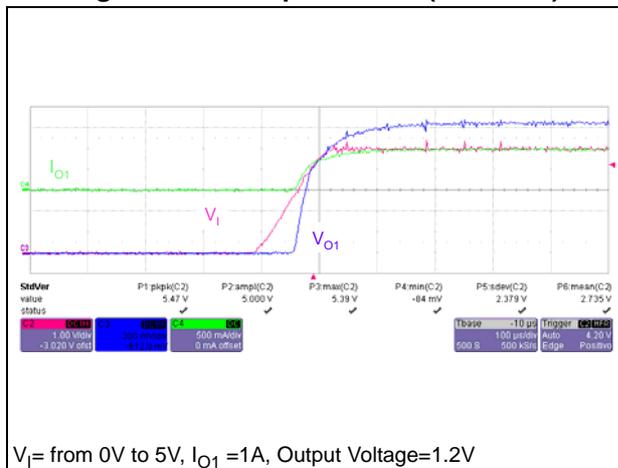
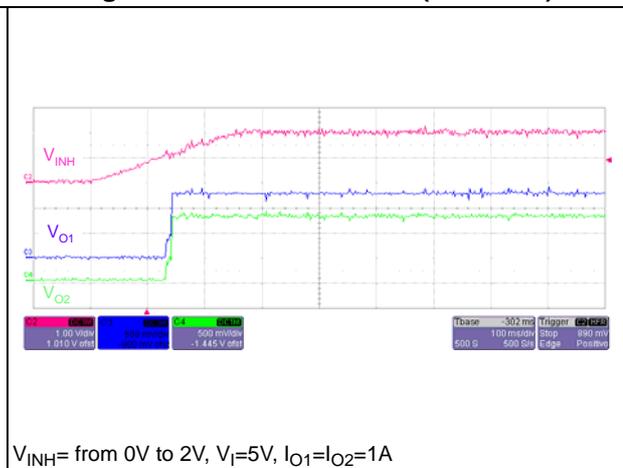


Figure 20. Inhibit transient (ST2S06B)



6 Typical application

Figure 21. Application circuit for the ST2S06A33

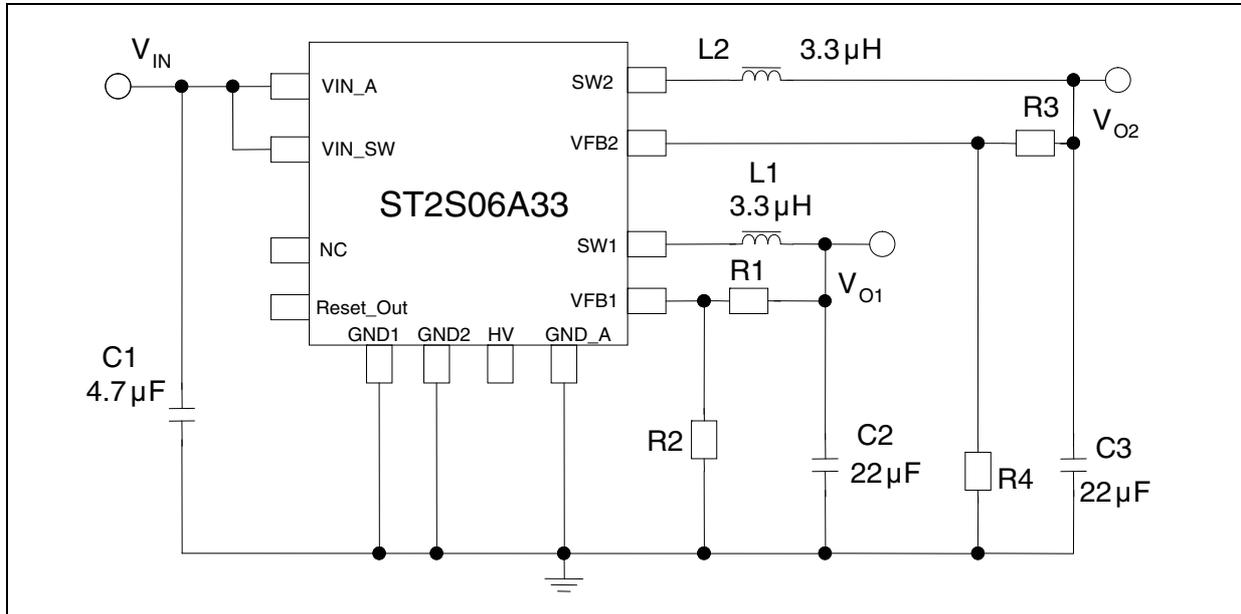
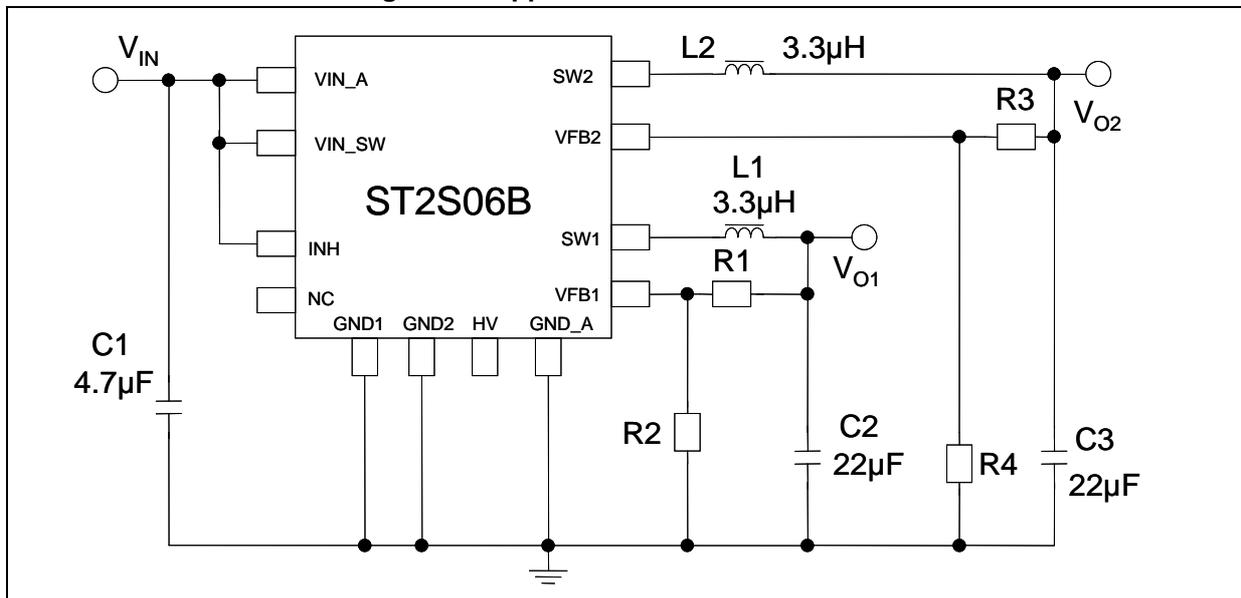


Figure 22. Application circuit for ST2S06B



7 Application information

The ST2S06A33 and ST2S06B represent a series of dual adjustable current mode PWM step-down DC-DC converters with an internal 0.5 A power switch, packaged in a QFN12L (4x4 mm).

It is a complete 0.5 A switching regulator with internal compensation that eliminates the need for additional components.

The constant frequency, current mode, PWM architecture and stable operation with ceramic capacitors results in low, predictable output ripple.

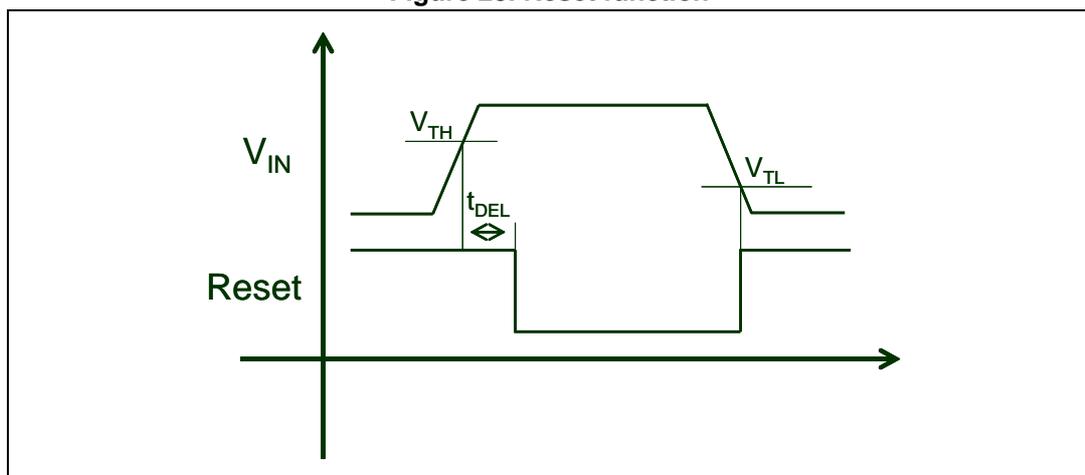
To clamp the error amplifier reference voltage a soft start control block generating a voltage ramp has been implemented. Other circuits fitted to the device protection are the thermal shut-down block, which turns off the regulator when the junction temperature exceeds 150 °C (typ.), and the cycle-by-cycle current limiting that provides protection against shorted outputs.

The output voltage is determined by an external resistor divider, as the ST2S06A33 and ST2S06B are adjustable regulators. The desired value is given by the following equation:

$$V_O = V_{FB} [1 + R1/R2]$$

Operation of the device requires few components: 2 inductors, 3 capacitors and a resistor divider. The chosen inductor must be capable of not saturating at the peak current level. Its value should be selected keeping in mind that a large inductor value increases the efficiency at low output current and reduces output voltage ripple, while a smaller inductor can be chosen when it is important to reduce package size and total application cost. Finally, the ST2S06A33 and ST2S06B have been designed to work properly with X5R or X7R SMD ceramic capacitors both at the input and at the output. These types of capacitors, due to their very low series resistance (ESR), minimize the output voltage ripple. Other low ESR capacitors can be used according to the need of the application without compromising the correct functionality of the device. Due to the high switching frequency and peak current, it is important to optimize the application environment by reducing the length of the PCB traces and placing all the external components near the device.

Figure 23. Reset function

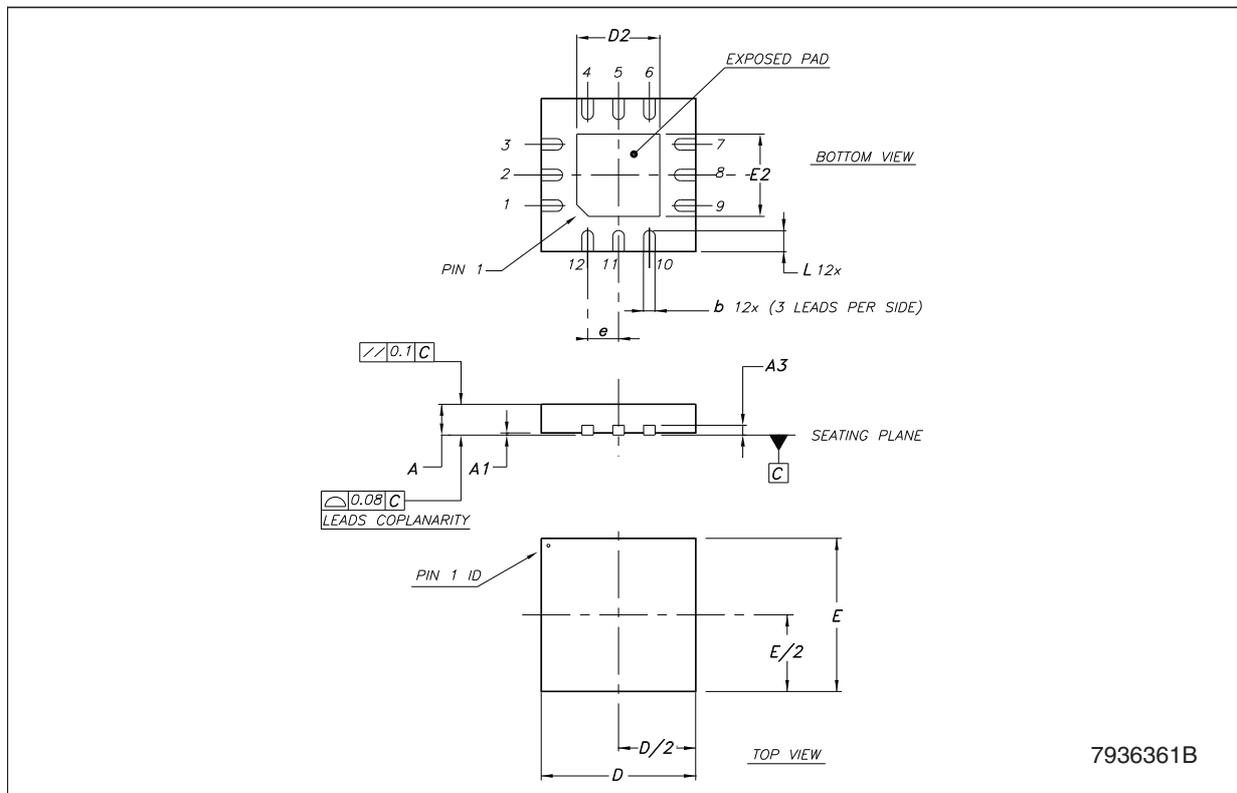


8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

QFN12L (4x4) mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.90	1.00	0.031	0.035	0.039
A1		0.02	0.05		0.001	0.002
A3		0.20			0.008	
b	0.25	0.30	0.35	0.010	0.012	0.014
D	3.90	4.00	4.10	0.154	0.157	0.161
D2	2.00	2.15	2.25	0.079	0.085	0.089
E	3.90	4.00	4.10	0.154	0.157	0.161
E2	2.00	2.15	2.25	0.079	0.085	0.089
e		0.80			0.031	
L	0.45	0.55	0.65	0.018	0.022	0.026



Tape & reel QFNxx/DFNxx (4x4) mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	99		101	3.898		3.976
T			14.4			0.567
Ao		4.35			0.171	
Bo		4.35			0.171	
Ko		1.1			0.043	
Po		4			0.157	
P		8			0.315	

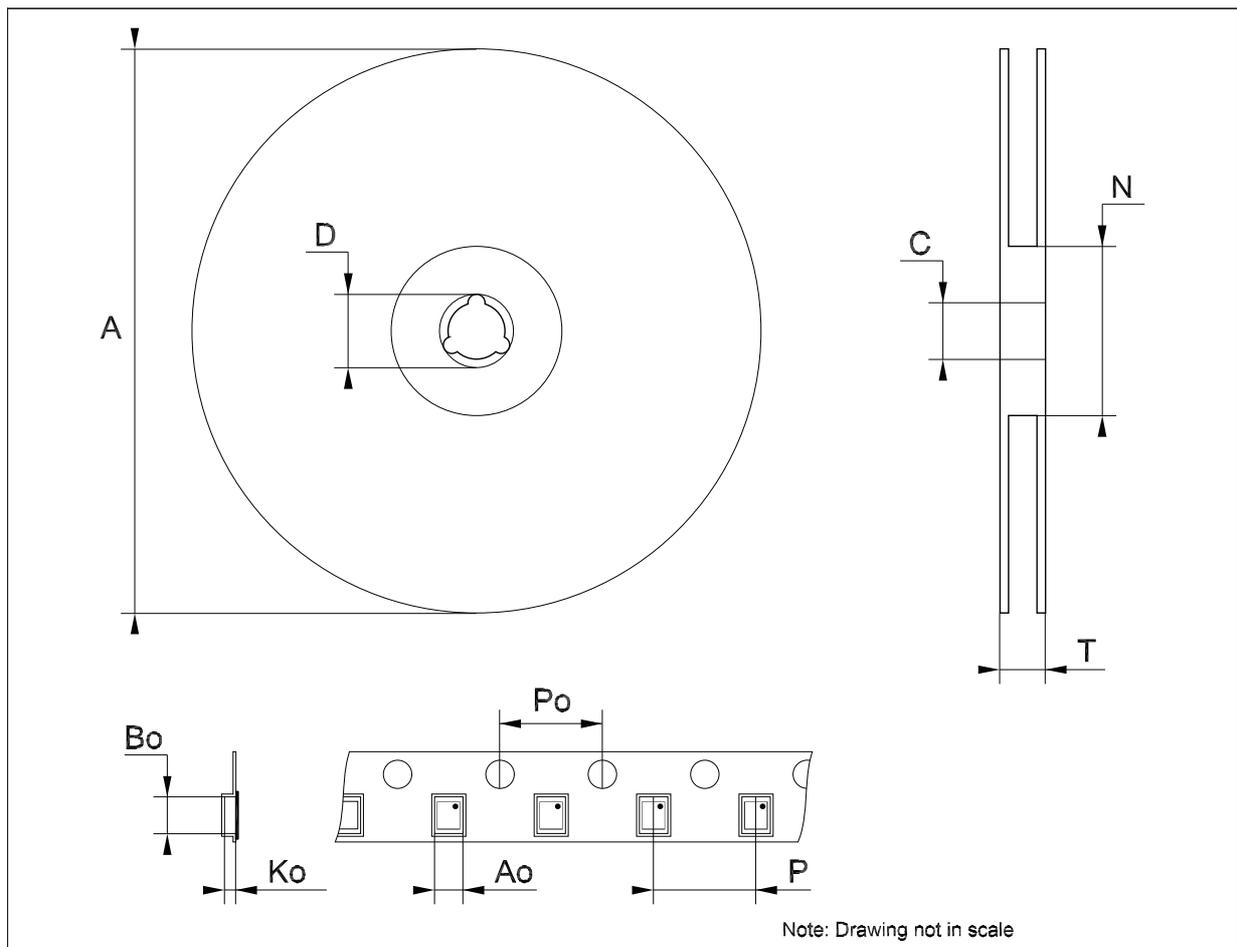
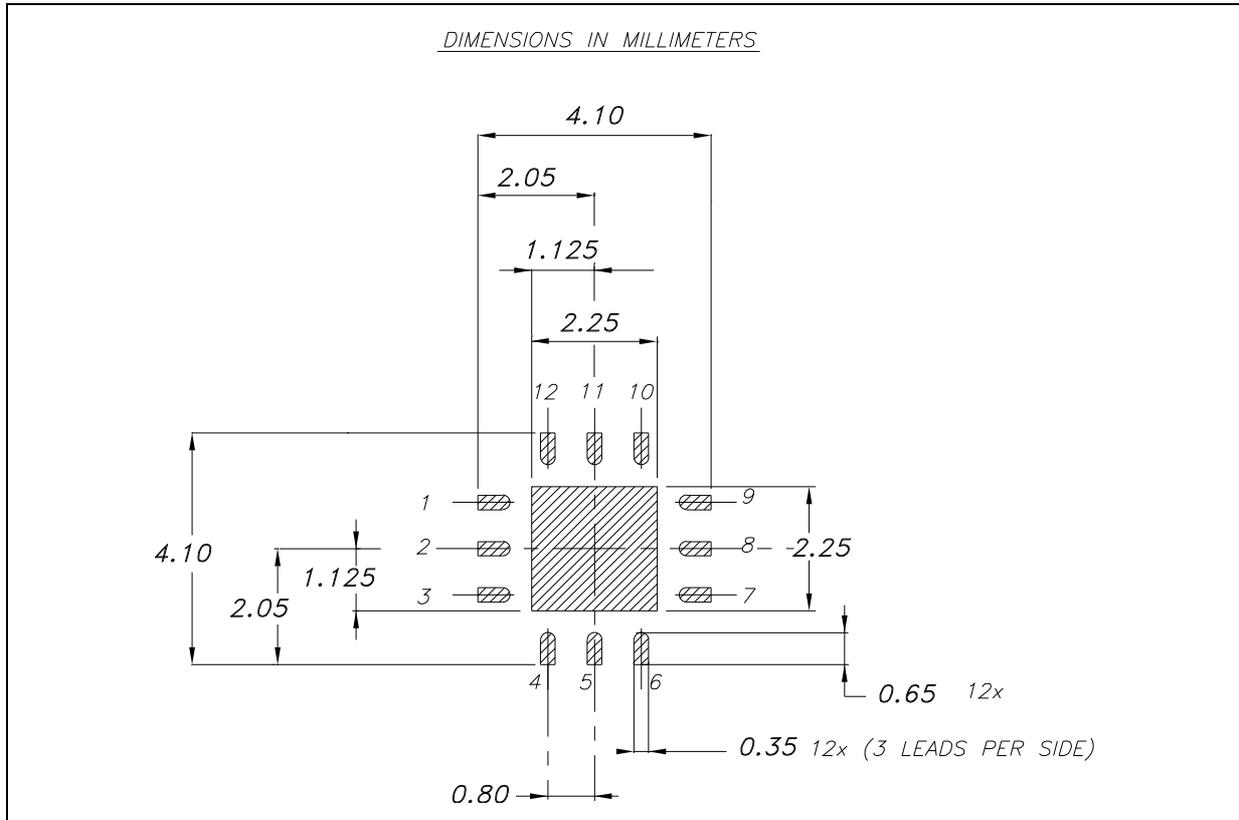


Figure 24. QFN12L (4x4 mm) footprint recommended data



9 Revision history

Table 8. Document revision history

Date	Revision	Changes
3-Sep-2007	1	Initial release.
21-Jan-2008	2	Added root part number ST2S06D33.
18-Mar-2008	3	Modified: Table 2 on page 4 .
28-Jul-2009	4	Modified: Table 1 on page 1 .
24-May-2012	5	<ul style="list-style-type: none">– Changed max value for Non-switching quiescent current to 1.2 mA in Features on page 1.– Updated part number in Figure 21 on page 11– Minor text changes throughout the document
22-May-2013	6	<ul style="list-style-type: none">– Changed title in cover page

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