ISL45042

LCD Module Calibrator

FN6072
Rev 9.00
Apr 13, 2011

The V_{COM} voltage of an LCD panel needs to be adjusted to remove flicker. The ISL45042 can be used to digitally adjust a panel's V_{COM} voltage by controlling its output sink current. The output of the ISL45042 is connected to an external voltage divider and an external V_{COM} buffer amplifier. In this application, the user can control the V_{COM} voltage with 7-bit accuracy (128 steps). Once the desired V_{COM} setting is obtained, the settings can be stored in the non-volatile EEPROM memory, which would then be automatically recalled during every power-up.

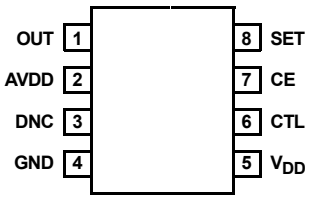
The V_{COM} adjustment and non-volatile memory programming is through a single interface pin (CTL). Once the desired programmed value is obtained, the Counter Enable pin (CE) can be used to prevent further adjustment or programming.

The full-scale sink current of the ISL45042 is set using an external resistor connected to the SET pin. The full-scale sink current determines the lowest voltage of the external voltage divider.

The ISL45042 is available in an 8 Ld 3mmx3mm TDFN package with a maximum thickness of 0.8mm for ultra thin LCD panel design.

Pinout

ISL45042
(8 LD TDFN)
TOP VIEW



Features

- 128-Step Adjustable Sink Current Output
- 2.6V to 3.6V Digital Supply Voltage Operating Range (3.0V Minimum Programming Voltage)
- 4.5V to 20V Analog Supply Voltage Operating Range (10.8V Minimum Programming Voltage)
- Rewritable EEPROM for Storing the Optimum V_{COM} Value
- Output Adjustment Enable/Disable Control
- Output Guaranteed Monotonic Over-Temperature
- Two Pin Adjustment, Programming and Enable
- Ultra Thin 8 Ld 3mmx3mm DFN (0.8mm Max)
- Pb-Free (RoHS Compliant)

Applications

- LCD Panels

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL45042IRZ	042Z	-40 to +85	8 Ld 3x3 TDFN	L8.3x3A

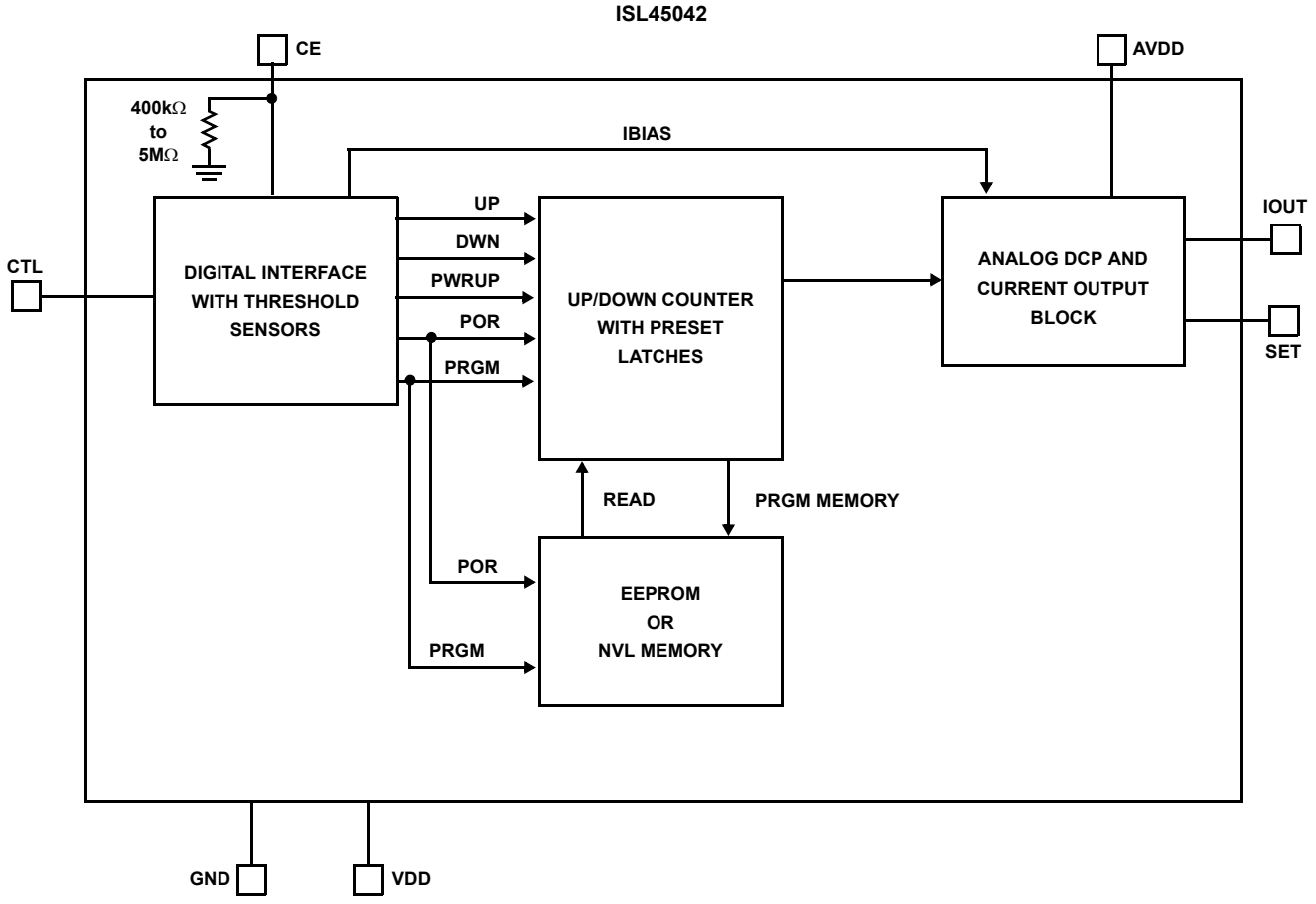
NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL45042. For more information on MSL please see techbrief TB363.

Pin Descriptions

PIN	FUNCTION
OUT	Adjustable Sink Current Output Pin. The current sinks into the OUT pin is equal to the DAC setting times the maximum adjustable sink current divided by 128. See SET pin function in “Pin Descriptions” on page 2 for the maximum adjustable sink current setting.
AVDD	High-Voltage Analog Supply. Connects to top of external resistor divider to determine the V_{COM} voltage. 10.8V to 20V for EEPROM programming, 4.5V to 20V normal operation (before/after programming). Bypass to GND with 0.1µF de-coupling capacitor.
DNC	Do Not Connect. This pin may be left unconnected or tied to GND. Do not apply any non-zero voltages or signals to this pin.
GND	Ground connection.
V_{DD}	Low-Voltage Digital Supply for digital logic. Typically 3V to 3.6V. Bypass to GND with 0.1µF de-coupling capacitor.
CTL	Internal Counter Up/Down Control and Internal EEPROM Programming Control Input. If CE is high, a mid-to-low transition increments the 7-bit counter, raising the DAC setting, increasing the OUT sink current, and lowering the divider voltage at OUT. A mid-to-high transition decrements the 7-bit counter, lowering the DAC setting, decreasing the OUT sink current, and increasing the divider voltage at OUT. Applying 4.9V and above with appropriately arranged timing will overwrite EEPROM with the contents in the 7-bit counter. See EEPROM Programming section in “Electrical Specifications” table on page 4 for details.
CE	Counter Enable Pin with internal pull-down resistor. Connect CE to VDD to enable adjustment of the output sink current. Float or connect CE to GND to prevent further adjustment or programming.
SET	Maximum Sink Current Adjustment Point. Connect a resistor from the SET pin to GND to set the maximum adjustable sink current of the OUT pin. The maximum adjustable sink current is equal to (AVDD/20) divided by RSET.

Block Diagram



Absolute Maximum Ratings

V_{DD} to GND . . . . . +4V
Input Voltages to GND
SET, CE . . . . . -0.3V to +4V
AVDD . . . . . -0.3V to +20V
CTL. . . . . -0.3V to +17V
Output Voltages to GND
OUT . . . . . -0.3V to +20V
ESD Rating
Human Body Model
Device. 2.75kV
CTL to GND (No EEPROM Content Disruption). 7kV

Thermal Information

Thermal Resistance (Typical, Notes 4, 5)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld TDFN Package.	47	12

Moisture Sensitivity (see Technical Brief TB363)
All Packages . . . . . Level 1
Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range. . . . . .-65°C to +150°C
Pb-free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp
Erase/Write Cycles 10,000
Data Retention. . . . . 10 years @ +85°C

Operating Conditions

Temperature Range
ISL45042IR . . . . . .-40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Test Conditions: V_{DD} = 3V, AV_{DD} = 18V, R_{SET} = 5kΩ, R1 = 10kΩ, R2 = 10kΩ; Unless Otherwise Specified. Typicals are at T_A = +25°C

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN (Note 13)	TYP	MAX (Note 13)	UNITS
DC CHARACTERISTICS							
V_{DD} Supply Range	V_{DD}	Range Allowing Programming	0 to 85	3	-	3.6	V
		Operation without Programming	Full	2.6	-	3.6	V
V_{DD} Supply Current	I_{DD}	CE = V_{DD} (Note 10)	Full	-	-	65	µA
		CE = GND	Full	-	-	65	µA
AVDD Supply Range	AVDD	Range Allowing Programming	Full	10.8	-	20	V
		Operation without Programming	Full	4.5		20	V
AV_{DD} Supply Current (Note 7)	I_{AVDD}		Full			38	µA
CTL High Voltage	CTL_{IH}	2.6V < V_{DD} < 3.6V	Full	0.7*V_{DD}	-	0.8*V_{DD}	V
CTL Low Voltage	CTL_{IL}	2.6V < V_{DD} < 3.6V	Full	0.2*V_{DD}	-	0.3*V_{DD}	V
CTL High Rejected Pulse Width	CTL_{IHRPW}		Full	20	-	-	µs
CTL Low Rejected Pulse Width	CTL_{ILRPW}		Full	20	-	-	µs
CTL High Minimum Pulse Width	CTL_{IHMPW}		Full	-	-	200	µs
CTL Low Minimum Pulse Width	CTL_{ILMPW}		Full	-	-	200	µs
CTL Minimum Time Between Counts	CTL_{MTC}		Full	-	-	10	µs
CTL Input Current	ICTL	CTL = GND	Full	-	-	10	µA
		CTL = V_{DD}	Full	-	-	10	µA
CTL Input Capacitance	CTL_{CAP}	(Note 9)	Full	-	10	-	pF
CE Input Low Voltage	CE_{IL}	2.6V < V_{DD} < 3.6V	Full	-	-	0.4	V
CE Input High Voltage	CE_{IH}	2.6V < V_{DD} < 3.6V	Full	0.7*V_{DD}	-	-	V
CE Minimum Start-Up Time	CE_{ST}	(Note 9)	Full	-	1	-	ms

Electrical Specifications Test Conditions: V_{DD} = 3V, AV_{DD} = 18V, R_{SET} = 5kΩ, R1 = 10kΩ, R2 = 10kΩ; Unless Otherwise Specified. Typicals are at T_A = +25°C **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN (Note 13)	TYP	MAX (Note 13)	UNITS
CTL EEPROM Program Voltage	CTL_{PROM}	2.6V < V_{DD} < 3.6V, (Note 6)	Full	4.9	-	15.75	V
CTL EEPROM Programming Signal Time	CTL_{PT}	>4.9V	Full	200	-	-	µs
Programming Time	P_T		Full	-	-	100	ms
SET Voltage Resolution	SET_{VR}	(Note 8)	Full	7	7	7	Bits
SET Differential Nonlinearity	SET_{DN}	Monotonic Over-Temperature	Full	-	-	±1	LSB
SET Zero-Scale Error	SET_{ZSE}		Full	-	-	±3	LSB
SET Full-Scale Error	SET_{FSE}		Full	-	-	±8	LSB
SET Current	ISET	Through R_{SET} (Note 11)	Full	-	20	-	µA
SET External Resistance	SET_{ER}	To GND, AVDD = 20V	Full	10	-	200	kΩ
		To GND, AVDD = 4.5V	Full	2.25	-	45	kΩ
		To GND, AV_{DD} = 15V, V_{DD} = 3V V_{OUT} > 2.5V (Note 12)	Full	1	-	200	kΩ
AVDD to SET Voltage Attenuation	AVDD to SET		Full	-	1:20	-	V/V
OUT Settling Time	OUT_{ST}	To ±0.5 LSB Error Band (Note 9)	Full	-	20	-	µs
OUT Voltage Range	V_{OUT}		Full	VSET + 0.5V	-	13	V
OUT Voltage Drift	OUT_{VD}	25°C < T_A < 55°C (Note 9)	25 to 55	-	<10	-	mV

NOTES:

6. CTL signal only needs to be greater than 4.9V to program EEPROM.
7. Tested at AV_{DD} = 20V.
8. The Counter value is set to mid-scale ±4 LSB's in the Production.
9. Simulated and Determined via Design and NOT Directly Tested.
10. Simulated Maximum Current Draw when Programming EEPROM is 23mA; should be considered when designing Power Supply.
11. A Typical Current of 20µA is Calculated using AV_{DD} = 10V and R_{SET} = 24.9kΩ. Reference "RSET Resistor" on page 6.
12. Minimum value of R_{SET} resistor guaranteed when: AV_{DD} = 15V, V_{DD} = 3.0V and when voltage on the VOUT pin is greater than 2.5V. Reference Equation 2 on page 6 with Setting = 128.
13. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

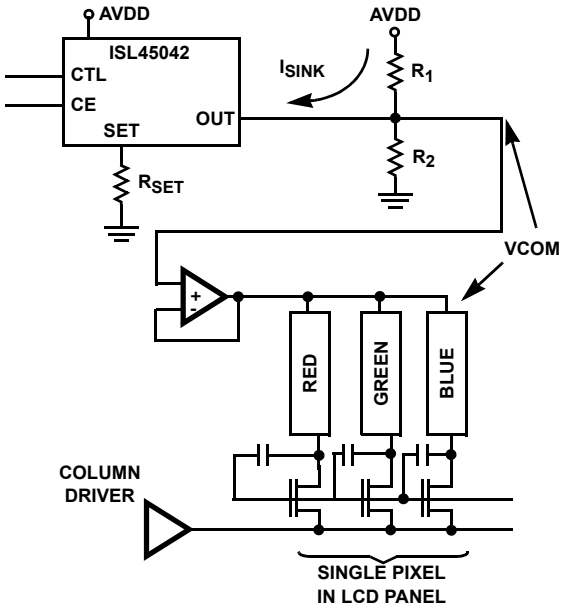


FIGURE 1. VCOM ADJUSTMENT IN AN LCD PANEL

Application Information

The application circuit to adjust the V_{COM} voltage in an LCD panel is shown in Figure 1. The ISL45042 has a 128-step sink current resolution. The output is connected to an external voltage divider that decreases the output V_{COM} voltage as you increase the ISL45042 sink current.

CTL Pin

The adjustment of the output V_{COM} voltage and the programming of the non-volatile memory are provided through a single pin called CTL when the CE pin is high.

The output V_{COM} voltage is increased with a mid (V_{DD}/2) to high transition (0.8*V_{DD}) on the CTL pin. The output V_{COM} voltage is decreased with a mid (V_{DD}/2) to low transition (0.3*V_{DD}) on the CTL pin (see Figure 8). Once the minimum or maximum value is reached on the 128 steps, the device will not overflow or underflow beyond that minimum or maximum value.

Programming of the non-volatile memory occurs when the CTL pin exceeds 4.9V. The CTL signal needs to remain above 4.9V for more than 200µs. The level and timing needed to program the non-volatile memory is given in Figure 2. It then takes a maximum of 100ms for the programming to be completed inside the device.

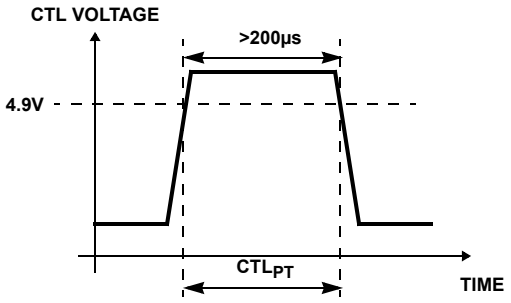


FIGURE 2. EEPROM PROGRAMMING

When the part is programmed, the counter setting is loaded into the non-volatile memory. This value will be loaded from the non-volatile memory during initial power-up or when the CE pin is pulled low.

Once the programming is completed, it is recommended that the user float the CTL pin. The CTL pin is internally tied to a resistor network connected to ground. If left floating, the voltage at the CTL pin will equal V_{DD}/2. Under these conditions, no additional pulses will be seen by the Up/Down counter via the CTL pin. To prevent further programming, ground the CE pin.

CTL should have a noise filter to reduce bouncing or noise on the input that could cause unwanted counting when the CE pin is high. The board should have an additional ESD protection circuit, with a series 1kΩ resistor and a shunt 0.01µF capacitor connected on the CTL pin, (see Figure 3).

To avoid unintentional adjustment, the ISL45042 guarantees to reject CTL pulses shorter than 20µs.

During Initial Power-up (only), to avoid the possibility of a false pulse (since the internal comparators come up in an unknown state), the very first CTL pulse is ignored. See Figure 8 for the timing information.

CE Pin

To adjust the output voltage, the CE pin must be pulled high (VDD). The CE pin has an internal pull-down resistor to prevent unwanted reprogramming of the EEPROM. To minimize current consumption, the impedance of this resistor is high: 400kΩ to 5MΩ (see $R_{INTERNAL}$ in Figure 7).

Transitions of the CE pin are recommended to be less than 10µs.

Replacing Existing Mechanical Potentiometer Circuits

Figure 4 shows the common adjustment mechanical circuits and equivalent replacement with the ISL45042.

Expected Output Voltage

The ISL45042 provides an output sink current, which lowers the voltage on the external voltage divider (V_{COM} output voltage). Equations 1 and 2 can be used to calculate the output current (I_{OUT}) and output voltage (V_{OUT}) values.

$$I_{OUT} = \frac{Setting}{128} x \frac{AV_{DD}}{20(R_{SET})} \quad \text{(EQ. 1)}$$

$$V_{OUT} = \left(\frac{R_2}{R_1 + R_2}\right) AV_{DD} \left(1 - \frac{Setting}{128} x \frac{R_1}{20(R_{SET})}\right) \quad \text{(EQ. 2)}$$

(Where “Setting” is an integer between 1 and 128.)

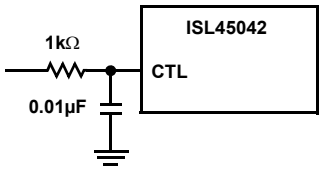


FIGURE 3. EXTERNAL ESD PROTECTION ON CTL PIN

Table 1 gives the calculated value of V_{OUT} for resistors values of: R_{SET} = 24.9kΩ, R_1 = 200kΩ, R_2 = 243kΩ, and AV_{DD} = 10V.

TABLE 1. CALCULATED VCOM OUTPUT VOLTAGES

SETTING VALUE	V_{OUT}
1	5.468
10	5.313
20	5.141
30	4.969
40	4.797
50	4.625
60	4.453
70	4.281
80	4.109

TABLE 1. CALCULATED VCOM OUTPUT VOLTAGES

SETTING VALUE	V_{OUT}
90	3.936
100	3.764
110	3.592
128	3.282

R_{SET} Resistor

The external R_{SET} resistor sets the full-scale sink current that determines the lowest voltage of the external voltage divider R_1 and R_2 (see Figure 1). The voltage difference between the V_{OUT} pin and I_{SET} pin (see Figure 5) has to be greater than 1.75V. This will keep the output MOS transistor in the saturation region. Expected current settings and 7-bit accuracy occurs when the output MOS transistor is operating in the saturation region. Figure 5 shows the internal connection for the output MOS transistor. The value of the AV_{DD} supply sets the voltage at the source of the output transistor. This voltage is equal to (Setting/128) x (AV_{DD}/20). The I_{SET} current is therefore equal to (Setting/128) x (AV_{DD}/20 x R_{SET}). The value of the Drain voltage is found using Equation 2. The values of R_1 and R_2 in Equation 2, should be determined (setting equal to 128) so the minimum value of V_{OUT} is greater than 1.75V + AV_{DD}/20.

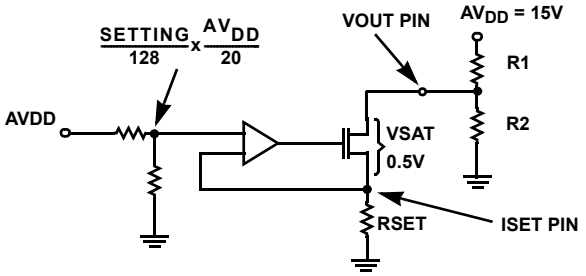


FIGURE 5. OUTPUT CONNECTION CIRCUIT EXAMPLE

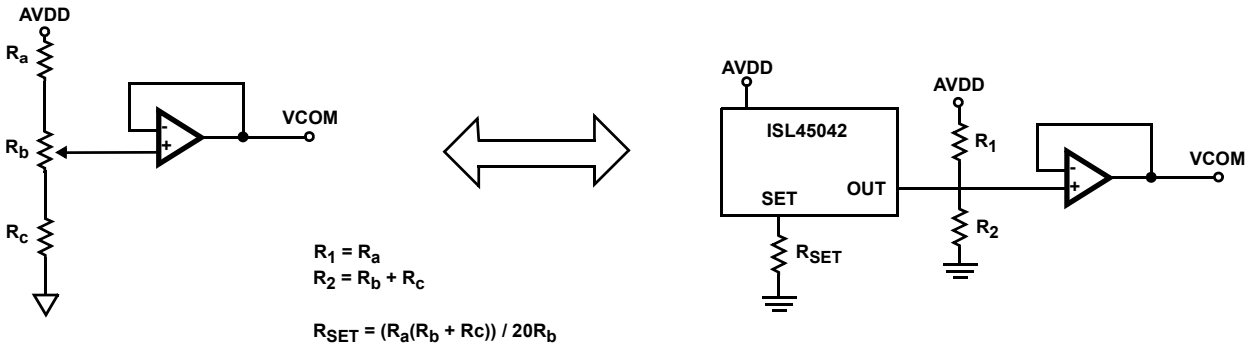


FIGURE 4. EXAMPLE OF THE REPLACEMENT FOR THE MECHANICAL POTENTIOMETER CIRCUIT USING THE ISL45042

Power Supply Sequence

The recommended power supply sequencing is shown in Figure 6. When applying power, VDD should be applied before or at the same time as AVDD. The minimum time for t_{VS} is 0µs. When removing power, the sequence of VDD and AVDD is not important. Do not remove VDD or AVDD within 100ms of the start of the EEPROM programming cycle. Removing power before the EEPROM programming cycle is completed may result in corrupted data in the EEPROM.

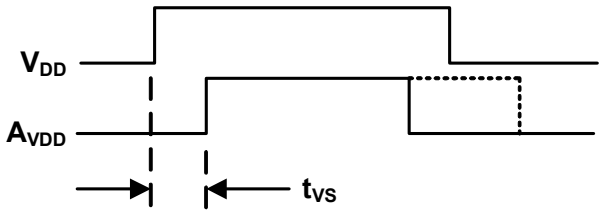


FIGURE 6. POWER SUPPLY SEQUENCE

Verifying the Programmed Value

The following sequence can be used to verify the programmed value without having to sequence the V_{DD} supply. To verify the programmed value, follow the following steps. The ISL45042 will read memory contents and be set to that value when the CE pin is grounded.

1. Power-up the ISL45042.
2. CE pin = V_{DD}.
3. Change counter value with CTL pin to desired value.
4. CTL = more than 4.9V and 200ms. Counter value programmed.
5. Change the counter value with CTL pin to a different value.
6. CE pin = Ground.
7. Check that the output value is the one programmed in Step 4.

Generating VDD and CE supply from a Larger Voltage Source

The CE pin has an internal pull-down resistor (see $R_{INTERNAL}$ in Figure 7). The impedance of this resistor is 400kΩ to 5MΩ. If your design is using a resistor divider network to generate the 3.3V supply (for both V_{DD} and CE to enable programming) from a larger voltage source, the 400kΩ (worst case) resistor needs to be taken into account as a parallel resistance when the CE pin is connected to this source. Another design concern is to be able to provide enough supply current during programming. The ISL45042 draws about 2mA during this process. Recommended resistor values are shown in Figure 7. This design will result in an additional 0.83mA quiescent current flowing through resistors R_A and R_B.

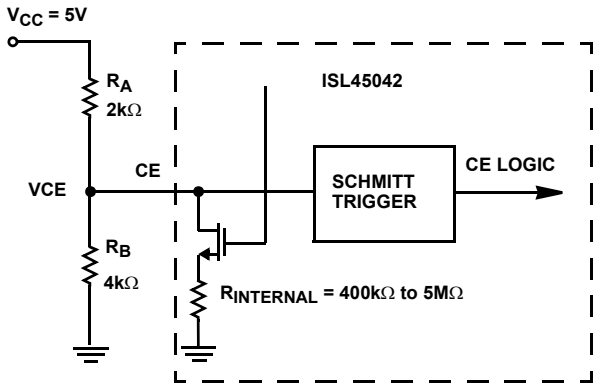


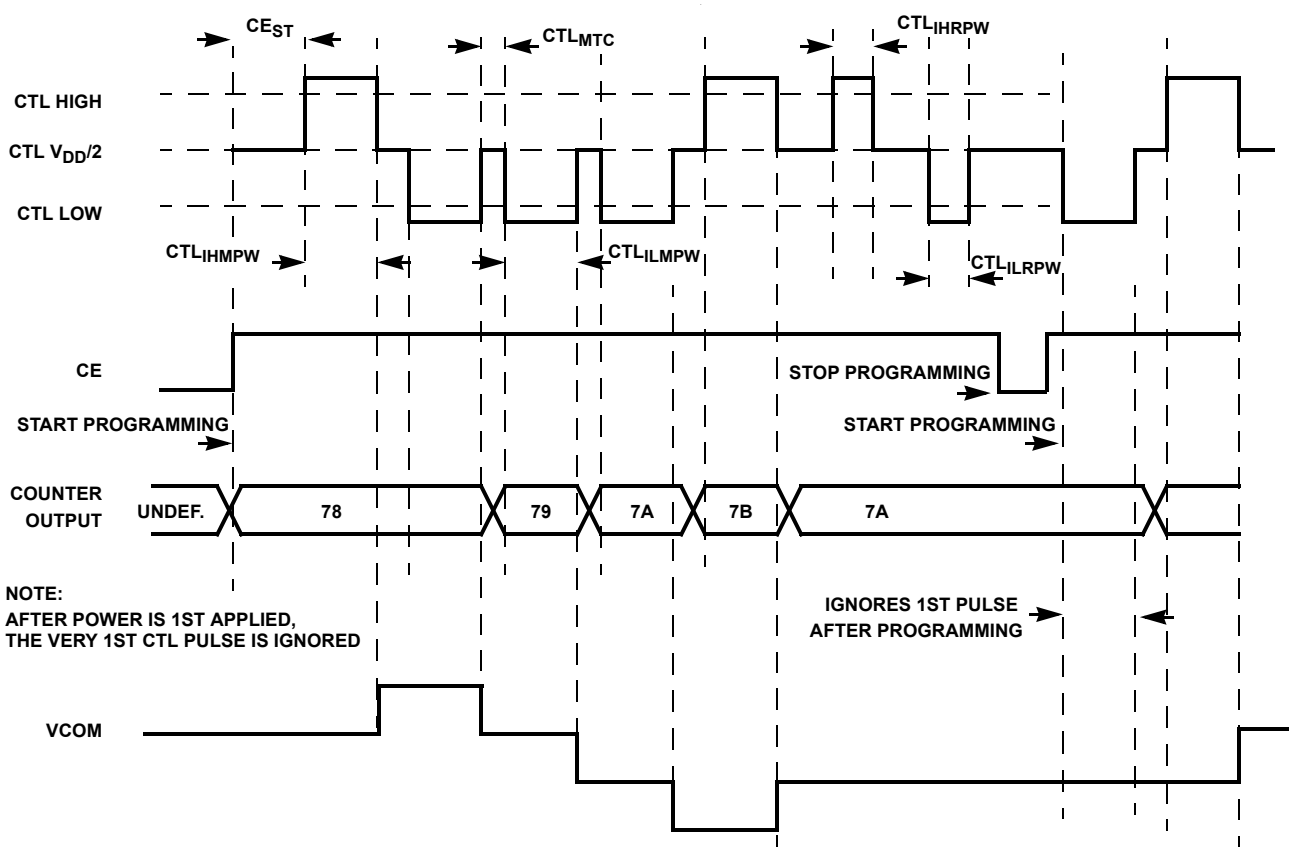
FIGURE 7. APPLICATION GENERATING VDD AND VCE VOLTAGES

ISL45042 Truth Table

The ISL45042 truth table is shown in Table 2. For proper operation the CE should be disabled (pulled low) before powering the device down to assure that the glitches and transients will not cause unwanted EEPROM overwriting.

TABLE 2. TRUTH TABLE

INPUT			OUTPUT		
CTL	CE	VDD	OUT	ICC	MEMORY
Mid to Hi	Hi	VDD	Increment	Normal	X
Mid to Lo	Hi	VDD	Decrement	Normal	X
X	Lo	VDD	No Change	Increased	Read
>4.9V	Hi	VDD	No Change	Increased	Program



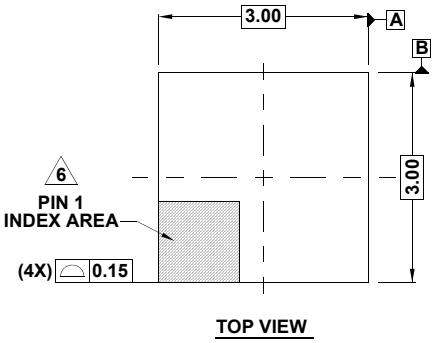
THE TIMING DIAGRAM ABOVE SHOWS POST POWER-UP TIMING.

FIGURE 8. ISL45042 TIMING DIAGRAM

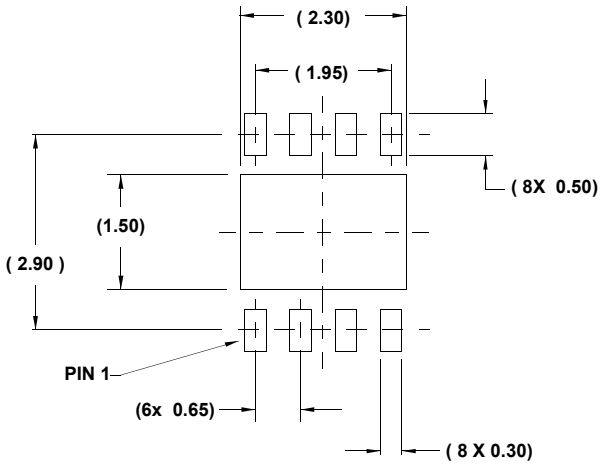
Package Outline Drawing

L8.3x3A

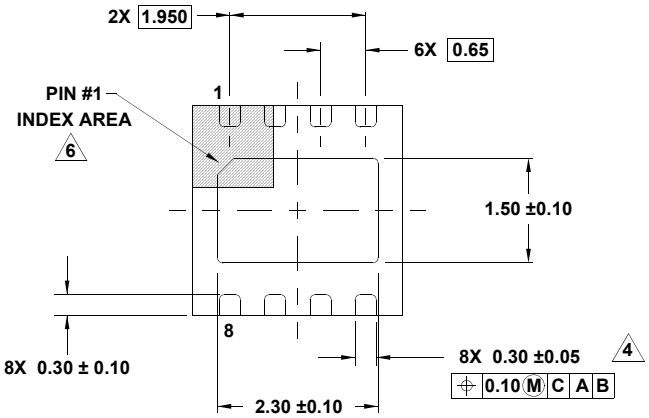
8 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE
Rev 4, 2/10



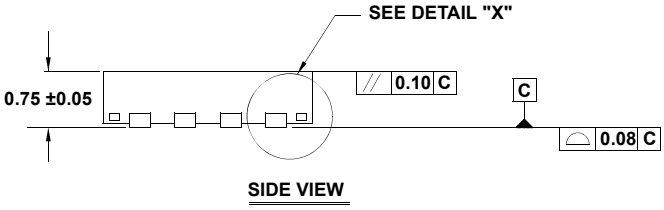
TOP VIEW



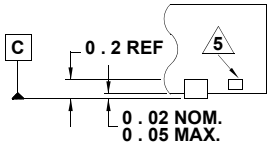
TYPICAL RECOMMENDED LAND PATTERN



BOTTOM VIEW



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.20mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Compliant to JEDEC MO-229 WEEC-2 except for the foot length.

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Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

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Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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