

CTLTVS5-4**SURFACE MOUNT SILICON
LOW CAPACITANCE
QUAD TVS/DIODE ARRAY**www.centrasemi.com**Ideal for
USB
3.0****TLM1031 CASE****DESCRIPTION:**

The CENTRAL SEMICONDUCTOR CTLTVS5-4 is a 4-line TVS/Diode array packaged in a TLM1031 surface mount case. With its ultra low capacitance, this device was designed to protect four high speed data or transmission lines from over-voltage transients and ESD damage.

MARKING CODE: CTL5**APPLICATIONS:**

- USB 3.0 Power and Data Line Protection
- HDMI Interface Protection
- Tablets, Monitors, Displays, Smart Phones
- Ethernet Ports

FEATURES:

- Low capacitance
- Low clamping voltage
- Protects four I/O lines

MAXIMUM RATINGS: ($T_A=25^\circ\text{C}$)

Peak Pulse Current (8x20 μs)	I_{PP}	2.5	A
Peak Power Dissipation (8x20 μs)	P_{PK}	32.5	W
Electrical Fast Transient (IEC 61000-4-4) (5x50ns)	EFT	40	A
ESD Voltage (IEC 61000-4-2, Air)	V_{ESD}	15	kV
ESD Voltage (IEC 61000-4-2, Contact)	V_{ESD}	8.0	kV
Operating and Storage Junction Temperature	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

SYMBOL**UNITS****ELECTRICAL CHARACTERISTICS PER DIODE:** ($T_A=25^\circ\text{C}$)

Maximum Reverse Stand-off Voltage V_{RWM}	Reverse Breakdown Voltage I/O to GND $V_Z @ 1.0\text{mA}$		Maximum Reverse Leakage Current I/O to GND $I_R @ V_{RWM}$	Maximum Clamping Voltage I/O to GND (8x20 μs) $V_C @ I_{PP}$		Typical TLP Clamping Voltage (Note 1) $V_{CL} @ I_{PP}$		Typical Dynamic Resistance (Note 1) R_{DYN}	Maximum Off State Junction Capacitance ($V_R=0, f=1.0\text{MHz}$)	
	V	MIN V		MAX V	μA	V	A		V	A
V	MIN V	MAX V	μA	V	A	V	A	Ω	pF	pF
5.0	6.0	9.0	1.0	12	1.0	12	4.0	0.5	0.8	0.4
				13	2.5	14	8.0			

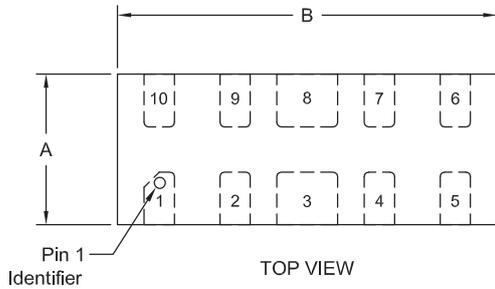
Note 1: Transmission Line Pulse (TLP) conditions: $Z_0=50\Omega, t_p=100\text{ns}$

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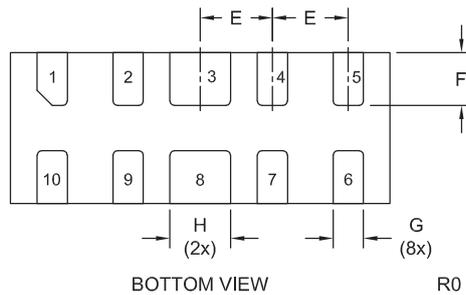
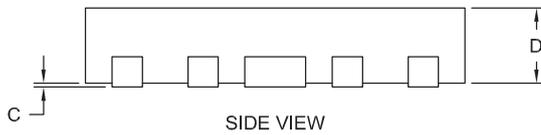


TLM1031 CASE - MECHANICAL OUTLINE



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.037	0.041	0.95	1.05
B	0.096	0.100	2.45	2.55
C	0.000	0.002	0.00	0.05
D	0.018	0.022	0.45	0.55
E	0.020		0.50	
F	0.012	0.016	0.30	0.40
G	0.006	0.010	0.15	0.25
H	0.014	0.018	0.35	0.45

TLM1031 (REV:R0)

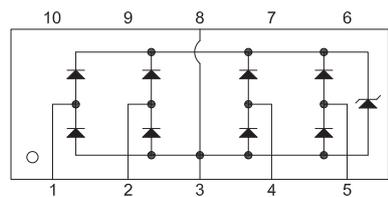


LEAD CODE:

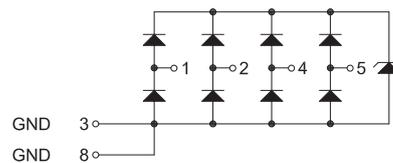
- 1) I/O 6) N/C
- 2) I/O 7) N/C
- 3) Ground 8) Ground
- 4) I/O 9) N/C
- 5) I/O 10) N/C

MARKING CODE: CTL5

PIN CONFIGURATION



SCHEMATIC



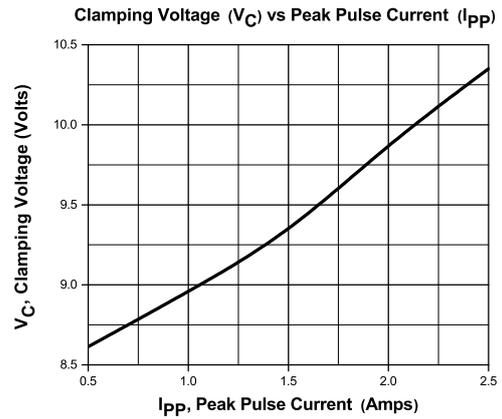
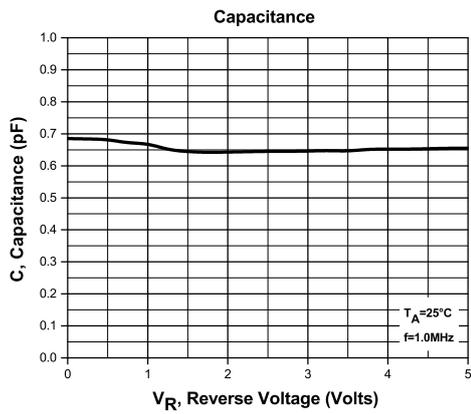
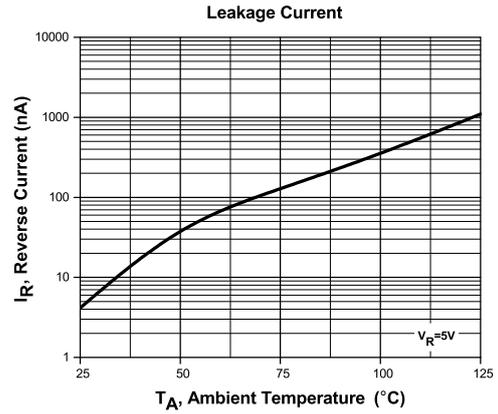
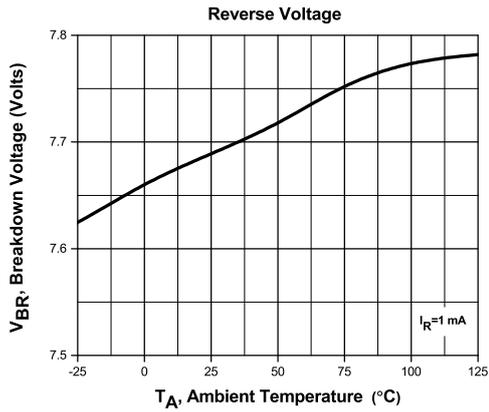
R4 (4-September 2015)

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TYPICAL ELECTRICAL CHARACTERISTICS



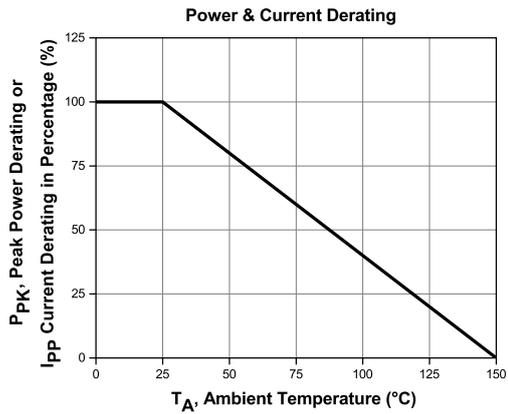
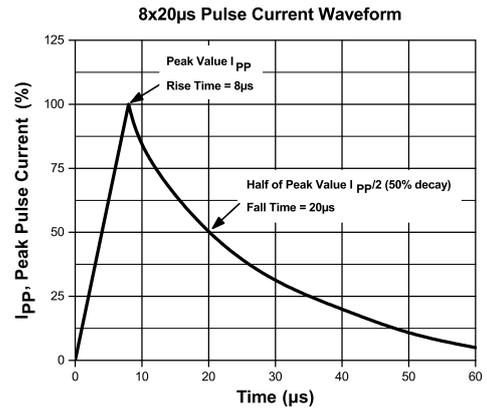
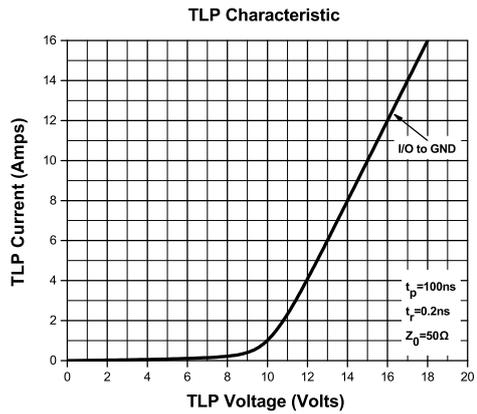
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- Application notes
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CONTACT US

Corporate Headquarters & Customer Support Team

Central Semiconductor Corp.
145 Adams Avenue
Hauppauge, NY 11788 USA
Main Tel: (631) 435-1110
Main Fax: (631) 435-1824
Support Team Fax: (631) 435-3388
www.centrasemi.com

Worldwide Field Representatives:
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Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru

moschip.ru_4

moschip.ru_6

moschip.ru_9