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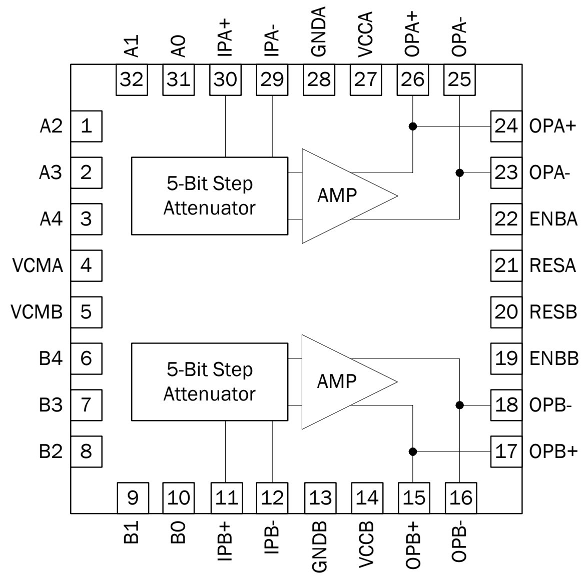
RFDA0035

DIGITAL CONTROLLED IF DUAL VGA 5 BIT 1dB LSB CONTROL

Package: QFN 32-Pin, 5.0mmx5.0mm



Functional Block Diagram

Features

- Dual Independent Digitally Controlled VGAs
- Bandwidth of 500MHz (-3dB)
- Gain Control Range=31dB (1dB Step Size)
- Differential Input and Output
- Max Gain=19.0dB@180MHz
- Noise Figure: 7.5dB@Maximum Gain
- High OIP3/P1dB=+42/21dBm @180MHz
- Relative Phase Shift<1°
- Single +5V Supply
- Dual 5-Bit Parallel Control Interface
- Individual Enable Control for Each VGA
- Current Adjustable for IP3 Trade Offs
- Small 32-Pin, 5.0mmx5.0mm, QFN

Applications

- Differential ADC Drivers
- Main and Diversity IF Sampling Receivers
- Wideband Multichannel Receivers
- Instrumentation

Product Description

RFMD's RFDA0035 is a dual-channel, digitally controlled variable gain amplifier featuring high linearity over the entire 32 gain control steps. It features independent channel power-up enable, independent channel current adjustability for optimizing DC versus IP3 and a 200Ω differential input and output impedance.

Ordering Information

RFDA0035SR	7" Sample reel with 100 pieces
RFDA0035SQ	25 piece Sample bag
RFDA0035TR7	7" Reel with 750 pieces
RFDA0035TR13	13" Reel with 2500 pieces
RFDA0035PCK-410	50MHz to 500MHz PCBA with 5-piece sample bag

Optimum Technology Matching® Applied

☐ GaAs HBT	☑ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	☐ BiFET HBT
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	☐ LDMOS

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	+6.0	V_{DC}
DC Supply Current	300	mA
Power Dissipation	1600	mW
Max RF Input Power	27	dBm
Operating Temperature (T_{CASE})	-40 to +85	°C
Storage Temperature	-40 to +150	°C
Junction Temperature	125	°C
ESD Rating (HBM)	500	V
Moisture Sensitivity Level	2	

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RFMD Green: RoHS compliant per EU Directive 2002/95/EC, halogen free per IEC 61249-2-21, < 1000 ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

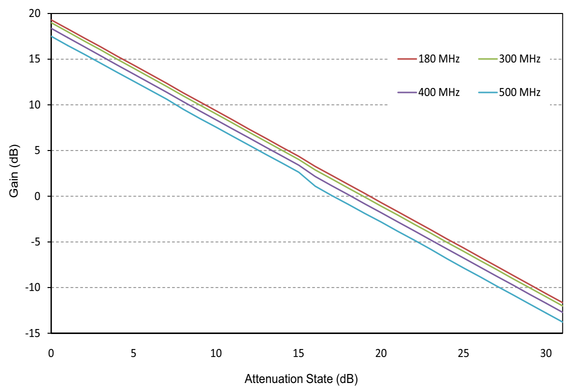
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25 °C, V_{CC}=V_{DD}=5V, Standard Application Circuit
Frequency Range	50		500	MHz	-3dB Bandwidth
Max Gain		19.3		dB	Attenuation=0dB, 180MHz
GainControlRange		31		dB	
Step Accuracy	+/- (0.1+1.5% attenuation setting)			dB	Major State Error up to 400MHz
Output P1dB		21		dBm	At 180MHz, Upper 24dB Steps
Output IP3		42		dBm	At 180MHz, P_{OUT}=5dBm/Tone, 1MHz Spacing
Control Interface		5		bit	Parallel Interface
Relative Phase Shift			1	°	50MHz~300MHz
Settling Time		15		ns	tON, tOFF (10%/90% RF)
Noise Figure		7.5		dB	Attenuation=0dB
Impedance		200		Ω	Differential
Input Return Loss			-12	dB	
Output Return Loss			-15	dB	
Total Supply Voltage	4.75	5.0	5.25	V	
Supply Current		240		mA	Both Channels Are Enabled. Can be Adjusted by External Resistors from RESA/B to Ground.

Typical RF Performance at Key Operating Frequencies

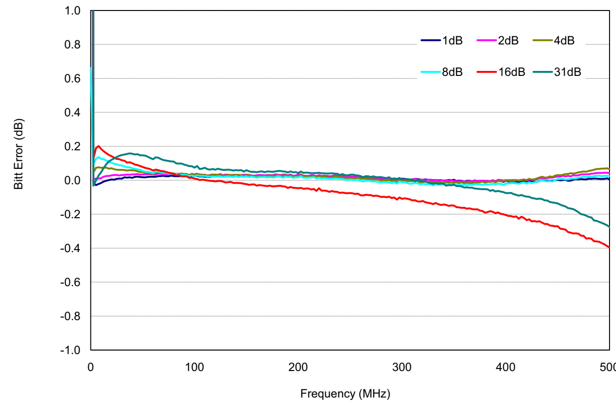
Parameter	Unit	100MHz	180MHz	300MHz
Max Small Signal Gain	dB	19.3	19.3	19.0
Output P1dB	dBm	21	21	21
Output IP3 [1]	dBm	43	42	40
Input Return Loss	dB	-15	-13	-15
Output Return Loss	dB	-17	-20	-17
Noise Figure	dB	7.0	7.2	7.5

Note: [1] OIP3 is tested at P_{OUT}=5dBm/Tone and 1MHz spacing.

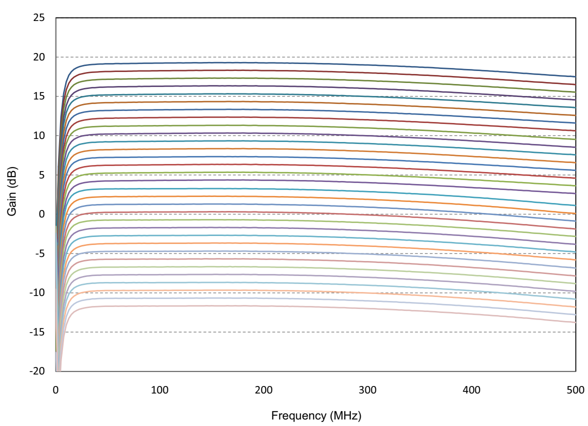
Gain (dB) versus Attenuation at Different Frequencies



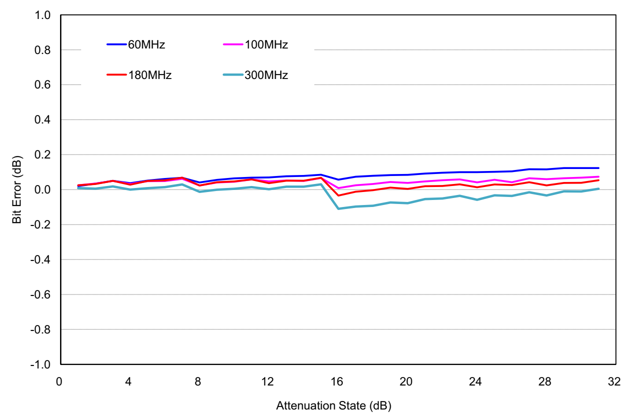
Major Attenuation States Bit Error (dB) versus Frequency



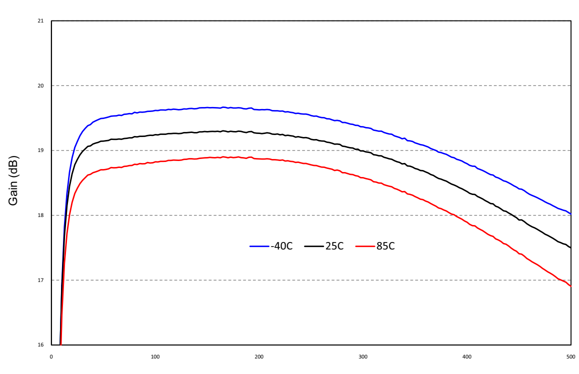
All States' Gain (dB) versus Frequency



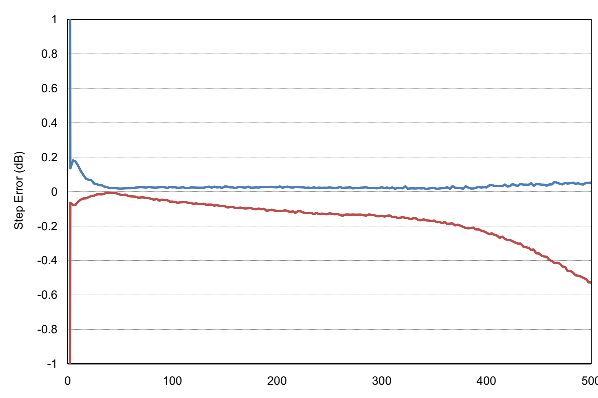
Bit Error (dB) versus Attenuation State



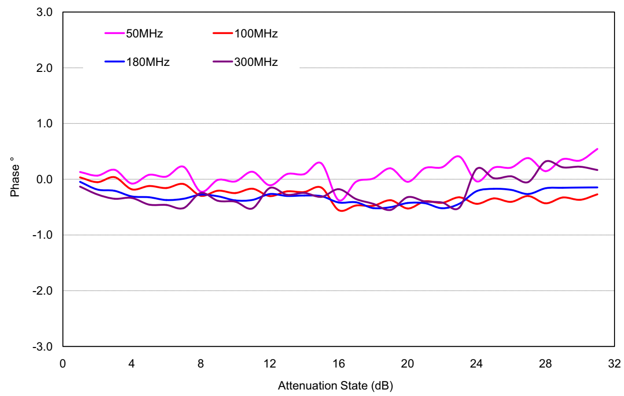
Max Gain (dB) versus Frequency, Three Temperatures



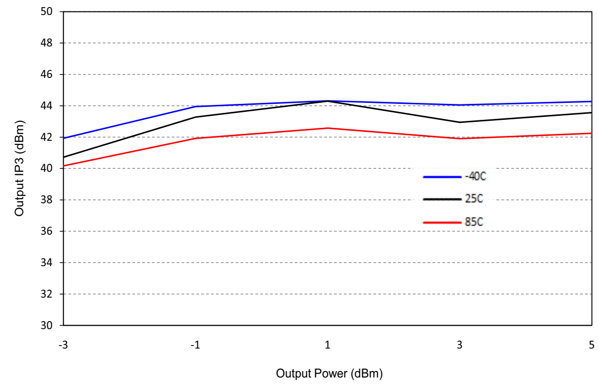
Worst Case Step Error (dB) Between Successive Attenuation States



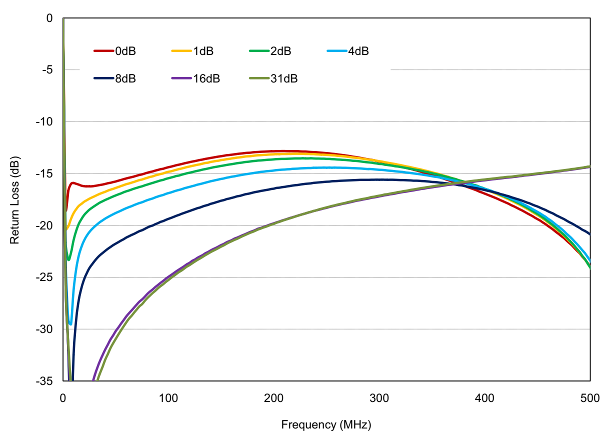
Relative Phase ° Related to Max Gain Step



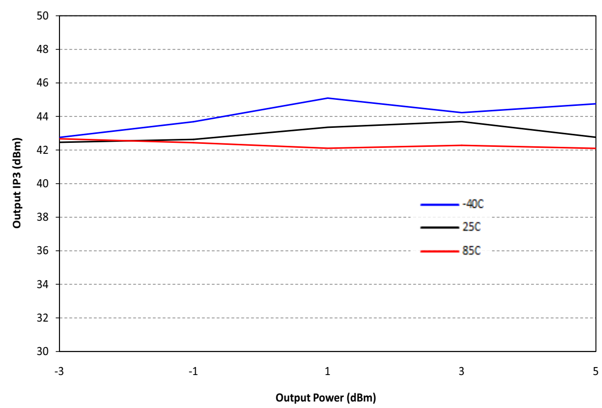
Max Gain Output IP3 (dBm) versus P_{OUT}, Frequency 180MHz



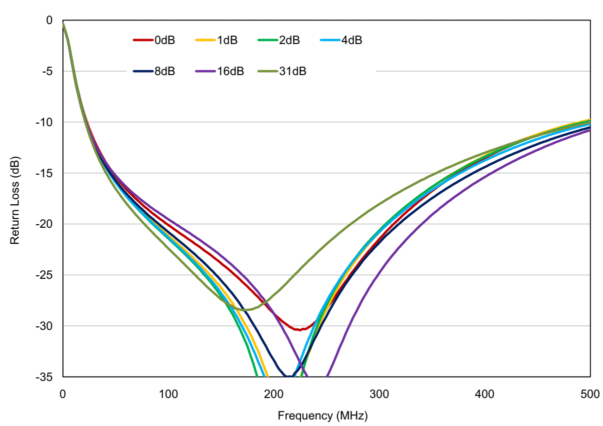
Input Return Loss (dB) versus Frequency



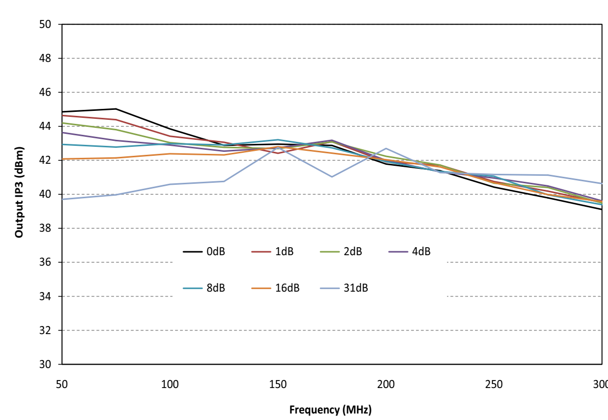
25dB Attenuation State Output IP3 (dBm) versus P_{OUT}, Frequency 180MHz



Output Return Loss (dB) versus Frequency



Output IP3 (dBm) versus Frequency, P_{OUT} 5dBm/Tone



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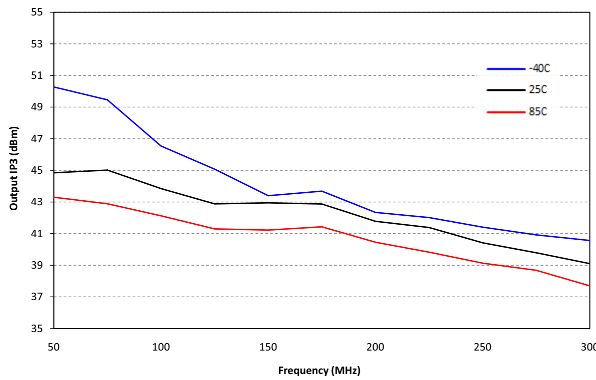
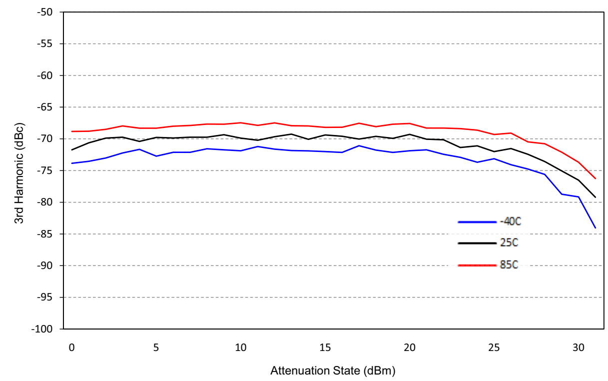
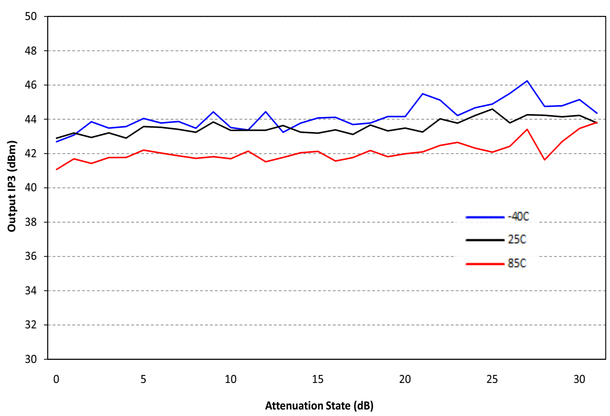
Max Gain Output IP3 (dBm) versus Frequency, P_{OUT} 5dBm/Tone



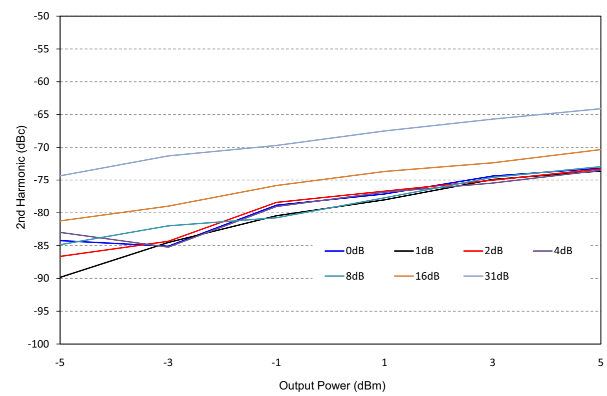
3rd Harmonic (dBc) versus Attenuation at 180MHz, P_{OUT} 5dBm



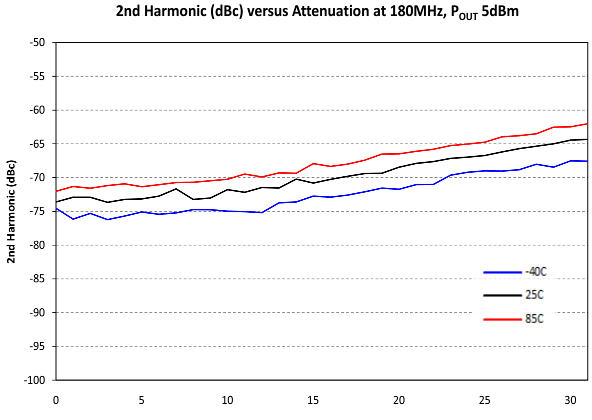
Output IP3 (dBm) versus Attenuation at 180MHz, P_{OUT} 5dBm/Tone



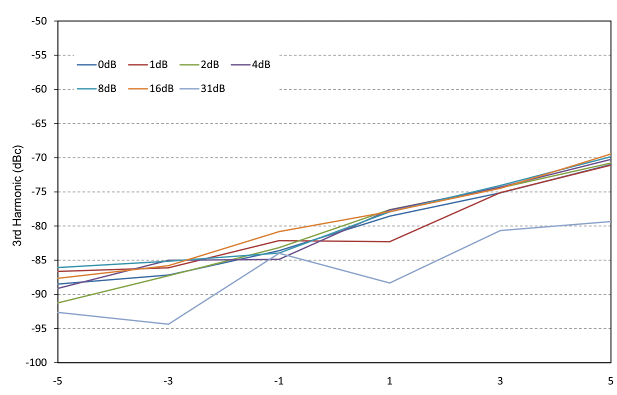
2nd Harmonic (dBc) versus P_{OUT} at 180MHz



2nd Harmonic (dBc) versus Attenuation at 180MHz, P_{OUT} 5dBm



3rd Harmonic (dBc) versus P_{OUT} at 180MHz



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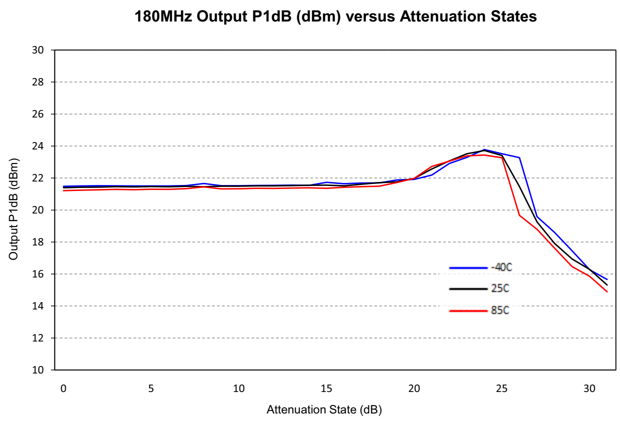

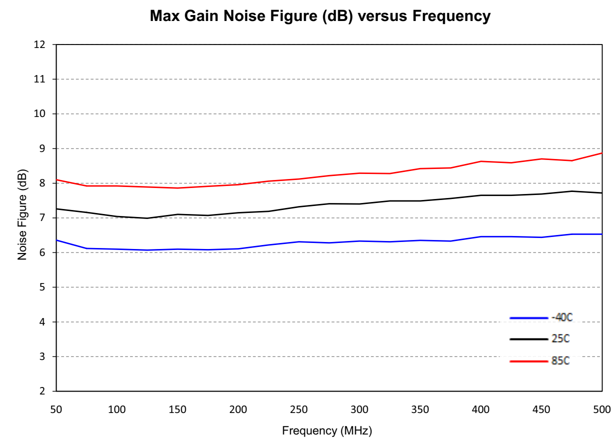

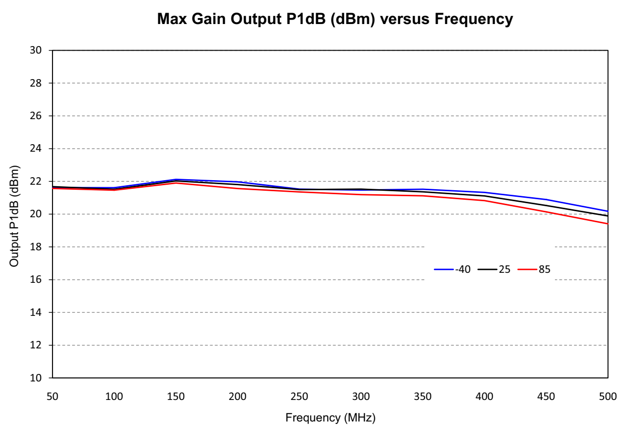

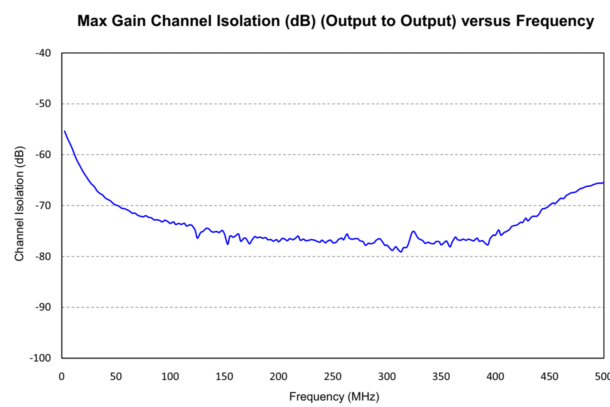

Truth Table

Control Bits					Gain Relative to Maximum Gain
A4/B4	A3/B3	A2/B2	A1/B1	A0/B0	
0	0	0	0	0	0dB
0	0	0	0	1	-1dB
0	0	0	1	0	-2dB
0	0	0	1	1	-3dB
0	0	1	0	0	-4dB
0	0	1	0	1	-5dB
0	0	1	1	0	-6dB
0	0	1	1	1	-7dB
0	1	0	0	0	-8dB
0	1	0	0	1	-9dB
0	1	0	1	0	-10dB
0	1	0	1	1	-11dB
0	1	1	0	0	-12dB
0	1	1	0	1	-13dB
0	1	1	1	0	-14dB
0	1	1	1	1	-15dB
1	0	0	0	0	-16dB
1	0	0	0	1	-17dB
1	0	0	1	0	-18dB
1	0	0	1	1	-19dB
1	0	1	0	0	-20dB
1	0	1	0	1	-21dB
1	0	1	1	0	-22dB
1	0	1	1	1	-23dB
1	1	0	0	0	-24dB
1	1	0	0	1	-25dB
1	1	0	1	0	-26dB
1	1	0	1	1	-27dB
1	1	1	0	0	-28dB
1	1	1	0	1	-29dB
1	1	1	1	0	-30dB
1	1	1	1	1	-31dB

Logic Voltage Levels	
State	Logic
Low	0.0V to 1.0V
High	1.8V to 5.0V

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Pin Names and Descriptions

Pin	Function	Description
1	A2	MSB - 2 for the Gain Control Interface for Channel A.
2	A3	MSB - 1 for the Gain Control Interface for Channel A.
3	A4	MSB for the 5-Bit Gain Control Interface for Channel A.
4	VCMA	Channel A Input Common-Mode Voltage. Typically Bypassed to Ground Through Capacitor.
5	VCMB	Channel B Input Common-Mode Voltage. Typically Bypassed to Ground Through Capacitor.
6	B4	MSB for the 5-Bit Gain Control Interface for Channel B.
7	B3	MSB - 1 for the Gain Control Interface for Channel B.
8	B2	MSB - 2 for the Gain Control Interface for Channel B.
9	B1	LSB + 1 for the Gain Control Interface for Channel B.
10	B0	LSB for the Gain Control Interface for Channel B.
11	IPB+	Channel B Positive Input.
12	IPB-	Channel B Negative Input.
13	GNDB	Device Common (DC Ground) for Channel B.
14	VCCB	Positive Supply Pin for Channel B. Should be Bypassed to Ground Using Suitable Bypass Capacitor.
15	OPB+	Positive Output Pins (Open Collector) for Channel B. Require DC Bias of +5V Nominal.
16	OPB-	Negative Output Pins (Open Collector) for Channel B. Require DC Bias of +5V Nominal.
17	OPB+	Positive Output Pins (Open Collector) for Channel B. Require DC Bias of +5V Nominal.
18	OPB-	Negative Output Pins (Open Collector) for Channel B. Require DC Bias of +5V Nominal.
19	ENBB	Power Enable Pin for Channel B. Channel B is Enabled with a Logic High and Disabled with a Logic Low.
20	RESB	Current Adjust Pin. Connect a Resistor from RESB to Ground can Adjust the Channel B DC Current from 90mA to 120mA. Leave Pin Floating for Nominal Bias of 120mA.
21	RESA	Current Adjust Pin. Connect a Resistor from RESA to Ground can Adjust the Channel A DC Current from 90mA to 120mA. Leave Pin Floating for Nominal Bias of 120mA.
22	ENBA	Power Enable Pin for Channel A. Channel A is Enabled with a Logic High and Disabled with a Logic Low.
23	OPA-	Negative Output Pins (Open Collector) for Channel A. Require DC Bias of +5V Nominal.
24	OPA+	Positive Output Pins (Open Collector) for Channel A. Require DC Bias of +5V Nominal.
25	OPA-	Negative Output Pins (Open Collector) for Channel A. Require DC Bias of +5V Nominal.
26	OPA+	Positive Output Pins (Open Collector) for Channel A. Require DC Bias of +5V Nominal.
27	VCCA	Positive Supply Pins for Channel A. Should be Bypassed to Ground Using Suitable Bypass Capacitor.
28	GNDA	Device Common (DC Ground) for Channel A
29	IPA-	Channel A Negative Input.
30	IPA+	Channel A Positive Input.
31	A0	LSB for the Gain Control Interface for Channel A.
32	A1	LSB + 1 for the Gain Control Interface for Channel A.

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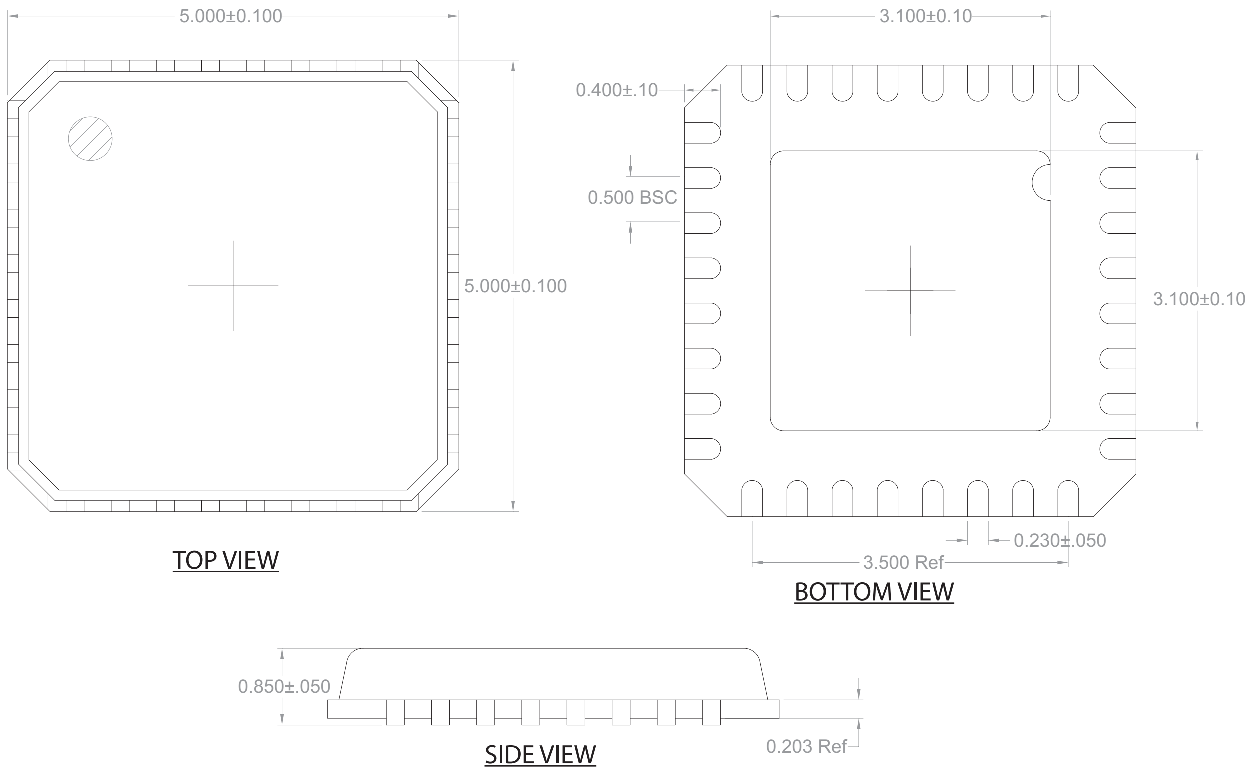
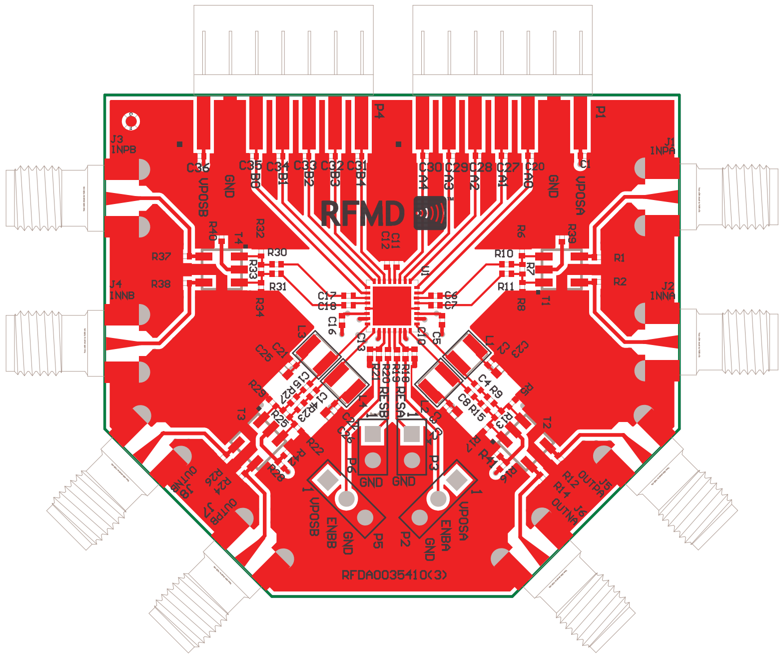
Package Drawing

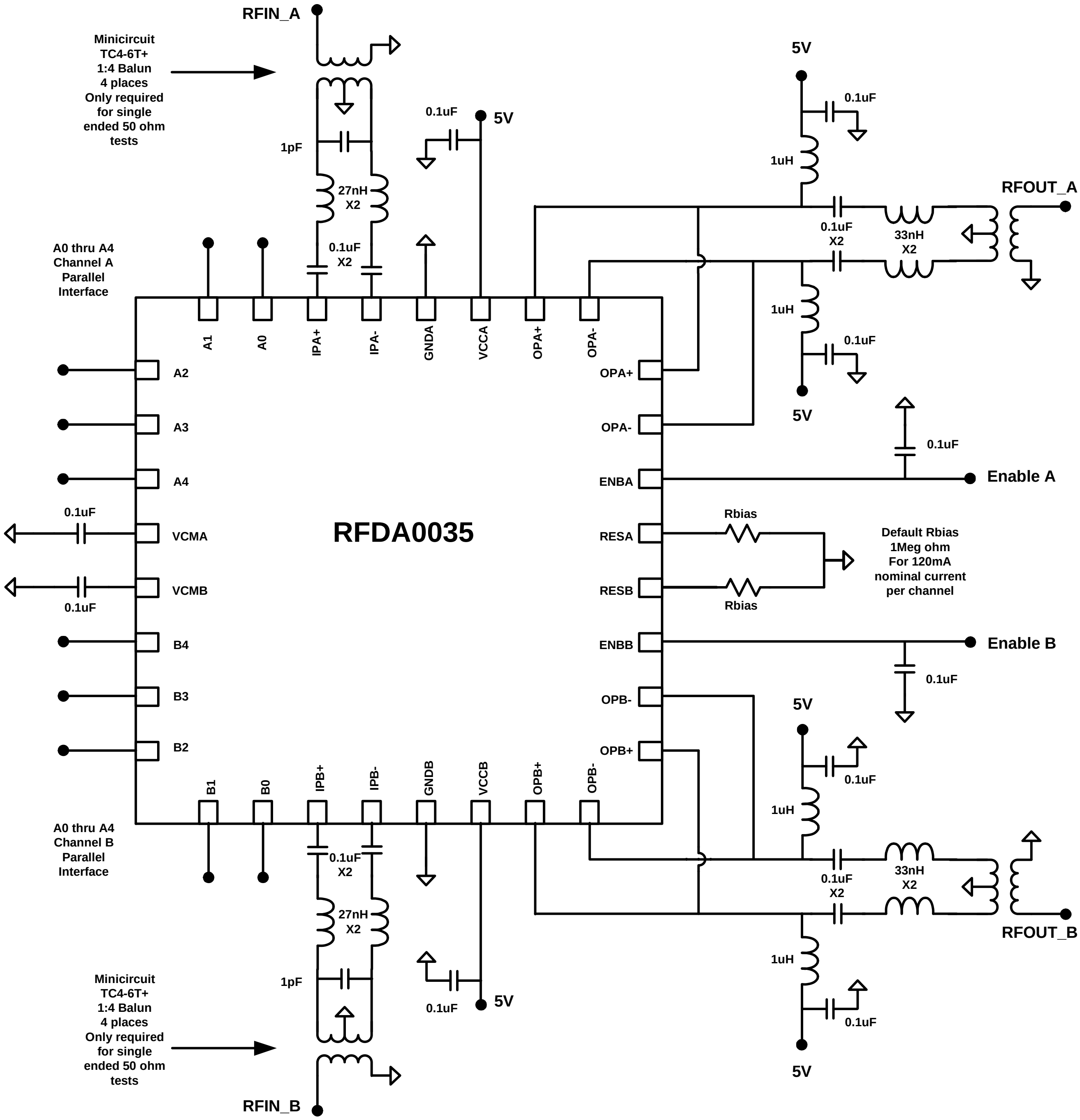
5.0mmx5.0mm, 32 lead, QFN



Evaluation Board Assembly Drawing



Application Schematic



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Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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