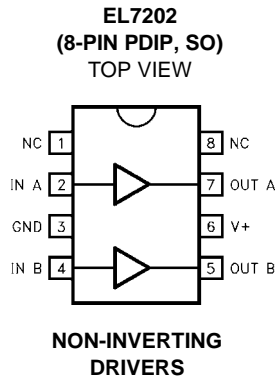
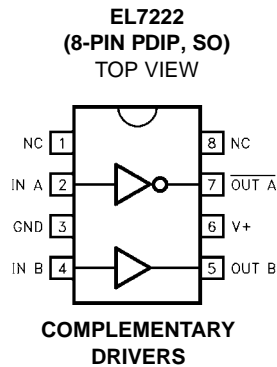
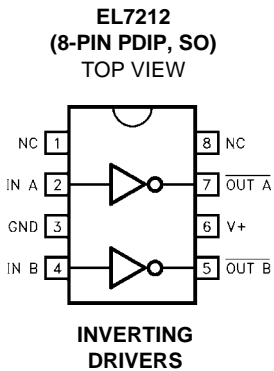


High Speed, Dual Channel Power MOSFET Drivers

The EL7202, EL7212, EL7222 ICs are matched dual-drivers that improve the operation of the industry standard DS0026 clock drivers. The Elantec versions are very high speed drivers capable of delivering peak currents of 2.0 amps into highly capacitive loads. The high speed performance is achieved by means of a proprietary "Turbo-Driver" circuit that speeds up input stages by tapping the wider voltage swing at the output. Improved speed and drive capability are enhanced by matched rise and fall delay times. These matched delays maintain the integrity of input-to-output pulse-widths to reduce timing errors and clock skew problems. This improved performance is accompanied by a 10 fold reduction in supply currents over bipolar drivers, yet without the delay time problems commonly associated with CMOS devices. Dynamic switching losses are minimized with non-overlapped drive techniques.

Pinouts



Manufactured under U.S. Patent Nos. 5,334,883, #5,341,047

Features

- Industry standard driver replacement
- Improved response times
- Matched rise and fall times
- Reduced clock skew
- Low output impedance
- Low input capacitance
- High noise immunity
- Improved clocking rate
- Low supply current
- Wide operating voltage range
- Pb-Free available (RoHS compliant)

Applications

- Clock/line drivers
- CCD Drivers
- Ultra-sound transducer drivers
- Power MOSFET drivers
- Switch mode power supplies
- Class D switching amplifiers
- Ultrasonic and RF generators
- Pulsed circuits

Ordering Information

| Part Number | PART MARKING | TAPE & REEL | PACKAGE | PKG. DWG. # |
|-----------------------------|--------------|-------------|-------------------------|-------------|
| EL7202CN | EL7202CN | - | 8 Ld PDIP | MDP0031 |
| EL7202CS | 7202CS | - | 8 Ld SOIC | MDP0027 |
| EL7202CS-T7 | 7202CS | 7" | 8 Ld SOIC | MDP0027 |
| EL7202CS-T13 | 7202CS | 13" | 8 Ld SOIC | MDP0027 |
| EL7202CSZ (See Note) | 7202CSZ | - | 8 Ld SOIC (Pb-free) | MDP0027 |
| EL7202CSZ-T7 (See Note) | 7202CSZ | 7" | 8 Ld SOIC (Pb-free) | MDP0027 |
| EL7202CSZ-T13 (See Note) | 7202CSZ | 13" | 8 Ld SOIC (Pb-free) | MDP0027 |
| EL7212CN | EL7212CN | - | 8 Ld PDIP | MDP0031 |
| EL7212CNZ | EL7212CN Z | - | 8 Ld PDIP* (Pb-free) | MDP0031 |
| EL7212CS | 7212CS | - | 8 Ld SOIC | MDP0027 |
| EL7212CS-T7 | 7212CS | 7" | 8 Ld SOIC | MDP0027 |
| EL7212CS-T13 | 7212CS | 13" | 8 Ld SOIC | MDP0027 |
| EL7212CSZ (See Note) | 7212CSZ | - | 8 Ld SOIC (Pb-free) | MDP0027 |
| EL7212CSZ-T7 (See Note) | 7212CSZ | 7" | 8 Ld SOIC (Pb-free) | MDP0027 |
| EL7212CSZ-T13 (See Note) | 7212CSZ | 13" | 8 Ld SOIC (Pb-free) | MDP0027 |
| EL7222CN | EL7222CN | - | 8 Ld PDIP | MDP0031 |
| EL7222CS | 7222CS | - | 8 Ld SOIC | MDP0027 |
| EL7222CS-T7 | 7222CS | 7" | 8 Ld SOIC | MDP0027 |
| EL7222CS-T13 | 7222CS | 13" | 8 Ld SOIC | MDP0027 |
| EL7222CSZ (See Note) | 7222CSZ | - | 8 Ld SOIC (Pb-free) | MDP0027 |
| EL7222CSZ-T7 (See Note) | 7222CSZ | 7" | 8 Ld SOIC (Pb-free) | MDP0027 |
| EL7222CSZ-T13 (See Note) | 7222CSZ | 13" | 8 Ld SOIC (Pb-free) | MDP0027 |

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

EL7202, EL7212, EL7222

Absolute Maximum Ratings (T_A = 25°C)

| | |
|--|--|
| Supply (V+ to Gnd) 16.5V | Operating Junction Temperature 125°C |
| Input Pins -0.3V to +0.3V above V+ | Power Dissipation |
| Combined Peak Output Current 4A | SOIC 570mW |
| Storage Temperature Range -65°C to +150°C | PDIP 1050mW |
| Ambient Operating Temperature -40°C to +85°C | |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: T_J = T_C = T_A

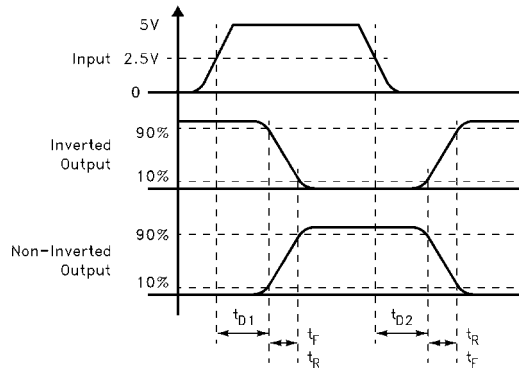
DC Electrical Specifications T_A = 25°C, V = 15V unless otherwise specified

| parameter | Description | Test Conditions | Min | Typ | Max | Units |
|---------------------|---------------------------|--|-----|-----------------|-------------------|-------|
| INPUT | | | | | | |
| V _{IH} | Logic "1" Input Voltage | | 2.4 | | | V |
| I _{IH} | Logic "1" Input Current | @V+ | | 0.1 | 10 | μA |
| V _{IL} | Logic "0" Input Voltage | | | | 0.8 | V |
| I _{IL} | Logic "0" Input Current | @0V | | 0.1 | 10 | μA |
| V _{HVS} | Input Hysteresis | | | 0.3 | | V |
| OUTPUT | | | | | | |
| R _{OH} | Pull-Up Resistance | I _{OUT} = -100mA | | 3 | 6 | Ω |
| R _{OL} | Pull-Down Resistance | I _{OUT} = +100mA | | 4 | 6 | Ω |
| I _{PK} | Peak Output Current | Source Sink | | 2 2 | | A |
| I _{DC} | Continuous Output Current | Source/Sink | 100 | | | mA |
| POWER SUPPLY | | | | | | |
| I _S | Power Supply Current | Inputs High/EL7202 Inputs High/EL7212 Inputs High/EL7222 | | 4.5 1 2.5 | 7.5 2.5 5.0 | mA |
| V _S | Operating Voltage | | 4.5 | | 15 | V |

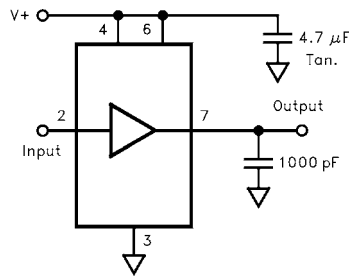
AC Electrical Specifications T_A = 25°C, V = 15V unless otherwise specified

| parameter | Description | Test Conditions | Min | Typ | Max | Units |
|----------------------------------|---------------------|---|-----|-----------|-----|-------|
| SWITCHING CHARACTERISTICS | | | | | | |
| t _R | Rise Time | C _L = 500pF C _L = 1000pF | | 7.5 10 | 20 | ns |
| t _F | Fall Time | C _L = 500pF C _L = 1000pF | | 10 13 | 20 | ns |
| t _{D1} | Turn-On Delay Time | See Timing Table | | 18 | 25 | ns |
| t _{D2} | Turn-Off Delay Time | See Timing Table | | 20 | 25 | ns |

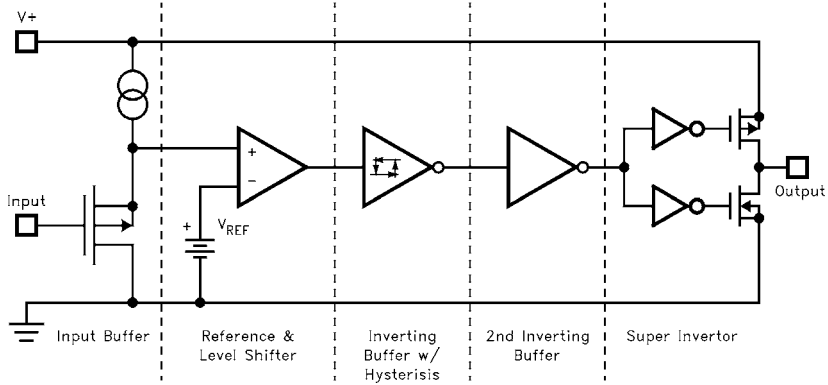
Timing Table



Standard Test Configuration

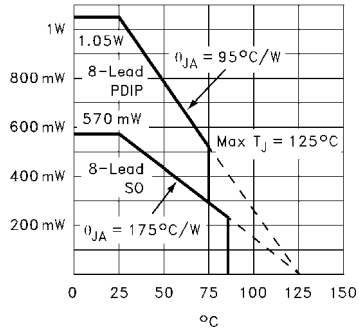


Simplified Schematic

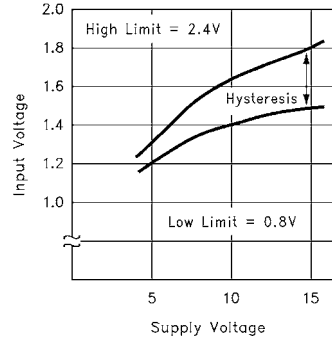


Typical Performance Curves

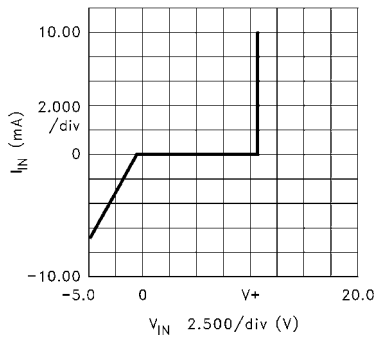
MAX POWER/DERATING CURVES



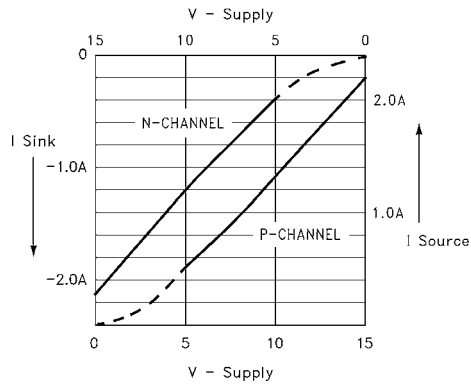
SWITCH THRESHOLD vs SUPPLY VOLTAGE



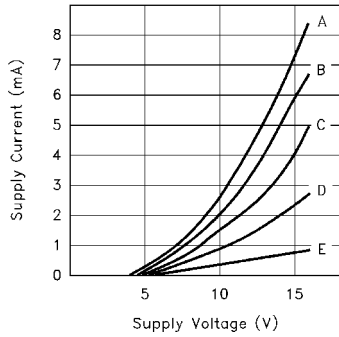
INPUT CURRENT vs VOLTAGE



PEAK DRIVE vs SUPPLY VOLTAGE



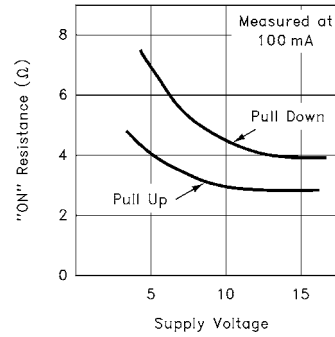
QUIESCENT SUPPLY CURRENT



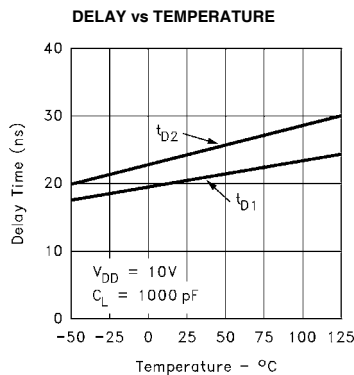
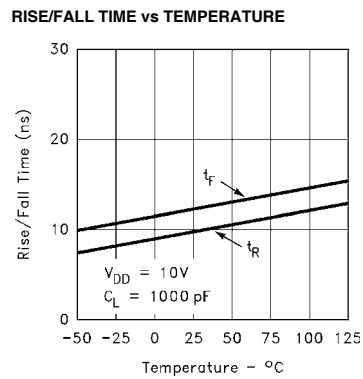
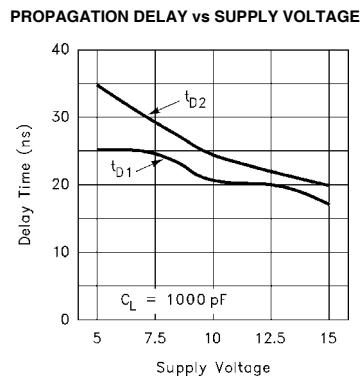
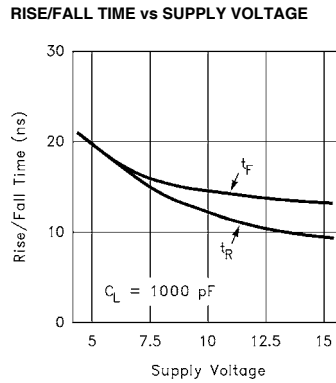
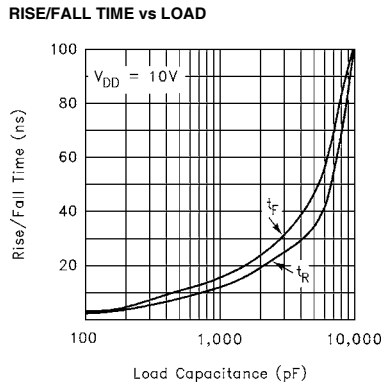
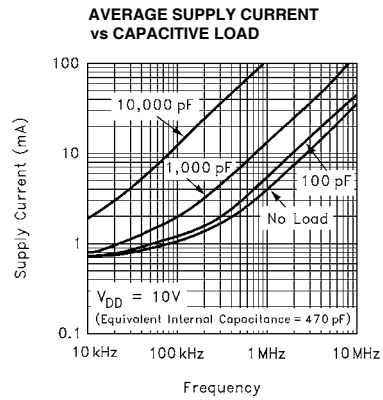
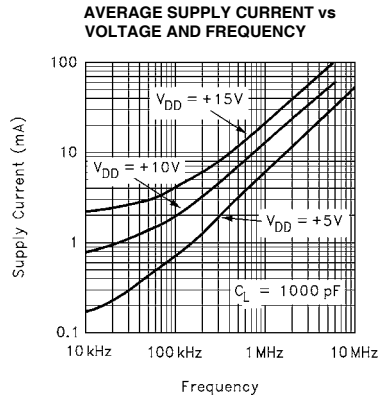
CASE:

| Device | Input Level | Curve |
|--------|-------------|-------|
| EL7202 | GND | A |
| EL7202 | GND, V+ | B |
| EL7202 | V+ | C |
| EL7212 | GND | C |
| EL7212 | GND, V+ | D |
| EL7212 | V+ | E |
| EL7222 | GND | B |
| EL7222 | GND, V+ | C |
| EL7222 | V+ | D |

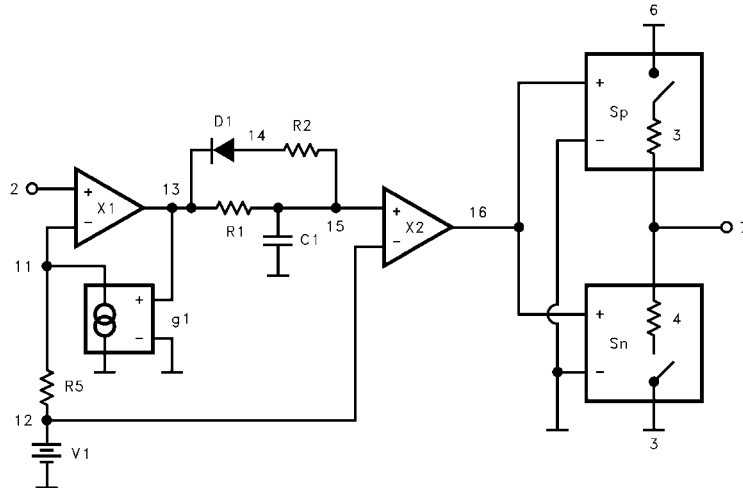
"ON" RESISTANCE vs SUPPLY VOLTAGE



Typical Performance Curves (Continued)



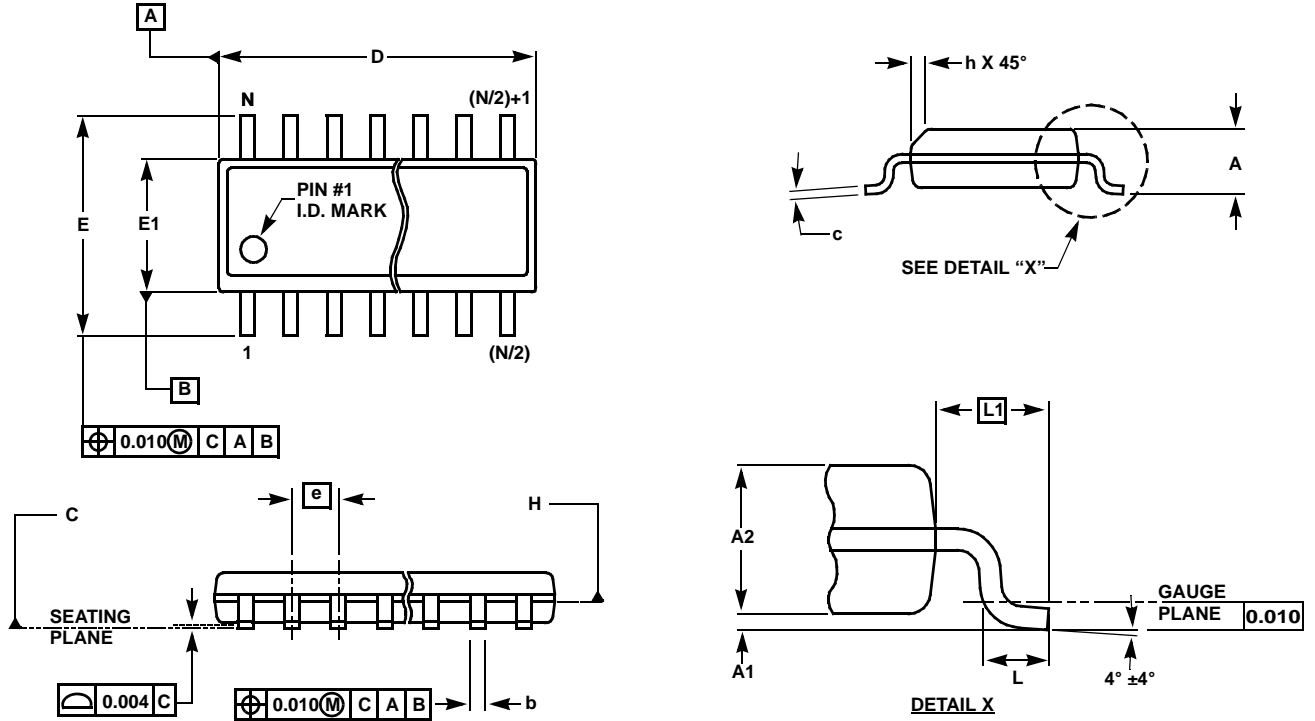
EL7212 Macro Model



```

**** EL7212 model ****
*           input
*           |   gnd
*           |   |   Vsupply
*           |   |   |   Vout
*           |   |   |   |
.subckt M7212 2 3 6 7
V1 12 3 1.6
R1 13 15 1k
R2 14 15 5k
R5 11 12 100
C1 15 3 43.3 pF
D1 14 13 dmod
X1 13 11 2 3 comp1
X2 16 12 15 3 comp1
sp 6 7 16 3 spmod
sn 7 3 16 3 snmod
g1 11 0 13 0 938μ
.model dmod d
.model spmod vswitch ron3 roff2meg von1 voff1.5
.model snmod vswitch ron4 roff2meg von3 voff2
.ends M7212
.subckt comp1 out inp inm vss
e1 out vss table { (v(inp) v(inm))* 5000} (0,0) (3.2,3.2)
Rout out vss 10meg
Rinp inp vss 10meg
Rinm inm vss 10meg
.ends comp1
    
```

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

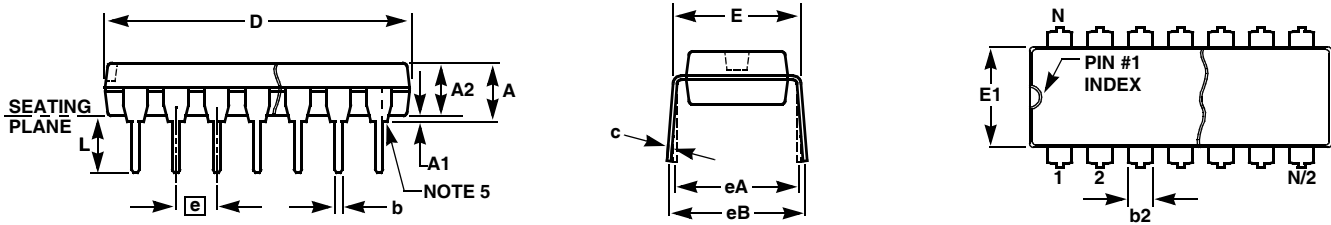
| SYMBOL | SO-8 | SO-14 | SO16 (0.150") | SO16 (0.300") (SOL-16) | SO20 (SOL-20) | SO24 (SOL-24) | SO28 (SOL-28) | TOLERANCE | NOTES |
|--------|-------|-------|------------------|---------------------------|------------------|------------------|------------------|-------------|-------|
| A | 0.068 | 0.068 | 0.068 | 0.104 | 0.104 | 0.104 | 0.104 | MAX | - |
| A1 | 0.006 | 0.006 | 0.006 | 0.007 | 0.007 | 0.007 | 0.007 | ± 0.003 | - |
| A2 | 0.057 | 0.057 | 0.057 | 0.092 | 0.092 | 0.092 | 0.092 | ± 0.002 | - |
| b | 0.017 | 0.017 | 0.017 | 0.017 | 0.017 | 0.017 | 0.017 | ± 0.003 | - |
| c | 0.009 | 0.009 | 0.009 | 0.011 | 0.011 | 0.011 | 0.011 | ± 0.001 | - |
| D | 0.193 | 0.341 | 0.390 | 0.406 | 0.504 | 0.606 | 0.704 | ± 0.004 | 1, 3 |
| E | 0.236 | 0.236 | 0.236 | 0.406 | 0.406 | 0.406 | 0.406 | ± 0.008 | - |
| E1 | 0.154 | 0.154 | 0.154 | 0.295 | 0.295 | 0.295 | 0.295 | ± 0.004 | 2, 3 |
| e | 0.050 | 0.050 | 0.050 | 0.050 | 0.050 | 0.050 | 0.050 | Basic | - |
| L | 0.025 | 0.025 | 0.025 | 0.030 | 0.030 | 0.030 | 0.030 | ± 0.009 | - |
| L1 | 0.041 | 0.041 | 0.041 | 0.056 | 0.056 | 0.056 | 0.056 | Basic | - |
| h | 0.013 | 0.013 | 0.013 | 0.020 | 0.020 | 0.020 | 0.020 | Reference | - |
| N | 8 | 14 | 16 | 16 | 20 | 24 | 28 | Reference | - |

Rev. L 2/01

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

Plastic Dual-In-Line Packages (PDIP)



**MDP0031
PLASTIC DUAL-IN-LINE PACKAGE**

| SYMBOL | PDIP8 | PDIP14 | PDIP16 | PDIP18 | PDIP20 | TOLERANCE | NOTES |
|--------|-------|--------|--------|--------|--------|---------------|-------|
| A | 0.210 | 0.210 | 0.210 | 0.210 | 0.210 | MAX | |
| A1 | 0.015 | 0.015 | 0.015 | 0.015 | 0.015 | MIN | |
| A2 | 0.130 | 0.130 | 0.130 | 0.130 | 0.130 | ±0.005 | |
| b | 0.018 | 0.018 | 0.018 | 0.018 | 0.018 | ±0.002 | |
| b2 | 0.060 | 0.060 | 0.060 | 0.060 | 0.060 | +0.010/-0.015 | |
| c | 0.010 | 0.010 | 0.010 | 0.010 | 0.010 | +0.004/-0.002 | |
| D | 0.375 | 0.750 | 0.750 | 0.890 | 1.020 | ±0.010 | 1 |
| E | 0.310 | 0.310 | 0.310 | 0.310 | 0.310 | +0.015/-0.010 | |
| E1 | 0.250 | 0.250 | 0.250 | 0.250 | 0.250 | ±0.005 | 2 |
| e | 0.100 | 0.100 | 0.100 | 0.100 | 0.100 | Basic | |
| eA | 0.300 | 0.300 | 0.300 | 0.300 | 0.300 | Basic | |
| eB | 0.345 | 0.345 | 0.345 | 0.345 | 0.345 | ±0.025 | |
| L | 0.125 | 0.125 | 0.125 | 0.125 | 0.125 | ±0.010 | |
| N | 8 | 14 | 16 | 18 | 20 | Reference | |

Rev. B 2/99

NOTES:

1. Plastic or metal protrusions of 0.010" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions E and eA are measured with the leads constrained perpendicular to the seating plane.
4. Dimension eB is measured with the lead tips unconstrained.
5. 8 and 16 lead packages have half end-leads as shown.

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