Quad, Current-Output, Serial-Input 16-Bit DAC

Enhanced Product

AD5544-EP

FEATURES

2 mA full-scale current ± 20%, with V_{REF} = ±10 V
0.9 μs settling time to ±0.1%
12 MHz multiplying bandwidth
Midscale glitch of −1 nV-sec
Midscale or zero-scale reset
4 separate, 4-quadrant multiplying reference inputs
SPI-compatible, 3-wire interface
Double-buffered registers enable
Simultaneous multichannel change
Internal power-on reset
Compact 28-lead SSOP

ENHANCED PRODUCT FEATURES

Supports defense and aerospace applications (AQEC)
Military temperature range (−55°C to +125°C)
Controlled manufacturing baseline
1 assembly/test site
1 fabrication site
Enhanced product change notification
Qualification data available on request

APPLICATIONS

Automatic test equipment
Instrumentation
Digitally controlled calibration

FUNCTIONAL BLOCK DIAGRAM

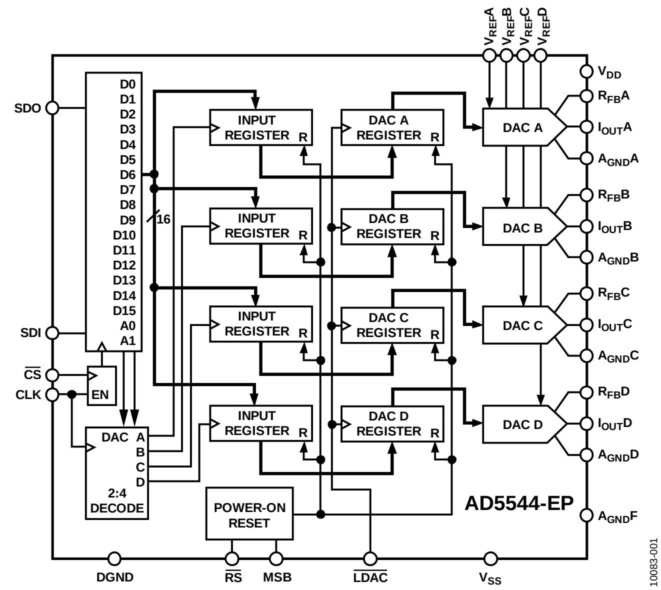

Figure 1.

GENERAL DESCRIPTION

The AD5544-EP quad, 16-bit, current output, digital-to-analog converter (DAC) is designed to operate from a 2.7 V to 5.5 V supply range.

The applied external reference input voltage (V_{REF}x) determines the full-scale output current. Integrated feedback resistors (R_{FB}) provide temperature-tracking, full-scale voltage outputs when combined with an external I-to-V precision amplifier.

A double-buffered serial data interface offers high speed, 3-wire, SPI- and microcontroller-compatible inputs using serial data in (SDI), a chip select ($\overline{CS}$), and clock (CLK) signals. In addition, a serial data out pin (SDO) allows for daisy chaining when multiple packages are used. A common, level-sensitive, load DAC strobe ($\overline{LDAC}$) input allows the simultaneous update of all DAC outputs from previously loaded input registers. Additionally, an internal power-on reset forces the output voltage to 0 at system turn-on. The MSB pin allows system reset assertion ($\overline{RS}$) to force all registers to zero code when MSB = 0 or to half-scale code when MSB = 1. The AD5544-EP is packaged in the compact 28-lead SSOP.

Additional application and technical information can be found in the AD5544 data sheet.

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REVISION HISTORY

4/12—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V, V_{SS} = 0 V, I_{OUT}x = virtual GND, A_{GND}x = 0 V, V_{REF}A = V_{REF}B = V_{REF}C = V_{REF}D = 10 V, T_A = full operating temperature range of −55°C to +125°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Condition/Comments	Min	Typ	Max	Unit
STATIC PERFORMANCE[1]						
Resolution	N	1 LSB = V_{REF}x/2^{16} = 153 µV when V_{REF} = 10 V			16	Bits
Relative Accuracy	INL				±1.5	LSB
Differential Nonlinearity	DNL				±1.5	LSB
Output Leakage Current	I_{OUT}x	Data = 0x0000, T_A = 25°C			10	nA
		Data = 0x0000, T_A = 85°C			20	nA
Full-Scale Gain Error	G_{FSE}	Data = 0xFFFF		±0.75	±4	mV
Full-Scale Tempco[2]	TCV_{FS}			1		ppm/°C
Feedback Resistor	R_{FB}x	V_{DD} = 5 V	4	6	8	kΩ
REFERENCE INPUT						
V_{REF}x Range	V_{REF}x		−15		+15	V
Input Resistance	R_{REF}x		4	6	8	kΩ
Input Resistance Match	R_{REF}x	Channel-to-channel		0.35		%
Input Capacitance[2]	C_{REF}x			5		pF
ANALOG OUTPUT						
Output Current	I_{OUT}x	Data = 0xFFFF	1.25		2.5	mA
Output Capacitance[2]	C_{OUT}x	Code dependent		35		pF
LOGIC INPUT AND OUTPUT						
Logic Input Low Voltage	V_{IL}				0.8	V
Logic Input High Voltage	V_{IH}		2.4			V
Input Leakage Current	I_{IL}				1	µA
Input Capacitance[2]	C_{IL}				10	pF
Logic Output Low Voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Logic Output High Voltage	V_{OH}	I_{OH} = 100 µA	4			V
INTERFACE TIMING[2, 3]						
Clock Width High	t_{CH}		25			ns
Clock Width Low	t_{CL}		25			ns
$\overline{CS}$ to Clock Setup	t_{CSS}		0			ns
Clock to $\overline{CS}$ Hold	t_{CSH}		25			ns
Clock to SDO Propagation Delay	t_{PD}		2		20	ns
Load DAC Pulse Width	t_{LDAC}		25			ns
Data Setup	t_{DS}		20			ns
Data Hold	t_{DH}		20			ns
Load Setup	t_{LDS}		5			ns
Load Hold	t_{LDH}		25			ns
SUPPLY CHARACTERISTICS						
Power Supply Range	$V_{DD\ RANGE}$		2.7		5.5	V
Positive Supply Current	I_{DD}	Logic inputs = 0 V			5	µA
Negative Supply Current	I_{SS}	Logic inputs = 0 V, V_{SS} = −5 V		0.001	9	µA
Power Dissipation	P_{DISS}	Logic inputs = 0 V			1.25	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%			0.006	%/%

Parameter	Symbol	Test Condition/Comments	Min	Typ	Max	Unit
AC CHARACTERISTICS[4]						
Output Voltage Settling Time	t_S	To ±0.1% of full scale, data = 0x0000 to 0xFFFF to 0x0000		0.9		μs
Reference Multiplying Bandwidth (BW)	BW − 3 dB	V_{REF}x = 5 V p-p, data = 0xFFFF, C_{FB} = 2.0 pF,		12		MHz
DAC Glitch Impulse	Q	V_{REF}x = 8 V, data = 0x0000 to 0x8000 to 0x0000		−1		nV-sec
Feedthrough Error	V_{OUT}x/V_{REF}x	Data = 0x0000, V_{REF}x = 100 mV rms, f = 100 kHz		−65		dB
Crosstalk Error	V_{OUT}A/V_{REF}B	Data = 0x0000, V_{REF}B = 100 mV rms, adjacent channel, f = 100 kHz		−90		dB
Digital Feedthrough	Q	$\overline{CS}$ = 1, f_{CLK} = 1 MHz		0.6		nV-sec
Total Harmonic Distortion	THD	V_{REF}x = 5 V p-p, data = 0xFFFF, f = 1 kHz		−98		dB
Output Spot Noise Voltage	e_N	f = 1 kHz, BW = 1 Hz		7		nV/√Hz

[1] All static performance tests (except I_{OUT}x) are performed in a closed-loop system using an external precision OP177 I-to-V converter amplifier. The AD5544 R_{FB} terminal is tied to the amplifier output. Typical values represent average readings measured at 25°C.
[2] These parameters are guaranteed by design and not subject to production testing.
[3] All input control signals are specified with $t_R = t_F$ = 2.5 ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V.
[4] All ac characteristic tests are performed in a closed-loop system using an AD8038 I-to-V converter amplifier.

TIMING DIAGRAMS

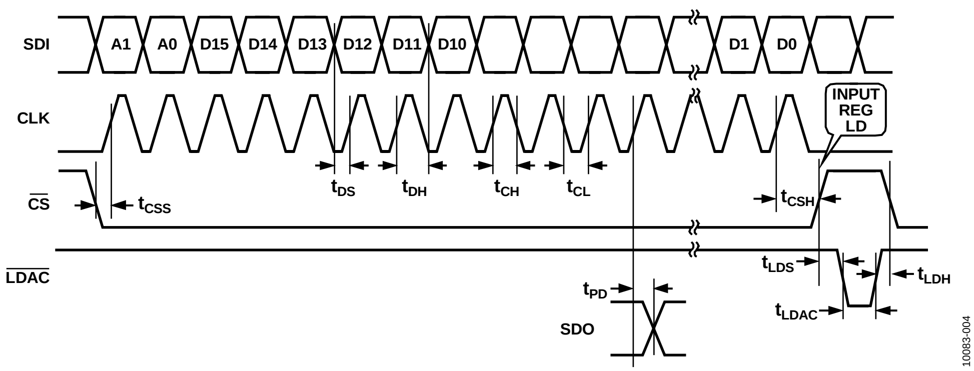


Figure 2. Timing Diagram

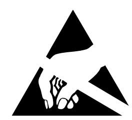
ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
V_{DD} to GND	−0.3 V, +8 V
V_{SS} to GND	+0.3 V, −7 V
$V_{REF}x$ to GND	−18 V, +18 V
Logic Input and Output to GND	−0.3 V, +8 V
$V(I_{OUT}x)$ to GND	−0.3 V, V_{DD} + 0.3 V
$A_{GND}x$ to DGND	−0.3 V, +0.3 V
Input Current to Any Pin Except Supplies	±50 mA
Package Power Dissipation	$(T_J \max - T_A)/\theta_{JA}$
Thermal Resistance	θ_{JA}
28-Lead SSOP	100°C/W
32-Lead LFCSP	32.5°C/W
Maximum Junction Temperature (T_J Max)	150°C
Operating Temperature Range, Enhanced Product (EP Version)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	
Vapor Phase, 60 Sec	215°C
Infrared, 15 Sec	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

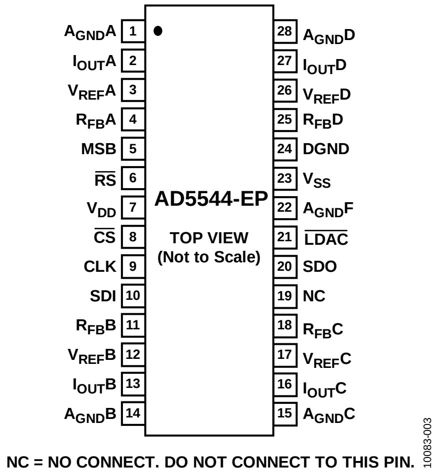


Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$A_{GND}A$	DAC A Analog Ground.
2	$I_{OUT}A$	DAC A Current Output.
3	$V_{REF}A$	DAC A Reference Voltage Input Terminal. Establishes DAC A full-scale output voltage. This pin can be tied to the V_{DD} pin.
4	$R_{FB}A$	Establish the voltage output for DAC A by connecting to an external amplifier output.
5	MSB	MSB Pin. Set pin during a reset pulse ($\overline{RS}$) or at system power-on if tied to ground or V_{DD}.
6	$\overline{RS}$	Reset Pin, Active Low Input. Input registers and DAC registers are set to all 0s or half-scale code, determined by the voltage on the MSB pin. Register data = 0x0000 when MSB = 0.
7	V_{DD}	Positive Power Supply Input. Specified range of operation: 5 V ± 10%.
8	$\overline{CS}$	Chip Select, Active Low Input. Disables shift register loading when high. Transfers serial register data to the input register when $\overline{CS}$/$\overline{LDAC}$ returns high. Does not affect $\overline{LDAC}$ operation.
9	CLK	Clock Input. Positive edge clocks data into the shift register.
10	SDI	Serial Data Input. Input data loads directly into the shift register.
11	$R_{FB}B$	Establish the voltage output for DAC B by connecting to an external amplifier output.
12	$V_{REF}B$	DAC B Reference Voltage Input Terminal. Establishes DAC B full-scale output voltage. This pin can be tied to the V_{DD} pin.
13	$I_{OUT}B$	DAC B Current Output.
14	$A_{GND}B$	DAC B Analog Ground.
15	$A_{GND}C$	DAC C Analog Ground.
16	$I_{OUT}C$	DAC C Current Output.
17	$V_{REF}C$	DAC C Reference Voltage Input Terminal. Establishes DAC C full-scale output voltage. This pin can be tied to the V_{DD} pin.
18	$R_{FB}C$	Establish the voltage output for DAC C by connecting to an external amplifier output.
19	NC	No Connect. Do not connect to this pin.
20	SDO	Serial Data Output. Input data loads directly into the shift register. Data appears at SDO at 19 clock pulses for the AD5544-EP after input at the SDI pin.
21	$\overline{LDAC}$	Load DAC Register Strobe, Level Sensitive Active Low. Transfers all input register data to DAC registers. Asynchronous active low input.
22	$A_{GND}F$	High Current Analog Force Ground.
23	V_{SS}	Negative Bias Power Supply Input. Specified range of operation: −5.5 V to +0.3 V.
24	DGND	Digital Ground Pin.
25	$R_{FB}D$	Establish the voltage output for DAC D by connecting to an external amplifier output.

Pin No.	Mnemonic	Description
26	$V_{REF}D$	DAC D Reference Voltage Input Terminal. Establishes DAC D full-scale output voltage. This pin can be tied to the V_{DD} pin.
27	$I_{OUT}D$	DAC D Current Output.
28	$A_{GND}D$	DAC D Analog Ground.

TYPICAL PERFORMANCE CHARACTERISTICS

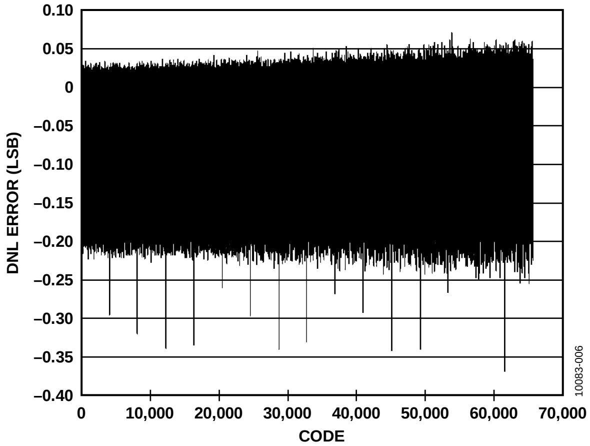


Figure 4. DNL Error vs. Code, T_A = 25°C

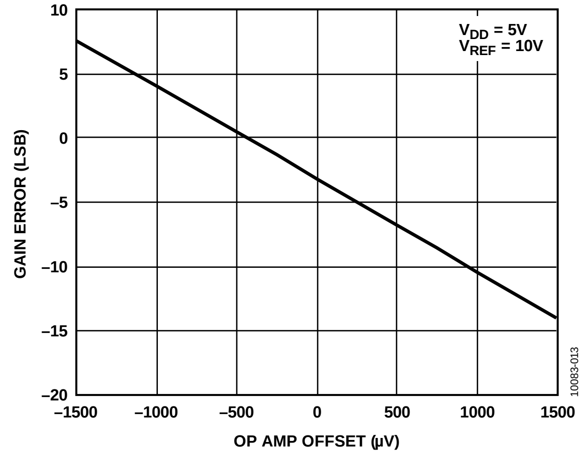


Figure 7. Gain Error vs. Op Amp Offset

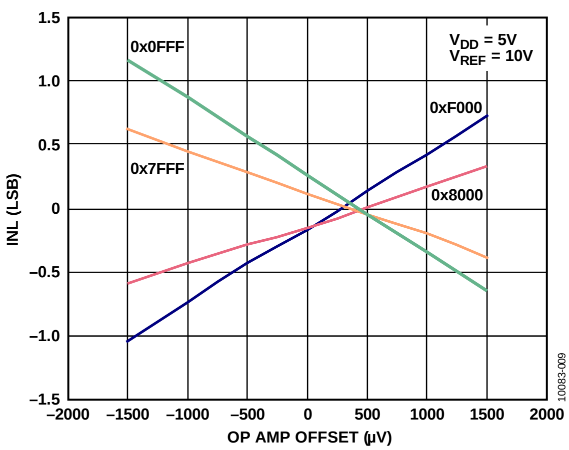


Figure 5. INL Error vs. Op Amp Offset

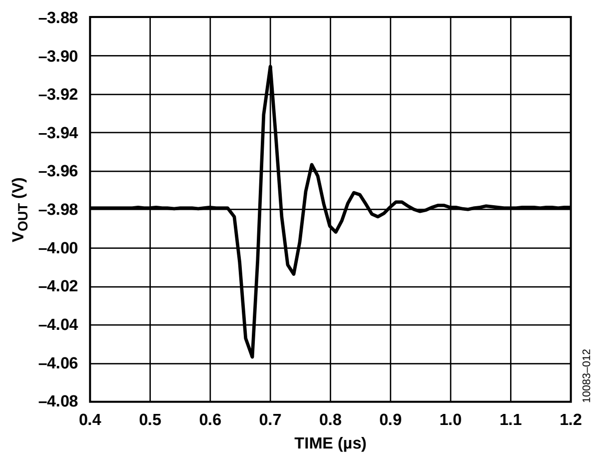


Figure 8. Midscale Transition

Figure 6. DNL Error vs. Op Amp Offset

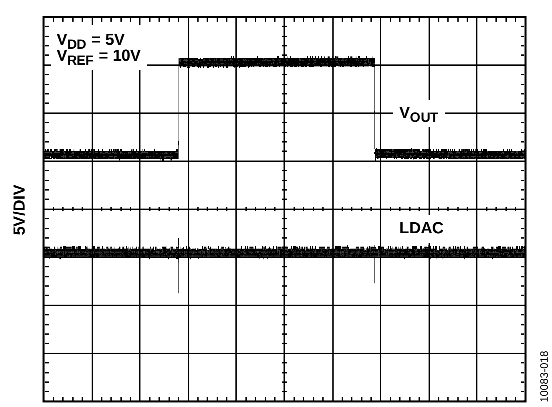


Figure 9. Large Signal Settling Time

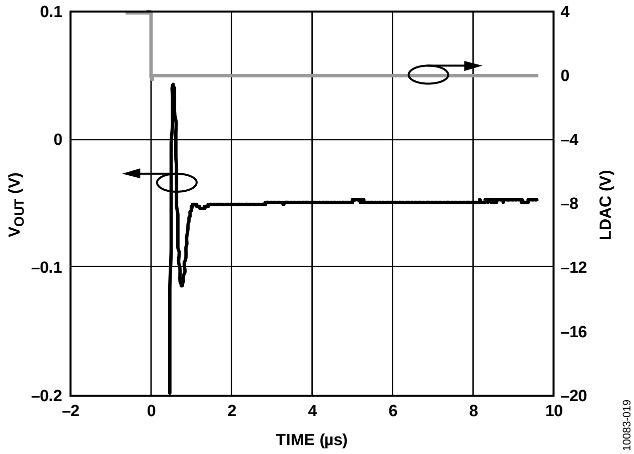


Figure 10. Small Signal Settling Time

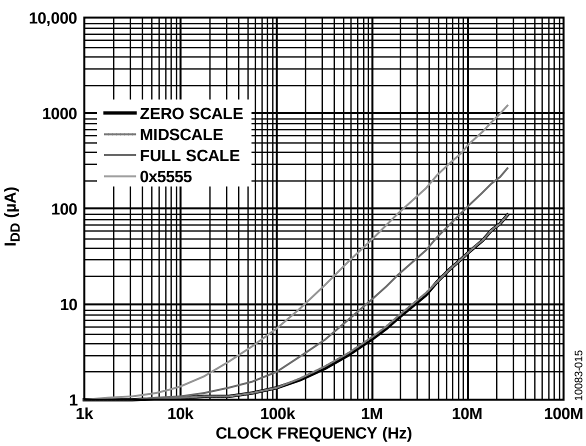


Figure 11. Power Supply Current vs. Clock Frequency

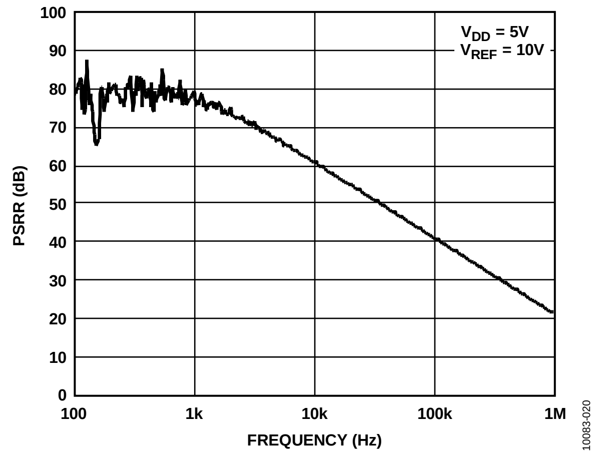


Figure 12. Power Supply Rejection vs. Frequency

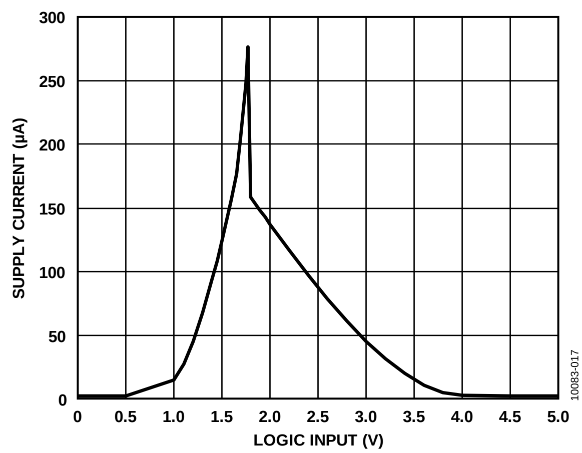


Figure 13. Power Supply Current vs. Logic Input Voltage

OUTLINE DIMENSIONS

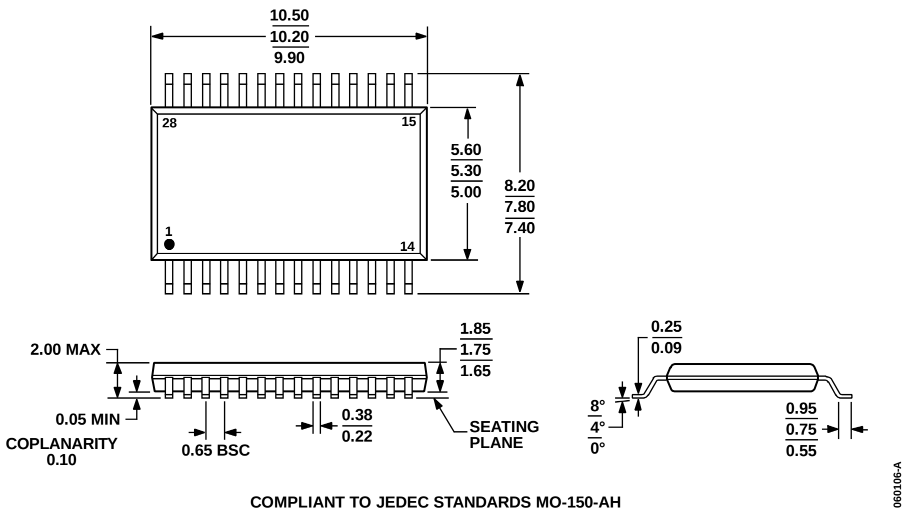


Figure 4. 28-Lead Shrink Small Outline Package [SSOP]
(RS-28)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Resolution (Bits)	INL LSB	DNL LSB	Temperature Range	Package Description	Package Option
AD5544SRS-EP	16	±1.5	±1.5	−55°C to +125°C	28-Lead Shrink Small Outline Package [SSOP]	RS-28

NOTES

NOTES

Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

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Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

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На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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