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November 2013

## **FDB035AN06A0**

# N-Channel PowerTrench<sup>®</sup> MOSFET 60 V, 80 A, 3.5 m $\Omega$

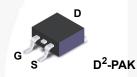
#### **Features**

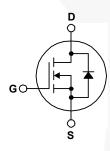
- $R_{DS(on)}$  = 3.2 m $\Omega$  ( Typ.) @  $V_{GS}$  = 10 V,  $I_D$  = 80 A
- $Q_{G(tot)}$  = 95 nC ( Typ.) @  $V_{GS}$  = 10 V
- · Low Miller Charge
- Low Q<sub>rr</sub> Body Diode
- UIS Capability (Single Pulse and Repetitive Pulse)

Formerly developmental type 82584

#### **Applications**

- Synchronous Rectification for ATX / Server / Telecom PSU
- · Battery Protection Circuit
- · Motor drives and Uninterruptible Power Supplies





### MOSFET Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted

Symbol	Parameter	FDB035AN06A0	Unit
V <sub>DSS</sub>	Drain to Source Voltage	60	V
V <sub>GS</sub>	Gate to Source Voltage	±20	V
	Drain Current		
$I_D$	Continuous (T <sub>C</sub> < 153°C, V <sub>GS</sub> = 10V)	80	Α
	Continuous ( $T_{amb} = 25^{\circ}C$ , $V_{GS} = 10V$ , with $R_{\theta JA} = 43^{\circ}C/W$ )	22	Α
	Pulsed	Figure 4	А
E <sub>AS</sub>	Single Pulse Avalanche Energy (Note 1)	625	mJ
P <sub>D</sub>	Power dissipation	310	W
	Derate above 25°C	2.07	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature	-55 to 175	°C

#### **Thermal Characteristics**

$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.48	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max. (Note 2)	62	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, 1in <sup>2</sup> copper pad area, Max.	43	°C/W

Device I	Marking	Device	Package	Reel Size	Tape \	Width	Quar	ntity
FDB035AN06A0 FDB035AN06A0		D²-PAK	330 mm	24 mm		800 units		
Electric	al Char	racteristics T <sub>C</sub> = 25°C	unless otherwise	noted				
Symbol		Parameter	Test C	onditions	Min	Тур	Max	Unit
Off Chara	cteristic				-	- 71-		
B <sub>VDSS</sub>	1	Source Breakdown Voltage	I <sub>D</sub> = 250μA, V	<sub>GS</sub> = 0V	60	_	-	V
VD33	2.s to obtained broadwarf voltage		V <sub>DS</sub> = 50V		-	-	1	
I <sub>DSS</sub>	Zero Gate	e Voltage Drain Current	$V_{GS} = 0V$	$T_{\rm C} = 150^{\rm o}{\rm C}$	-	-	250	μА
I <sub>GSS</sub>	Gate to S	Source Leakage Current	V <sub>GS</sub> = ±20V		-	-	±100	nA
On Chara	cteristic	·s						
V <sub>GS(TH)</sub>	Gate to S	Source Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub>	= 250µA	2	-	4	V
00(111)	-//		I <sub>D</sub> = 80A, V <sub>GS</sub>		-	0.0032	0.0035	
	Drain to C	Course On Besistance	I <sub>D</sub> = 40A, V <sub>GS</sub>		-	0.0044	0.0066	Ω
r <sub>DS(ON)</sub>	S(ON) Drain to Source On Resistance		I <sub>D</sub> = 80A, V <sub>GS</sub> T <sub>J</sub> = 175°C		-	0.0065	0.0071	22
Dynamic	Characte	eristics	,					
C <sub>ISS</sub>	Input Cap		1		-	6400	-	pF
C <sub>OSS</sub>	<del></del>	apacitance	$V_{DS} = 25V, V_{GS} = 0V,$		-	1123	-	pF
C <sub>RSS</sub>		Transfer Capacitance	f = 1MHz		-	367	-	pF
Q <sub>g(TOT)</sub>		e Charge at 10V	V <sub>GS</sub> = 0V to 1	0V		95	124	nC
Q <sub>g(TH)</sub>	Threshold	d Gate Charge	V <sub>GS</sub> = 0V to 2		-	12	15	nC
Q <sub>gs</sub>	Gate to S	Source Gate Charge		I <sub>D</sub> = 80A	-	30	-	nC
Q <sub>gs2</sub>	Gate Cha	arge Threshold to Plateau		$I_g = 1.0 \text{mA}$	-	18	-	nC
Q <sub>gd</sub>	Gate to D	rain "Miller" Charge			-	24	-	nC
	g Charac	eteristics (V <sub>GS</sub> = 10V)						
t <sub>ON</sub>	Turn-On				- /	-	163	ns
t <sub>d(ON)</sub>	Turn-On [	Delay Time	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		-	ns		
t <sub>r</sub>	Rise Time	е			-	93	-	ns
t <sub>d(OFF)</sub>	Turn-Off [	Delay Time			-	38	-	ns
t <sub>f</sub>	Fall Time				-	13	-	ns
t <sub>OFF</sub>	Turn-Off	Time	75				ns	
	urce Dio	de Characteristics						
			I <sub>SD</sub> = 80A		-	-	1.25	V
V <sub>SD</sub>	Source to	Drain Diode Voltage	I <sub>SD</sub> = 40A				1.0	V
t <sub>rr</sub>	Reverse I	Recovery Time	$I_{SD} = 75A, dI_{S}$	1/4	_	38	ns	

# $Q_{RR}$

Notes:
1: Starting T<sub>J</sub> = 25°C, L = 0.255mH, I<sub>AS</sub> = 70A.
2: Pulse Width = 100s

Reverse Recovered Charge

 $I_{SD} = 75A$ ,  $dI_{SD}/dt = 100A/\mu s$ 

39

nC

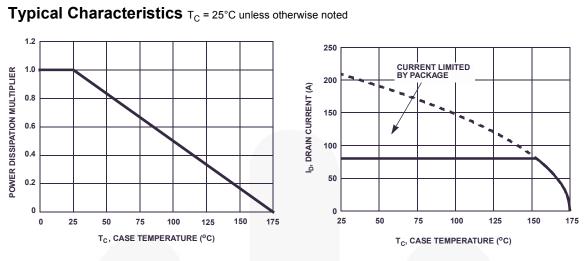


Figure 1. Normalized Power Dissipation vs
Ambient Temperature

Figure 2. Maximum Continuous Drain Current vs Case Temperature

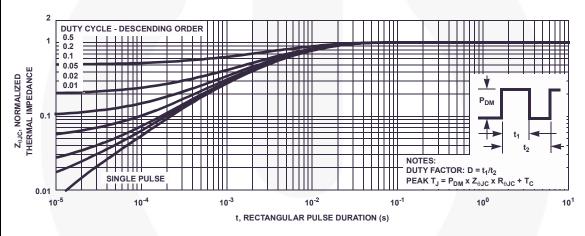


Figure 3. Normalized Maximum Transient Thermal Impedance

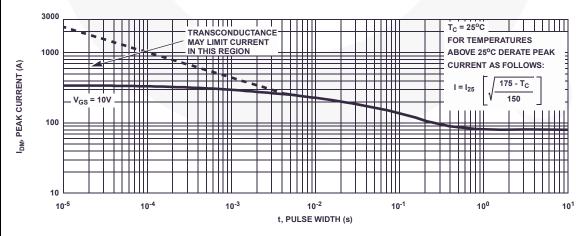
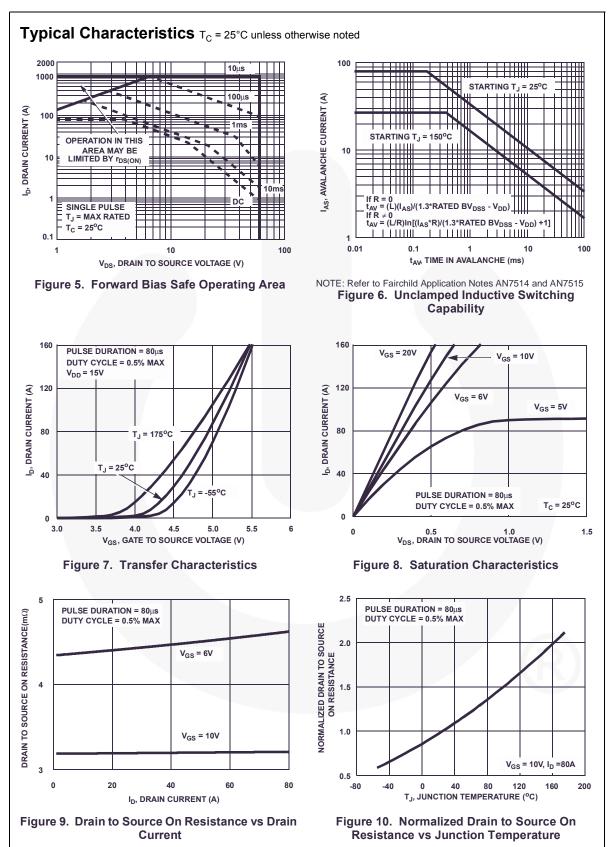


Figure 4. Peak Current Capability



## Typical Characteristics T<sub>C</sub> = 25°C unless otherwise noted

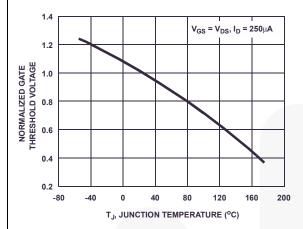


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

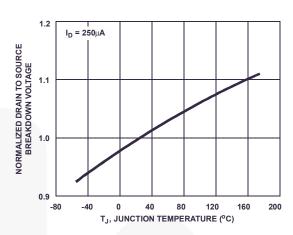


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

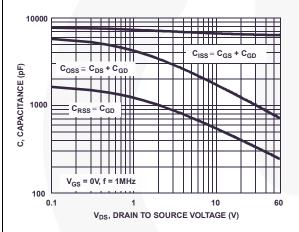


Figure 13. Capacitance vs Drain to Source Voltage

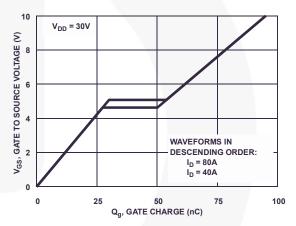


Figure 14. Gate Charge Waveforms for Constant Gate Current

### **Test Circuits and Waveforms**

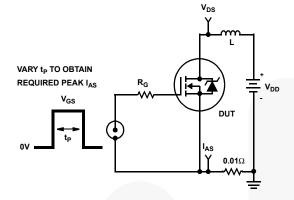


Figure 15. Unclamped Energy Test Circuit

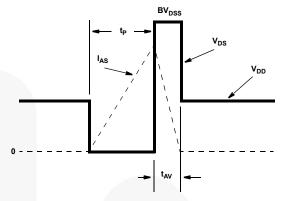


Figure 16. Unclamped Energy Waveforms

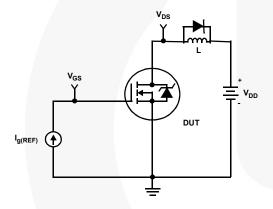


Figure 17. Gate Charge Test Circuit

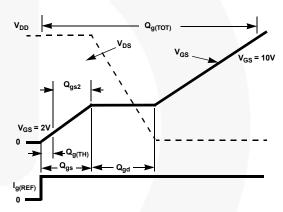


Figure 18. Gate Charge Waveforms

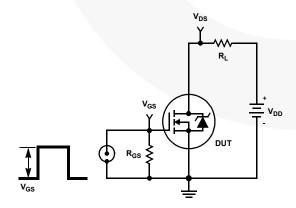


Figure 19. Switching Time Test Circuit

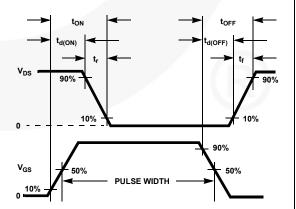


Figure 20. Switching Time Waveforms

### Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature,  $T_{JM}$ , and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation,  $P_{DM}$ , in an application. Therefore the application's ambient temperature,  $T_A$  (°C), and thermal resistance  $R_{\theta JA}$  (°C/W) must be reviewed to ensure that  $T_{JM}$  is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \tag{EQ. 1}$$

In using surface mount devices such as the TO-263 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of  $P_{DM}$  is complex and influenced by many factors:

- Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
- The number of copper layers and the thickness of the board.
- 3. The use of external heat sinks.
- 4. The use of thermal vias.
- 5. Air flow and board orientation.
- 6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 21 defines the  $R_{\theta JA}$  for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2 or 3. Equation 2 is used for copper area defined in inches square and equation 3 is for area in centimeters square. The area, in square inches or square centimeters is the top copper area including the gate and source pads.

$$R_{\theta JA} = 26.51 + \frac{19.84}{(0.262 + Area)}$$
 (EQ. 2)

Area in Inches Squared

$$R_{\theta JA} = 26.51 + \frac{128}{(1.69 + Area)}$$
 (EQ. 3)

Area in Centimeters Squared

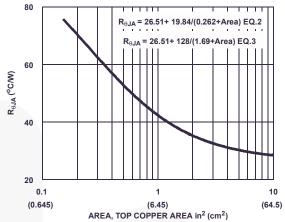
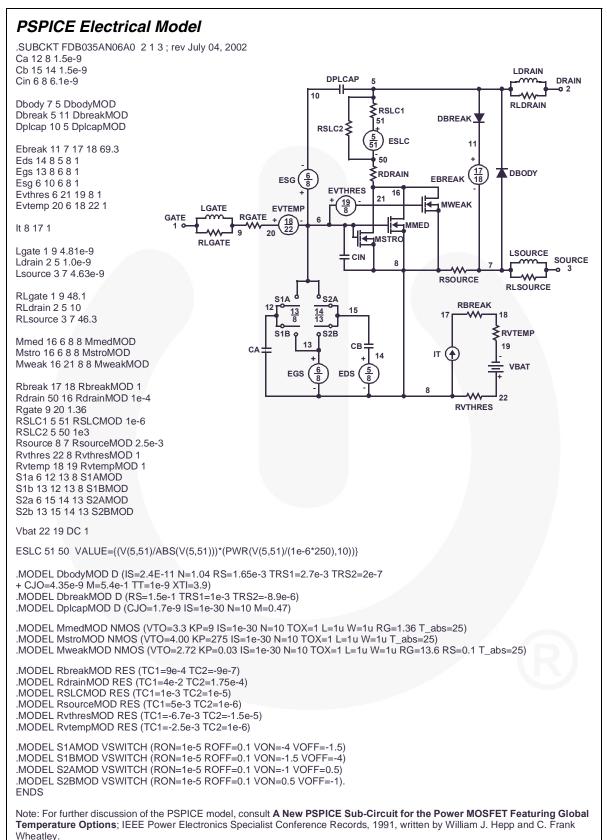


Figure 21. Thermal Resistance vs Mounting Pad Area



#### SABER Electrical Model rev July 4, 2002 template FDB035AN06A0 n2,n1,n3 = m\_temp electrical n2,n1,n3 number m\_temp=25 var i iscl dp..model dbodymod = (isl=2.4e-11,nl=1.04,rs=1.65e-3,trs1=2.7e-3,trs2=2e-7,cjo=4.35e-9,m=5.4e-1,tt=1e-9,xti=3.9) dp..model dbreakmod = (rs=1.5e-1,trs1=1e-3,trs2=-8.9e-6) dp..model dplcapmod = (cjo=1.7e-9,isl=10e-30,nl=10,m=0.47) $m..model mmedmod = (type=_n, vto=3.3, kp=9, is=1e-30, tox=1)$ m..model mstrongmod = $(type=_n, vto=4.00, kp=275, is=1e-30, tox=1)$ LDRAIN m..model mweakmod = (type=\_n,vto=2.72,kp=0.03,is=1e-30, tox=1,rs=0.1) DRAIN sw\_vcsp..model s1amod = (ron=1e-5,roff=0.1,von=-4,voff=-1.5) sw\_vcsp..model s1bmod = (ron=1e-5,roff=0.1,von=-1.5,voff=-4) RLDRAIN sw\_vcsp..model s2amod = (ron=1e-5,roff=0.1,von=-1,voff=0.5) RSLC1 sw\_vcsp..model s2bmod = (ron=1e-5,roff=0.1,von=0.5,voff=-1) RSLC2 € c.ca n12 n8 = 1.5e-9ISCL c.cb n15 n14 = 1.5e-9c.cin n6 n8 = 6.1e-9DBREAK RDRAIN dp.dbody n7 n5 = model=dbodymod ESG DBODY dp.dbreak n5 n11 = model=dbreakmod **EVTHRES** dp.dplcap n10 n5 = model=dplcapmod (<u>19</u>) MWEAK **LGATE EVTEMP** RGATE spe.ebreak n11 n7 n17 n18 = 69.3 EBREAK MMFD 20 spe.eds n14 n8 n5 n8 = 1 **RLGATE** spe.egs n13 n8 n6 n8 = 1 LSOURCE spe.esg n6 n10 n6 n8 = 1 CIN SOURCE spe.evthres n6 n21 n19 n8 = 1 spe.evtemp n20 n6 n18 n22 = 1 **RSOURCE** RLSOURCE i.it n8 n17 = 1RBREAK 17 18 I.lgate n1 n9 = 4.81e-9RVTEMP I.ldrain n2 n5 = 1.0e-9I.lsource n3 n7 = 4.63e-9СВ 19 CA ΙT 14 res.rlgate n1 n9 = 48.1 **EGS** res.rldrain n2 n5 = 10res risource n3 n7 = 46.3**RVTHRES** m.mmed n16 n6 n8 n8 = model=mmedmod, temp=m\_temp, l=1u, w=1u m.mstrong n16 n6 n8 n8 = model=mstrongmod, temp=m\_temp, l=1u, w=1u m.mweak n16 n21 n8 n8 = model=mweakmod, temp=m\_temp, l=1u, w=1u res.rbreak n17 n18 = 1, tc1=9e-4,tc2=-9e-7 res.rdrain n50 n16 = 1e-4, tc1=4e-2,tc2=1.75e-4 res.rgate n9 n20 = 1.36 res.rslc1 n5 n51 = 1e-6, tc1=1e-3,tc2=1e-5 res.rslc2 n5 n50 = 1e3res.rsource n8 n7 = 2.5e-3, tc1=5e-3,tc2=1e-6 res.rvthres n22 n8 = 1, tc1=-6.7e-3,tc2=-1.5e-5 res.rvtemp n18 n19 = 1, tc1=-2.5e-3,tc2=1e-6 sw\_vcsp.s1a n6 n12 n13 n8 = model=s1amod sw\_vcsp.s1b n13 n12 n13 n8 = model=s1bmod sw\_vcsp.s2a n6 n15 n14 n13 = model=s2amod sw\_vcsp.s2b n13 n15 n14 n13 = model=s2bmod v.vbat n22 n19 = dc=1 equations { i (n51->n50) +=iscl iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))\*((abs(v(n5,n51)\*1e6/250))\*\*10))

## SPICE Thermal Model JUNCTION th REV 23 July 4, 2002 FDB035AN06A0T CTHERM1 TH 6 6.45e-3 CTHERM2 6 5 3e-2 CTHERM3 5 4 1.4e-2 RTHERM1 CTHERM4 4 3 1.65e-2 CTHERM1 CTHERM5 3 2 4.85e-2 CTHERM6 2 TL 1e-1 RTHERM1 TH 6 3.24e-3 RTHERM2 6 5 8.08e-3 RTHERM3 5 4 2.28e-2 RTHERM4 4 3 1e-1 RTHERM2 CTHERM2 RTHERM5 3 2 1.1e-1 RTHERM6 2 TL 1.4e-1 SABER Thermal Model RTHERM3 CTHERM3 SABER thermal model FDB035AN06A0T template thermal\_model th tl thermal\_c th, tl ctherm.ctherm1 th 6 =6.45e-3 ctherm.ctherm2 6 5 = 3e-2 ctherm.ctherm3 5 4 = 1.4e-2 ctherm.ctherm4 4 3 = 1.65e-2 RTHERM4 CTHERM4 ctherm.ctherm5 3 2 =4.85e-2 ctherm.ctherm6 2 tl =1e-1 rtherm.rtherm1 th 6 =3.24e-3 3 rtherm.rtherm2 6 5 = 8.08e-3 rtherm.rtherm3 5 4 = 2.28e-2 rtherm.rtherm4 4 3 = 1e-1 rtherm.rtherm5 3 2 = 1.1e-1 rtherm.rtherm6 2 tl=1.4e-1 RTHERM5 CTHERM5 2 RTHERM6 CTHERM6 CASE

#### **Mechanical Dimensions**

# TO-263 2L (D<sup>2</sup>PAK)

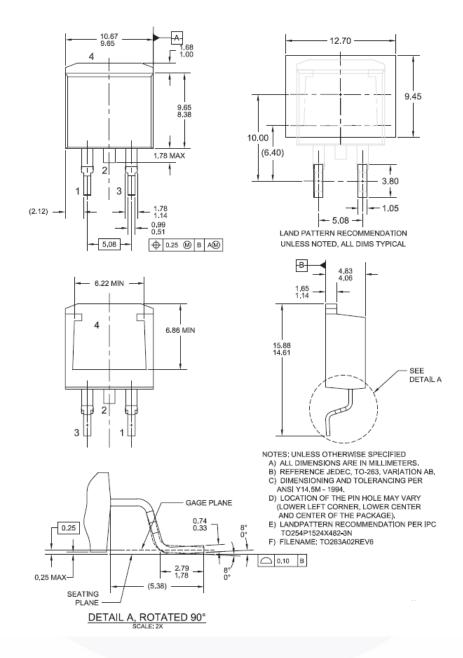


Figure 22. 2LD, TO263, Surface Mount

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Dimension in Millimeters





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FastvCore™ FETBench™ FPS™

F-PFS™ FRFET® Global Power Resource<sup>SM</sup>

GreenBridge™ Green FPS™

Green FPS™ e-Series™

G*max*™ GTO™ IntelliMAX™ ISOPLANAR™

Marking Small Speakers Sound Louder

and Better™ MegaBuck™ MICROCOUPLER™ MicroFET™ MicroPak™

MicroPak2™ MillerDrive™ MotionMax™ mWSaver® OptoHiT™ OPTOLOGIC® OPTOPLANAR® PowerTrench® PowerXS™

Programmable Active Droop™

**QFET** QS™ Quiet Series™ RapidConfigure™

Saving our world, 1mW/W/kW at a time™ SignalWise™

SmartMax™ SMART START™

Solutions for Your Success™

STEALTH™ SuperFET® SuperSOT™-3 SuperSOT™-6 SuperSOT™-8

SupreMOS® SvncFET™

Sync-Lock™ SYSTEM ®\* TinyBoost<sup>®</sup> TinyBuck<sup>®</sup> TinyCalc™ TinyLogic<sup>®</sup> TINYOPTO™ TinvPower™ TinyPWM™ TinyWire™ TranSiC™ TriFault Detect™ TRUECURRENT®\* μSerDes™

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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