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February 1997 Revised August 2004

### NC7ST00

# TinyLogic® HST 2-Input NAND Gate

### **General Description**

The NC7ST00 is a single 2-Input high performance CMOS NAND Gate, with TTL-compatible inputs. Advanced Silicon Gate CMOS fabrication assures high speed and low power circuit operation. ESD protection diodes inherently guard both inputs and output with respect to the  $\rm V_{CC}$  and GND rails. High gain circuitry offers high noise immunity and reduced sensitivity to input edge rate. The TTL-compatible inputs facilitate TTL to NMOS/CMOS interfacing. Device performance is similar to MM74HCT but with 1/2 the output current drive of HC/HCT.

### **Features**

- Space saving SOT23 or SC70 5-lead package
- Ultra small MicroPak™ leadless package
- High Speed;  $t_{PD}$  < 7 ns typ,  $V_{CC}$  = 5V,  $C_L$  = 15 pF
- $\blacksquare$  Low Quiescent Power;  $I_{CC} < 1~\mu\text{A typ},~V_{CC} = 5.5\text{V}$
- Balanced Output Drive; 2 mA I<sub>OL</sub>, -2 mA I<sub>OH</sub>
- TTL-compatible inputs

### **Ordering Code:**

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7ST00M5X	MA05B	8S00	5-Lead SOT23, JEDEC MO-178, 1.6mm	3k Units on Tape and Reel
NC7ST00P5X	MAA05A	T00	5-Lead SC70, EIAJ SC-88a, 1.25mm Wide	3k Units on Tape and Reel
NC7ST00L6X	MAC06A	E3	6-Lead MicroPak, 1.0mm Wide	5k Units on Tape and Reel

### **Logic Symbol**



### **Pin Descriptions**

Pin Names	Description
A, B	Inputs
Y	Output
NC	No Connect

### **Function Table**

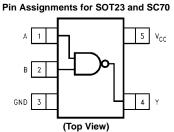
$$Y = \overline{AB}$$

Inp	Output			
Α	A B			
L	L	Н		
L	Н	Н		
Н	L	Н		
Н	Н	L		

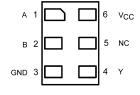
H = HIGH Logic Level L = LOW Logic Level

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### **Connection Diagrams**



#### Pad Assignments for MicroPak



(Top Thru View)

### **Absolute Maximum Ratings**(Note 1)

# Recommended Operating Conditions (Note 2)

$$\begin{split} &V_{\text{IN}} < -0.5 \text{V} & -20 \text{ mA} \\ &V_{\text{IN}} \ge V_{\text{CC}} + 0.5 \text{V} & +20 \text{ mA} \\ &\text{DC Input Voltage } V_{\text{IN}} & -0.5 \text{V to } V_{\text{CC}} + 0.5 \text{V} \end{split}$$

DC Output Diode Current (I<sub>OK</sub>)

$$\begin{split} & V_{\text{OUT}} < -0.5 \text{V} & -20 \text{ mA} \\ & V_{\text{OUT}} > V_{\text{CC}} + 0.5 \text{V} & +20 \text{ mA} \end{split}$$

Output Voltage ( $V_{OUT}$ ) -0.5V to  $V_{CC} + 0.5V$ 

DC Output Source or

Sink Current ( $I_{OUT}$ )  $\pm 12.5 \text{ mA}$ 

DC V<sub>CC</sub> or Ground Current per

Supply Pin ( $I_{CC}$  or  $I_{GND}$ )  $\pm 25$  mA Storage Temperature ( $T_{STG}$ )  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ 

Junction Temperature (T<sub>J</sub>) 150°C

Lead Temperature (T<sub>L</sub>);

(Soldering, 10 seconds) 260°C

Power Dissipation (PD) @ +85°C

SOT23-5 200 mW SC70-5 150 mW Supply Voltage 4.5V to 5.5V Input Voltage  $(V_{IN})$  0.0V to  $V_{CC}$  Output Voltage  $(V_{OUT})$  0V to  $V_{CC}$  Operating Temperature  $(T_A)$   $-40^{\circ}C$  to  $+85^{\circ}C$ 

Input Rise and Fall Time  $(t_r, t_f)$ 

 $V_{CC} = 5.0V$  0 to 500 ns

Thermal Resistance ( $\theta_{JA}$ )

SOT23-5 300°C/W

SC70-5 425°C/W

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the design is reliable over its power supply, temperature, and output/input loading variables Fairchild does not recommend operation of circuits outside the databook specifications.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

#### **DC Electrical Characteristics**

Symbol	Parameter	v <sub>cc</sub>	T <sub>A</sub> = +25°C			$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		Units	Conditions	
Cymbol	raiailletei	(V)	Min	Тур	Max	Min	Max	Ullits	Conditions	
V <sub>IH</sub>	HIGH Level Input Voltage	4.5-5.5	2.0			2.0		V		
V <sub>IL</sub>	LOW Level Input Voltage	4.5-5.5			8.0		0.8	V		
V <sub>OH</sub>	HIGH Level Output Voltage	4.5	4.4	4.5		4.4			$I_{OH} = -20 \mu A$	
		4.5	4.18	4.35		4.13		V	$I_{OH} = -2 \text{ mA}$	
									$V_{IN} = V_{IL}$	
V <sub>OL</sub>	LOW Level Output Voltage	4.5		0	0.1		0.1		$I_{OL} = 20 \mu A$	
		4.5		0.10	0.26		0.33	V	I <sub>OL</sub> = 2 mA	
									$V_{IN} = V_{IH}$	
I <sub>IN</sub>	Input Leakage Current	5.5			±0.1		±1.0	μΑ	$0 \le V_{IN} \le 5.5V$	
I <sub>CC</sub>	Quiescent Supply Current	5.5			1.0		10.0	μΑ	$V_{IN} = V_{CC}$ or GND	
I <sub>CCT</sub>	I <sub>CC</sub> per Input	CC per Input 5.5		2.0		2.9		mA	One Input $V_{IN} = 0.5V$ or 2.4V,	
									Other Input V <sub>CC</sub> or GND	

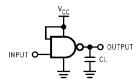
## **AC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ $T_A = +25^{\circ}C$		$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		Units	Conditions	Figure		
		(V)	Min	Тур	Max	Min	Max	Units	Conditions	Number
t <sub>PLH</sub> ,	Propagation Delay	5.0		3.4	12				C <sub>I</sub> = 15 pF	
t <sub>PHL</sub>		ľ		6.3	17				C <sub>L</sub> = 15 pr	
		4.5		6.0	16		20	ns		Figures
				11.5	27		31	_	C <sub>L</sub> = 50 pF	1, 3
		5.5		4.1	14		18	1		
				11.2	26		30			
t <sub>TLH</sub> ,	Output Transition Time	5.0		4	10			ns	C <sub>L</sub> = 15 pF	_
$t_{THL}$	THL			11	25		31	ns	C <sub>I</sub> = 50 pF	Figures 1, 3
		5.5		10	21		26	115	C <sub>L</sub> = 50 pr	., -
C <sub>IN</sub>	Input Capacitance	Open		2	10			рF		
C <sub>PD</sub>	Power Dissipation Capacitance	5.0		6				pF	(Note 3)	Figure 2

Note 3: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current. Current consumption (I<sub>CCD</sub>) at no output loading and operating at 50% duty cycle. (See Figure 2). CPD is related to I<sub>CCD</sub> dynamic operating current by the expression:

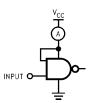
I<sub>CCD</sub> = (C<sub>PD</sub>)(V<sub>CC</sub>)(f<sub>IN</sub>) + (I<sub>CCStatic</sub>).

### **AC Loading and Waveforms**



 ${
m C_L}$  includes load and stray capacitance Input PRR = 1.0 MHz;  ${
m t_W}$  = 500 ns

FIGURE 1. AC Test Circuit



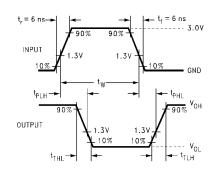


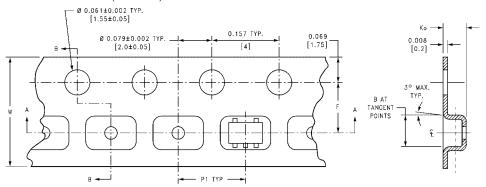
FIGURE 3. AC Waveforms

# **Tape and Reel Specification**

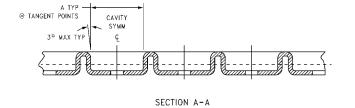
### TAPE FORMAT

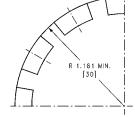
Package	Tape	Number	Cavity	Cover Tape
Designator	Section	Cavities	Status	Status
	Leader (Start End)	125 (typ)	Empty	Sealed
M5X, P5X	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

### TAPE DIMENSIONS inches (millimeters)



DIRECTION OF FEED SECTION B-B

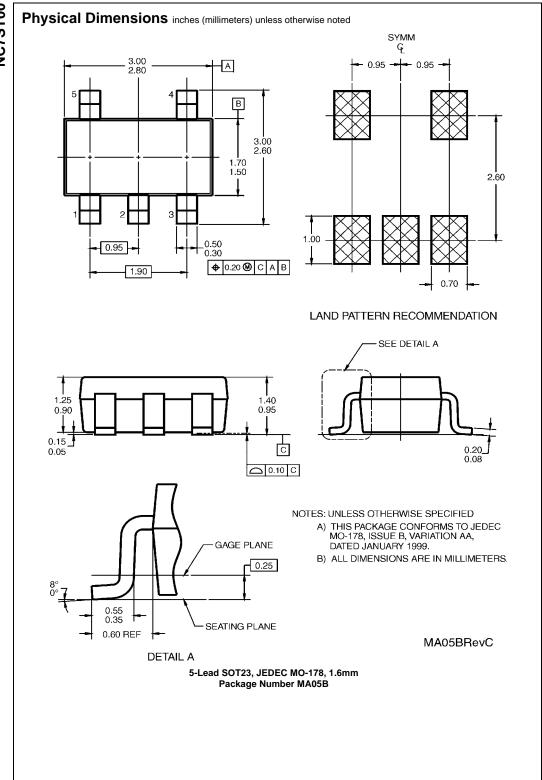


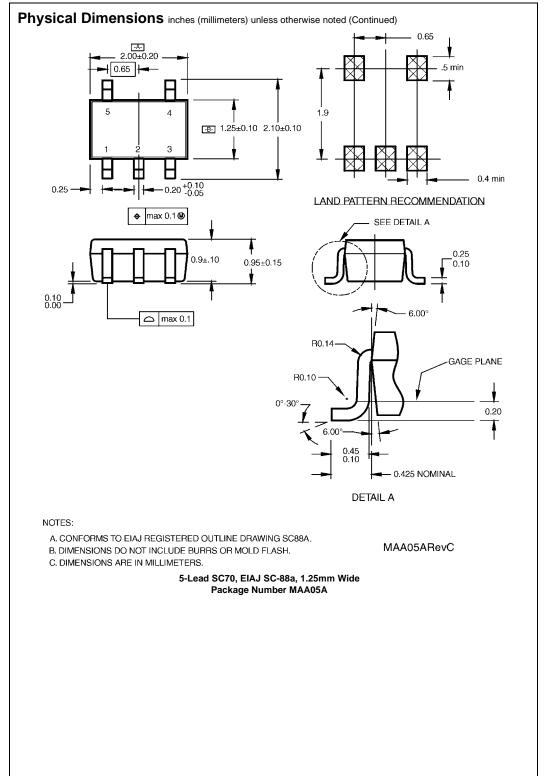


BEND RADIUS NOT TO SCALE

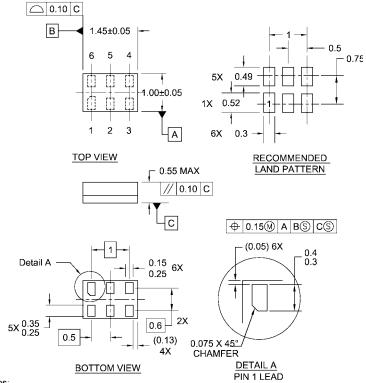
Package	Tape Size	DIM A	DIM B	DIM F	DIM K <sub>o</sub>	DIM P1	DIM W
SC70-5	8 mm	0.093	0.096	$0.138 \pm 0.004$	$0.053 \pm 0.004$	0.157	$0.315 \pm 0.004$
		(2.35)	(2.45)	$(3.5 \pm 0.10)$	$(1.35 \pm 0.10)$	(4)	(8 ± 0.1)
SOT23-5	8 mm	0.130	0.130	$0.138 \pm 0.002$	$0.055 \pm 0.004$	0.157	$0.315 \pm 0.012$
		(3.3)	(3.3)	$(3.5 \pm 0.05)$	$(1.4 \pm 0.11)$	(4)	$(8 \pm 0.3)$

#### Tape and Reel Specification (Continued) TAPE FORMAT for MicroPak Package Tape Number Cavity Cover Tape Designator Section Cavities Status Status Leader (Start End) 125 (typ) Empty Sealed L6X Carrier 5000 Filled Sealed Trailer (Hub End) 75 (typ) **Empty** Sealed 2.00-1.75±0.10 В 8.00 <sup>+0.30</sup> -0.10 3.50±0.05 1.15±0.05 **-** → В◄ -ø 0.50 ±0.05 SECTION B-B DIRECTION OF FEED SCALE:10X 0.254±0.020 Г 0.70±0.05 SECTION A-A SCALE:10X **REEL DIMENSIONS** inches (millimeters) TAPE SLOT DETAIL X **DETAIL X** SCALE: 3X W1 W3 Tape В W2 Size 7.0 0.059 0.512 0.795 2.165 0.331 + 0.059/-0.000 0.567 W1 + 0.078/-0.039 8 mm (8.40 + 1.50/-0.00) (W1 + 2.00/-1.00)(177.8)(1.50)(13.00)(20.20)(55.00)(14.40)





### Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



#### Notes:

- 1. JEDEC PACKAGE REGISTRATION IS ANTICIPATED 2. DIMENSIONS ARE IN MILLIMETERS
- 3. DRAWING CONFORMS TO ASME Y14.5M-1994

MAC06ARevB

6-Lead MicroPak, 1.0mm Wide Package Number MAC06A

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### Офис по работе с юридическими лицами:

105318, г. Москва, ул. Щербаковская д. 3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru moschip.ru\_6 moschip.ru\_4 moschip.ru\_9