KSZ8061MNX/KSZ8061MNG

10Base-T/100Base-TX Physical Layer Transceiver

Revision 1.0

General Description

The KSZ8061MN is a single-chip 10Base-T/100Base-TX Ethernet physical layer transceiver for transmission and reception of data over unshielded twisted pair (UTP) cable.

The KSZ8061MN features Quiet-WIRE® internal filtering to reduce line emissions. It is ideal for applications, such as automotive or industrial networks, where stringent radiated emission limits need to be met. Quiet-WIRE can use low-cost unshielded cable, where previously only shielded cable solutions were possible. The KSZ8061MN also features enhanced immunity to environmental EM noise.

The KSZ8061MN offers the Media Independent Interface (MII) for direct connection with MII-compliant Ethernet MAC processors and switches.

It is designed to exceed Automotive AEC-Q100 and EMC requirements, and features an extended temperature range of –40°C to +105°C.

The KSZ8061MNX is supplied in a 32-lead, 5mm × 5mm QFN or WQFN package, while the KSZ8061MNG is in a 48-lead, 7mm × 7mm QFN package.

The KSZ8061RNB and KSZ8061RND devices have an RMII interface and are described in a separate datasheet.

Datasheets and support documentation are available on Micrel's website at: www.micrel.com.

Quiet-WIRE®

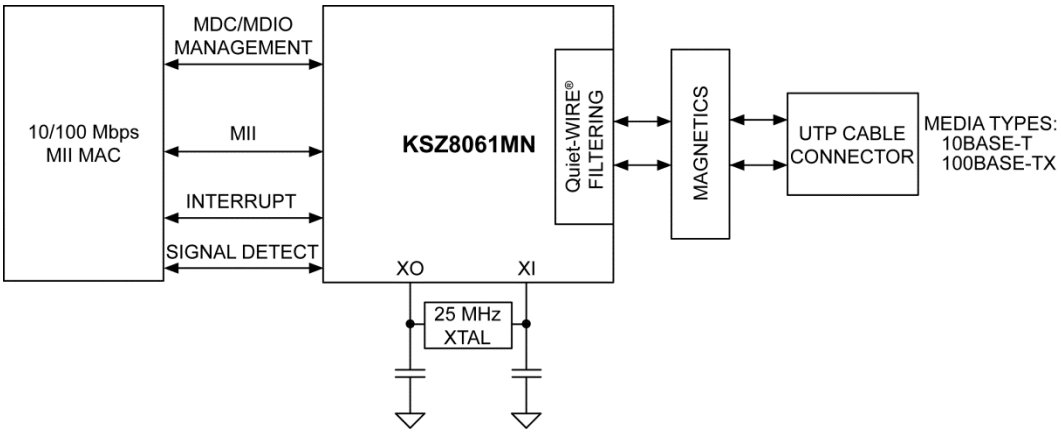
Features

- Quiet-WIRE programmable EMI filter
- MII interface with MDC/MDIO management interface for register configuration
- On-chip termination resistors for the differential pairs
- LinkMD®+ receive signal quality indicator
- Fast start-up and link
- Low-power design with IEEE 802.3az Energy Efficient Ethernet support
- Ultra-Deep Sleep standby mode: CPU or signal detect activated.
- Loopback modes for diagnostics
- Programmable interrupt output

Applications

- Industrial control
- Vehicle on-board diagnostics (OBD)
- Automotive gateways
- Camera and sensor networking
- Infotainment

Functional Diagram



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Ordering Information

Part Number	Temperature Range	Package	Lead Finish	Description
KSZ8061MNXI	–40°C to 85°C	QFN-32LD	Pb-Free	Industrial Temperature
KSZ8061MNXV[1]	–40°C to 105°C	WQFN-32LD	Pb-Free	AEC-Q100 Automotive Qualified (Extended Temperature)
KSZ8061MNGW	–40°C to 105°C	QFN-48LD	Pb-Free	Industrial Extended Temperature
KSZ8061MNX-EVAL[1]	0°C to 70°C	–	–	KSZ8061MNX Evaluation Board (with KSZ8061MNX device installed)

Note:

1. Contact factory for availability.

Revision History

Date	Change Description/Edits by:	Rev.
08/27/15	Initial release of datasheet. By T. Nelson.	1.0

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Pin Configuration – KSZ8061MNX (32-Pin Packages)

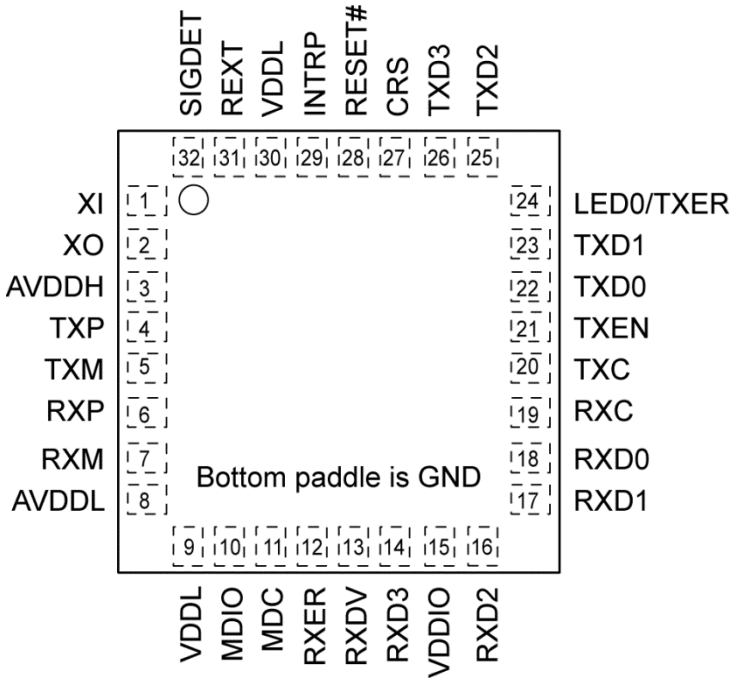


Figure 1. 32-Pin 5mm x 5mm QFN or WQFN

Pin Description – KSZ8061MNX (32-Pin Packages)

Pin Number	Pin Name	Type[2]	Pin Function
1	XI	I	Crystal/Oscillator/External Clock Input 25MHz ±50ppm. This input references the AVDDH power supply.
2	XO	O	Crystal feedback for 25MHz crystal This pin is a no connect if oscillator or external clock source is used.
3	AVDDH	Pwr	3.3V supply for analog TX drivers and XI/XO oscillator circuit.
4	TXP	I/O	Physical transmit or receive signal (+ differential) Transmit when in MDI mode; Receive when in MDI-X mode
5	TXM	I/O	Physical transmit or receive signal (– differential) Transmit when in MDI mode; Receive when in MDI-X mode
6	RXP	I/O	Physical receive or transmit signal (+ differential) Receive when in MDI mode; Transmit when in MDI-X mode
7	RXM	I/O	Physical receive or transmit signal (– differential) Receive when in MDI mode; Transmit when in MDI-X mode
8	AVDDL	Pwr	1.2V (nominal) supply for analog core
9	VDDL	Pwr	1.2V (nominal) supply for digital core
10	MDIO	Ipu/Opu	Management Interface (MIIM) Data I/O This pin has a weak pull-up, is open-drain like, and requires an external 1.0kΩ pull-up resistor.
11	MDC	Ipu	Management Interface (MIIM) Clock Input This clock pin is synchronous to the MDIO data pin.
12	RXER / QWF	Ipd/O	MII Receive Error Output Config Mode: The pull-up/pull-down value is latched as QWF at the de-assertion of reset. See Strapping Options – KSZ8061MNX (32-Pin Packages) section for details.
13	RXDV / CONFIG2	Ipd/O	MII Receive Data Valid Output Config Mode: The pull-up/pull-down value is latched as CONFIG2 at the de-assertion of reset. See Strapping Options – KSZ8061MNX (32-Pin Packages) section for details.
14	RXD3 / PHYAD0	Ipu/O	MII Receive Data Output[3][3] Config Mode: The pull-up/pull-down value is latched as PHYADDR[0] at the de-assertion of reset. See Strapping Options – KSZ8061MNX (32-Pin Packages) section for details.

Notes:

2. Pwr = Power supply.
   Gnd = Ground.
   I = Input.
   O = Output.
   I/O = Bi-directional.
   Ipu = Input with internal pull-up (see Electrical Characteristics for value).
   Ipd = Input with internal pull-down (see Electrical Characteristics for value).
   Ipu/O = Input with internal pull-up (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.
   Ipd/O = Input with internal pull-down (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.
   Ipu/Opu = Input and output with internal pull-up (see Electrical Characteristics for value).
3. MII Mode: The RXD[3:0] bits are synchronous with RXC. When RXDV is asserted, RXD[3:0] presents valid data to the MAC device.

Pin Description – KSZ8061MNX (32-Pin Packages) (Continued)

Pin Number	Pin Name	Type[2]	Pin Function
15	VDDIO	Pwr	3.3V, 2.5V or 1.8V supply for digital I/O
16	RXD2 / PHYAD1	Ipd/O	MII Receive Data Output[2][3] Config Mode: The pull-up/pull-down value is latched as PHYADDR[1] at the de-assertion of reset. See Strapping Options – KSZ8061MNX (32-Pin Packages) section for details.
17	RXD1 / PHYAD2	Ipd/O	MII Receive Data Output[1][3] Config Mode: The pull-up/pull-down value is latched as PHYADDR[2] at the de-assertion of reset. See Strapping Options – KSZ8061MNX (32-Pin Packages) section for details.
18	RXD0 / AUTONEG	Ipu/O	MII Receive Data Output[0][3] Config Mode: The pull-up/pull-down value is latched as AUTONEG at the de-assertion of reset. See Strapping Options – KSZ8061MNX (32-Pin Packages) section for details.
19	RXC / CONFIG0	Ipd/O	MII Receive Clock Output Config Mode: The pull-up/pull-down value is latched as CONFIG0 at the de-assertion of reset. See Strapping Options – KSZ8061MNX (32-Pin Packages) section for details.
20	TXC	O	MII Transmit Clock Output
21	TXEN	I	MII Transmit Enable Input
22	TXD0	I	MII Transmit Data Input[0][4]
23	TXD1	I	MII Transmit Data Input[1][4]
24	LED0 / TXER	Ipd/O	LED0 Output (default) or MII Transmit Error Input Function of this pin is determined by bit [4] of register 1Ch and by EEE enable. The default function is LED0. When EEE is on, or when 1Ch.4 = 0, the function is TXER.
25	TXD2	I	MII Transmit Data Input[2][4]
26	TXD3	I	MII Transmit Data Input[3][4]
27	CRS / CONFIG1	Ipd/O	MII Carrier Sense Output Config Mode: The pull-up/pull-down value is latched as CONFIG1 at the de-assertion of reset. See Strapping Options – KSZ8061MNX (32-Pin Packages) section for details.
28	RESET#	Ipu	Chip Reset (active low)
29	INTRP / NAND_Tree#	Ipu/O	Programmable Interrupt Output (active low (default) or active high) This pin has a weak pull-up, is open drain like, and requires an external 1.0kΩ pull-up resistor. Config Mode: The pull-up/pull-down value is latched as NAND_Tree# at the de-assertion of reset. See Strapping Options – KSZ8061MNX (32-Pin Packages) section for details.
30	VDDL	Pwr	1.2V (nominal) supply for digital (and analog)
31	REXT	I	Set PHY transmit output current Connect a 6.04kΩ 1% resistor from this pin to ground.
32	SIGDET	O	Signal Detect, active high
Bottom paddle	GND	Gnd	Ground

Notes:

4. MII Mode: The TXD[3:0] bits are synchronous with TXC. When TXEN is asserted, TXD[3:0] accepts valid data from the MAC device.

Strapping Options – KSZ8061MNX (32-Pin Packages)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type(5)</th><th>Pin Function</th></tr>
<tr><td>17
16
14</td><td>RXD1 / PHYAD2
RXD2 / PHYAD1
RXD3 / PHYAD0</td><td>Ipd/O
Ipd/O
Ipu/O</td><td>The PHY Address is latched at de-assertion of reset and is configurable to any value from 0 to 7.
The default PHY Address is 00001.
PHY Address bits [4:3] are set to 00 by default.</td></tr>
<tr><td>13
27
19</td><td>RXDV / CONFIG2
CRS / CONFIG1
RXC / CONFIG0</td><td>Ipd/O
Ipd/O
Ipd/O</td><td>The CONFIG[2:0] strap-in pins are latched at the de-assertion of reset.
<table>
<tr><th>CONFIG[2:0]</th><th colspan="2">Mode</th></tr>
<tr><td>000 (default)</td><td>MII normal mode</td><td>Auto MDI/MDI-X disabled</td></tr>
<tr><td>001</td><td colspan="2">Reserved – not used</td></tr>
<tr><td>010</td><td>MII normal mode</td><td>Auto MDI/MDI-X enabled</td></tr>
<tr><td>011 - 101</td><td colspan="2">Reserved – not used</td></tr>
<tr><td>110</td><td>MII Back-to-Back</td><td>Auto MDI/MDI-X enabled</td></tr>
<tr><td>111</td><td colspan="2">Reserved – not used</td></tr>
</table></td></tr>
<tr><td>18</td><td>RXD0 / AUTONEG</td><td>Ipu/O</td><td>Auto-Negotiation Disable
Pull-up (default) = Disable Auto-Negotiation
Pull-down = Enable Auto-Negotiation
At the de-assertion of reset, this pin value is inverted, and then latched into register 0h, bit [12].</td></tr>
<tr><td>29</td><td>INTRP / NAND_Tree#</td><td>Ipu/O</td><td>NAND Tree Mode
Pull-up (default) = Disable NAND Tree (normal operation)
Pull-down = Enable NAND Tree
At the de-assertion of reset, this pin value is latched by the chip.</td></tr>
<tr><td>12</td><td>RXER / QWF</td><td>Ipd/O</td><td>Quiet-WIRE® Filtering Disable
Pull-up = Disable Quiet-WIRE Filtering
Pull-down (default) = Enable Quiet-WIRE Filtering
At the de-assertion of reset, this pin value is latched by the chip.</td></tr>
</table>

Note:

5. Ipu/O = Input with internal pull-up (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.
   Ipd/O = Input with internal pull-down (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.

The strap-in pins are latched at the de-assertion of reset. In some systems, the MAC MII receive input pins may drive high/low during power-up or reset, and consequently cause the PHY strap-in pins on the MII signals to be latched to the unintended high/low states. In this case, external pull-up or pull-down resistors (4.7kΩ) should be added on these PHY strap-in pins to ensure the intended values are strapped-in correctly.

Pin Configuration – KSZ8061MNG (48-Pin Package)

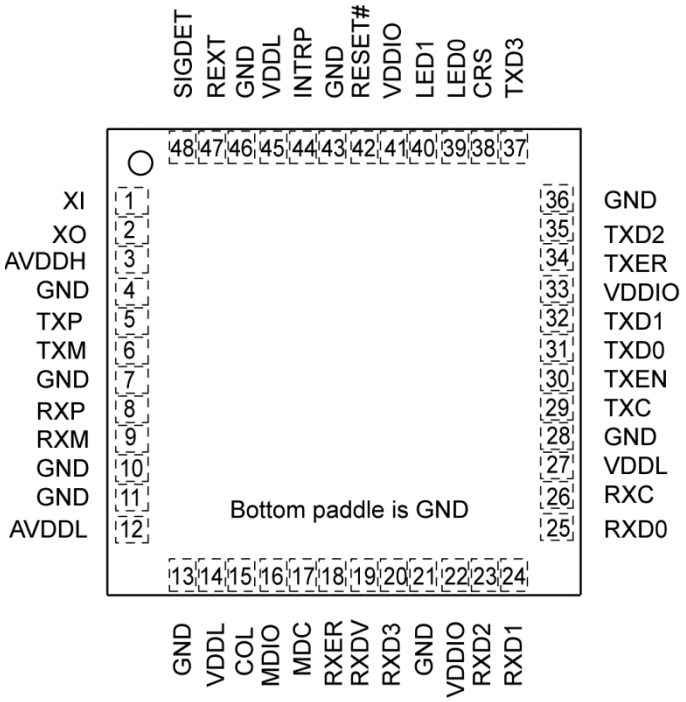


Figure 2. 48-Pin 7mm x 7mm QFN

Pin Description – KSZ8061MNG (48-Pin Package)

Pin Number	Pin Name	Type[6]	Pin Function
1	XI	I	Crystal/Oscillator/External Clock Input 25MHz ±50ppm. This input references the AVDDH power supply.
2	XO	O	Crystal feedback for 25MHz crystal This pin is a no connect if oscillator or external clock source is used.
3	AVDDH	Pwr	3.3V supply for analog TX drivers and XI/XO oscillator circuit.
4	GND	Gnd	Ground
5	TXP	I/O	Physical transmit or receive signal (+ differential)
6	TXM	I/O	Physical transmit or receive signal (– differential)
7	GND	Gnd	Ground
8	RXP	I/O	Physical receive or transmit signal (+ differential)
9	RXM	I/O	Physical receive or transmit signal (– differential)
10	GND	Gnd	Ground
11	GND	Gnd	Ground
12	AVDDL	Pwr	1.2V (nominal) supply for analog core
13	GND	Gnd	Ground
14	VDDL	Pwr	1.2V (nominal) supply for digital core
15	COL / B-CAST_OFF	Ipd/O	MII Collision Detect Output Config Mode: The pull-up/pull-down value is latched as B-CAST_OFF at the de-assertion of reset. See Strapping Options – KSZ8061MNG (48-Pin Package) section for details.
16	MDIO	Ipu/Opu	Management Interface (MIIM) Data I/O This pin has a weak pull-up, is open-drain like, and requires an external 1.0kΩ pull-up resistor.
17	MDC	Ipu	Management Interface (MIIM) Clock Input This clock pin is synchronous to the MDIO data pin.
18	RXER / QWF	Ipd/O	MII Receive Error Output Config Mode: The pull-up/pull-down value is latched as QWF at the de-assertion of reset. See Strapping Options – KSZ8061MNG (48-Pin Package) section for details.
19	RXDV / CONFIG2	Ipd/O	MII Receive Data Valid Output Config Mode: The pull-up/pull-down value is latched as CONFIG2 at the de-assertion of reset. See Strapping Options – KSZ8061MNG (48-Pin Package) section for details.

Notes:

6. Pwr = Power supply.
   Gnd = Ground.
   I = Input.
   O = Output.
   I/O = Bi-directional.
   Ipu = Input with internal pull-up (see Electrical Characteristics for value).
   Ipd = Input with internal pull-down (see Electrical Characteristics for value).
   Ipu/O = Input with internal pull-up (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.
   Ipd/O = Input with internal pull-down (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.
   Ipu/Opu = Input and output with internal pull-up (see Electrical Characteristics for value).

Pin Description – KSZ8061MNG (48-Pin Package) (Continued)

Pin Number	Pin Name	Type[6]	Pin Function
20	RXD3 / PHYAD0	Ipu/O	MII Receive Data Output[3][7] Config Mode: The pull-up/pull-down value is latched as PHYADDR[0] at the de-assertion of reset. See Strapping Options – KSZ8061MNG (48-Pin Package) section for details.
21	GND	Gnd	Ground
22	VDDIO	Pwr	3.3V, 2.5V or 1.8V supply for digital I/O
23	RXD2 / PHYAD1	Ipd/O	MII Receive Data Output[2][7] Config Mode: The pull-up/pull-down value is latched as PHYADDR[1] at the de-assertion of reset. See Strapping Options – KSZ8061MNG (48-Pin Package) section for details.
24	RXD1 / PHYAD2	Ipd/O	MII Receive Data Output[1][7] Config Mode: The pull-up/pull-down value is latched as PHYADDR[2] at the de-assertion of reset. See Strapping Options – KSZ8061MNG (48-Pin Package) section for details.
25	RXD0 / DUPLEX	Ipu/O	MII Receive Data Output[0][7] Config Mode: The pull-up/pull-down value is latched as DUPLEX at the de-assertion of reset. See Strapping Options – KSZ8061MNG (48-Pin Package) section for details.
26	RXC / CONFIG0	Ipd/O	MII Receive Clock Output Config Mode: The pull-up/pull-down value is latched as CONFIG0 at the de-assertion of reset. See Strapping Options – KSZ8061MNG (48-Pin Package) section for details.
27	VDDL	Pwr	1.2V (nominal) supply for digital core
28	GND	Gnd	Ground
29	TXC	O	MII Transmit Clock Output
30	TXEN	I	MII Transmit Enable Input
31	TXD0	I	MII Transmit Data Input[0][8]
32	TXD1	I	MII Transmit Data Input[1][8]
33	VDDIO	Pwr	3.3V, 2.5V, or 1.8V supply for digital I/O
34	TXER	Ipd	MII Transmit Error Input If the MAC does not provide a TXER output signal, this pin should be tied low.
35	TXD2	I	MII Transmit Data Input[2][8]
36	GND	Gnd	Ground
37	TXD3	I	MII Transmit Data Input[3][8]
38	CRS / CONFIG1	Ipd/O	MII Carrier Sense Output Config Mode: The pull-up/pull-down value is latched as CONFIG1 at the de-assertion of reset. See Strapping Options – KSZ8061MNG (48-Pin Package) section for details.

Notes:

7. MII Mode: The RXD[3:0] bits are synchronous with RXC. When RXDV is asserted, RXD[3:0] presents valid data to the MAC device.
8. MII Mode: The TXD[3:0] bits are synchronous with TXC. When TXEN is asserted, TXD[3:0] accepts valid data from the MAC device.

Pin Description – KSZ8061MNG (48-Pin Package) (Continued)

Pin Number	Pin Name	Type[6]	Pin Function
39	LED0 / AUTONEG	Ipu/O	LED0 Active low. Its function is programmable; by default it indicates link/activity. Config Mode: The pull-up/pull-down value is latched as AUTONEG at the de-assertion of reset. See Strapping Options – KSZ8061MNG (48-Pin Package) section for details.
40	LED1 / SPEED	Ipu/O	LED1 Active low. Its function is programmable; by default it indicates link speed. Config Mode: The pull-up/pull-down value is latched as SPEED at the de-assertion of reset. See Strapping Options – KSZ8061MNG (48-Pin Package) section for details.
41	VDDIO	Pwr	3.3V, 2.5V, or 1.8V supply for digital I/O
42	RESET#	Ipu	Chip Reset (active low)
43	GND	Gnd	Ground
44	INTRP / NAND_Tree#	Ipu/O	Programmable Interrupt Output (active low (default) or active high) This pin has a weak pull-up, is open drain like, and requires an external 1.0kΩ pull-up resistor. Config Mode: The pull-up/pull-down value is latched as NAND_Tree# at the de-assertion of reset. See Strapping Options – KSZ8061MNG (48-Pin Package) section for details.
45	VDDL	Pwr	1.2V (nominal) supply for digital (and analog)
46	GND	Gnd	Ground
47	REXT	I	Set PHY transmit output current Connect a 6.04kΩ 1% resistor from this pin to ground.
48	SIGDET	O	Signal Detect, active high
Bottom paddle	GND	Gnd	Ground

Strapping Options – KSZ8061MNG (48-Pin Package)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type[9]</th><th>Pin Function</th></tr>
<tr><td>24
23
20</td><td>RXD1 / PHYAD2
RXD2 / PHYAD1
RXD3 / PHYAD0</td><td>Ipd/O
Ipd/O
Ipu/O</td><td>The PHY Address is latched at de-assertion of reset and is configurable to any value from 0 to 7.
The default PHY Address is 00001.
PHY Address bits [4:3] are set to 00 by default.</td></tr>
<tr><td>19
38
26</td><td>RXDV / CONFIG2
CRS / CONFIG1
RXC / CONFIG0</td><td>Ipd/O
Ipd/O
Ipd/O</td><td>The CONFIG[2:0] strap-in pins are latched at the de-assertion of reset.
<table>
<tr><th>CONFIG[2:0]</th><th colspan="2">Mode</th></tr>
<tr><td>000 (default)</td><td>MII normal mode</td><td>Auto MDI/MDI-X disabled</td></tr>
<tr><td>001</td><td colspan="2">Reserved – not used</td></tr>
<tr><td>010</td><td>MII normal mode</td><td>Auto MDI/MDI-X enabled</td></tr>
<tr><td>011 - 101</td><td colspan="2">Reserved – not used</td></tr>
<tr><td>110</td><td>MII Back-to-Back</td><td>Auto MDI/MDI-X enabled</td></tr>
<tr><td>111</td><td colspan="2">Reserved – not used</td></tr>
</table></td></tr>
<tr><td>39</td><td>LED0 / AUTONEG</td><td>Ipu/O</td><td>Auto-Negotiation Enable
Pull-up (default) = Enable Auto-Negotiation
Pull-down = Disable Auto-Negotiation
At the de-assertion of reset, this pin value is latched into register 0h, bit [12].</td></tr>
<tr><td>44</td><td>INTRP / NAND_Tree#</td><td>Ipu/O</td><td>NAND Tree Mode
Pull-up (default) = Disable
Pull-down = Enable
At the de-assertion of reset, this pin value is latched by the chip.</td></tr>
<tr><td>18</td><td>RXER / QWF</td><td>Ipd/O</td><td>Quiet-WIRE Filtering Disable
Pull-up = Disable Quiet-WIRE Filtering
Pull-down (default) = Enable Quiet-WIRE Filtering
At the de-assertion of reset, this pin value is latched by the chip.</td></tr>
<tr><td>40</td><td>LED1 / SPEED</td><td>Ipu/O</td><td>Speed mode
Pull-up (default) = 100Mbps
Pull-down = 10Mbps
At the de-assertion of reset, this pin value is latched into register 0h, bit [13] as the speed select, and also is latched into register 4h (auto-negotiation advertisement) as the speed capability support.</td></tr>
<tr><td>25</td><td>RXD0 / DUPLEX</td><td>Ipu/O</td><td>Duplex mode
Pull-up (default) = Half-duplex
Pull-down = Full-duplex
At the de-assertion of reset, this pin value is inverted, and then latched into register 0h, bit [8].</td></tr>
<tr><td>15</td><td>COL / B-CAST_OFF</td><td>Ipd/O</td><td>Broadcast off – for PHY Address 0
Pull-up = PHY Address 0 is set as a unique PHY address
Pull-down (default) = PHY Address 0 is set as a broadcast PHY address
At the de-assertion of reset, this pin value is latched by the chip.</td></tr>
</table>

Note:

9. Ipu/O = Input with internal pull-up (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.
Ipd/O = Input with internal pull-down (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.

The strap-in pins are latched at the de-assertion of reset. In some systems, the MAC MII receive input pins may drive high/low during power-up or reset, and consequently cause the PHY strap-in pins on the MII signals to be latched to the unintended high/low states. In this case, external pull-ups or pull-down resistors (4.7kΩ) should be added on these PHY strap-in pins to ensure the intended values are strapped-in correctly.

Functional Description: 10Base-T/100Base-TX Transceiver

The KSZ8061MN is an integrated Fast Ethernet transceiver that features Quiet-WIRE® internal filtering to reduce line emissions. When Quiet-WIRE® filtering is disabled, it is fully compliant with the IEEE 802.3 specification. The KSZ8061 also has high noise immunity.

On the copper media side, the KSZ8061MN supports 10Base-T and 100Base-TX for transmission and reception of data over a standard CAT-5 or similar unshielded twisted pair (UTP) cable and HP Auto MDI/MDI-X for reliable detection of and correction for straight-through and crossover cables.

On the MAC processor side, the KSZ8061MN offers the Media Independent Interface (MII) for direct connection with MII-compliant Ethernet MAC processors and switches.

The MII management bus gives the MAC processor complete access to the KSZ8061MN control and status registers. Additionally, an interrupt pin eliminates the need for the processor to poll for PHY status change.

Auto-negotiation and Auto MDI/MDI-X can be disabled at power-on to significantly reduce initial time to link up.

A signal detect pin (SIGDET) is available to indicate when the link partner in inactive. An option is available for the KSZ8061MN to automatically enter Ultra-Deep Sleep mode automatically when SIGDET is de-asserted. Ultra-Deep Sleep mode may also be entered by command of the MAC processor. Additional low power modes are available.

100Base-TX Transmit

The 100Base-TX transmit function performs parallel-to-serial conversion, 4B/5B encoding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion that converts the MII data from the MAC into a 125MHz serial bit stream. The data and control stream is then converted into 4B/5B coding and followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. The output current is set by a precision external resistor on REXT for the 1:1 transformer ratio.

The output signal has a typical rise/fall time of 4ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10Base-T output is also incorporated into the 100Base-TX transmitter.

100Base-TX Receive

The 100Base-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, and then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and to improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII format and provided as the input data to the MAC.

Scrambler/De-Scrambler (100Base-TX only)

The scrambler is used to spread the power spectrum of the transmitted signal to reduce EMI and baseline wander. The de-scrambler is needed to recover the scrambled signal.

10Base-T Transmit

The 10Base-T drivers are incorporated with the 100Base-TX drivers to allow for transmission using the same magnetic. The drivers perform internal wave-shaping and pre-emphasis, and output 10Base-T signals with a typical amplitude of 2.5V peak. The 10Base-T signals have harmonic contents that are at least 27dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

10Base-T Receive

On the receive side, input buffer and level detecting squelch circuits are employed. A differential input receiver circuit and a PLL performs the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400mV or with short pulse widths to prevent noise at the RXP and RXM inputs from falsely trigger the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8061MN decodes a data frame. The receive clock is kept active during idle periods in between data reception.

SQE and Jabber Function (10Base-T only, not supported in 32-pin package)

In 10Base-T operation, a short pulse is put out on the COL pin after each frame is transmitted. This SQE test is required as part of the 10Base-T transmit/receive path. If transmit enable (TXEN) is high for more than 20ms (jabbering), the 10Base-T transmitter is disabled and COL is asserted high. If TXEN is then driven low for more than 250ms, the 10Base-T transmitter is re-enabled and COL is de-asserted (returns to low).

PLL Clock Synthesizer

The KSZ8061MN generates all internal clocks and all external clocks for system timing from an external 25MHz crystal, oscillator, or reference clock.

Auto-Negotiation

The KSZ8061MN conforms to the auto-negotiation protocol, defined in Clause 28 of the IEEE 802.3 specification. Auto-negotiation allows unshielded twisted pair (UTP) link partners to select the highest common mode of operation.

During auto-negotiation, link partners advertise capabilities across the UTP link to each other and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the mode of operation.

The following list shows the speed and duplex operation mode from highest to lowest priority.

- Priority 1: 100Base-TX, full-duplex
- Priority 2: 100Base-TX, half-duplex
- Priority 3: 10Base-T, full-duplex
- Priority 4: 10Base-T, half-duplex

Note that the 32-pin device does not have a COL pin on the MII interface, and therefore does not operate properly in half-duplex mode. If there is a possibility that the link partner will be operating in half-duplex mode, then the 48-pin device should be used because it fully supports both half- and full-duplex.

If the KSZ8061MN is using auto-negotiation, but its link partner is not, then the KSZ8061MN sets its operating speed by observing the signal at its receiver. This is known as parallel detection and allows the KSZ8061MN to establish link by listening for a fixed signal protocol in the absence of auto-negotiation advertisement protocol. Duplex is set by register 0h, bit [8] because the KSZ8061MN cannot determine duplex by parallel detection.

If auto-negotiation is disabled, the speed is set by register 0h, bit [13], and the duplex is set by register 0h, bit [8]. For the 48-pin device, these two bits are initialized at power-up/reset by strapping options on pins 40 and 25, respectively. For the 32-pin device, the default is 100Base-TX, full-duplex, and there are no strapping options to change this default.

Auto-negotiation is enabled or disabled by hardware pin strapping (AUTONEG) and by software (register 0h, bit [12]). By default, auto-negotiation is enabled in the 48-pin device after power-up or hardware reset, but it may be disabled by pulling the LED0 pin low at that time. For the 32-pin device, auto-negotiation is disabled by default, but it may be enabled by pulling the RXD0 pin low during reset. Afterwards, auto-negotiation can be enabled or disabled by register 0h, bit [12]. When the link is 10Base-T or the link partner is using auto-negotiation, and the Ultra-Deep Sleep mode is used, then the Signal Detect assertion timing delay bit, register 14h bit [1], must be set.

The auto-negotiation link up process is shown in Figure 3.

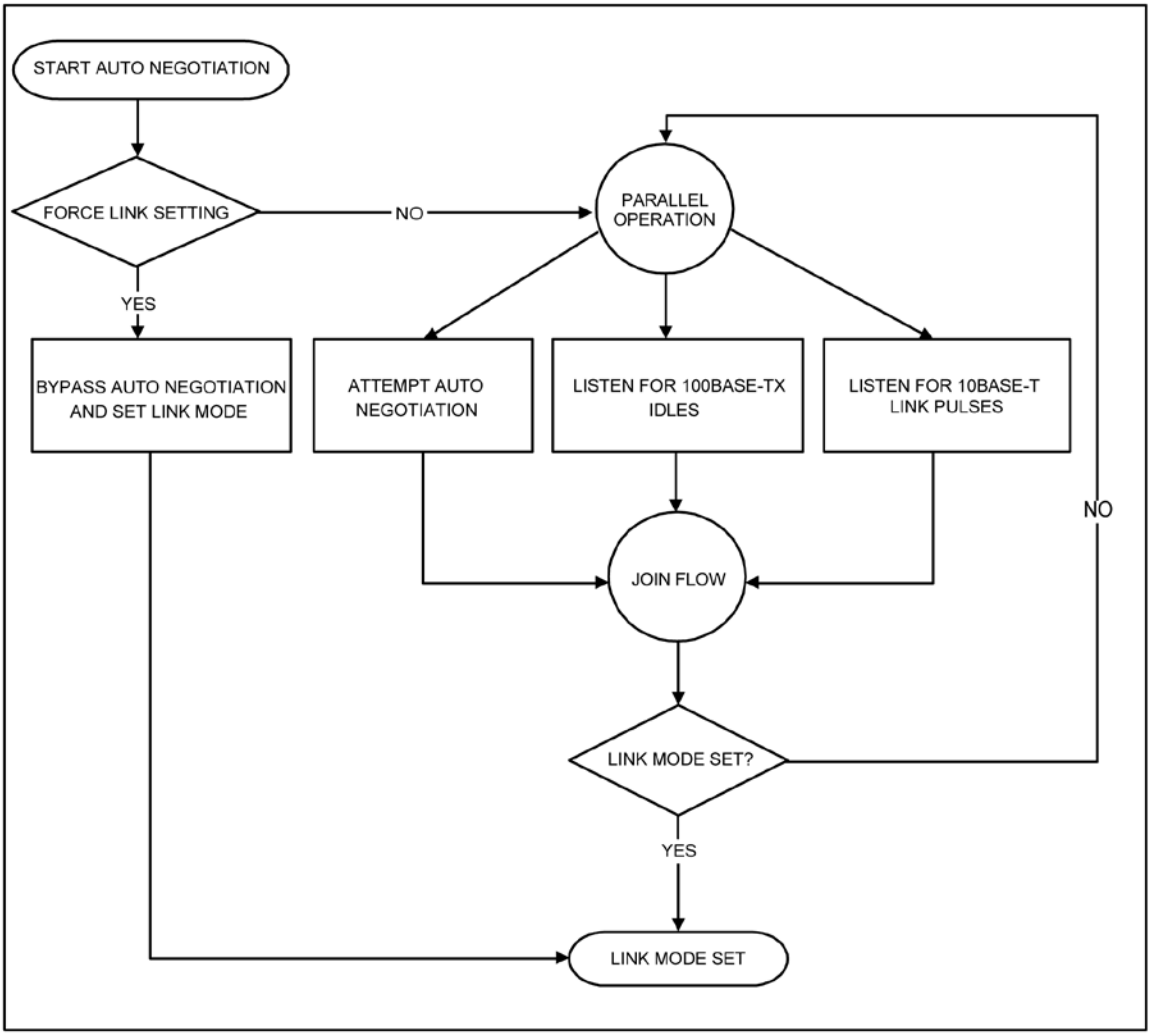


Figure 3. Auto-Negotiation Flow Chart

Quiet-WIRE® Filtering

Quiet-WIRE is a feature to enhance 100Base-TX EMC performance by reducing both conducted and radiated emissions from the TXP/M signal pair. It can be used either to reduce absolute emissions, or to enable replacement of shielded cable with unshielded cable, all while maintaining interoperability with standard 100Base-TX devices.

Quiet-WIRE filtering is implemented internally, with no additional external components required. It is enabled or disabled at power-up and reset by a strapping option on the RXER pin. Once the KSZ8061 is powered up, Quiet-WIRE can be enabled or disable by writing to register 16h, bit [12].

The default setting for Quiet-WIRE reduces emissions primarily above 60MHz, with less reduction at lower frequencies. Several dB of reduction is possible. Signal attenuation is approximately equivalent to increasing the cable length by 10 to 20 meters, thus reducing cable reach by that amount. For applications needing more modest improvement in emissions, the level of filtering can be reduced by writing a series of registers.

Fast Link-Up

Link up time is normally determined by the time it takes to complete auto-negotiation. Additional time may be added by the auto MDI/MDI-X feature. The total link up time from power-up or cable connect is typically a second or more.

Fast Link-up mode significantly reduces 100Base-TX link-up time by disabling both auto-negotiation and auto MDI/MDI-X, and fixing the TX and RX channels. This is done via the CONFIG[2:0] and AUTONEG strapping options. Because these are strapping options, fast link-up is available immediately upon power-up. Fast Link-up is available only for 100Base-TX link speed. To force the link speed to 10Base-TX requires a register write.

Fast Link-up is intended for specialized applications where both link partners are known in advance. The link must also be known so that the fixed transmit channel of one device connects to the fixed receive channel of the other device, and vice versa. [The TX and RX channel assignments are determined by the MDI/MDI-X strapping option on LED2_0.]

If a device in Fast Link-up mode is connected to a normal device (auto-negotiate and auto-MDI/MDI-X), there will be no problems linking, but the speed advantage of Fast Link-up will be realized only on one end.

Internal and External RX Termination

By default, the RX differential pair is internally terminated. This minimizes board component count by eliminating all components between the KSZ8061MN and the magnetics (transformer and common mode choke). The KSZ8061MN has the option to turn off the internal termination and allow the use of external termination. External termination does increase the external component count, but these external components can be of tighter tolerances than the internal termination resistors. Enabling or disabling of internal RX termination is controlled by register 14h, bit [2].

External termination should consist of a 50Ω resistor between each signal (RXP and RXM) and AVDD.

MII Interface

The Media Independent Interface (MII) is compliant with the IEEE 802.3 Specification. It provides a common interface between MII PHYs and MACs, and has the following key characteristics:

KSZ8061MNG (48-pin package) has full MII:

- Pin count is 16 pins (7 pins for data transmission, 7 pins for data reception, and 2 pins for carrier and collision indication).
- 10Mbps and 100Mbps data rates are supported at both half and full duplex.
- Data transmission and reception are independent and belong to separate signal groups.
- Transmit data and receive data are each 4-bit wide, a nibble.

KSZ8061MNX (32-pin package) has MII-Lite:

- Pin count is 15 pins (no COL signal).
- Full duplex only. Half duplex is not supported.

MII Signal Definition

Table 1 describes the MII signals. Refer to Clause 22 of the IEEE 802.3 specification for detailed information.

Table 1. MII Signal Definition

MII Signal Name	Direction (KSZ8061MN signal)	Direction (with respect to MAC device)	Description
TXC	Output	Input	Transmit Clock (2.5MHz for 10Mbps; 25MHz for 100Mbps)
TXEN	Input	Output	Transmit Enable
TXD[3:0]	Input	Output	Transmit Data [3:0]
TXER	Input	Output	Transmit Error (for EEE function only)
RXC	Output	Input	Receive Clock (2.5MHz for 10Mbps; 25MHz for 100Mbps)
RXDV	Output	Input	Receive Data Valid
RXD[3:0]	Output	Input	Receive Data [3:0]
RXER	Output	Input, or (not required)	Receive Error
CRS	Output	Input	Carrier Sense
COL	Output	Input	Collision Detection (KSZ8061MNG only)

Transmit Clock (TXC)

TXC is sourced by the PHY. It is a continuous clock that provides the timing reference for TXEN and TXD[3:0]. When the PHY links at 10Mbps, TXC is 2.5MHz. When the PHY links at 100Mbps, TXC is 25MHz.

Transmit Enable (TXEN)

TXEN indicates the MAC is presenting nibbles on TXD[3:0] for transmission. It is asserted synchronously with the first nibble of the preamble and remains asserted while all nibbles to be transmitted are presented on the MII, and is negated prior to the first TXC following the final nibble of a frame. TXEN transitions synchronously with respect to TXC.

Transmit Error (TXER)

TXER is implemented for the Energy Efficient Ethernet (EEE) function only. It is asserted by the MAC to enable the EEE's low power idle mode. The symbol error function for the transmitted frame onto the line is not implemented. TXER transitions synchronously with respect to TXC.

Transmit Data [3:0] (TXD[3:0])

When TXEN is asserted, TXD[3:0] are the data nibbles accepted by the PHY for transmission. TXD[3:0] is 00 to indicate idle when TXEN is de-asserted. TXD[3:0] transitions synchronously with respect to TXC.

Receive Clock (RXC)

RXC provides the timing reference for RXDV, RXD[3:0], and RXER.

- In 10Mbps mode, RXC is recovered from the line while carrier is active. RXC is derived from the PHY's reference clock when the line is idle, or link is down.
- In 100Mbps mode, RXC is continuously recovered from the line. If link is down, RXC is derived from the PHY's reference clock.

When the PHY links at 10Mbps, RXC is 2.5MHz. When the PHY links at 100Mbps, RXC is 25MHz.

Receive Data Valid (RXDV)

RXDV is driven by the PHY to indicate that the PHY is presenting recovered and decoded nibbles on RXD[3:0].

- In 10Mbps mode, RXDV is asserted with the first nibble of the SFD (Start of Frame Delimiter), 5Dh, and remains asserted until the end of the frame.
- In 100Mbps mode, RXDV is asserted from the first nibble of the preamble to the last nibble of the frame.

RXDV transitions synchronously with respect to RXC.

Receive Data[3:0] (RXD[3:0])

RXD[3:0] transitions synchronously with respect to RXC. For each clock period in which RXDV is asserted, RXD[3:0] transfers a nibble of recovered data from the PHY.

Receive Error (RXER)

RXER is asserted for one or more RXC periods to indicate that a Symbol Error (e.g. a coding error that a PHY is capable of detecting, and that may otherwise be undetectable by the MAC sub-layer) was detected somewhere in the frame presently being transferred from the PHY. RXER transitions synchronously with respect to RXC.

Carrier Sense (CRS)

CRS is asserted and de-asserted as follows:

- In 10Mbps mode, CRS assertion is based on the reception of valid preambles. CRS de-assertion is based upon the reception of an end-of-frame (EOF) marker.
- In 100Mbps mode, CRS is asserted when a start-of-stream delimiter or /J/K symbol pair is detected. CRS is de-asserted when an end-of-stream delimiter or /T/R symbol pair is detected. Additionally, the PMA layer de-asserts CRS if IDLE symbols are received without /T/R.

Carrier Sense (COL)

COL is asserted in half-duplex mode whenever the transmitter and receiver are simultaneously active on the line. This informs the MAC that a collision has occurred during its transmission to the PHY. COL is supported only in the 48-pin package option. Therefore the 32-pin package option does not support half duplex. When interfacing the 32-pin device to a MAC with a COL input, that input should be pulled low.

MII Signal Diagram

The KSZ8061MN MII pin connections to the MAC are shown in Figure 4.

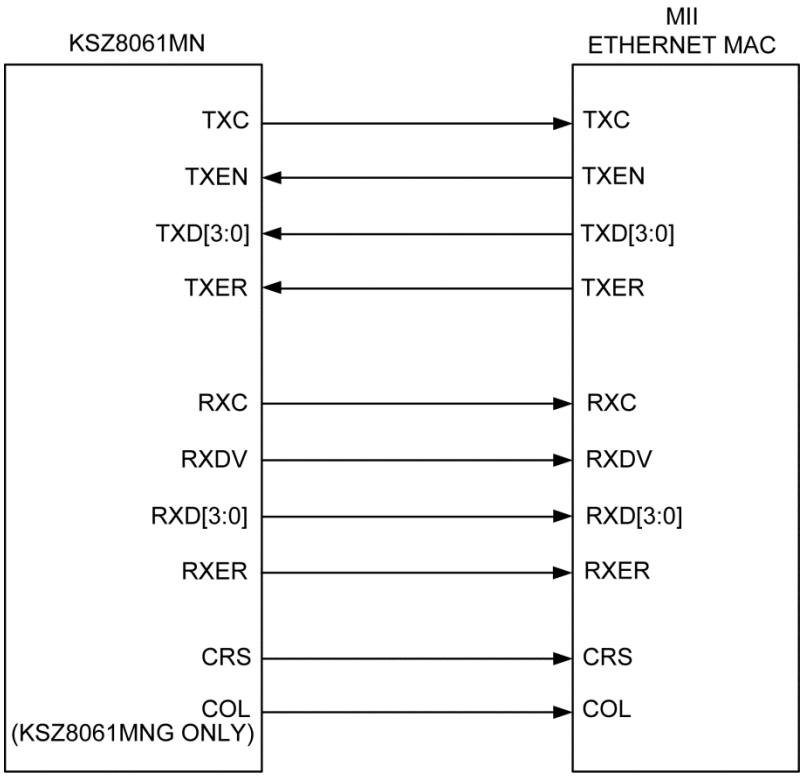


Figure 4. KSZ8061MN MII Interface

Back-to-Back Mode – 100Mbps Repeater

Two KSZ8061MN devices can be connected back-to-back to form a 100Base-TX to 100Base-TX repeater. For testing purposes, it can also be used to loopback data on the MII bus by physically connecting the MII receive bus to the MII transmit bus.

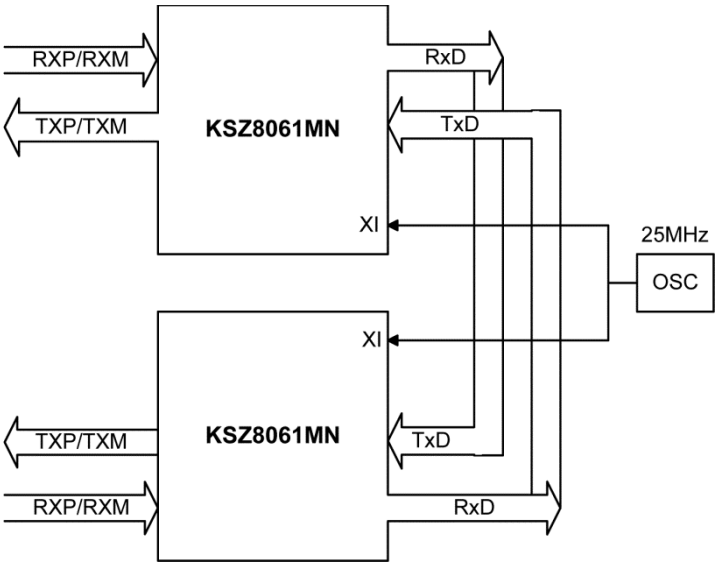


Figure 5. KSZ8061MN to KSZ8061MN Back-to-Back Repeater

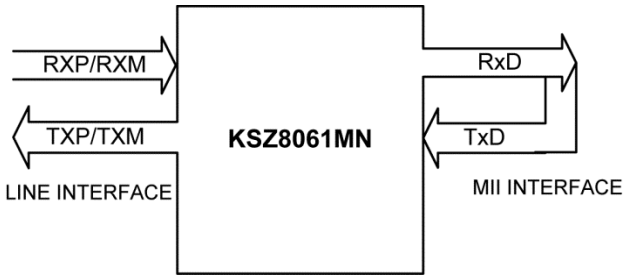


Figure 6. KSZ8061MN Back-to-Back for MII Bus Loopback

MII Back-to-Back Mode

In MII Back-to-Back mode, a KSZ8061MN interfaces with another KSZ8061MN to provide a complete 100Mbps repeater solution. RXC and TXC are not connected; they are both outputs.

The KSZ8061MN devices are configured to MII Back-to-Back mode after power-up or reset with the following:

- Strapping pin CONFIG[2:0] set to ‘110’
- A common 25MHz reference clock connected to XI of both KSZ8061MN devices
- MII signals connected as shown in Table 2.

Table 2. MII Signal Connection for MII Back-to-Back Mode

KSZ8061MN (100Base-TX) [Device 1]		KSZ8061MN (100Base-TX) [Device 1 or 2]	
Pin Name	**Pin Type**	**Pin Name**	**Pin Type**
RXDV	Output	TXEN	Input
RXD3	Output	TXD3	Input
RXD2	Output	TXD2	Input
RXD1	Output	TXD1	Input
RXD0	Output	TXD0	Input
TXEN	Input	RXDV	Output
TXD3	Input	RXD3	Output
TXD2	Input	RXD2	Output
TXD1	Input	RXD1	Output
TXD0	Input	RXD0	Output

Back-to-Back Mode and 10Base-T

If Back-to-Back mode is used and the line interface is operating at 10Base-T, it is necessary to also set register 18h bit [6].

MII Management (MIIM) Interface

The KSZ8061MN supports the IEEE 802.3 MII Management Interface, also known as the Management Data Input/Output (MDIO) Interface. This interface enables an upper-layer device, like a MAC processor, to monitor and control the state of the KSZ8061MN. An external device with MIIM capability is used to read the PHY status and/or configure the PHY settings. Further details on the MIIM interface can be found in Clause 22.2.4 of the IEEE 802.3 specification.

The MIIM interface consists of the following:

- A physical connection that incorporates the clock line (MDC) and the data line (MDIO).
- A specific protocol that operates across the aforementioned physical connection that allows the external controller to communicate with one or more PHY devices.
- A set of 16-bit MDIO registers. Supported registers [0:8] are standard registers, and their functions are defined per the IEEE 802.3 Specification. The additional registers are provided for expanded functionality. See Register Map section for details.

The KSZ8061MN supports unique PHY addresses 1 to 7, and broadcast PHY address 0. The broadcast address is defined per the IEEE 802.3 specification, and can be used to write to multiple KSZ8061MN devices simultaneously.

The PHYAD[2:0] strapping pins are used to assign a unique PHY address between 0 and 7 to each KSZ8061MN device.

Table 3 shows the MII Management frame format.

Table 3. MII Management Frame Format

	Preamble	Start of Frame	Read/Write OP Code	PHY Address Bits [4:0]	REG Address Bits [4:0]	TA	Data Bits [15:0]	Idle
Read	32 1's	01	10	00AAA	RRRRR	Z0	DDDDDDDD_DDDDDDDD	Z
Write	32 1's	01	01	00AAA	RRRRR	10	DDDDDDDD_DDDDDDDD	Z

LED Output Pins

The LED0 and LED1 pins indicate line status and are intended for driving LEDs. They are active low and can sink current directly from LEDs. By default, LED0 indicates Link/Activity, and LED1 indicates Link Speed. Bits [5:4] in register 1Fh allow the definition of these pins to be changed to Link Status and Activity respectively.

On the KSZ8061MNX, pin 24 is a dual-function pin that can function either as LED0 or TXER. TXER is needed only for EEE. At reset, EEE is disabled and this pin function is LED0. If EEE is enabled and the link partner also supports EEE, the pin becomes TXER, and no LED signal is available on the KSZ8061MNX. The default function for LED0 on the KSZ8061MNX is Link Status, but it may be changed to Link/Activity.

- Link Status: The LED indicates that the serial link is up.
- Link/Activity: When the link is up but there is no traffic, the LED will be on. When packets are being received or transmitted, the LED will blink.
- Activity: The LED blinks when packets are received or transmitted. It is off when there is no activity.
- Speed: When the link is up, the LED is on to indicate a 100Base-TX link, and is off to indicate a 10Base-T link.

Interrupt (INTRP)

INTRP is an interrupt output signal that may be used to inform the external controller that there has been a status update to the KSZ8061MN PHY register. This eliminates the need for the processor to poll the PHY for status changes such as link up or down.

Register 1Bh, bits [15:8] are the interrupt control bits to enable and disable the conditions for asserting the INTRP signal. Register 1Bh, bits [7:0] are the interrupt status bits to indicate which interrupt conditions have occurred. The interrupt status bits are cleared after reading register 1Bh.

Register 1Fh, bit [9] sets the interrupt level to active high or active low. The default is active low.

HP Auto MDI/MDI-X

HP Auto MDI/MDI-X configuration eliminates the confusion of whether to use a straight cable or a crossover cable between the KSZ8061MN and its link partner. This feature allows the KSZ8061MN to use either type of cable to connect with a link partner that is in either MDI or MDI-X mode. The auto-sense function detects transmit and receive pairs from the link partner and then assigns transmit and receive pairs of the KSZ8061MN accordingly.

Auto MDI/MDI-X is initially either enabled or disabled at a hardware reset by strapping the hardware pin (CONFIG[2:0]). Afterwards, it can be enabled or disabled by register 1Fh, bit [13]. When Auto MDI/MDI-X is disabled, serial data is normally transmitted on the pin pair TXP/TXM, and data is received on RXP/RXM. However, this may be reversed by writing to register 1Fh, bit [14].

An isolation transformer with symmetrical transmit and receive data paths is recommended to support Auto MDI/MDI-X.

Table 4 illustrates how the IEEE 802.3 Standard defines MDI and MDI-X.

Table 4. MDI/MDI-X Pin Definition

MDI		MDI-X	
RJ-45 Pin	**Signal**	**RJ-45 Pin**	**Signal**
1	TX+	1	RX+
2	TX-	2	RX-
3	RX+	3	TX+
6	RX-	6	TX-

Straight Cable

A straight cable connects an MDI device to an MDI-X device, or a MDI-X device to a MDI device. Figure 7 depicts a typical straight cable connection between a NIC card (MDI device) and a switch, or hub (MDI-X device).

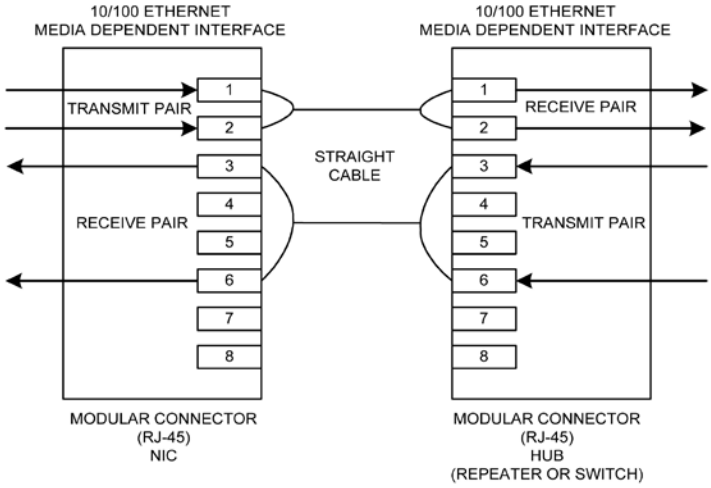


Figure 7. Typical Straight Cable Connection

Crossover Cable

A crossover cable connects an MDI device to another MDI device, or an MDI-X device to another MDI-X device. Figure 8 depicts a typical crossover cable connection between two switches or hubs (two MDI-X devices).

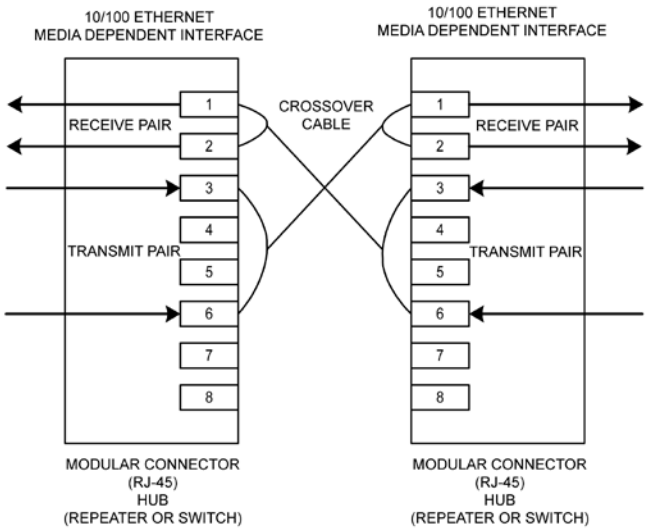


Figure 8. Typical Crossover Cable Connection

Loopback Modes

The KSZ8061MN supports the following loopback operations to verify analog and/or digital data paths.

- Local (Digital) Loopback
- Remote (Analog) Loopback

Local (Digital) Loopback Mode

This loopback mode is a diagnostic mode for checking the MII transmit and receive data paths between KSZ8061MN and external MAC, and is supported for both speeds (10/100 Mbps) at full-duplex.

The loopback data path is shown in Figure 9.

1. MII MAC transmits frames to KSZ8061MN.
2. Frames are wrapped around inside KSZ8061MN.
3. KSZ8061MN transmits frames back to MII MAC.

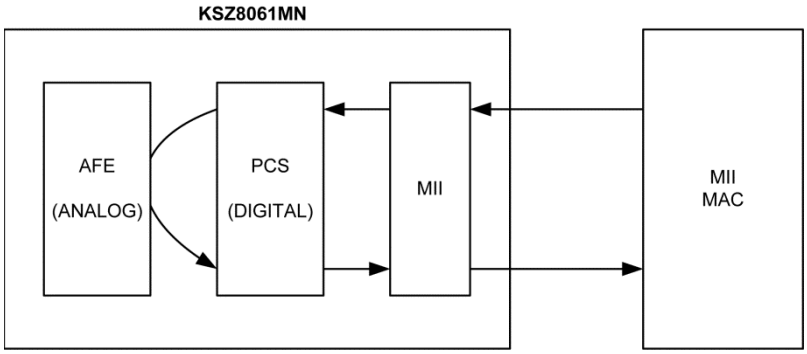


Figure 9. Local (Digital) Loopback

The following programming steps and register settings are used for Local Loopback mode.

For 10/100 Mbps loopback,

1. Set Register 0h,
   - Bit [14] = 1 // Enable Local Loopback mode
   - Bit [13] = 0/1 // Select 10Mbps / 100Mbps speed
   - Bit [12] = 0 // Disable Auto-Negotiation
   - Bit [8] = 1 // Select full-duplex mode
2. Set Register 1Ch,
   - Bit [5] = 1

Remote (Analog) Loopback

This loopback mode checks the line (differential pairs, transformer, RJ-45 connector, Ethernet cable) transmit and receive data paths between KSZ8061MN and its link partner, and is supported for 100Base-TX full-duplex mode only.

The loopback data path is shown in the following Figure 10.

1. Fast Ethernet (100Base-TX) PHY Link Partner transmits frames to KSZ8061MN.
2. Frames are wrapped around inside KSZ8061MN.
3. KSZ8061MN transmits frames back to Fast Ethernet (100Base-TX) PHY Link Partner.

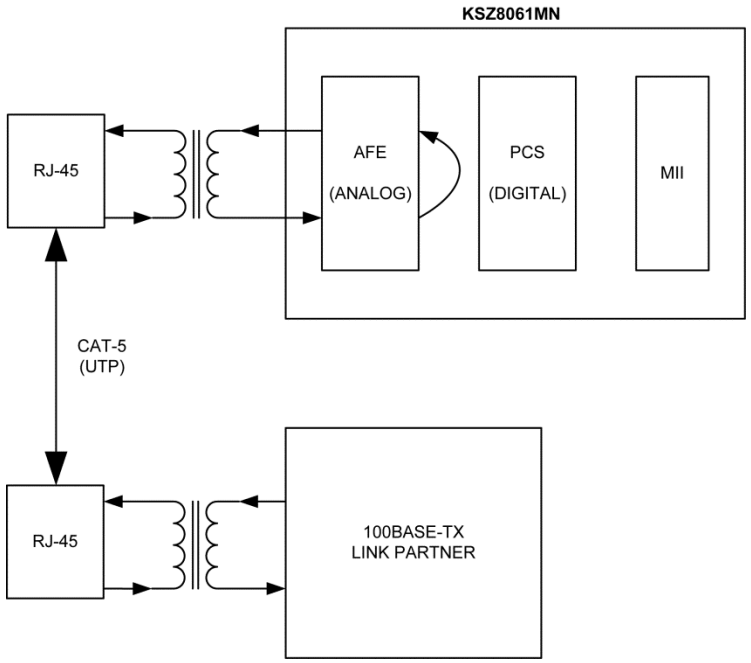


Figure 10. Remote (Analog) Loopback

The following programming steps and register settings are used for Remote Loopback mode.

1. Set Register 0h,
   - Bit [13] = 1 // Select 100Mbps speed
   - Bit [12] = 0 // Disable Auto-Negotiation
   - Bit [8] = 1 // Select full-duplex mode

Or just simply auto-negotiate and link up at 100Base-TX full-duplex mode with link partner

2. Set Register 1Fh,
   - Bit [2] = 1 // Enable Remote Loopback mode

LinkMD® Cable Diagnostics

The LinkMD® function utilizes time domain reflectometry (TDR) to analyze the cabling plant for common cabling problems, such as open circuits, short circuits, and impedance mismatches.

LinkMD works by sending a pulse of known amplitude and duration down the MDI or MDI-X pair, and then analyzing the shape of the reflected signal to determine the type of fault. The time duration for the reflected signal to return provides the approximate distance to the cabling fault. The LinkMD function processes this TDR information and presents it as a numerical value that can be translated to a cable distance.

LinkMD is initiated by accessing the LinkMD Control/Status Register (register 1Dh) and the PHY Control 2 Register (register 1Fh). The latter register is used to disable auto MDI/MDI-X and to select either MDI or MDI-X as the cable differential pair for testing.

A two-step process is used to analyze the cable. The first step uses a small pulse (for short cables), while the second step uses a larger pulse (for long cables). The steps are shown here:

For short cables:

1. Write MMD address 1Bh, register 0, bits [7:4] = 0x2. Note that this is the power-up default value.
2. Write register 13h, bit [15] = 0. Note that this is the power-up default value.
3. Write register 1Fh. Disable auto MDI/MDI-X in bit [13], and select either MDI or MDI-X in bit [14] to specify the twisted pair to test.
4. Write register 1Dh bit [15] to initiate the LinkMD test.
5. Read register 1Dh to determine the result of the first step. Bit [15] = 0 indicates that the test is complete. After that, the result is read in bits [14:12]. Remember the result.

For long cables:

1. Write MMD address 1Bh, register 0, bits [7:4] = 0x7.
2. Write register 13h, bit [15] = 1.
3. Write register 1Dh bit [15] to initiate the LinkMD test.
4. Read register 1Dh to determine the result of the first step. Bit [15] = 0 indicates that the test is complete. After that, the result is read in bits [14:12].

If either test reveals a short, then there is a short. If either test reveals an open, then there is an open. If both tests indicate normal, ten the cable is normal.

LinkMD®+ Enhanced Diagnostics: Receive Signal Quality Indicator

The KSZ8061MN provides a receive Signal Quality Indicator (SQI) feature that indicates the relative quality of the 100Base-TX receive signal. It approximates a signal-to-noise ratio, and is affected by cable length, cable quality, and coupled of environmental noise.

The raw SQI value is available for reading at any time from indirect register: MMD 1Ch, register ACh, bits [14:8]. A lower value indicates better signal quality, while a higher value indicates worse signal quality. Even in a stable configuration in a low-noise environment, the value read from this register may vary. The value should therefore be averaged by taking multiple readings. The update interval of the SQI register is 2µs, so measurements taken more frequently than 2µs will be redundant. In a quiet environment, six to ten readings are suggested for averaging. In a noisy environment, individual readings are unreliable, so a minimum of thirty readings are suggested for averaging. The SQI circuit does not include any hysteresis.

Table 5 lists typical SQI values for various CAT5 cable lengths when linked to a typical 100Base-TX device in a quiet environment. In a noisy environment or during immunity testing, the SQI value will increase.

Table 5. Typical SQI Values

CAT5 Cable Length	Typical SQI Value (MMD 1Ch, register ACh, bits [14:8])
10m	2
30m	2
50m	3
80m	3
100m	4
130m	5

NAND Tree Support

The KSZ8061MN provides parametric NAND tree support for fault detection between chip I/Os and board. The NAND tree is a chain of nested NAND gates in which each KSZ8061MN digital I/O (NAND tree input) pin is an input to one NAND gate along the chain. At the end of the chain, the CRS pin provides the output for the next NAND gates.

The NAND tree test process includes:

- Enabling NAND tree mode
- Pulling all NAND tree input pins high
- Driving low each NAND tree input pin sequentially per the NAND tree pin order
- Checking the NAND tree output to ensure there is a toggle high-to-low or low-to-high for each NAND tree input driven low

Table 6 and Table 7 list the NAND tree pin order.

Table 6. KSZ8061MNX NAND Tree Test Pin Order

Pin Number	Pin Name	NAND Tree Description
10	MDIO	Input
11	MDC	Input
12	RXER	Input
13	RXDV	Input
14	RXD3	Input
16	RXD2	Input
17	RXD1	Input
18	RXD0	Input
19	RXC	Input
20	TXC	Input
21	TXEN	Input
22	TXD0	Input
23	TXD1	Input
24	LED0/TXER	Input
25	TXD2	Input
26	TXD3	Input
29	INTRP	Input
27	CRS	Output

Table 7. KSZ8061MNG NAND Tree Test Pin Order

Pin Number	Pin Name	NAND Tree Description
15	COL	Input
16	MDIO	Input
17	MDC	Input
18	RXER	Input
19	RXDV	Input
20	RXD3	Input
23	RXD2	Input
24	RXD1	Input
25	RXD0	Input
26	RXC	Input
29	TXC	Input
30	TXEN	Input
31	TXD0	Input
32	TXD1	Input
34	LED0/TXER	Input
35	TXD2	Input
37	TXD3	Input
39	LED0	Input
40	LED1	Input
44	INTRP	Input
38	CRS	Output

NAND Tree I/O Testing

The following procedure can be used to check for faults on the KSZ8061MN digital I/O pin connections to the board:

1. Enable NAND tree mode by INTRP pin strapping option.
2. Use board logic to drive all KSZ8061MN NAND tree input pins high.
3. Use board logic to drive each NAND tree input pin, per KSZ8061MN NAND tree pin order, as follows:
   a. Toggle the first pin (MDIO) from high to low, and verify the CRS pin switch from high to low to indicate that the first pin is connected properly.
   b. Leave the first pin (MDIO) low.
   c. Toggle the second pin (MDC) from high to low, and verify the CRS pin switch from low to high to indicate that the second pin is connected properly.
   d. Leave the first pin (MDIO) and the second pin (MDC) low.
   e. Toggle the third pin (RXD3) from high to low, and verify the CRS pin switch from high to low to indicate that the third pin is connected properly.
   f. Continue with this sequence until all KSZ8061MN NAND tree input pins have been toggled.

Each KSZ8061MN NAND tree input pin must cause the CRS output pin to toggle high-to-low or low-to-high to indicate a good connection. If the CRS pin fails to toggle when the KSZ8061MN input pin toggles from high to low, the input pin has a fault.

Power Management

The KSZ8061MN offers the following power management modes which are enabled and disabled by register control.

Power Saving Mode

Power saving mode is used to reduce the transceiver power consumption when the cable is unplugged. This mode does not interfere with normal device operation. It is enabled by writing a one to register 1Fh, bit [10], and is in effect when auto-negotiation mode is enabled and cable is disconnected (no link).

In this mode, the KSZ8061MN shuts down all transceiver blocks except for the transmitter, energy detect, and PLL circuits. By default, power saving mode is disabled after power-up.

Energy Detect Power Down Mode

Energy detect power down (EDPD) mode is used to further reduce the transceiver power consumption when the cable is unplugged, relative to power saving mode. This mode does not interfere with normal device operation. It is enabled by writing a zero to register 18h, bit [11], and is in effect when auto-negotiation mode is enabled and cable is disconnected (no link).

EDPD mode can be optionally enhanced with a PLL Off feature, which turns off all KSZ8061MN transceiver blocks, except for transmitter and energy detect circuits. PLL Off is set by writing a one to register 10h, bit [4].

Further power reduction is achieved by extending the time interval in between transmissions of link pulses while in this mode. The periodic transmission of link pulses is needed to ensure two link partners in the same low power state and with auto MDI/MDI-X disabled can wake up when the cable is connected between them. By default, energy detect power down mode is disabled after power-up.

Power Down Mode

Power down mode is used to power down the KSZ8061MN when it is not in use after power-up. It is enabled by writing a one to register 0h, bit [11].

In this mode, the KSZ8061MN disables all internal functions except the MII management interface. The KSZ8061MN exits (disables) power down mode after register 0h, bit [11] is set back to zero.

Slow Oscillator Mode

Slow oscillator mode is used to disconnect the input reference crystal/clock on XI (pin 1) and select the on-chip slow oscillator when the KSZ8061MN is not in use after power-up. It is enabled by writing a one to register 11h, bit [6].

Slow oscillator mode works in conjunction with power down mode to put the KSZ8061MN into a lower power state with all internal functions disabled, except for the MII management interface. To properly exit this mode and return to normal PHY operation, use the following programming sequence:

1. Disable slow oscillator mode by writing a zero to register 11h, bit [6].
2. Disable power down mode by writing a zero to register 0h, bit [11].
3. Initiate software reset by writing a one to register 0h, bit [15].

Ultra-Deep Sleep Mode

Ultra-deep sleep mode is used to achieve the lowest possible power consumption while retaining the ability to detect activity on the Tx/Rx cable pairs, and is intended for achieving negligible battery drain during long periods of inactivity. It is controlled by several register bits. Ultra-deep sleep mode may be entered by writing to a register, or it may be initiated automatically when signal detect (SIGDET) is de-asserted. Details are given in the Signal Detect (SIGDET) and Ultra-Deep Sleep Mode section.

In Ultra-deep sleep mode, the KSZ8061MN disables all internal functions and I/Os except for the ultra-low power signal detect circuit and the signal detect pin (SIGDET), which are powered by VDDIO. For the lowest power consumption, the 1.2V supply (VDDL and AVDDL) may be turned off externally. A hardware reset is required to exit Ultra-deep sleep mode.

Non-Volatile Registers

Most of the logic circuitry of the KSZ8061MN, including the status and control registers, is powered by the 1.2V supply. When the 1.2V supply is turned off in Ultra-deep sleep mode, the content of the registers is lost. Because of the importance of register 14h and bit [0] of register 13h, which control the various power modes, these bits are duplicated in a logic block powered by the 3.3V supply. These register bits are therefore “non-volatile” while in Ultra-deep sleep mode.

To access the non-volatile (3.3V) registers, bit [4] of register 14h must first be set. Otherwise, writes to these registers will modify only the volatile versions of these registers and not the non-volatile versions.

Signal Detect (SIGDET) and Ultra-Deep Sleep Mode

SIGDET is an output signal which may be used for power reduction, either by directly turning off selected power or by signaling to a host controller when no signal is detected on the line interface. It is asserted when sufficient energy is detected on either of the differential pairs, and is de-asserted when cable energy is not detected. The signal detection circuit consumes almost no power from the VDDIO supply, and does not use the 1.2V supply at all.

Ultra-deep sleep mode may be entered either automatically in unison with the Signal Detect signal (automatic method), or manually by setting a register bit (CPU control method).

The signal detect feature and Ultra-deep sleep mode are controlled via multiple bits in register 14h:

- Register 14h, bit [6] Ultra-deep sleep method: either automatic or CPU control.
- Register 14h, bit [5] Manually enter Ultra-deep sleep mode when CPU control method is selected.
- Register 14h, bit [4] Enable R/W access to non-volatile versions of register 14h and bits [9:8] and [1:0] of register 13h. Set this bit when bit [3] is set.
- Register 14h, bit [3] Enable Ultra-deep sleep mode and SIGDET
- Register 14h, bit [1] Extend timing for SIGDET de-assertion and entry into Ultra-deep sleep mode
- Register 14h, bit [0] SIGDET output polarity

CPU Control Method (MIIM interface)

In the CPU control method, the KSZ8061MN drives SIGDET signal to the CPU. SIGDET defaults to force high, in order to not interfere with PHY initialization by the CPU. At power-on, the KSZ8061MN drives SIGDET high, without consideration of cable energy level. During initialization, the CPU writes data 0x0058 to register 14h.

- Bit [4] enables access to the non-volatile copy of register 14h.
- Enable ultra-deep sleep mode and SIGDET by setting register 14h, bit [3].
- Automatic ultra-deep sleep functionality is disabled by setting register 14h, bit [6].

SIGDET is now enabled and will change state as cable energy changes. Typically, in response to the de-assertion of SIGDET, the CPU puts KSZ8061MN into ultra-deep sleep mode by setting register 14h, bit [5]. To further reduce power, the CPU may disable the 1.2V supply to the KSZ8061MN. The KSZ8061MN will assert SIGDET when energy is detected on the cable. To activate the KSZ8061MN, the CPU enables the 1.2V supply and asserts hardware reset (RESET#) to the KSZ8061MN. Because the KSZ8061MN has been completely reset, the registers must also be re-initialized.

Alternatively, it is possible to maintain register access during ultra-deep sleep mode by preserving the 1.2V power supply and setting register 13h, bit [0] to enable slow oscillator mode. Ultra-deep sleep mode can then be exited by writing to register 14h. The 1.2V supply results in increased power consumption.

Automatic Ultra-Deep Sleep Method

The board may be designed such that the KSZ8061MN SIGDET signal enables the 1.2V power supply to KSZ8061MN. At power-on, the KSZ8061MN drives SIGDET high, without consideration of cable energy level. During initialization, CPU writes data 0x001A or 0x0018 to register 14h.

- Bit [4] enables access to the non-volatile copy of register 14h.
- Enable ultra-deep sleep mode and SIGDET by setting register 14h, bit [3].
- Automatic ultra-deep sleep functionality is enabled by clearing register 14h, bit [6].
- SIGDET timing bit [1] must be set unless the link partner is not using auto-negotiation, auto-MDI/MDI-X is disabled, and link is at 100 Mbps.

When the KSZ8061MN detects signal loss, it automatically enters ultra-deep sleep mode and de-asserts SIGDET. SIGDET may be used to disable the 1.2V supply. When the KSZ8061MN detects a signal, it asserts SIGDET (which enables the 1.2V supply) and automatically wakes up. SIGDET may be used to wake up the CPU, which then re-initializes the KSZ8061MN.

Alternatively, a hardware reset (RESET#) will bring the KSZ8061MN out of ultra-deep sleep mode. Note that the contents of register 14h and bits [9:8] and [1:0] of register 13h are preserved during ultra-deep sleep mode, but are lost during hardware reset.

Energy Efficient Ethernet (EEE)

The KSZ8061MN implements Energy Efficient Ethernet (EEE) for Media Independent Interface (MII) in accordance to the IEEE 802.3az Specification. Implementation is defined around an EEE-compliant MAC on the host side and an EEE-compliant Link Partner on the line side that support special signaling associated with EEE.

EEE saves power by keeping the voltage for the AC signal on the Ethernet cable at approximately 0V peak-to-peak for as often as possible during periods of no traffic activity, while maintaining the link-up status. This is referred to as the Low Power Idle (LPI) state.

In the LPI state, the copper link responds automatically when it receives traffic and resumes normal PHY operation immediately, without blockage of traffic or loss of packet. This involves exiting LPI state and returning to normal 100Mbps operating mode. Wake-up time is <30µs for 100Base-TX.

The LPI state is controlled independently for transmit and receive paths, allowing the LPI state to be active (enabled) for:

- Transmit cable path only
- Receive cable path only
- Both transmit and receive cable paths

Upon power-up or reset, the EEE function is off. To enable the EEE function for 100Mbps mode, follow this programming sequence:

1. Enable 100Mbps EEE mode advertisement by writing a ‘1’ to MMD address 7h, register 3Ch, bit [1].
2. Restart auto-negotiation by writing a ‘1’ to standard register 0h, bit [9].

In 100Base-TX EEE operation, “refresh” transmissions are used to maintain link and the quiet periods are when the power savings takes place. Approximately every 20ms - 22ms a refresh transmission of 200µs - 220µs sent to the link partner. The refresh transmissions and quiet periods are shown in Figure 11.

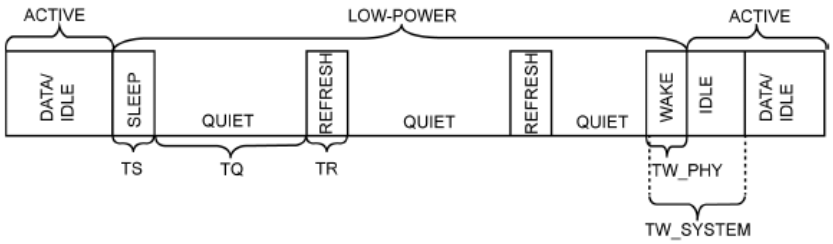


Figure 11. LPI Mode (Refresh Transmissions and Quiet Periods)

Transmit Direction Control

The KSZ8061MN enters the LPI state for the transmit direction when the attached EEE-compliant MAC de-asserts TXEN, asserts TXER, and drives TXD[3:0] to 0001. It remains in the transmit LPI state while MAC maintains the states of these signals. The TXC clock is not stopped because it is sourced from the PHY and is used by the MAC for MII transmit.

When the attached EEE-compliant MAC changes any of the TXEN and TXD[3:0] signals from the set LPI state value, the KSZ8061MN exits the LPI transmit state.

Receive Direction Control

The KSZ8061MN enters the LPI state for the receive direction upon receiving the P Code bit pattern (Sleep/Refresh) from the EEE-compliant link partner. It then de-asserts RXDV, asserts RXER, and drives RXD[3:0] to 0001. The KSZ8061MN remains in the receive LPI state while it continues to receive the refresh from the link partner, so it will continue to maintain and drive the LPI output states for the MII receive signals to inform the attached MAC that it is in the LPI receive state.

Additionally, after nine or more clock cycles in the receive LPI state, the KSZ8061MN will stop the RXC clock output to the MAC.

When the KSZ8061MN receives a non-P Code bit pattern (non-refresh), it exits the LPI state and sets the RXDV and RXD[3:0] signals accordingly for a normal frame or normal idle.

Reference Circuit for Power and Ground Connections

The KSZ8061MNX and KSZ8061MNG require a minimum of two supply voltages. 1.2V is required for VDDL and AVDDL. 3.3V is required for VDDIO and AVDDH. Optionally, VDDIO may be operated at 2.5V or 1.8V.

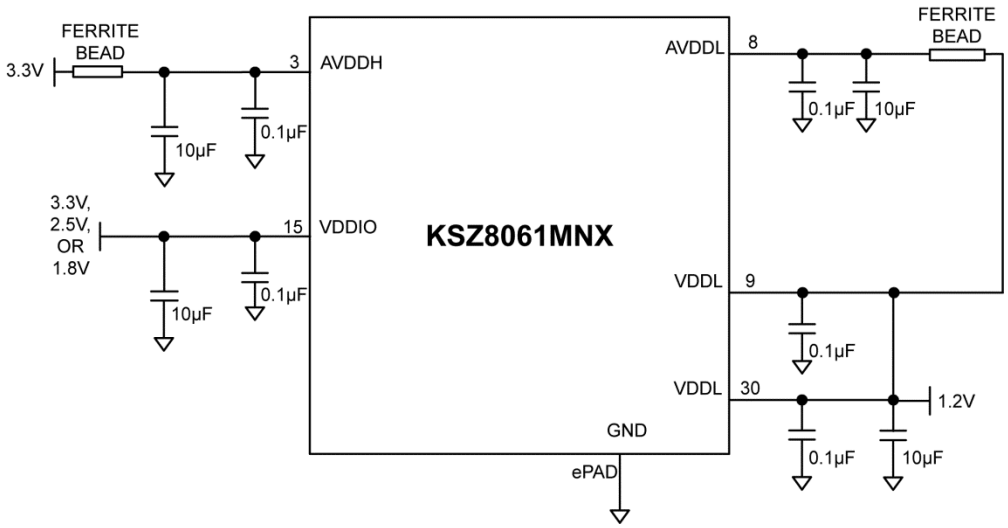


Figure 12. KSZ8061MNX Power and Ground Connections

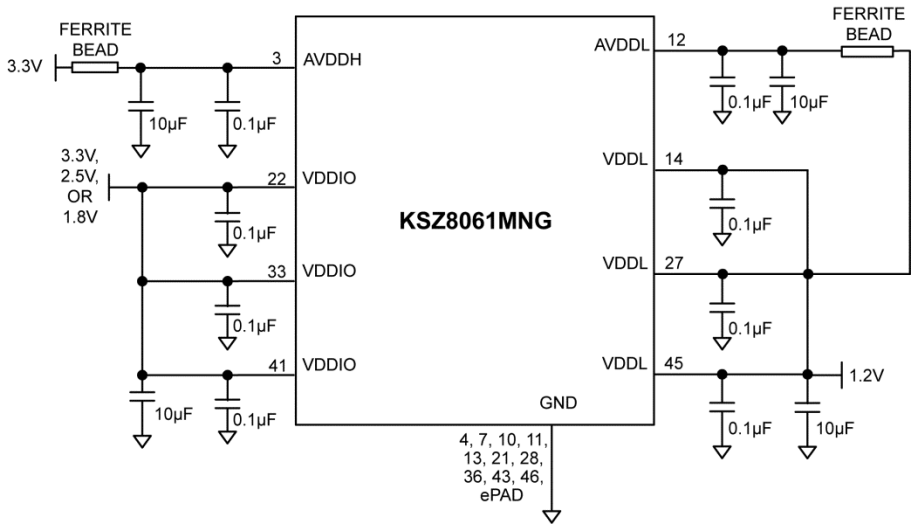


Figure 13. KSZ8061MNG Power and Ground Connections

Register Map

The register space within the KSZ8061MN consists of two distinct areas.

- Standard registers // Direct register access
- MDIO Manageable device (MMD) registers // Indirect register access

Table 8. Standard Registers

Register Number (hex)	Description
IEEE-Defined Registers	
0h	Basic Control
1h	Basic Status
2h	PHY Identifier 1
3h	PHY Identifier 2
4h	Auto-Negotiation Advertisement
5h	Auto-Negotiation Link Partner Ability
6h	Auto-Negotiation Expansion
7h	Auto-Negotiation Next Page
8h	Auto-Negotiation Link Partner Next Page Ability
9h – Ch	Reserved
Dh	MMD Access Control Register
Eh	MMD Access Address Data Register
Fh	Reserved
Vendor-Specific Registers	
10h	Digital Control
11h	AFE Control 0
12h	Reserved
13h	AFE Control 2
14h	AFE Control 3
15h	RXER Counter
16h	Operation Mode
17h	Operation Mode Strap Status
18h	Expanded Control
19h – 1Ah	Reserved
1Bh	Interrupt Control/Status
1Ch	Function Control
1Dh	LinkMD® Control/Status
1Eh	PHY Control 1
1Fh	PHY Control 2

The KSZ8061MN supports the following MMD device addresses and their associated register addresses, which make up the indirect MMD registers.

Table 9. MMD Registers

Device Address (Hex)	Register Address (Hex)	Description
7h	3Ch	EEE Advertisement
	3Dh	Link Partner EEE Advertisement
1Bh	0h	AFED Control
1Ch	ACh	Signal Quality

Standard Registers

Standard registers provide direct read/write access to a 32-register address space, as defined in Clause 22 of the IEEE 802.3 standard. Within this address space, the first 16 registers (0h to Fh) are defined according to the IEEEE specification, while the remaining 16 registers (10h to 1Fh) are defined specific to the PHY vendor.

Standard Register Description

Address	Name	Description	Mode[10]	Default
Register 0h – Basic Control				
0.15	Reset	1 = Software reset 0 = Normal operation This bit is self-cleared after a '1' is written to it.	RW/SC	0
0.14	Loopback	1 = Loop-back mode (MII TX to MII RX. Line side is disconnected.) 0 = Normal operation Loopback must be enabled both here and in register 1Ch.	RW	0
0.13	Speed Select	1 = 100Mbps 0 = 10Mbps This bit is ignored if auto-negotiation is enabled (register 0.12 = 1). At reset, this bit is set by strapping in pin 40 of the 48-pin device. (The 32-pin device has no strapping option for speed; this bit default is 1.) After reset, this bit may be overwritten.	RW	1
0.12	Auto-Negotiation Enable	1 = Enable auto-negotiation process 0 = Disable auto-negotiation process If enabled, auto-negotiation result overrides settings in register 0.13 and 0.8.	RW	Set by AUTONEG strapping pin. See "Strapping Options" section for details.
0.11	Power Down	1 = Power down mode 0 = Normal operation If software reset (register 0.15) is used to exit Power Down mode (register 0.11 = 1), two software reset writes (register 0.15 = 1) are required. First write clears Power Down mode; second write resets chip and re-latches the pin strapping pin values.	RW	0
0.10	Isolate	1 = Electrical isolation of PHY from MII 0 = Normal operation	RW	0

Note:

10. RW = Read/Write. RO = Read only.
SC = Self-cleared. LH = Latch high.
LL = Latch low.

Register Description (Continued)

Address	Name	Description	Mode[10]	Default
0.9	Restart Auto-Negotiation	1 = Restart auto-negotiation process 0 = Normal operation. This bit is self-cleared after a '1' is written to it.	RW/SC	0
0.8	Duplex Mode	1 = Full-duplex 0 = Half-duplex At reset, the duplex mode is set by strapping in pin 25 of the 48-pin device. This bit value is the inverse of the strapping input. (The 32-pin device has no strapping option for duplex mode.) After reset, this bit may be overwritten.	RW	1
0.7	Collision Test	1 = Enable COL test 0 = Disable COL test Note: COL is not supported in the 32-pin package.	RW	0
0.6:0	Reserved		RO	000_0000
Register 1h – Basic Status				
1.15	100Base-T4	1 = T4 capable 0 = Not T4 capable	RO	0
1.14	100Base-TX Full-Duplex	1 = Capable of 100Mbps full-duplex 0 = Not capable of 100Mbps full-duplex	RO	1
1.13	100Base-TX Half-Duplex	1 = Capable of 100Mbps half-duplex 0 = Not capable of 100Mbps half-duplex	RO	1
1.12	10Base-T Full-Duplex	1 = Capable of 10Mbps full-duplex 0 = Not capable of 10Mbps full-duplex	RO	1
1.11	10Base-T Half-Duplex	1 = Capable of 10Mbps half-duplex 0 = Not capable of 10Mbps half-duplex	RO	1
1.10:7	Reserved		RO	000_0
1.6	No Preamble	1 = Preamble suppression acceptable 0 = Normal preamble required	RW	1
1.5	Auto-Negotiation Complete	1 = Auto-negotiation process completed 0 = Auto-negotiation process not completed	RO	0
1.4	Remote Fault	1 = Remote fault 0 = No remote fault	RO/LH	0
1.3	Auto-Negotiation Ability	1 = Capable to perform auto-negotiation 0 = Not capable to perform auto-negotiation	RO	1
1.2	Link Status	1 = Link is up 0 = Link is down	RO/LL	0
1.1	Jabber Detect	1 = Jabber detected 0 = Jabber not detected (default is low)	RO/LH	0
1.0	Extended Capability	1 = Supports extended capabilities registers	RO	1

Register Description (Continued)

Address	Name	Description	Mode[10]	Default
Register 2h – PHY Identifier 1				
2.15:0	PHY ID Number	Assigned to the 3rd through 18th bits of the Organizationally Unique Identifier (OUI). Kendin Communication's OUI is 0010A1 (hex)	RO	0022h
Register 3h – PHY Identifier 2				
3.15:10	PHY ID Number	Assigned to the 19th through 24th bits of the Organizationally Unique Identifier (OUI). Kendin Communication's OUI is 0010A1 (hex)	RO	0001_01
3.9:4	Model Number	Six bit manufacturer's model number	RO	01_0111
3.3:0	Revision Number	Four bit manufacturer's revision number	RO	Indicates silicon revision
Register 4h – Auto-Negotiation Advertisement				
4.15	Next Page	1 = Next page capable 0 = No next page capability	RW	1
4.14	Reserved		RO	0
4.13	Remote Fault	1 = Remote fault supported 0 = No remote fault	RW	0
4.12	Reserved		RO	0
4.11:10	Pause	[00] = No PAUSE [10] = Asymmetric PAUSE [01] = Symmetric PAUSE [11] = Asymmetric & Symmetric PAUSE	RW	00
4.9	100Base-T4	1 = T4 capable 0 = No T4 capability	RO	0
4.8	100Base-TX Full-Duplex	1 = 100Mbps full-duplex capable 0 = No 100Mbps full-duplex capability	RW	1
4.7	100Base-TX Half-Duplex	1 = 100Mbps half-duplex capable 0 = No 100Mbps half-duplex capability	RW	1
4.6	10Base-T Full-Duplex	1 = 10Mbps full-duplex capable 0 = No 10Mbps full-duplex capability	RW	1
4.5	10Base-T Half-Duplex	1 = 10Mbps half-duplex capable 0 = No 10Mbps half-duplex capability	RW	1
4.4:0	Selector Field	[00001] = IEEE 802.3	RW	0_0001

Register Description (Continued)

Address	Name	Description	Mode[10]	Default
Register 5h – Auto-Negotiation Link Partner Ability				
5.15	Next Page	1 = Next page capable 0 = No next page capability	RO	0
5.14	Acknowledge	1 = Link code word received from partner 0 = Link code word not yet received	RO	0
5.13	Remote Fault	1 = Remote fault detected 0 = No remote fault	RO	0
5.12	Reserved		RO	0
5.11:10	Pause	[00] = No PAUSE [10] = Asymmetric PAUSE [01] = Symmetric PAUSE [11] = Asymmetric & Symmetric PAUSE	RO	00
5.9	100Base-T4	1 = T4 capable 0 = No T4 capability	RO	0
5.8	100Base-TX Full-Duplex	1 = 100Mbps full-duplex capable 0 = No 100Mbps full-duplex capability	RO	0
5.7	100Base-TX Half-Duplex	1 = 100Mbps half-duplex capable 0 = No 100Mbps half-duplex capability	RO	0
5.6	10Base-T Full-Duplex	1 = 10Mbps full-duplex capable 0 = No 10Mbps full-duplex capability	RO	0
5.5	10Base-T Half-Duplex	1 = 10Mbps half-duplex capable 0 = No 10Mbps half-duplex capability	RO	0
5.4:0	Selector Field	[00001] = IEEE 802.3	RO	0_0001
Register 6h – Auto-Negotiation Expansion				
6.15:5	Reserved		RO	0000_0000_000
6.4	Parallel Detection Fault	1 = Fault detected by parallel detection 0 = No fault detected by parallel detection	RO/LH	0
6.3	Link Partner Next Page Able	1 = Link partner has next page capability 0 = Link partner does not have next page capability	RO	0
6.2	Next Page Able	1 = Local device has next page capability 0 = Local device does not have next page capability	RO	1
6.1	Page Received	1 = New page received 0 = New page not received yet	RO/LH	0
6.0	Link Partner Auto-Negotiation Able	1 = Link partner has auto-negotiation capability 0 = Link partner does not have auto-negotiation capability	RO	0

Register Description (Continued)

Address	Name	Description	Mode[10]	Default
Register 7h – Auto-Negotiation Next Page				
7.15	Next Page	1 = Additional next page(s) will follow 0 = Last page	RW	0
7.14	Reserved		RO	0
7.13	Message Page	1 = Message page 0 = Unformatted page	RW	1
7.12	Acknowledge2	1 = Will comply with message 0 = Cannot comply with message	RW	0
7.11	Toggle	1 = Previous value of the transmitted link code word equaled logic one 0 = Logic zero	RO	0
7.10:0	Message Field	11-bit wide field to encode 2048 messages	RW	000_0000_0001
Register 8h – Link Partner Next Page Ability				
8.15	Next Page	1 = Additional Next Page(s) will follow 0 = Last page	RO	0
8.14	Acknowledge	1 = Successful receipt of link word 0 = No successful receipt of link word	RO	0
8.13	Message Page	1 = Message page 0 = Unformatted page	RO	0
8.12	Acknowledge2	1 = Able to act on the information 0 = Not able to act on the information	RO	0
8.11	Toggle	1 = Previous value of transmitted link code word equal to logic zero 0 = Previous value of transmitted link code word equal to logic one	RO	0
8.10:0	Message Field		RO	000_0000_0000

Register Description (Continued)

Address	Name	Description	Mode[10]	Default
Register Dh – MMD Access Control Register				
D.15:14	Function	00 = address 01 = data, no post increment 10 = data, post increment on reads and writes 11 = data, post increment on writes only	RW	00
D.13:5	Reserved	Write as 0, ignore on read	RW	00_0000_000
D.4:0	DEVAD	Device address	RW	0_0000
Register Eh – MMD Access Address Data Register				
E.15:0	Address Data	If D.15:14 = 00, this is MMD DEVAD's address register. Otherwise, this is MMD DEVAD's data register as indicated by the contents of its address register.	RW	0000_0000_0000_0000
Register 10h – Digital Control Register				
10.15:5	Reserved		RW	0000_0000_000
10.4	PLL off in EDPD Mode	This mode may optionally be combined with EDPD mode for additional power reduction. 1 = PLL is off in EDPD mode 0 = PLL is on in EDPD mode	RW	0
10.3:0	Reserved		RW	0000
Register 11h – AFE Control 0 Register				
11.15:7	Reserved		RW	0000_0000_0
11.6	Slow Oscillator Mode	This mode substitutes the 25MHz clock with a slow oscillator clock, to save oscillator power during power down. 1 = Slow Oscillator mode enabled 0 = Slow Oscillator mode disabled	RW	0
11.5:0	Reserved		RW	00_0000
Register 13h – AFE Control 2 Register				
13.15	LinkMD Detector Threshold	Sets the threshold for the LinkMD pulse detector. Use high threshold with the large LinkMD pulse, and the low threshold with the small LinkMD pulse. Also see MMD address 1Bh, register 0h bits [7:4]. 1 = Enable high threshold comparator 0 = Disable high threshold comparator	RW	0
13.14:1	Reserved		RW	000_0000_0000_000
13.0	Slow Oscillator Mode for Ultra-Deep Sleep Mode	This mode substitutes the 25MHz clock with a slow oscillator clock, to save oscillator power if register access is required during Ultra Deep Sleep Mode. Note that the 1.2V supply is required if this mode is used. 1 = Slow Oscillator mode enabled 0 = Slow Oscillator mode disabled	RW	0

Register Description (Continued)

Address	Name	Description	Mode[10]	Default
Register 14h – AFE Control Register 3				
14.15:7	Reserved		RW	0000_0000_0
14.6	Ultra-Deep Sleep Method	1 = CPU Control method. Entry into Ultra-Deep Sleep Mode determined by value of register bit 14.5 0 = Automatic method. Enter into Ultra-Deep Sleep Mode automatically when no cable energy is detected	RW	0
14.5	Manual Ultra-Deep Sleep Mode	1 = Enter into Ultra-Deep Sleep Mode 0 = Normal operation This bit is used to enter Ultra-Deep Sleep Mode when the CPU Control method is selected in bit 14.6. To exit Ultra-Deep Sleep Mode, a hardware reset is required.	RW	0
14.4	NV Register Access	1 = Enable non-volatile copy of register 14h and bits [9:8] and [1:0] of register 13h 0 = Disable access to non-volatile registers When Ultra-Deep Sleep Mode is enabled, this bit must be set to 1.	RW	0
14.3	Ultra-Deep Sleep Mode and SIGDET Enable	1 = Ultra-Deep Sleep Mode is not enabled (but not necessarily entered), and SIGDET indicates cable energy detected 0 = Ultra-Deep Sleep Mode is disabled, and SIGDET output signal is forced true.	RW	0
14.2	Disable RX Internal Termination	1 = Disable RX internal termination 0 = Enable RX internal termination [Has no effect on TX internal termination.]	RW	0
14.1	Signal Detect De-assertion Timing Delay	When Ultra-Deep Sleep Mode is enabled, this bit determines the delay from loss of cable energy to de-assertion of SIGDET. When automatic method is selected for Ultra-Deep Sleep Mode, this delay also applies to powering down. 1 = Increased delay. This setting is required to allow automatic exiting of Ultra-Deep Sleep Mode (automatic method) if the link partner auto-negotiation is enabled, if auto-MDI/MDI-X is enabled, or if linking at 10Base-T. 0 = Minimum delay. When using the Automatic method for Ultra-Deep Sleep, use this setting only if the link partner's auto-negotiation is disabled, auto-MDI/MDI-X is disabled, and linking is at 100Base-TX. This setting may also be used for CPU Control method.	RW	0
14.0	Signal Detect Polarity	1 = SIGDET is active low (low = signal detected) 0 = SIGDET is active high (high = signal detected)	RW	0

Register Description (Continued)

Address	Name	Description	Mode[10]	Default
Register 15h – RXER Counter				
15.15:0	RXER Counter	Receive error counter for symbol error frames	RO/SC	0000h
Register 16h – Operation Mode				
16.15:13	Reserved		RW	000
16.12	QWF disable	1 = Disable Quiet-WIRE Filtering 0 = Enable Quiet- WIRE Filtering	RW	Strapping input at RXER pin
16.11:0	Reserved		RW	0000_0000_0000
Register 17h – Operation Mode Strap Status				
17.15:13	PHYAD[2:0] strap-in status	[000] = Strap to PHY Address 0 [001] = Strap to PHY Address 1 [010] = Strap to PHY Address 2 [011] = Strap to PHY Address 3 [100] = Strap to PHY Address 4 [101] = Strap to PHY Address 5 [110] = Strap to PHY Address 6 [111] = Strap to PHY Address 7	RO	
17.12:9	Reserved		RO	
17.8	QWF strap-in status	1 = Strap to disable Quiet-WIRE Filtering 0 = Strap to enable Quiet- WIRE Filtering	RO	Strapping input at RXER pin
17.7	MII B-to-B strap-in status	1 = Strap to MII Back-to-Back mode	RO	
17.6	Reserved		RO	
17.5	NAND Tree strap-in status	1 = Strap to NAND Tree mode	RO	
17.4:1	Reserved		RO	
17.0	MII strap-in status	1 = Strap to MII normal mode	RO	
Register 18h – Expanded Control				
18.15:12	Reserved		RW	0000
18.11	Energy Detect Power Down Mode disable	1 = Disable Energy Detect Power Down (EDPD) Mode 0 = Enable EDPD Mode	RW	1
18.10	RX PHY Latency	1 = Variable RX PHY latency with no preamble suppression 0 = Fixed RX PHY latency with possible suppression of one preamble octet	RW	0
18.9:7	Reserved		RW	00_0
18.6	Enable 10BT Preamble	When in Back-to-Back Mode and in 10Base-T, this bit must be set.	RW	0
18.5:0	Reserved		RW	00_0001

Register Description (Continued)

Address	Name	Description	Mode[10]	Default
Register 1Bh – Interrupt Control/Status				
1B.15	Jabber Interrupt Enable	1 = Enable Jabber Interrupt 0 = Disable Jabber Interrupt	RW	0
1B.14	Receive Error Interrupt Enable	1 = Enable Receive Error Interrupt 0 = Disable Receive Error Interrupt	RW	0
1B.13	Page Received Interrupt Enable	1 = Enable Page Received Interrupt 0 = Disable Page Received Interrupt	RW	0
1B.12	Parallel Detect Fault Interrupt Enable	1 = Enable Parallel Detect Fault Interrupt 0 = Disable Parallel Detect Fault Interrupt	RW	0
1B.11	Link Partner Acknowledge Interrupt Enable	1 = Enable Link Partner Acknowledge Interrupt 0 = Disable Link Partner Acknowledge Interrupt	RW	0
1B.10	Link Down Interrupt Enable	1= Enable Link Down Interrupt 0 = Disable Link Down Interrupt	RW	0
1B.9	Remote Fault Interrupt Enable	1 = Enable Remote Fault Interrupt 0 = Disable Remote Fault Interrupt	RW	0
1B.8	Link Up Interrupt Enable	1 = Enable Link Up Interrupt 0 = Disable Link Up Interrupt	RW	0
1B.7	Jabber Interrupt	1 = Jabber occurred 0 = Jabber did not occurred	RO/SC	0
1B.6	Receive Error Interrupt	1 = Receive Error occurred 0 = Receive Error did not occurred	RO/SC	0
1B.5	Page Receive Interrupt	1 = Page Receive occurred 0 = Page Receive did not occur	RO/SC	0
1B.4	Parallel Detect Fault Interrupt	1 = Parallel Detect Fault occurred 0 = Parallel Detect Fault did not occur	RO/SC	0
1B.3	Link Partner Acknowledge Interrupt	1 = Link Partner Acknowledge occurred 0 = Link Partner Acknowledge did not occur	RO/SC	0
1B.2	Link Down Interrupt	1 = Link Down occurred 0 = Link Down did not occur	RO/SC	0
1B.1	Remote Fault Interrupt	1 = Remote Fault occurred 0 = Remote Fault did not occur	RO/SC	0
1B.0	Link Up Interrupt	1 = Link Up occurred 0 = Link Up did not occur	RO/SC	0

Register Description (Continued)

Address	Name	Description	Mode[10]	Default
Register 1Ch – Function Control				
1C.15:6	Reserved		RW	0000_0000_00
1C. 5	Local Loopback Option	1 = Enable local loopback 0 = Disable local loopback Local loopback must be enabled both here and in register 0h.	RW	0
1C.4	LED0/TXER Pin Mode (KSZ8061MNX Pin 24)	This control bit only affects the 32-pin KSZ8061MNX. It does not apply to the 48-pin KSZ8061MNG. 1 = LED0/TXER pin functionality is determined by EEE enable/disable. When EEE is disabled (default), the pin is LED0. When EEE is enabled, the pin is TXER. 0 = LED0/TXER pin function is forced to be TXER.	RW	1
1C.3:2	Reserved		RW	00
1C.1:0	Reserved		RO	00
Register 1Dh – LinkMD® Control/Status				
1D.15	Cable Diagnostic Test Enable	1 = Enable cable diagnostic test. After test has completed, this bit is self-cleared. 0 = Indicates cable diagnostic test (if enabled) has completed and the status information is valid for read.	RW/SC	0
1D.14:13	Cable Diagnostic Test Result	[00] = normal condition [01] = open condition has been detected in cable [10] = short condition has been detected in cable [11] = cable diagnostic test has failed	RO	00
1D.12	Short Cable Indicator	1 = Short cable (<10 meter) has been detected by LinkMD.	RO	0
1D.11:9	Reserved		RW	000
1D.8:0	Cable Fault Counter	Distance to fault	RO	0_0000_0000

Register Description (Continued)

Address	Name	Description	Mode[10]	Default
Register 1Eh – PHY Control 1				
1E.15:10	Reserved		RO	0000_00
1E.9	Enable Pause (Flow Control)	1 = Flow control capable 0 = No flow control capability	RO	0
1E.8	Link Status	1 = Link is up 0 = Link is down	RO	
1E.7	Polarity Status	1 = Polarity is reversed 0 = Polarity is not reversed	RO	
1E.6	Reserved		RO	0
1E.5	MDI/MDI-X State	1 = MDI-X 0 = MDI	RO	
1E.4	Energy Detect	1 = Presence of signal on receive differential pair 0 = No signal detected on receive differential pair	RO	
1E.3	PHY Isolate	1 = PHY in isolate mode 0 = PHY in normal operation [Same as register bit 0.10]	RW	0
1E.2:0	Operation Mode Indication	[000] = still in auto-negotiation [001] = 10Base-T half-duplex [010] = 100Base-TX half-duplex [011] = reserved [100] = reserved [101] = 10Base-T full-duplex [110] = 100Base-TX full-duplex [111] = reserved	RO	

Register Description (Continued)

Address	Name	Description	Mode[10]	Default
Register 1Fh – PHY Control 2				
1F.15	HP_MDIX	1 = HP Auto MDI/MDI-X mode 0 = Micrel Auto MDI/MDI-X mode	RW	1
1F.14	MDI/MDI-X Select	When Auto MDI/MDI-X is disabled, 1 = MDI-X Mode Transmit on RXP,RXM and Receive on TXP,TXM 0 = MDI Mode Transmit on TXP,TXM and Receive on RXP,RXM	RW	0
1F.13	Pair Swap Disable	1 = Disable auto MDI/MDI-X 0 = Enable auto MDI/MDI-X	RW	Value determined by strapping option
1F.12	Reserved		RW	0
1F.11	Force Link	1 = Force link pass 0 = Normal link operation This bit bypasses the control logic and allow transmitter to send pattern even if there is no link.	RW	0
1F.10	Power Saving	1 = Enable power saving 0 = Disable power saving	RW	0
1F.9	Interrupt Level	1 = Interrupt pin active high 0 = Interrupt pin active low	RW	0
1F.8	Enable Jabber	1 = Enable jabber counter 0 = Disable jabber counter	RW	1
1F.7:6	Reserved		RW	00
1F.5:4	LED Mode	[00] = LED1: Speed, LED0: Link / Activity [01] = LED1: Activity, LED0: Link [10] = reserved [11] = reserved	RW	01 (KSZ8061MNX) 00 (KSZ8061MNG)
1F.3	Disable Transmitter	1 = Disable transmitter 0 = Enable transmitter	RW	0
1F.2	Remote Loopback	1 = Remote (analog) loopback is enabled 0 = Normal mode	RW	0
1F.1	Enable SQE Test	1 = Enable SQE test 0 = Disable SQE test	RW	0
1F.0	Disable Data Scrambling	1 = Disable scrambler 0 = Enable scrambler	RW	0

MMD Registers

MMD registers provide indirect read/write access to up to 32 MMD device addresses with each device supporting up to 65,536 16-bit registers, as defined in clause 22 of the IEEE 802.3 specification. The KSZ8061, however, uses only a small fraction of the available registers. See the Register Map section for a list of supported MMD device addresses and their associated register addresses.

The following two standard registers serve as the portal registers to access the indirect MMD registers.

- Standard register Dh – MMD Access – Control
- Standard register Eh – MMD Access – Register/Data

Address	Name	Description	Mode[10]	Default
Register Dh – MMD Access Control Register				
D.15:14	Function	00 = address 01 = data, no post increment 10 = data, post increment on reads and writes 11 = data, post increment on writes only	RW	00
D.13:5	Reserved	Write as 0, ignore on read	RW	00_0000_000
D.4:0	DEVAD	These five bits set the MMD device address	RW	0_0000
Register Eh – MMD Access Address Data Register				
E.15:0	Address/Data	When register Dh, bits [15:14] = 00, this register contains the MMD DEVAD's address register. Otherwise, this register contains the MMD DEVAD's data register as indicated by the contents of its address register.	RW	0000_0000_0

Examples:

MMD Register Write

Write MMD – Device Address 7h, Register 3Ch = 0002h to enable EEE advertisement.

1. Write Register Dh with 0007h // Set up register address for MMD – Device Address 7h.
2. Write Register Eh with 003Ch // Select register 3Ch of MMD – Device Address 7h.
3. Write Register Dh with 4007h // Select register data for MMD – Device Address 7h, Register 3Ch.
4. Write Register Eh with 0002h // Write value 0002h to MMD – Device Address 7h, Register 3Ch.

MMD Register Read

Read MMD – Device Address 1Fh, Register 19h – 1Bh

1. Write Register Dh with 001Fh // Set up register address for MMD – Device Address 1Fh.
2. Write Register Eh with 0019h // Select register 19h of MMD – Device Address 1Fh.
3. Write Register Dh with 801Fh // Select register data for MMD – Device Address 1Fh, Register 19h
   // with post increments.
4. Read Register Eh // Read data in MMD – Device Address 1Fh, Register 19h.
5. Read Register Eh // Read data in MMD – Device Address 1Fh, Register 1Ah.
6. Read Register Eh // Read data in MMD – Device Address 1Fh, Register 1Bh.

MMD Registers

Address	Name	Description	Mode[10]	Default
MMD Address 7h, Register 3Ch – EEE Advertisement				
7.3C.15:8	Reserved	Reserved	RO	0000_0000
7.3C.7:3	Reserved	Reserved	RW	0000_0
7.3C.2	1000Base-T EEE Capable	0 = 1000Mbps EEE is not supported	RW	0
7.3C.1	100Base-TX EEE Capable	1 = 100Mbps EEE capable 0 = No 100Mbps EEE capability This bit is set to '0' as the default after power-up or reset. Set this bit to '1' to enable 100Mbps EEE mode.	RW	0
7.3C.0	Reserved	Reserved	RW	0
MMD Address 7h, Register 3Dh – Link Partner EEE Advertisement				
7.3D.15:3	Reserved	Reserved	RO	0000_0000_0000_0
7.3D.2	Link Partner 1000Base-T EEE Capable	1 = Link partner is 1000Mbps EEE capable 0 = Link partner is not 1000Mbps EEE capable	RO	0
7.3D.1	Link Partner 100Base-TX EEE Capable	1 = Link partner is 100Mbps EEE capable 0 = Link partner is not 100Mbps EEE capable	RO	0
7.3D.0	Reserved	Reserved	RO	0
MMD Address 1Bh, Register 0h – AFED Control Register				
1B.0.15:8	Reserved	Reserved	RW	0000_0000
1B.0.7:4	LinkMD Pulse Amplitude	Sets the amplitude of the LinkMD pulse. Default value (0x2) is a small pulse. Set to 0x7 for a large pulse. Also see register 13h bit [15].	RW	0010
1B.0.3:0	Reserved	Reserved	RW	0000
MMD Address 1Ch, Register ACh – Signal Quality Register				
1C.AC.15	Reserved	Reserved	RO	0
1C.AC.14:8	Signal Quality Indicator	SQI indicates relative quality of the signal. A lower value indicates better signal quality.	RO	xxx_xxxx
1C.AC.7:0	Reserved	Reserved	RO	0000_0000

Absolute Maximum Ratings[11]

Supply Voltage
- (VDDIO, AVDDH) ..... –0.5V to +5.0V
- (VDDL, AVDDL) ..... –0.5V to +1.8V

Input Voltage (all inputs) ..... –0.5V to +5.0V
Output Voltage (all outputs) ..... –0.5V to +5.0V
Lead Temperature (soldering, 10sec.) ..... 260°C
Storage Temperature (T_s) ..... –55°C to +150°C
HBM ESD Rating 5kV

Operating Ratings[12]

Supply Voltage
- (AVDDH @ 3.3V) ..... +3.135V to +3.465V
- (VDDIO @ 3.3V) ..... +3.135V to +3.465V
- (VDDIO @ 2.5V) ..... +2.375V to +2.625V
- (VDDIO @ 1.8V)[13] ..... +1.71V to +1.89V
- (VDDL, AVDDL) ..... +1.14V to +1.26V

Ambient Temperature
- (T_A, Industrial) ..... –40°C to +85°C
- (T_A, Extended) ..... –40°C to +105°C

Maximum Junction Temperature (T_J max.) ..... 125°C
Thermal Resistance (θ_{JA}, 32-QFN, 32-WQFN) ..... 34°C/W
Thermal Resistance (θ_{JC}, 32-QFN, 32-WQFN) ..... 6°C/W
Thermal Resistance (θ_{JA}, 48-QFN) ..... 36°C/W
Thermal Resistance (θ_{JC}, 48-QFN) ..... 9°C/W

Electrical Characteristics[14]

T_A = 25°C, **bold** values indicate –40°C≤ T_A ≤ +85°C, unless noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Supply Current for VDDL, AVDDL						
I_{CORE}	1.2V Current for VDDL + AVDDL	No link, attempting to auto-negotiate		59		mA
		100BASE-TX full-duplex at 100% utilization		45		mA
		100BASE-TX link up, no traffic		45		mA
		10BASE-T full-duplex at 100% utilization		17		mA
		10BASE-T link up, no traffic		17		mA
		Energy Efficient Ethernet (EEE), both TX and RX in LPI state		14		mA
		Energy Detect Power Down (EDPD) mode, no link partner (reg. 18h.11 = 0)		16		mA
		EDPD mode with PLL off, no link partner (reg. 18h.11 = 0; reg. 10h.4 = 1)		0.7		mA
		Power Down mode (reg. 0h.11 = 1)		0.5		mA
		Power Down mode, MII isolate, slow oscillator mode (reg. 0h.11 = 1; reg. 0h.10 = 1; reg. 11h.6 = 1)		0.05		mA
		Ultra Deep Sleep mode with 1.2V (reg. 14h = 0x0078)		46		µA
		Ultra Deep Sleep mode, VDDL and AVDDL = 0V (reg. 14h = 0x0078)		0		µA

Notes:

11. Exceeding the absolute maximum rating may damage the device. Stresses greater than the absolute maximum rating may cause permanent damage to the device. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.
12. The device is not guaranteed to function outside its operating ratings.
13. VDDIO may be operated at 1.8V only for the KSZ8061MNX and KSZ8061MNG devices. The lowest allowed VDDIO voltage for the KSZ8061RNB and KSZ8061RND is 2.5V.
14. Specification is for packaged product only.

Electrical Characteristics[14] (Continued)

T_A = 25°C, **bold** values indicate –40°C≤ T_A ≤ +85°C, unless noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Supply Current for VDDIO						
$I_{VDDIO_1.8}$	1.8V Current for Digital I/Os	No link, attempting to auto-negotiate		2.3		mA
		100BASE-TX full-duplex at 100% utilization		3.8		mA
		100BASE-TX link up, no traffic		2.3		mA
		10BASE-T full-duplex at 100% utilization		0.5		mA
		10BASE-T link up, no traffic		0.4		mA
		Energy Efficient Ethernet (EEE), both TX and RX in LPI state		1.3		mA
		Energy Detect Power Down (EDPD) mode, no link partner (reg. 18h.11 = 0)		2.3		mA
		EDPD mode with PLL off, no link partner (reg. 18h.11 = 0; reg. 10h.4 = 1)		0.15		mA
		Power Down mode (reg. 0h.11 = 1)		0.17		mA
		Power Down mode, MII isolate, slow oscillator mode (reg. 0h.11 = 1; reg. 0h.10 = 1; reg. 11h.6 = 1)		0.04		mA
		Ultra-Deep Sleep mode with 1.2V (reg. 14h = 0x0078)		43		µA
		Ultra-Deep Sleep mode, VDDL and AVDDL = 0V (reg. 14h = 0x0078)		0.2		µA
$I_{VDDIO_2.5}$	2.5V Current for Digital I/Os	No link, attempting to auto-negotiate		3.3		mA
		100BASE-TX full-duplex at 100% utilization		5.9		mA
		100BASE-TX link up, no traffic		3.3		mA
		10BASE-T full-duplex at 100% utilization		1.0		mA
		10BASE-T link up, no traffic		0.6		mA
		Energy Efficient Ethernet (EEE), both TX and RX in LPI state		1.9		mA
		Energy Detect Power Down (EDPD) mode, no link partner (reg. 18h.11 = 0)		3.9		mA
		EDPD mode with PLL off, no link partner (reg. 18h.11 = 0; reg. 10h.4 = 1)		0.23		mA
		Power Down mode (reg. 0h.11 = 1)		0.23		mA
		Power Down mode, MII isolate, slow oscillator mode (reg. 0h.11 = 1; reg. 0h.10 = 1; reg. 11h.6 = 1)		0.10		mA
		Ultra-Deep Sleep mode with 1.2V (reg. 14h = 0x0078)		100		µA
		Ultra-Deep Sleep mode, VDDL and AVDDL = 0V (reg. 14h = 0x0078)		0.01		µA

Electrical Characteristics[14] (Continued)

T_A = 25°C, **bold** values indicate –40°C≤ T_A ≤ +85°C, unless noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Supply Current for VDDIO						
$I_{VDDIO_3.3}$	3.3V Current for Digital I/Os	No link, attempting to auto-negotiate		6.5		mA
		100BASE-TX full-duplex at 100% utilization		11		mA
		100BASE-TX link up, no traffic		6.5		mA
		10BASE-T full-duplex at 100% utilization		1.7		mA
		10BASE-T link up, no traffic		1.1		mA
		Energy Efficient Ethernet (EEE), both TX and RX in LPI state		3.6		mA
		Energy Detect Power Down (EDPD) mode, no link partner (reg. 18h.11 = 0)		6.6		mA
		EDPD mode with PLL off, no link partner (reg. 18h.11 = 0; reg. 10h.4 = 1)		0.56		mA
		Power Down mode (reg. 0h.11 = 1)		0.51		mA
		Power Down mode, MII isolate, slow oscillator mode (reg. 0h.11 = 1; reg. 0h.10 = 1; reg. 11h.6 = 1)		0.18		mA
		Ultra-Deep Sleep mode with 1.2V (reg. 14h = 0x0078)		180		µA
		Ultra-Deep Sleep mode, VDDL and AVDDL = 0V (reg. 14h = 0x0078)		0.01		µA

Electrical Characteristics[14] (Continued)

T_A = 25°C, **bold** values indicate –40°C≤ T_A ≤ +85°C, unless noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Supply Current for AVDDH						
$I_{AVDDH_3.3}$	3.3V Current for Transceiver	No link, attempting to auto-negotiate		19		mA
		100BASE-TX full-duplex at 100% utilization		24		mA
		100BASE-TX link up, no traffic		24		mA
		10BASE-T full-duplex at 100% utilization		28		mA
		10BASE-T link up, no traffic		16		mA
		Energy Efficient Ethernet (EEE), both TX and RX in LPI state		10		mA
		Energy Detect Power Down (EDPD) mode, no link partner (reg. 18h.11 = 0)		4.3		mA
		EDPD mode with PLL off, no link partner (reg. 18h.11 = 0; reg. 10h.4 = 1)		2.2		mA
		Power Down mode (reg. 0h.11 = 1)		1.0		mA
		Power Down mode, MII isolate, slow oscillator mode (reg. 0h.11 = 1; reg. 0h.10 = 1; reg. 11h.6 = 1)		0.18		mA
		Ultra-Deep Sleep mode with 1.2V (reg. 14h = 0x0078)		0.5		µA
		Ultra-Deep Sleep mode, VDDL and AVDDL = 0V (reg. 14h = 0x0078)		0.4		µA

Electrical Characteristics[14] (Continued)

T_A = 25°C, **bold** values indicate –40°C≤ T_A ≤ +85°C, unless noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
CMOS Inputs (MDC, RESET, TXD, TXEN, TXER)						
V_{IH}	Input High Voltage	VDDIO = 3.3V	2.0			V
		VDDIO = 2.5V	1.5			
		VDDIO = 1.8V	1.1			
V_{IL}	Input Low Voltage	VDDIO = 3.3V			1.3	V
		VDDIO = 2.5V			1.0	
		VDDIO = 1.8V			0.7	
$\|I_{IN}\|$	Input Current	V_{IN} = GND ~ VDDIO			10	µA
CMOS Outputs (COL, CRS, LED, RXC, RXD, RXDV, RXER, SIGDET, TXC)						
V_{OH}	Output High Voltage	VDDIO = 3.3V, I_{OH} = 12 mA	2.4			V
		VDDIO = 2.5V, I_{OH} = 6 mA	2.0			
		VDDIO = 1.8V, I_{OH} = 10 mA	1.4			
V_{OL}	Output Low Voltage	VDDIO = 3.3V, I_{OL} = 6 mA			0.4	V
		VDDIO = 2.5V, I_{OL} = 5 mA			0.4	
		VDDIO = 1.8V, I_{OL} = 10 mA			0.4	
$\|I_{oz}\|$	Output Tri-State Leakage	V_{OUT} = GND ~ VDDIO			10	µA
All Pull-Up/Pull-Down Pins (including Strapping Pins)						
pu	Internal Pull-Up Resistance	VDDIO = 3.3V, external 4.7kΩ pull-down		33		kΩ
		VDDIO = 2.5V, external 4.7kΩ pull-down		47		kΩ
		VDDIO = 1.8V, external 4.7kΩ pull-down		82		kΩ
pd	Internal Pull-Down Resistance	VDDIO = 3.3V, external 4.7kΩ pull-up		36		kΩ
		VDDIO = 2.5V, external 4.7kΩ pull-up		48		kΩ
		VDDIO = 1.8V, external 4.7kΩ pull-up		80		kΩ
100Base-TX Transmit (measured differentially after 1:1 transformer)						
V_O	Peak Differential Output Voltage	100Ω termination across differential output	0.95		1.05	V
V_{IMB}	Output Voltage Imbalance	100Ω termination across differential output			2	%
t_r, t_f	Rise/Fall Time		3		5	ns
	Rise/Fall Time Imbalance		0		0.5	ns
	Duty Cycle Distortion				± 0.25	ns
	Overshoot				5	%
	Output Jitter	Peak-to-peak		0.7		ns
10Base-T Transmit (measured differentially after 1:1 transformer)						
V_P	Peak Differential Output Voltage	100Ω termination across differential output	2.2		2.8	V
	Jitter Added	Peak-to-peak			3.5	ns
t_r, t_f	Rise/Fall Time			25		ns
10Base-T Receive						
V_{SQ}	Squelch Threshold	5MHz square wave		400		mV

Electrical Characteristics[14] (Continued)

T_A = 25°C, **bold** values indicate –40°C≤ T_A ≤ +85°C, unless noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
100Mbps Mode – Industrial Applications Parameters						
	Clock Phase Delay – XI input to MII TXC output	XI (25MHz clock input) to MII TXC (25MHz clock output) delay, referenced to rising edges of both clocks.	15	20	25	ns
t_{llr}	Link Loss Reaction (Indication) Time	Link loss detected at receive differential inputs to PHY signal indication time for each of the following: 1. For LED Mode “00”, Speed LED output change from low (100Mbps) to high (10Mbps – default state for link-down). 2. For LED Mode “01”, Link LED output change from low (link-up) to high (link-down). 3. INTRP pin assertion for link-down status change.		4.8		µs

Timing Diagrams

MII Transmit Timing (10Base-T)

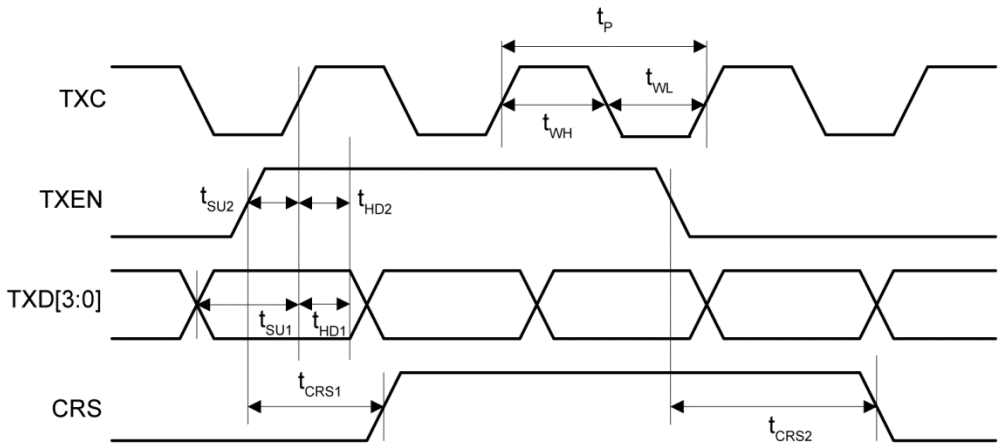


Figure 14. MII Transmit Timing (10Base-T)

Table 10. MII Transmit Timing (10Base-T) Parameters

Timing Parameter	Description	Min.	Typ.	Max.	Unit
t_P	TXC period		400		ns
t_{WL}	TXC pulse width low		200		ns
t_{WH}	TXC pulse width high		200		ns
t_{SU1}	TXD[3:0] setup to rising edge of TXC	120			ns
t_{SU2}	TXEN setup to rising edge of TXC	120			ns
t_{HD1}	TXD[3:0] hold from rising edge of TXC	0			ns
t_{HD2}	TXEN hold from rising edge of TXC	0			ns
t_{CRS1}	TXEN high to CRS asserted latency		600		ns
t_{CRS2}	TXEN low to CRS de-asserted latency		1.0		µs

MII Receive Timing (10Base-T)

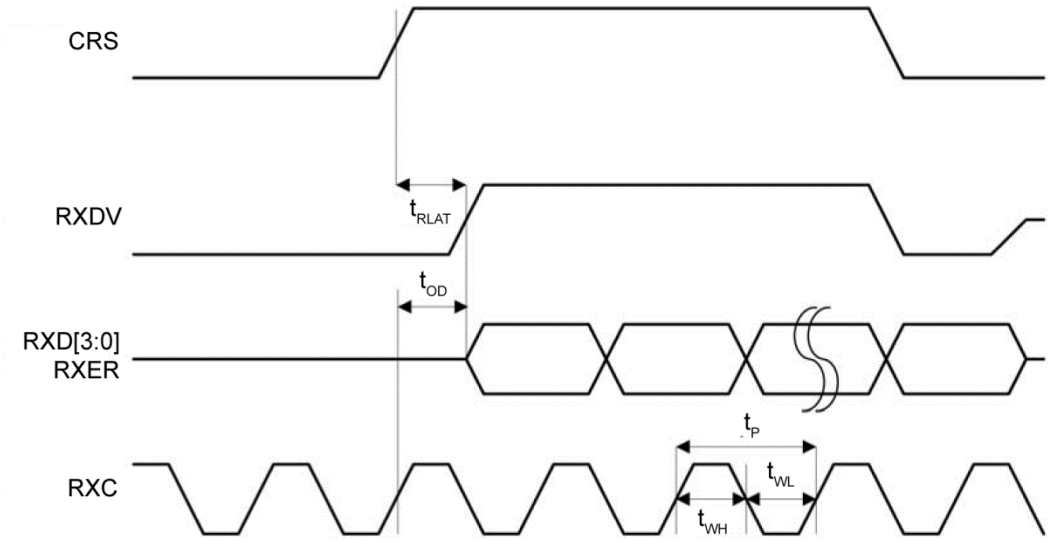


Figure 15. MII Receive Timing (10Base-T)

Table 11. MII Receive Timing (10Base-T) Parameters

Timing Parameter	Description	Min.	Typ.	Max.	Unit
t_P	RXC period		400		ns
t_{WL}	RXC pulse width low		200		ns
t_{WH}	RXC pulse width high		200		ns
t_{OD}	(RXDV, RXD[3:0], RXER) output delay from rising edge of RXC		205		ns
t_{RLAT}	CRS to (RXDV, RXD[3:0]) latency		7.2		µs

MII Transmit Timing (100Base-TX)

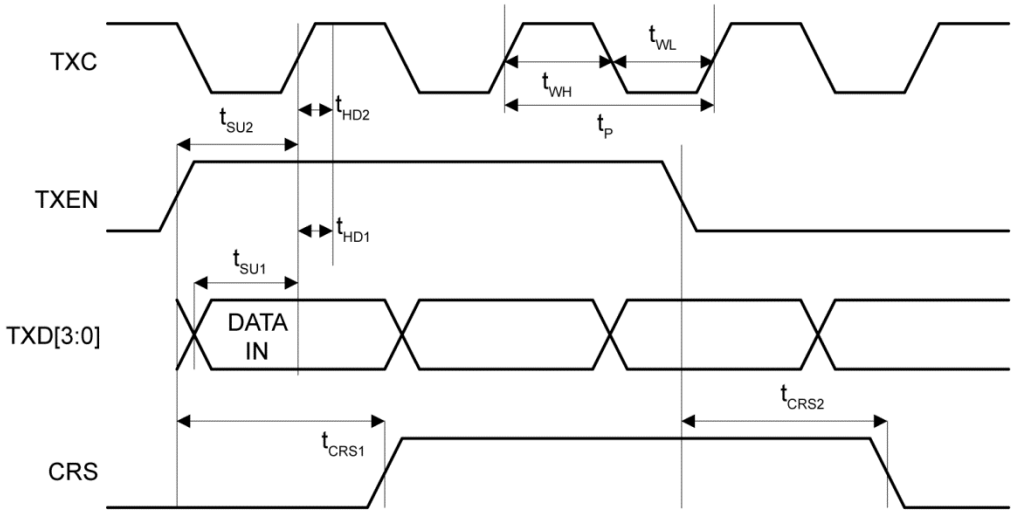


Figure 16. MII Transmit Timing (100Base-TX)

Table 12. MII Transmit Timing (100Base-TX) Parameters

Timing Parameter	Description	Min.	Typ.	Max.	Unit
t_P	TXC period		40		ns
t_{WL}	TXC pulse width low		20		ns
t_{WH}	TXC pulse width high		20		ns
t_{SU1}	TXD[3:0] setup to rising edge of TXC	10			ns
t_{SU2}	TXEN setup to rising edge of TXC	10			ns
t_{HD1}	TXD[3:0] hold from rising edge of TXC	0			ns
t_{HD2}	TXEN hold from rising edge of TXC	0			ns
t_{CRS1}	TXEN high to CRS asserted latency		72		ns
t_{CRS2}	TXEN low to CRS de-asserted latency		72		ns

MII Receive Timing (100Base-TX)

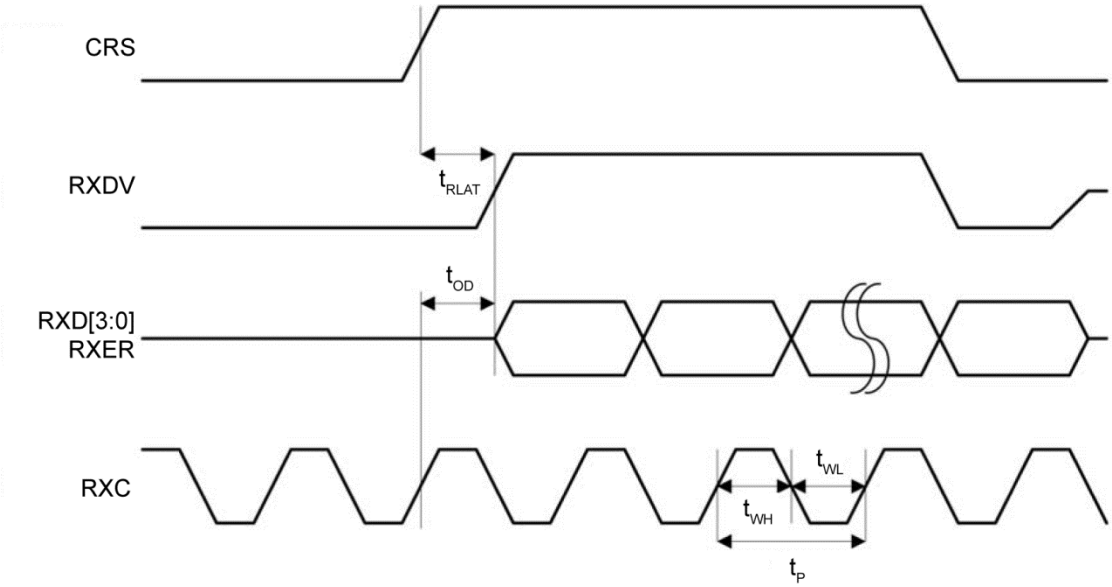


Figure 17. MII Receive Timing (100Base-TX)

Table 13. MII Receive Timing (100Base-TX) Parameters

Timing Parameter	Description	Min.	Typ.	Max.	Unit
t_P	RXC period		40		ns
t_{WL}	RXC pulse width low		20		ns
t_{WH}	RXC pulse width high		20		ns
t_{OD}	(RXDV, RXD[3:0], RXER) output delay from rising edge of RXC	13	22	28	ns
t_{RLAT}	CRS to (RXDV, RXD[3:0] latency		170		ns

Auto-Negotiation Timing

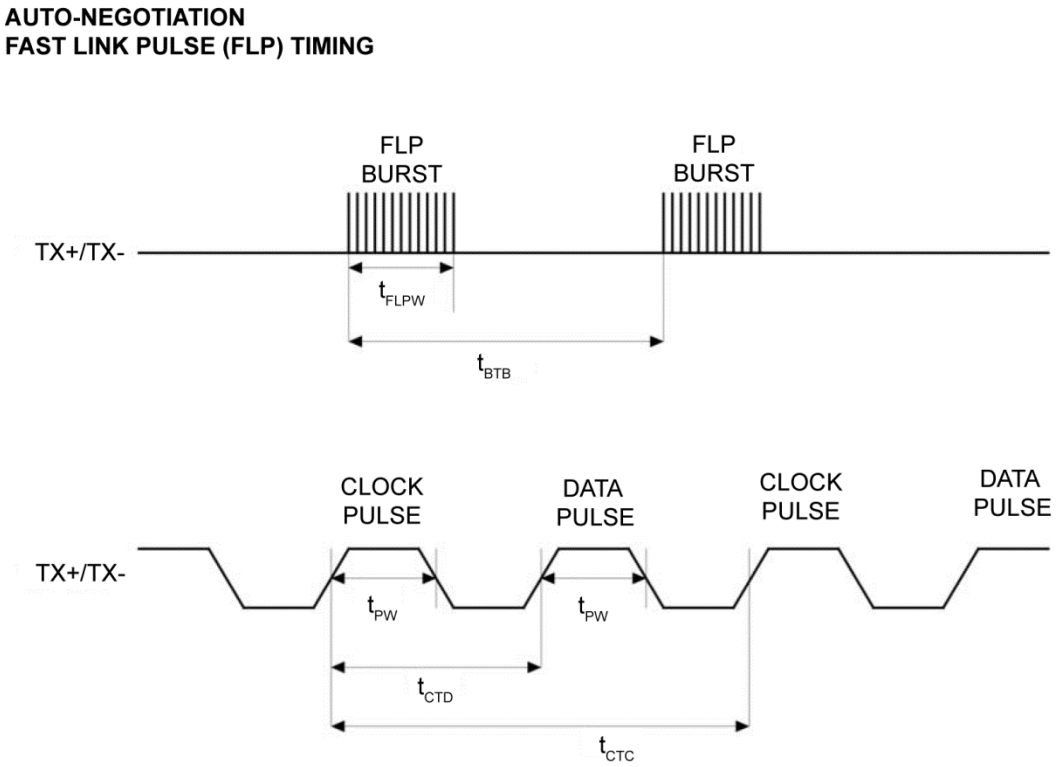


Figure 18. Auto-Negotiation Fast Link Pulse (FLP) Timing

Table 14. Auto-Negotiation Fast Link Pulse (FLP) Timing Parameters

Timing Parameter	Description	Min.	Typ.	Max.	Units
t_{BTB}	FLP Burst to FLP Burst	8	16	24	ms
t_{FLPW}	FLP Burst width		2		ms
t_{PW}	Clock/Data Pulse width		100		ns
t_{CTD}	Clock Pulse to Data Pulse	55.5	64	69.5	µs
t_{CTC}	Clock Pulse to Clock Pulse	111	128	139	µs
	Number of Clock/Data Pulse per FLP Burst	17		33	

MDC/MDIO Timing

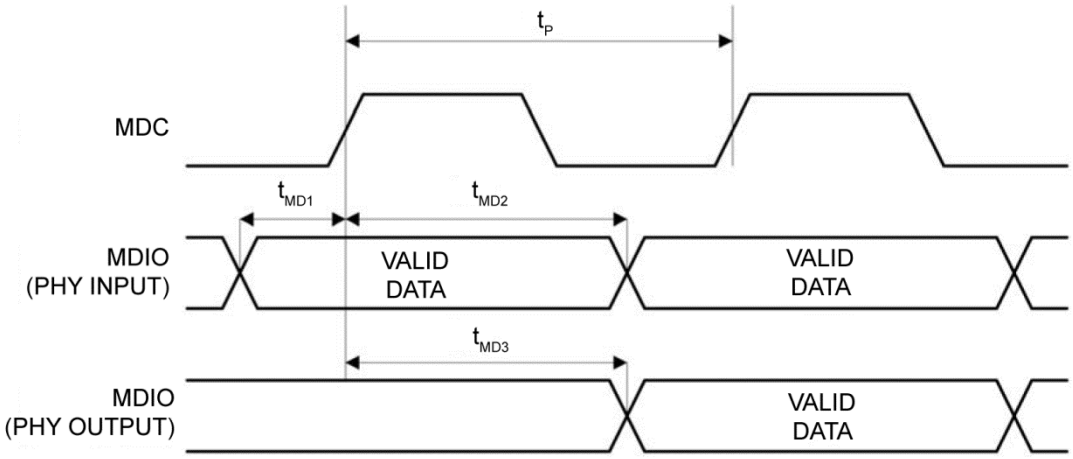


Figure 19. MDC/MDIO Timing

Table 14. MDC/MDIO Timing Parameters

Timing Parameter	Description	Min.	Typ.	Max.	Unit
t_P	MDC period	400			ns
t_{MD1}	MDIO (PHY input) setup to rising edge of MDC	10			ns
t_{MD2}	MDIO (PHY input) hold from rising edge of MDC	4			ns
t_{MD3}	MDIO (PHY output) delay from rising edge of MDC	5		Note 15	ns

Note:

15. Maximum high-to-low time is 25ns. Maximum low-to-high time is determined by the external pull-up resistor. Maximum low-to-high time is 25ns.

Power-up/Reset Timing

The KSZ8061MN reset timing requirement is summarized in Figure 20 and Table 15.

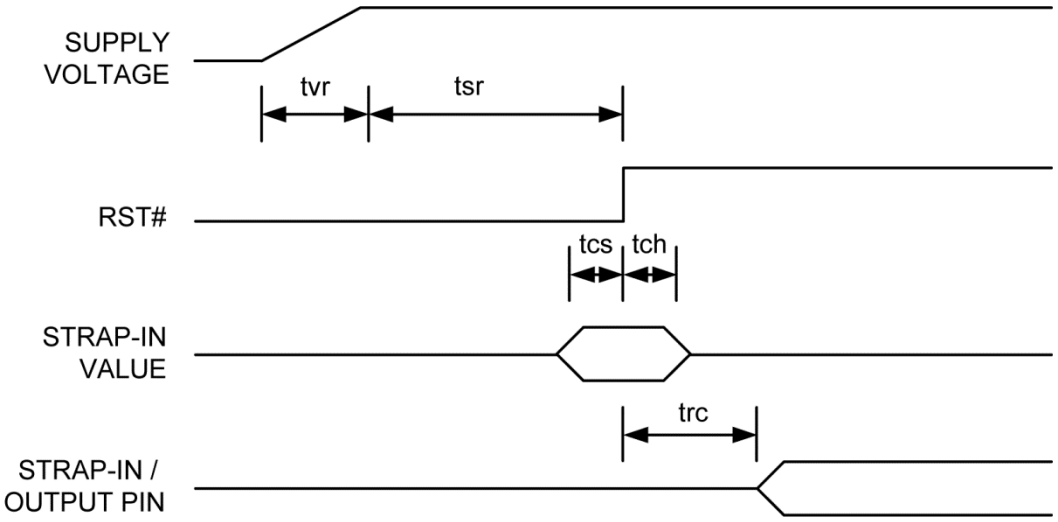


Figure 20. Power-up/Reset Timing

Table 15. Power-up/Reset Timing Parameters

Parameter	Description	Min.	Max.	Units
t_{vr}	Supply voltage (VDDIO, AVDD, VDDL, AVDDL) rise time	300		µs
t_{sr}	Stable supply voltage (VDDIO, AVDD, VDDL, AVDDL) to reset high	10		ms
t_{cs}	Configuration setup time	5		ns
t_{ch}	Configuration hold time	5		ns
t_{rc}	Reset to strap-in pin output	6		ns

The supply voltage (VDDIO, AVDD, VDDL, AVDDL) power-up waveforms should be monotonic, and the 300µs minimum rise time is from 10% to 90%.

For warm reset, the reset (RESET#) pin should be asserted low for a minimum of 500µs. The strap-in pin values are read and updated at the de-assertion of reset.

After the de-assertion of reset, it is recommended to wait a minimum of 100µs before starting programming on the MIIM (MDC/MDIO) Interface.

Reset Circuit

Figure 21 shows a reset circuit recommended for powering up the KSZ8061MN if reset is triggered by the power supply.

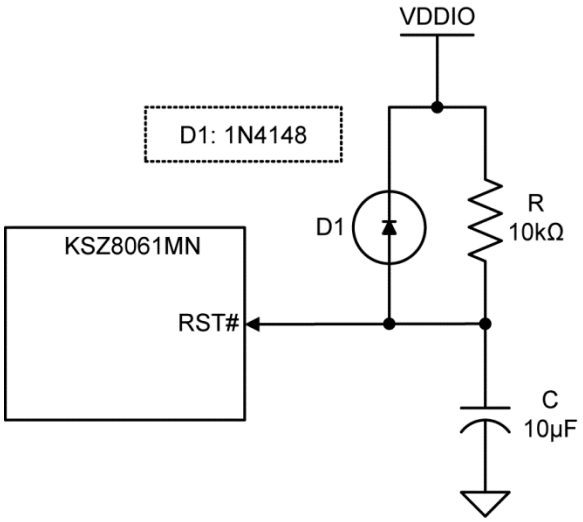


Figure 21. Recommended Reset Circuit

Figure 22 represents a reset circuit recommended for applications where reset is driven by another device (e.g., CPU or FPGA). At power-on-reset, R, C and D1 provide the necessary ramp rise time to reset the KSZ8061MN. The RST_OUT_n from CPU/FPGA provides the warm reset after power up.

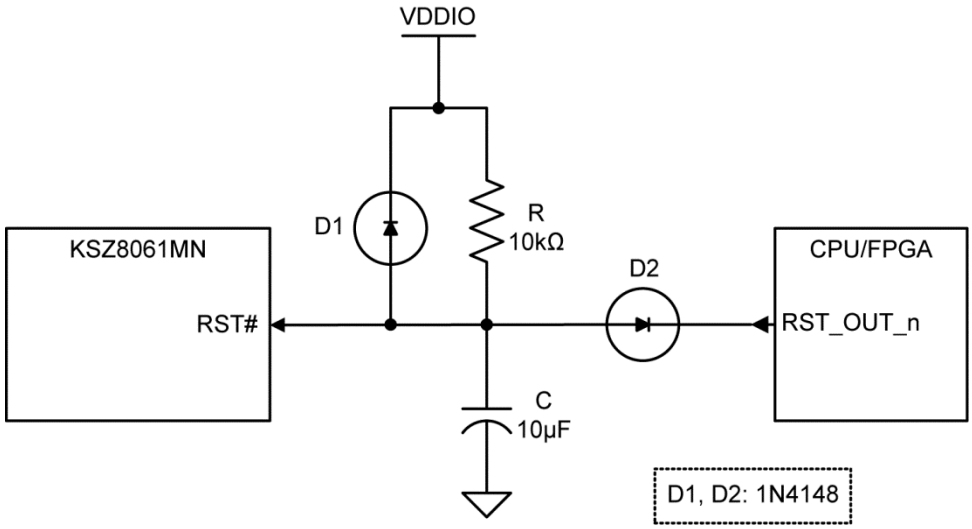


Figure 22. Recommended Reset Circuit for interfacing with CPU/FPGA Reset Output

Reference Clock – Connection and Selection

A crystal or external clock source, such as an oscillator, is used to provide the reference clock for the KSZ8061MN. For the KSZ8061MN in all operating modes, the reference clock is 25MHz. The reference clock connections to XI (pin 1) and XO (pin 2), and the reference clock selection criteria are provided in Figure 23 and Table 16.

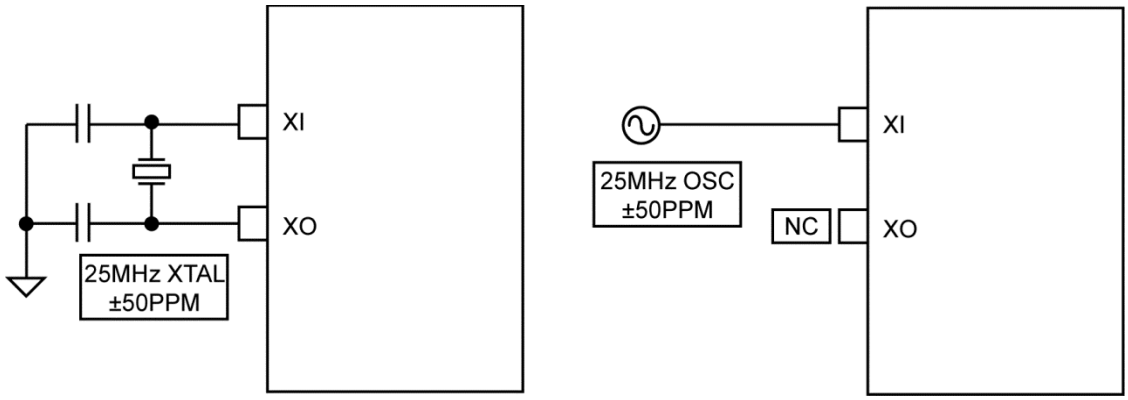


Figure 23. 25MHz Crystal/Oscillator Reference Clock Connection

Table 16. 25MHz Crystal/Reference Clock Selection Criteria

Characteristics	Value	Units
Frequency	25	MHz
Frequency tolerance (max)	±50	ppm

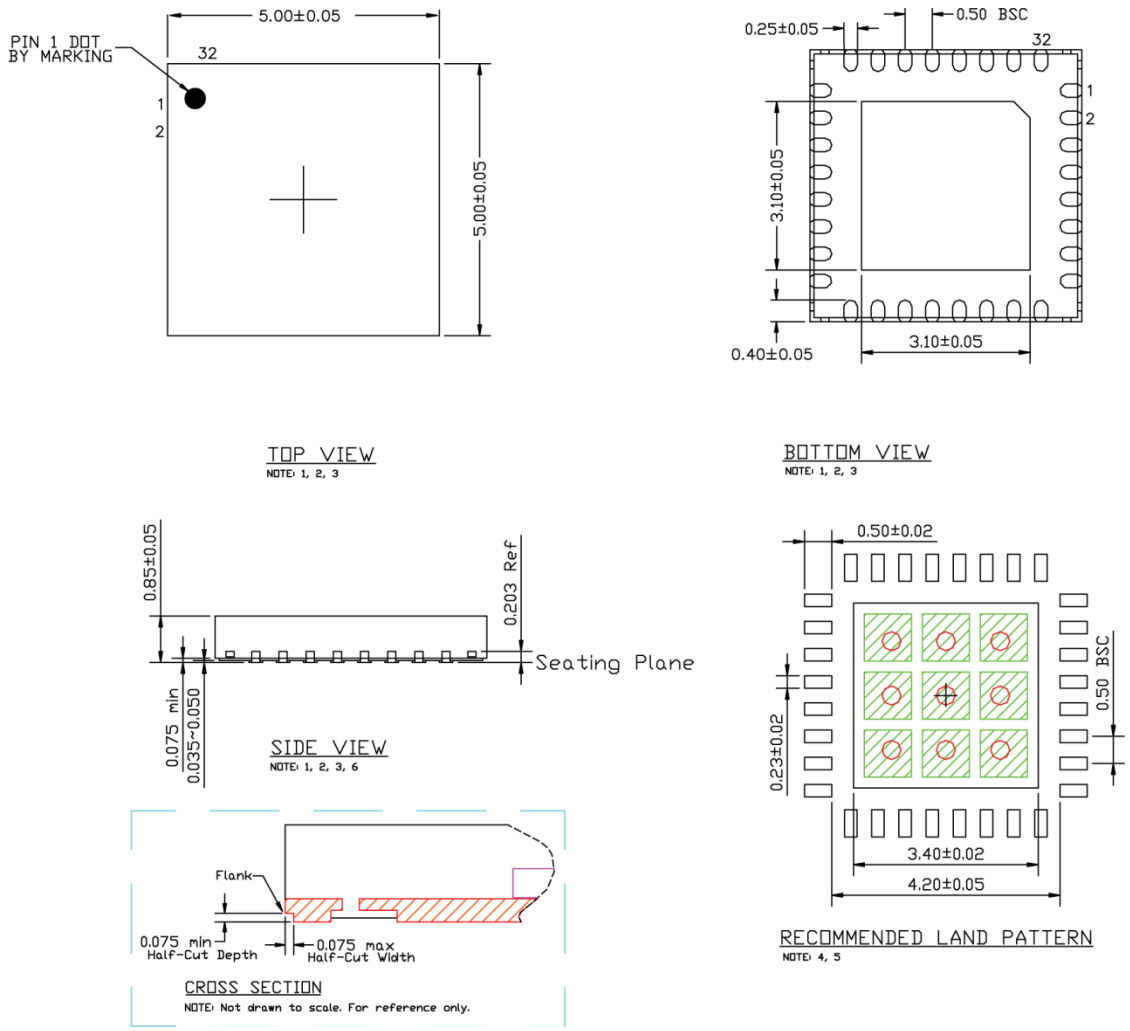
Table 17. Recommended Crystals

Manufacturer	Part Number
NDK[16]	NX2016SA
Murata[17]	XRCGB25M000F3A00R0

Notes:

16. NDK: www.ndk.com.
17. Murata: www.murata.com.

Package Information and Recommended Land Pattern[18]



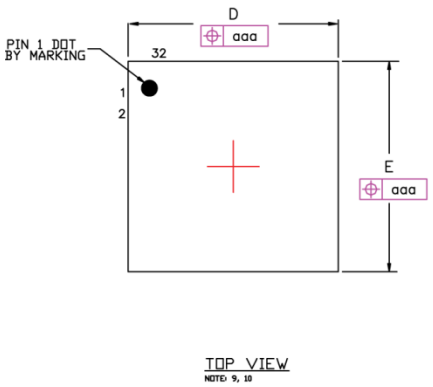
NOTE:
1. MAX PACKAGE WARPAGE IS 0.05mm.
2. MAX ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS.
3. PIN #1 IS ON TOP WILL BE LASER MARKED.
4. RED CIRCLES IN LAND PATTERN INDICATES THERMAL VIA. SIZE SHOULD BE 0.30-0.35mm IN DIAMETER, 1.00mm PITCH & SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE.
5. GREEN RECTANGLES (SHADED AREA) REPRESENT SOLDER STENCIL OPENING ON EXPOSED PAD AREA. RECOMMENDED SIZE IS 0.87x0.87mm, 1.07mm PITCH.
6. "W" IN WQFN IS WETTABLE FLANK PACKAGE.

32-Pin 5mm × 5mm WQFN

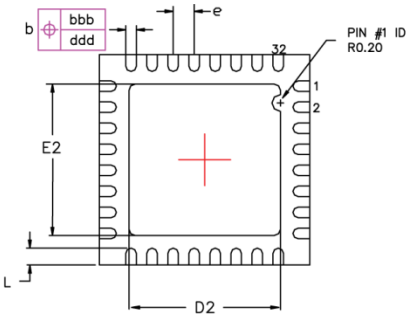
Note:

18. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

Package Information and Recommended Land Pattern[18] (Continued)

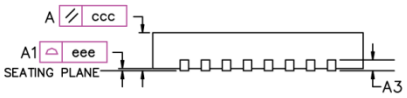


TOP VIEW
NOTE: 9, 10



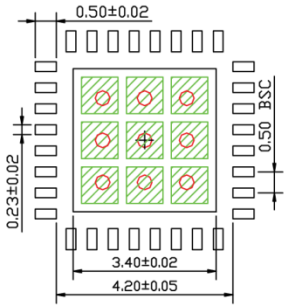
BOTTOM VIEW
NOTE: 9, 10

	DIMENSION IN mm		
SYMBOL	MIN	NOM	MAX
A	0.80	0.85	1.00
A1	0.00	0.02	0.05
A3		0.20 (REF)	
D		5.00 BSC	
D2	3.00	3.10	3.20
E		5.00 BSC	
E2	3.00	3.10	3.20
L	0.35	0.40	0.45



SIDE VIEW
NOTE: 9, 10

	b (mm)			e (mm)		
N	MIN	NOM	MAX	MIN	NOM	MAX
32	0.18	0.25	0.30		0.50 BSC	



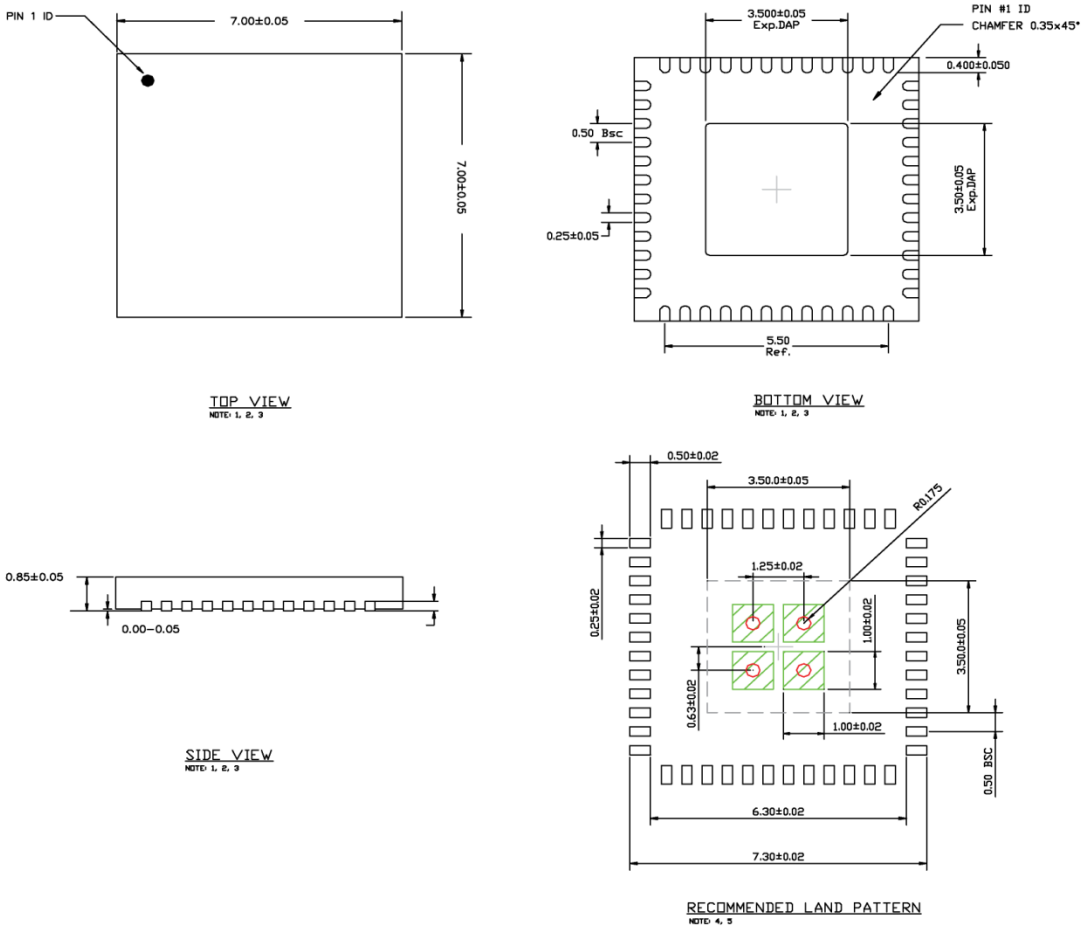
RECOMMENDED LAND PATTERN
NOTE: 11, 12

TOLERANCE OF FORM AND POSITION	
aaa	0.15
bbb	0.10
ccc	0.10
ddd	0.05
eee	0.08

NOTE:
1. REFER TO JEDEC STANDARD MO-220 VHHD-2.
2. DIMENSION "b" APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm TO 0.30mm FROM THE TERMINAL TIP.
3. "aaa" THE BILATERAL PROFILE TOLERANCE THAT CONTROLS THE POSITION OF THE PLASTIC BODY SIDES. THE CENTERS OF THE PROFILE ZONES ARE DEFINED BY THE BASIC DIMENSIONS "D" AND "E".
4. "bbb" THE TOLERANCE THAT CONTROLS THE POSITION OF THE ENTIRE TERMINAL PATTERN WITH RESPECT TO DATUM'S A AND B. THE CENTER OF THE TOLERANCE ZONE OF EACH TERMINAL IS DEFINED BY THE BASIC DIMENSION "e" AS RELATED TO DATUM A AND B.
5. "ccc" THE TOLERANCE LOCATED PARALLEL TO THE SEATING PLANE IN WHICH THE TOP SURFACE OF THE PACKAGE MUST BE LOCATED.
6. "ddd" THE TOLERANCE THAT CONTROLS THE POSITION OF THE TERMINALS TO EACH OTHER. THE CENTERS OF THE PROFILE ZONES ARE DEFINED BY BASIC DIMENSION "e".
7. "eee" THE UNILATERAL TOLERANCE LOCATED ABOVE THE SEATING PLANE WHEREIN THE BOTTOM SURFACE OF THE TERMINALS MUST BE LOCATED.
8. THE TOLERANCE THAT CONTROLS THE POSITION OF THE EXPOSED METAL HEAT FEATURE. THE CENTER OF THE TOLERANCE ZONE WILL BE THE DATUM'S DEFINED BY THE CENTERLINES OF THE PACKAGE BODY.
9. MAX PACKAGE WARPAGE IS 0.05 MM.
10. PIN #1 IS ON TOP WILL BE LASER MARKED.
11. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.35M IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE.
12. GREEN RECTANGLES (SHADED AREA) indicate SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.87x0.87 MM IN SIZE, 1.07 MM PITCH.
13. THIS DOCUMENT IS FOR AUTOMOTIVE PRODUCT USE ONLY.

32-Pin 5mm × 5mm QFN

Package Information and Recommended Land Pattern[18] (Continued)



NOTE:
1. MAX PACKAGE WARPAGE IS 0.05mm
2. MAX ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS.
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATES THERMAL VIA. SIZE SHOULD BE 0.30-0.35mm IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE. PITCH is 1.25mm.
5. GREEN RECTANGLES (SHADED AREA) REPRESENT SOLDER STENCIL OPENING ON EXPOSED PAD AREA. RECOMMENDED SIZE IS 1.00mm x 1.00mm, SPACING IS 0.25mm, PITCH is 1.25mm.

48-Pin 7mm × 7mm QFN

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Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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