

Evaluating the **ADXL356/ADXL357** Low Noise, Low Drift, Low Power, 3-Axis MEMS Accelerometers

FEATURES

- 2 sets of spaced vias for populating 6-pin headers
- Easily attaches to prototyping board or PCB
- Small size and board stiffness minimizes impact on the user system and acceleration measurements

EQUIPMENT NEEDED

External host processor

DOCUMENTS NEEDED

[ADXL356/ADXL357 data sheet](#)

GENERAL DESCRIPTION

The [EVAL-ADXL356BZ](#), the [EVAL-ADXL356CZ](#), and the [EVAL-ADXL357Z](#) are evaluation boards that allow quick evaluation of the performance of the [ADXL356](#) and the [ADXL357](#) low noise, low power, 3-axis, MEMS accelerometers. The [EVAL-ADXL356BZ](#) is an analog output supporting a ± 10 g or ± 20 g accelerometer, the [EVAL-ADXL356CZ](#) is an analog output supporting a ± 10 g or ± 40 g, and the [EVAL-ADXL357Z](#) is a digital output supporting a ± 10.24 g, ± 20.48 g, or ± 40.96 g accelerometer.

These evaluation boards are ideal for evaluating the [ADXL356](#) and [ADXL357](#) in an existing system because the stiffness and the small size of the evaluation board minimize the effect of the board on both the system and acceleration measurements.

Full details about the [ADXL356/ADXL357](#) are available in the [ADXL356/ADXL357 data sheet](#), which is available from Analog Devices, Inc., and must be consulted in conjunction with this user guide when using this evaluation board.

Note that the layout for the [EVAL-ADXL354BZ/EVAL-ADXL354CZ](#) applies to both the [EVAL-ADXL354BZ/EVAL-ADXL354CZ](#) and the [EVAL-ADXL356BZ/EVAL-ADXL356CZ](#), and that the layout for the [EVAL-ADXL355Z](#) applies to both the [EVAL-ADXL355Z](#) and the [EVAL-ADXL357Z](#).

EVALUATION BOARD PHOTOGRAPHS

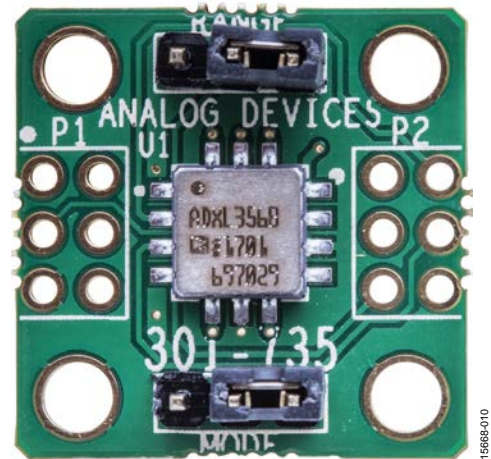


Figure 1. [EVAL-ADXL356BZ/EVAL-ADXL356CZ](#)



Figure 2. [EVAL-ADXL357Z](#)

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REVISION HISTORY

9/2018—Rev. 0 to Rev. A

| | |
|---|---|
| Changed Printed Circuit Board Layouts Section to Evaluation Board Photographs Section..... | 1 |
| Replaced Figure 1 and Figure 2 | 1 |
| Changes to General Description Section | 1 |
| Changes to Evaluation Board Hardware Section, Figure 3, Figure 4, Figure 5, Figure 6, and Circuit Description Section.... | 3 |
| Changes to Figure 7 and Figure 8..... | 4 |
| Changes to Table 1 and Table 2..... | 5 |

2/2017—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

The [EVAL-ADXL356BZ](#), the [EVAL-ADXL356CZ](#), and the [EVAL-ADXL357Z](#) allow users to access the individual connections of the [ADXL356](#) and the [ADXL357](#). Each of the evaluation boards includes decoupling capacitors for the supplies, a few discrete resistors that provide isolation on the V_{1P8ANA} and V_{1P8DIG} pins, and two 6-pin headers. Refer to the [ADXL356/ADXL357](#) data sheet for more details on the specific pin definitions. The power supplies for the [ADXL356](#) and the [ADXL357](#) are decoupled using multiple 0.1 μF ceramic (0603) capacitors.

The [EVAL-ADXL356BZ/EVAL-ADXL356CZ](#) has capacitors on each axis output to set the output low-pass filter and two 3-position jumpers to configure RANGE and MODE (tied to the [ADXL356](#) STBY pin). The two 6-pin headers provide access to all other pins.

Header P1 provides access to V_{DDIO} (used to set the RANGE pin and the STBY levels on the [ADXL356](#)), V_{DD} (which supplies the [ADXL356](#) V_{SUPPLY} pin), V_{SS}/V_{SSIO} (supply common connection), and X_{OUT} , Y_{OUT} , and Z_{OUT} , as shown in Figure 3.

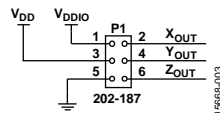


Figure 3. [EVAL-ADXL356BZ/EVAL-ADXL356CZ](#) Functional Block Diagram for Header P1

Header P2 provides access to V_{1P8ANA} , V_{1P8DIG} , TEMP, ST1, ST2, and V_{SS} (supply common connection), as shown in Figure 4.

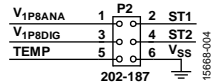


Figure 4. [EVAL-ADXL356BZ/EVAL-ADXL356CZ](#) Functional Block Diagram for Header P2

The [EVAL-ADXL357Z](#) uses two 6-pin headers to provide access to all pins. Header P1 provides access to V_{DDIO} , V_{DD} (which connects to the [ADXL357](#) V_{SUPPLY} pin), V_{SS}/V_{SSIO} (supply common connection), INT1, INT2, and DRDY, as shown in Figure 5.

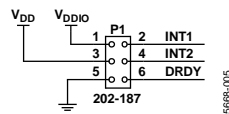


Figure 5. [EVAL-ADXL357Z](#) Functional Block Diagram for Header P1

Header P2 provides access to V_{1P8ANA} , V_{1P8DIG} , MISO/ASEL, $\overline{\text{CS}}$ /SCL, SCLK/ V_{SSIO} , and MOSI/SDA, as shown in Figure 6.

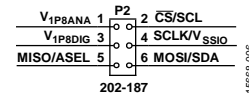


Figure 6. [EVAL-ADXL357Z](#) Functional Block Diagram for Header P2

The vias or headers allow the evaluation boards to attach to either a prototyping breadboard or a printed circuit board (PCB) in an existing user system. Four holes are provided in the corners of the evaluation boards for mechanical attachment of the evaluation boards in many applications. An external host processor is required for communication to the [ADXL357](#). The analog output of the [ADXL356](#) must be connected to a band limited analog-to-digital converter (ADC).

The dimensions of the evaluation boards are 0.8 in. \times 0.8 in.

CIRCUIT DESCRIPTION

The evaluation board photograph of the [EVAL-ADXL356BZ/EVAL-ADXL356CZ](#) is shown in Figure 1, and the evaluation board photograph of the [EVAL-ADXL357Z](#) is shown in Figure 2. The [ADXL356/ADXL357](#) each have two power modes. They can be powered either by integrated, low dropout (LDO) regulators or by external user supplied 1.8 V regulated supplies. Refer to the [ADXL356/ADXL357](#) data sheet for more information.

HANDLING CONSIDERATIONS

The [EVAL-ADXL356BZ](#), the [EVAL-ADXL356CZ](#), and the [EVAL-ADXL357Z](#) are not reverse polarity protected. Reversing any of the supply connections, including the V_{SS} and the V_{SSIO} pins, can cause damage to the [ADXL356/ADXL357](#).

Dropping the evaluation boards on a hard surface can generate several thousand g of acceleration, which can exceed the [ADXL356/ADXL357](#) data sheet absolute maximum limits.

EVALUATION BOARD SCHEMATICS

Note that the layout for the [EVAL-ADXL354BZ/EVAL-ADXL354CZ](#) applies to both the [EVAL-ADXL354BZ/EVAL-ADXL354CZ](#) and the [EVAL-ADXL356BZ/EVAL-ADXL356CZ](#)

(see Figure 1), and that the layout for the [EVAL-ADXL355Z](#) applies to both the [EVAL-ADXL355Z](#) and the [EVAL-ADXL357Z](#) (see Figure 2).

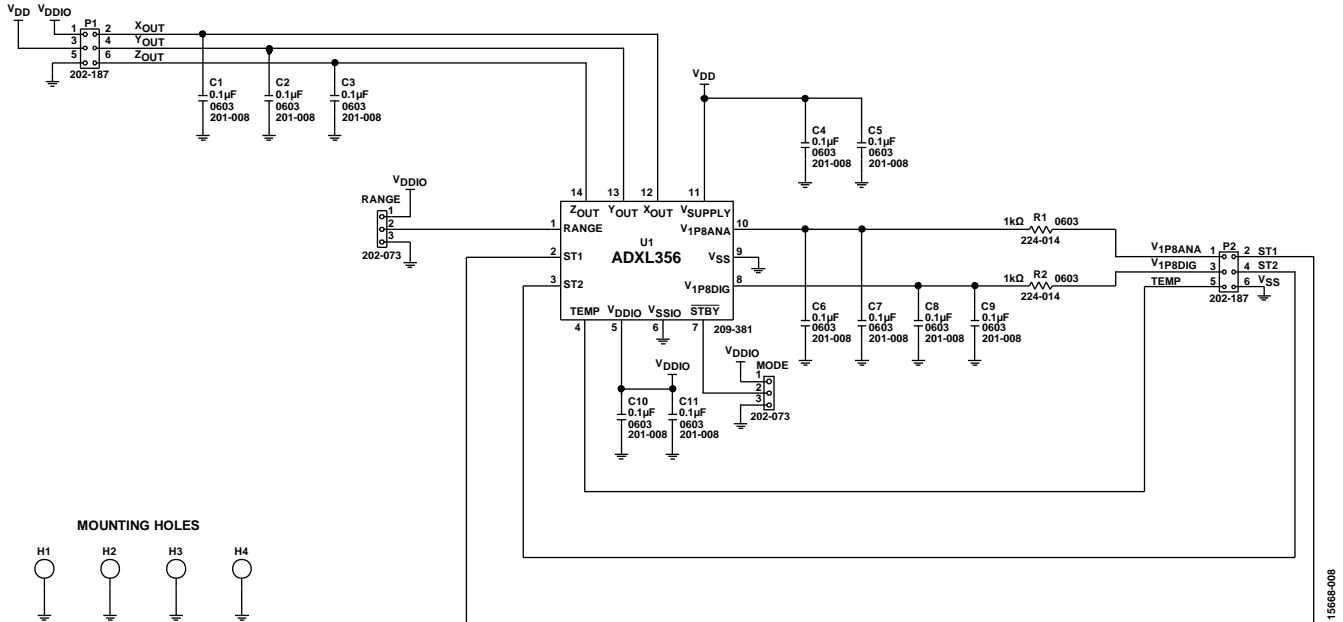


Figure 7. EVAL-ADXL356BZ/EVAL-ADXL356CZ Schematic

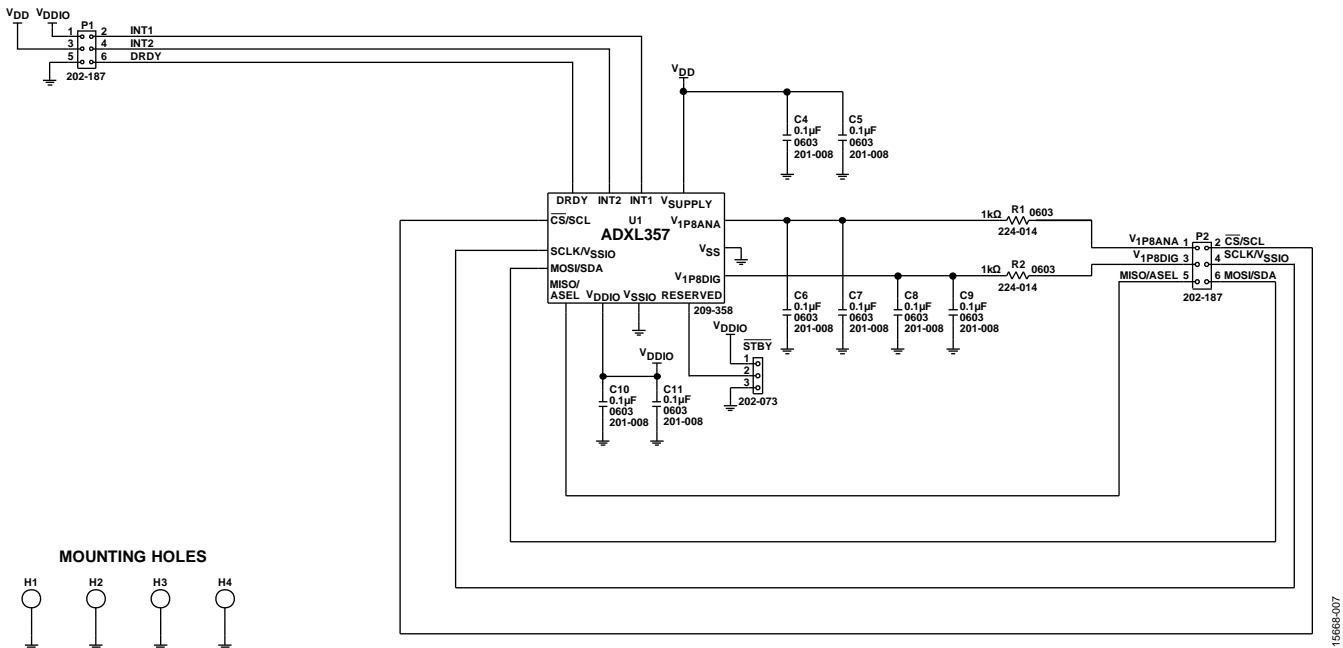


Figure 8. EVAL-ADXL357Z Schematic

ORDERING INFORMATION

BILL OF MATERIALS

Table 1. Bill of Materials for the [EVAL-ADXL356BZ/EVAL-ADXL356CZ](#)

| Qty | Reference Designator | Description | Manufacturer | Part Number |
|-----|----------------------|--|----------------------|-------------------------|
| 1 | U1 | High performance, 3-axis MEMS accelerometer, 14-terminal LCC | Analog Devices, Inc. | ADXL356 |
| 11 | C1 to C11 | Capacitors, ceramic, 0.1 μ F, 50 V, 10%, X7R, 0603 | Cal-Chip | GMC10X7R104K50NTLF |
| 2 | R1, R2 | Resistors, 1 k Ω , 0.1 W, 1%, 0603 | Cal-Chip | CR0603F1001T1LF |
| 2 | MODE, RANGE | Jumpers, 3-position, through hole | Prolex | 2556P03UA00 |
| 2 | P1, P2 | Headers, male, nonshrouded, 2 \times 3, 0.1 in. spacing, through hole, do not insert | FCI | 67996-206HLF |
| 1 | PCB | EVAL-ADXL356BZ/EVAL-ADXL356CZ | Analog Devices, Inc. | |

Table 2. Bill of Materials for the [EVAL-ADXL357Z](#)

| Qty | Reference Designator | Description | Manufacturer | Part Number |
|-----|----------------------|--|----------------------|-------------------------|
| 1 | U1 | High performance, 3-axis MEMS accelerometer, 14-terminal LCC | Analog Devices, Inc. | ADXL357 |
| 8 | C4 to C11 | Capacitors, ceramic, 0.1 μ F, 50 V, 10%, X7R, 0603 | Cal-Chip | GMC10X7R104K50NTLF |
| 2 | R1, R2 | Resistors, 1 k Ω , 0.1 W, 1%, 0603 | Cal-Chip | CR0603F1001T1LF |
| 1 | STBY | Jumper, 3-position, through hole | Prolex | 2556P03UA00 |
| 2 | P1, P2 | Headers, male, nonshrouded, 2 \times 3, 0.1 in. spacing, through hole, do not insert | FCI | 67996-206HLF |
| 1 | PCB | EVAL-ADXL357Z | Analog Devices, Inc. | |



ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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