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Product Standards

Part No.	AN44071A
Package Code No.	HSOP056-P-0300B

Semiconductor Company
Panasonic Corporation

Established by	Applied by	Checked by	Prepared by
H. Shidooka	M.Hiramatsu	J.Kaneda	T.Yokouchi

Contents

AN44071A

Driver IC for Stepping Motor

■ Overview

AN44071A is a quad channel H-bridge driver IC. Two bipolar stepping motor can be controlled by a single driver IC. Interface control is 1CLK_type, it can be selected 2-phase excitation, half- step, 1-2 phase excitation, W1-2 phase excitation and 2W1-2 phase excitation.

■ Features

- 2-channel stepping motor driver
  → A signal driver controls 2 stepping motors
- Built-in decoder for micro steps (2-phase, half step, 1-2 phase, W1-2 phase and 2W1-2 phase excitation)
  → Stepping motor can be driven by only external clock signal.
- PWM can be driven by built-in CR (3-value can be selected during PWM OFF period.)
  → The selection of PWM OFF period enables the best PWM drive.
- Mix Decay control (4-value can be selected for Fast Decay ratio)
  → Mix Decay control can improve accuracy of motor current waveform.
- Built-in over-current protection (OCP)
  → If the current flows to motor output more than the setup value due to ground-fault etc., the OCP operates and all motor outputs are turned OFF.
- Built-in under voltage lockout (UVLO)
  → If supply voltage falls to less than the operating supply voltage range, the UVLO operates and all motor outputs are turned OFF.
- Built-in thermal protection (TSD)
  → If chip junction temperature rises and reaches to the setup temperature, all motor outputs are turned OFF.
- Built-in abnormal detection output function
  → If OCP or TSD operates, an abnormal detection signal is output.
- Built-in standby function
  → The operation of standby function can lower current consumption of this IC.
- Built-in Home Position function
  → Home Position function can detect the position of motor.
- Built-in step detection output function
  → If step detection output function detects clock input signal, it outputs a signal.
- Built-in 5 V power supply (accuracy : ±5%)

■ Applications

- Stepping motor drive

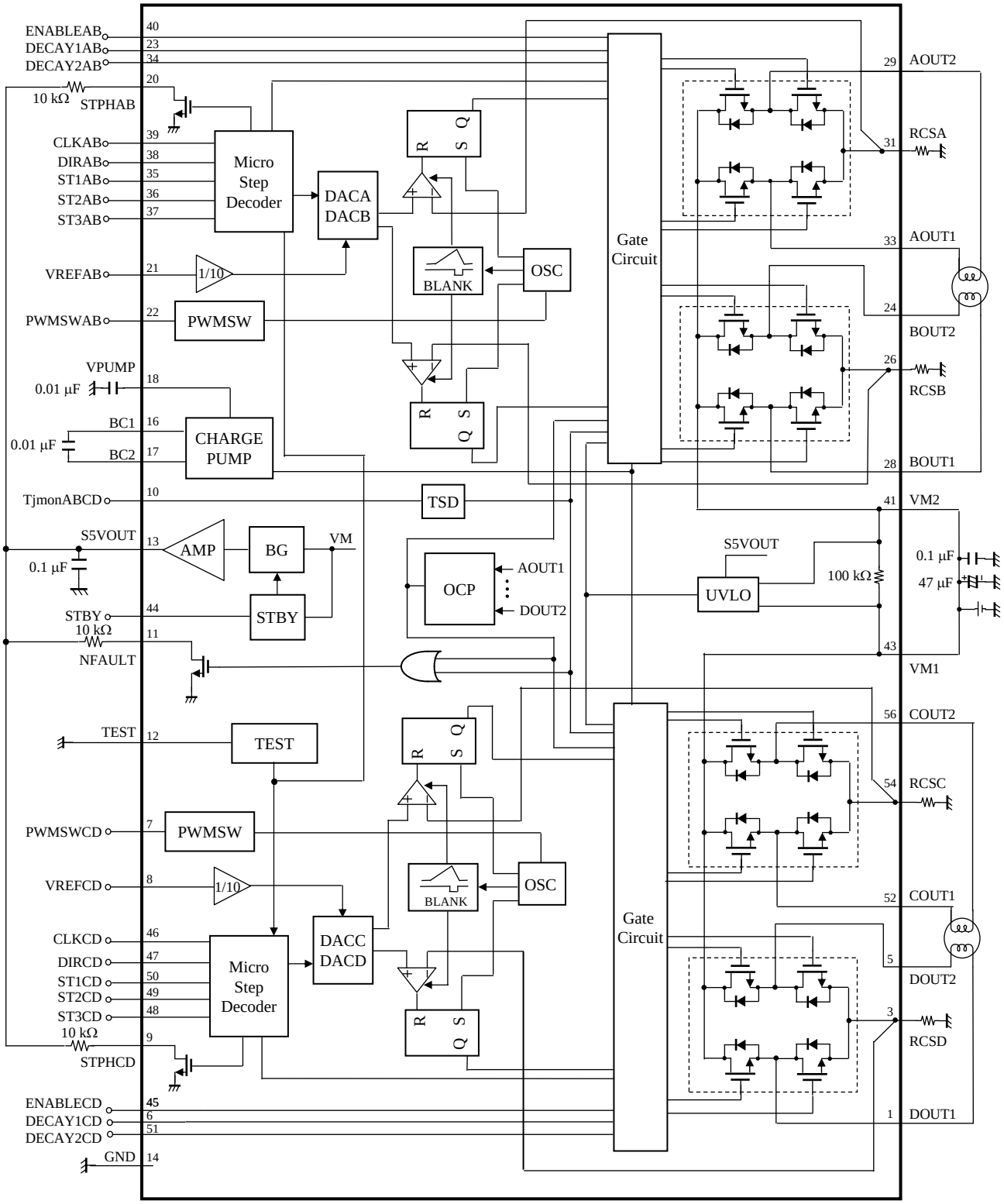
■ Package

- 56 pin Plastic Small Outline Package With Heat Sink (SOP Type)

■ Type

- Bi-CDMOS IC

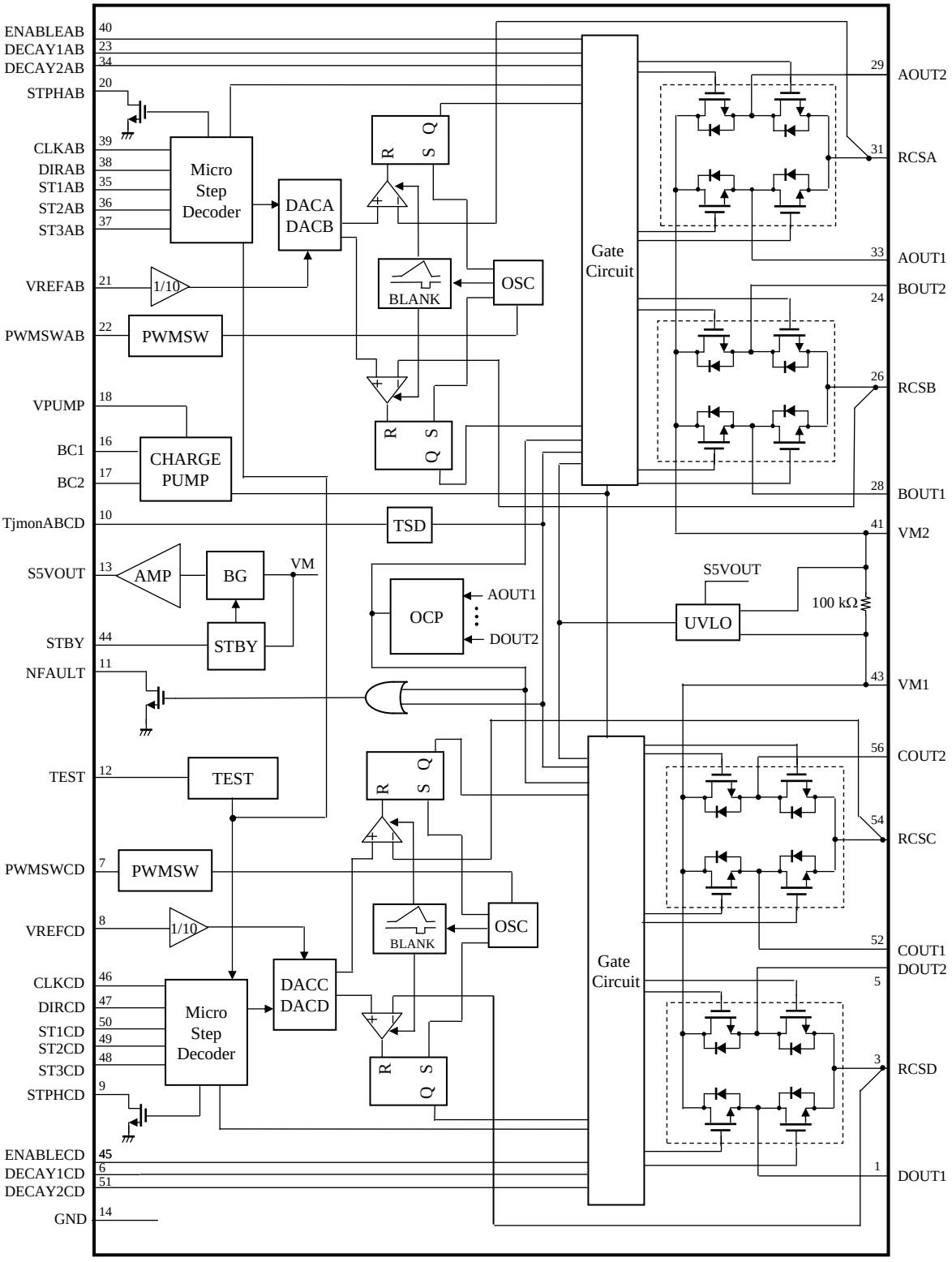
■ Application Circuit Example



Notes) • This application circuit is shown as an example but does not guarantee the design for mass production set.

• VM1 and VM2 should be connected outside.

■ Block Diagram



Note) This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

■ Pin Descriptions

Pin No.	Pin name	Type	Description
1	DOUT1	Output	Phase D motor drive output 1
2	N.C.	—	N.C.
3	RCSD	Input/Output	Phase D motor current detection
4	N.C.	—	N.C.
5	DOUT2	Output	Phase D motor drive output 2
6	DECAY1CD	Input	Phase C/D Mix Decay setup 1
7	PWMSWCD	Input	Phase C/D PWM OFF period selection input
8	VREFCD	Input	Phase C/D Torque reference voltage input
9	STPHCD	Output	Phase C/D Home Position / Step detection signal output
10	TjmonABCD	Output	Phase A/B, C/D VBE monitor
11	NFAULT	Output	Abnormal detection output
12	TEST	Input	Test mode setup
13	S5VOUT	Output	Internal reference voltage (output 5 V)
14	GND	Ground	Ground
15	COM1	—	Die pad ground 1
16	BC1	Output	Capacitor connection 1 for charge pump
17	BC2	Output	Capacitor connection 2 for charge pump
18	VPUMP	Output	Charge pump circuit output
19	N.C.	—	N.C.
20	STPHAB	Output	Phase A/B Home Position / Step detection signal output
21	VREFAB	Input	Phase A/B Torque reference voltage input
22	PWMSWAB	Input	Phase A/B PWM OFF period selection input
23	DECAY1AB	Input	Phase A/B Mix Decay setup 1
24	BOUT2	Output	Phase B motor drive output 2
25	N.C.	—	N.C.
26	RCSB	Input/Output	Phase B motor current detection
27	N.C.	—	N.C.
28	BOUT1	Output	Phase B motor drive output 1
29	AOUT2	Output	Phase A motor drive output 2
30	N.C.	—	N.C.
31	RCSA	Input/Output	Phase A motor current detection
32	N.C.	—	N.C.
33	AOUT1	Output	Phase A motor drive output 1
34	DECAY2AB	Input	Phase A/B Mix Decay setup 2

■ Pin Descriptions (continued)

Pin No.	Pin name	Type	Description
35	ST1AB	Input	Phase A/B excitation selection 1
36	ST2AB	Input	Phase A/B excitation selection 2
37	ST3AB	Input	Phase A/B excitation selection 3
38	DIRAB	Input	Phase A/B rotation direction setup
39	CLKAB	Input	Phase A/B clock input
40	ENABLEAB	Input	Phase A/B Enable / disable CTL
41	VM2	Power supply	Power supply 2 for motor
42	COM2	—	Die pad ground 2
43	VM1	Power supply	Power supply 1 for motor
44	STBY	Input	Standby
45	ENABLECD	Input	Phase C/D Enable / disable CTL
46	CLKCD	Input	Phase C/D clock input
47	DIRCD	Input	Phase C/D rotation direction setup
48	ST3CD	Input	Phase C/D excitation selection 3
49	ST2CD	Input	Phase C/D excitation selection 2
50	ST1CD	Input	Phase C/D excitation selection 1
51	DECAY2CD	Input	Phase C/D Mix Decay setup 2
52	COUT1	Output	Phase C motor drive output 1
53	N.C.	—	N.C.
54	RCSC	Input/Output	Phase C motor current detection
55	N.C.	—	N.C.
56	COUT2	Output	Phase C motor drive output 2

■ Absolute Maximum Ratings

Note) Absolute maximum ratings are limit values which do not result in damages to this IC, and IC operation is not guaranteed at these limit values.

A No.	Parameter	Symbol	Rating	Unit	Notes
1	Supply voltage (Pin 41, 43)	V_M	37	V	*1
2	Power dissipation	P_D	448	mW	*2
3	Operating ambient temperature	T_{opr}	–20 to +85	°C	*3
4	Storage temperature	T_{stg}	–55 to +150	°C	*3
5	Output pin voltage (Pin 1, 5, 24, 28, 29, 33, 52, 56)	V_{OUT}	37	V	*4
6	Motor drive current 1 (Pin 24, 28, 29, 33)	I_{OUT1}	±1.0	A	*5
7	Motor drive current 2 (Pin 1, 5, 52, 56)	I_{OUT2}	±1.7	A	*5
8	Flywheel diode current 1(Pin 24, 28, 29, 33)	I_{f1}	±1.0	A	*5
9	Flywheel diode current 2 (Pin 1, 5, 52, 56)	I_{f2}	±1.7	A	*5

Notes) *1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2 : The power dissipation shown is the value at T_a = 85°C for the independent (unmounted) IC package without a heat sink. When using this IC, refer to the P_D-T_a diagram of the package standard and design the heat radiation with sufficient margin so that the allowable value might not be exceeded based on the conditions of power supply voltage, load, and ambient temperature.

*3 : Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for T_a = 25°C.

*4 : This is a rated value of output voltage, and do not apply input voltage from outside to these pins. Set not to exceed the allowable range at any time.

*5 : Do not apply external current to any pin specially mentioned. For circuit currents, (+) denotes current flowing into the IC and (–) denotes current flowing out of the IC.

■ Operating Supply Voltage Range

Parameter	Symbol	Range	Unit	Notes
Supply voltage range	V_M	10.0 to 34.0	V	*1

Note) *1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

■ Allowable Current and Voltage Range

Notes) • Allowable current and voltage ranges are limit ranges which do not result in damages to this IC, and IC operation is not guaranteed within these limit ranges.
• Voltage values, unless otherwise specified, are with respect to GND.
• Do not apply external currents or voltages to any pin not specifically mentioned.
• For the circuit currents, "+" denotes current flowing into the IC, and "−" denotes current flowing out of the IC.

Pin No.	Pin name	Rating	Unit	Notes
3	RCSD	2.5	V	—
6	DECAY1CD	–0.3 to 6	V	—
7	PWMSWCD	–0.3 to 6	V	—
8	VREFCD	–0.3 to 6	V	—
9	STPHCD	–0.3 to 6	V	*1
11	NFAULT	–0.3 to 6	V	*1
12	TEST	–0.3 to 6	V	—
17	BC2	(V_M – 1) to 43	V	*2
18	VPUMP	(V_M – 2) to 43	V	*2
20	STPHAB	–0.3 to 6	V	*1
21	VREFAB	–0.3 to 6	V	—
22	PWMSWAB	–0.3 to 6	V	—
23	DECAY1AB	–0.3 to 6	V	—
26	RCSB	2.5	V	—
31	RCSA	2.5	V	—
34	DECAY2AB	–0.3 to 6	V	—
35	ST1AB	–0.3 to 6	V	—
36	ST2AB	–0.3 to 6	V	—
37	ST3AB	–0.3 to 6	V	—
38	DIRAB	–0.3 to 6	V	—
39	CLKAB	–0.3 to 6	V	—
40	ENABLEAB	–0.3 to 6	V	—
44	STBY	–0.3 to 6	V	—
45	ENABLECD	–0.3 to 6	V	—
46	CLKCD	–0.3 to 6	V	—
47	DIRCD	–0.3 to 6	V	—
48	ST3CD	–0.3 to 6	V	—
49	ST2CD	–0.3 to 6	V	—
50	ST1CD	–0.3 to 6	V	—
51	DECAY2CD	–0.3 to 6	V	—
54	RCSC	2.5	V	—

Pin No.	Pin name	Rating	Unit	Notes
9	STPHCD	2	mA	*1
11	NFAULT	2	mA	*1
13	S5VOUT	–7 to 0	mA	—
20	STPHAB	2	mA	*1

Notes) *1 : This pin is connected to open drain circuit inside. Connect a resistor in series with power supply.
Do not exceed the rated value at any time. Refer to page 4 for the recommended value.
*2 : External voltage must not be applied to this pin. Do not exceed the rated value at any time.

■ Electrical Characteristics at V_M = 24.0 V

Note) T_a = 25°C±2°C unless otherwise specified.

B No.	Parameter	Symbol	Test circuits	Conditions	Limits			Unit	Notes
					Min	Typ	Max		
Power block									
1	Output saturation voltage 1 High	V_{OH1}	2	I = –0.5 A (Pin 24, 28, 29, 33)	V_M – 0.5	V_M – 0.3	—	V	—
2	Output saturation voltage 1 Low	V_{OL1}	2	I = 0.5 A (Pin 24, 28, 29, 33)	—	0.48	0.75	V	—
3	Output saturation voltage 2 High	V_{OH2}	2	I = –0.8 A (Pin 1, 5, 52, 56)	V_M – 0.55	V_M – 0.35	—	V	—
4	Output saturation voltage 2 Low	V_{OL2}	2	I = 0.8 A (Pin 1, 5, 52, 56)	—	0.64	0.97	V	—
5	Flywheel diode forward voltage 1	V_{DI1}	2	I = 0.5 A (Pin 24, 28, 29, 33)	0.5	1	1.5	V	—
6	Flywheel diode forward voltage 2	V_{DI2}	2	I = 0.8 A (Pin 1, 5, 52, 56)	0.5	1	1.5	V	—
7	Upper-side output OFF current	$I_{OUTOFF1}$	2	V_M = 37 V, V_{RCS} = 0 V, OUT = 0 V	–10	—	—	µA	*1
8	Lower-side output OFF current	$I_{OUTOFF2}$	2	V_M = 37 V, V_{RCS} = 0 V, OUT = 37 V	—	—	100	µA	*1
Supply current									
9	Supply current (Active)	I_M	1	ENABLEAB = ENABLECD = Low, STBY = High	—	10	19	mA	—
10	Supply current (STBY)	I_{MSTBY}	1	STBY = Low	—	22	40	µA	—
I/O block									
11	STBY High-level input voltage	V_{STBYH}	1	—	2.1	—	5.5	V	—
12	STBY Low-level input voltage	V_{STBYL}	1	—	0	—	0.6	V	—
13	STBY High-level input current	I_{STBYH}	1	STBY = 5 V	25	50	100	µA	—
14	STBY Low-level input current	I_{STBYL}	1	STBY = 0 V	–2	—	2	µA	—
15	CLK High-level input voltage	V_{CLKH}	1	—	2.1	—	5.5	V	*2
16	CLK Low-level input voltage	V_{CLKL}	1	—	0	—	0.6	V	*2
17	CLK High-level input current	I_{CLKH}	1	CLK = 5 V	25	50	100	µA	*2
18	CLK Low-level input current	I_{CLKL}	1	CLK = 0 V	–2	—	2	µA	*2
19	CLK maximum input frequency	f_{CLK}	1	—	50	—	—	kHz	*2
20	ENABLE High-level input voltage	$V_{ENABLEH}$	1	—	2.1	—	5.5	V	*3
21	ENABLE Low-level input voltage	$V_{ENABLEL}$	1	—	0	—	0.6	V	*3
22	ENABLE High-level input current	$I_{ENABLEH}$	1	ENABLE = 5 V	25	50	100	µA	*3
23	ENABLE Low-level input current	$I_{ENABLEL}$	1	ENABLE = 0 V	–2	—	2	µA	*3

Notes) *1 : OUT represents AOUT1, AOUT2, BOUT1, BOUT2, COUT1, COUT2, DOUT1 and DOUT2.
*2 : CLK represents CLKAB and CLKCD.
*3 : ENABLE represents ENABLEAB and ENABLECD.

■ Electrical Characteristics (continued) at V_M = 24.0 V

Note) T_a = 25°C±2°C unless otherwise specified.

B No.	Parameter	Symbol	Test circuits	Conditions	Limits			Unit	Notes
					Min	Typ	Max		
I/O block (continued)									
24	PWMSW High-level input voltage	V_{PWMSWH}	1	—	2.3	—	5.5	V	*4
25	PWMSW Middle-level input voltage	V_{PWMSWM}	1	—	1.3	—	1.7	V	*4
26	PWMSW Low-level input voltage	V_{PWMSWL}	1	—	0	—	0.6	V	*4
27	PWMSW High-level input current	I_{PWMSWH}	1	PWMSW = 5 V	40	83	150	µA	*4
28	PWMSW Low-level input current	I_{PWMSWL}	1	PWMSW = 0 V	–70	–36	–18	µA	*4
29	PWMSW open voltage	V_{PWMSWO}	1	—	1.3	1.5	1.7	V	*4
30	DECAY High-level input voltage	V_{DECAYH}	1	—	2.1	—	5.5	V	*5
31	DECAY Low-level input voltage	V_{DECAYL}	1	—	0	—	0.6	V	*5
32	DECAY High-level input current	I_{DECAYH}	1	DECAY = 5 V	25	50	100	µA	*5
33	DECAY Low-level input current	I_{DECAYL}	1	DECAY = 0 V	–2	—	2	µA	*5
34	DIR High-level input voltage	V_{DIRH}	1	—	2.1	—	5.5	V	*6
35	DIR Low-level input voltage	V_{DIRL}	1	—	0	—	0.6	V	*6
36	DIR High-level input current	I_{DIRH}	1	DIR = 5 V	25	50	100	µA	*6
37	DIR Low-level input current	I_{DIRL}	1	DIR = 0 V	–2	—	2	µA	*6
38	ST High-level input voltage	V_{STH}	1	—	2.1	—	5.5	V	*7
39	ST Low-level input voltage	V_{STL}	1	—	0	—	0.6	V	*7
40	ST High-level input current	I_{STH}	1	ST = 5 V	25	50	100	µA	*7
41	ST Low-level input current	I_{STL}	1	ST = 0 V	–2	—	2	µA	*7
Torque control block									
42	Input bias current 1	I_{REFH}	1	V_{REFAB} = V_{REFCD} = 5 V	–2	—	2	µA	—
43	Input bias current 2	I_{REFL}	1	V_{REFAB} = V_{REFCD} = 0 V	–2	—	2	µA	—
44	PWM OFF time 1	T_{OFF1}	1	PWMSW = Low	16.8	28	39.2	µs	*4
45	PWM OFF time 2	T_{OFF2}	1	PWMSW = High	9.1	15.2	21.3	µs	*4
46	PWM OFF time 3	T_{OFF3}	1	PWMSW = Middle	4.9	8.1	11.3	µs	*4
47	Pulse blanking time	T_B	1	V_{REFAB} = V_{REFCD} = 0 V	0.4	0.7	1.0	µs	—
48	Comp threshold	VT_{CMP}	1	V_{REFAB} = V_{REFCD} = 5 V	475	500	525	mV	—
Reference voltage block									
49	Reference voltage	V_{S5VOUT}	1	I_{S5VOUT} = 0 mA	4.75	5.0	5.25	V	—
50	Output impedance	Z_{S5VOUT}	1	I_{S5VOUT} = –7 mA	—	—	10	Ω	—

Notes) *4 : PWMSW represents PWMSWAB and PWMSWCD.

*5 : DECAY represents DECAY1AB, DECAY2AB, DECAY1CD and DECAY2CD.

*6 : DIR represents DIRAB and DIRCD.

*7 : ST represents ST1AB, ST2AB, ST3AB, ST1CD, ST2CD and ST3CD.

■ Electrical Characteristics (continued) at V_M = 24.0 V

Note) T_a = 25°C±2°C unless otherwise specified.

B No.	Parameter	Symbol	Test circuits	Conditions	Limits			Unit	Notes
					Min	Typ	Max		
Abnormal detection output block									
51	NFAULT pin output Low-level voltage	$V_{NFAULTL}$	1	I_{NFAULT} = 1 mA	—	—	0.2	V	—
52	NFAULT pin output leak current	$I_{NFAULT(leak)}$	1	V_{NFAULT} = 5 V	—	—	5	µA	—
Home Position/ STEP detection output block									
53	STPH pin output Low-level voltage	V_{STPHL}	1	I_{STPH} = 1 mA	—	—	0.2	V	*8
54	STPH pin output leak current	$I_{STPH(leak)}$	1	V_{STPH} = 5 V	—	—	5	µA	*8
Test input block									
55	TEST High-level input voltage	V_{TESTH}	1	—	4.0	—	5.5	V	—
56	TEST Low-level input voltage	V_{TESTL}	1	—	0	—	0.6	V	—
57	TEST High-level input current	I_{TESTH}	1	TEST = 5 V	25	50	100	µA	—
58	TEST Low-level input current	I_{TESTL}	1	TEST = 0 V	–2	—	2	µA	—

Note) *8 : STPH represents STPHAB and STPHCD.

■ Electrical Characteristics (Reference values for design) at V_M = 24.0 V

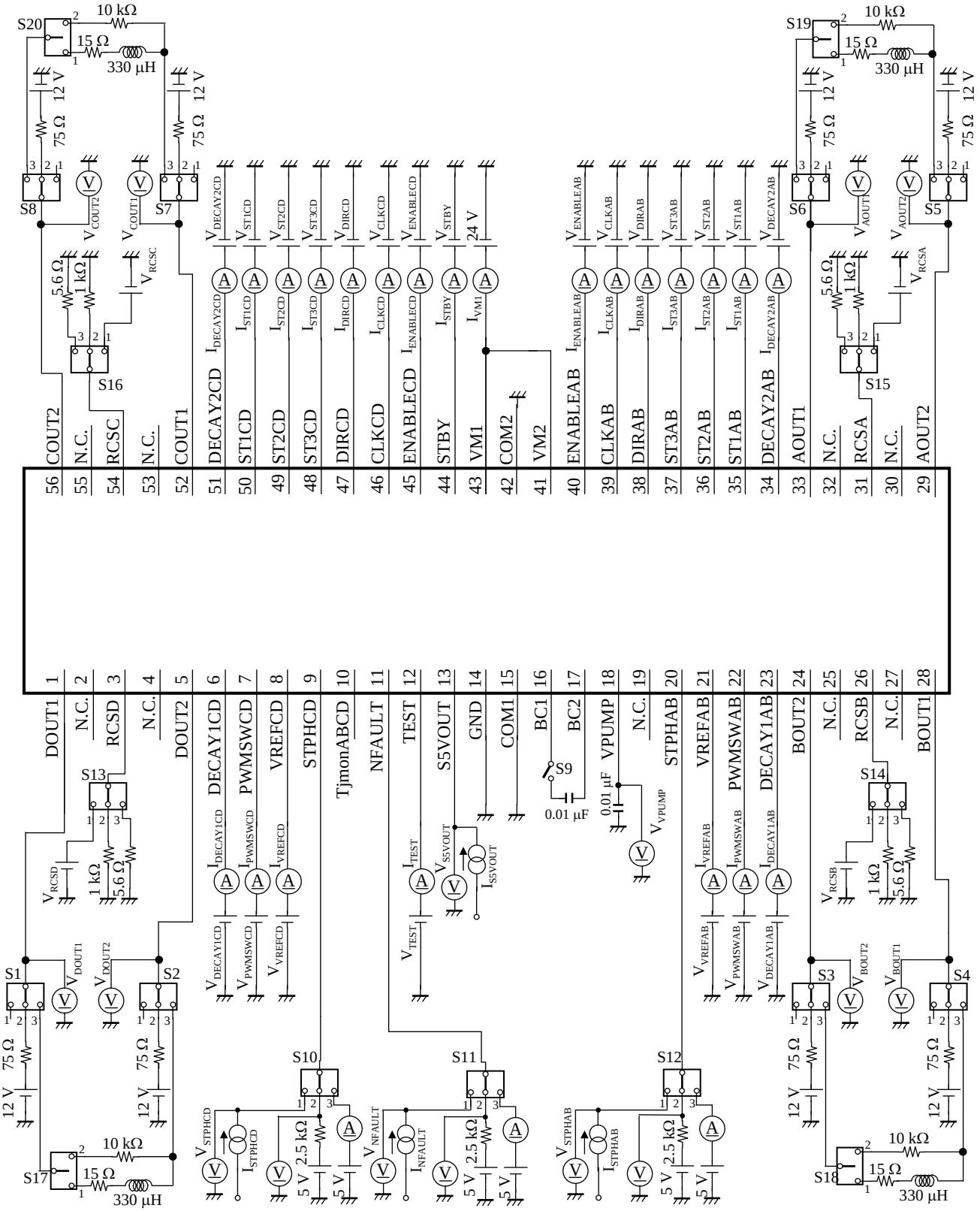
Notes) T_a = 25°C±2°C unless otherwise specified.
The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection.
If a problem does occur related to these characteristics, we will respond in good faith to user concerns.

B No.	Parameter	Symbol	Test circuits	Conditions	Reference values			Unit	Notes
					Min	Typ	Max		
Output block									
59	Output slew rate 1	VT_r	—	At the rising edge of output voltage, sink side of motor current	—	350	—	V/μs	*9
60	Output slew rate 2	VT_f	—	At the falling edge of output voltage, sink side of motor current	—	–400	—	V/μs	*9
61	Dead time	T_D	—	—	—	0.8	—	μs	*9
Thermal shutdown protection									
62	Thermal shutdown protection operating temperature	TSD_{on}	—	—	—	150	—	°C	—
Under voltage lockout									
63	Protection start voltage	V_{UVLO1}	—	—	—	7.5	—	V	—
64	Protection stop voltage	V_{UVLO2}	—	—	—	8.5	—	V	—

Note) *9 : The characteristics of all outputs of AOUT1, AOUT2, BOUT1, BOUT2, COUT1, COUT2, DOUT1 and DOUT2 are shown.

■ Test Circuit Diagram

1. Test Circuit 1



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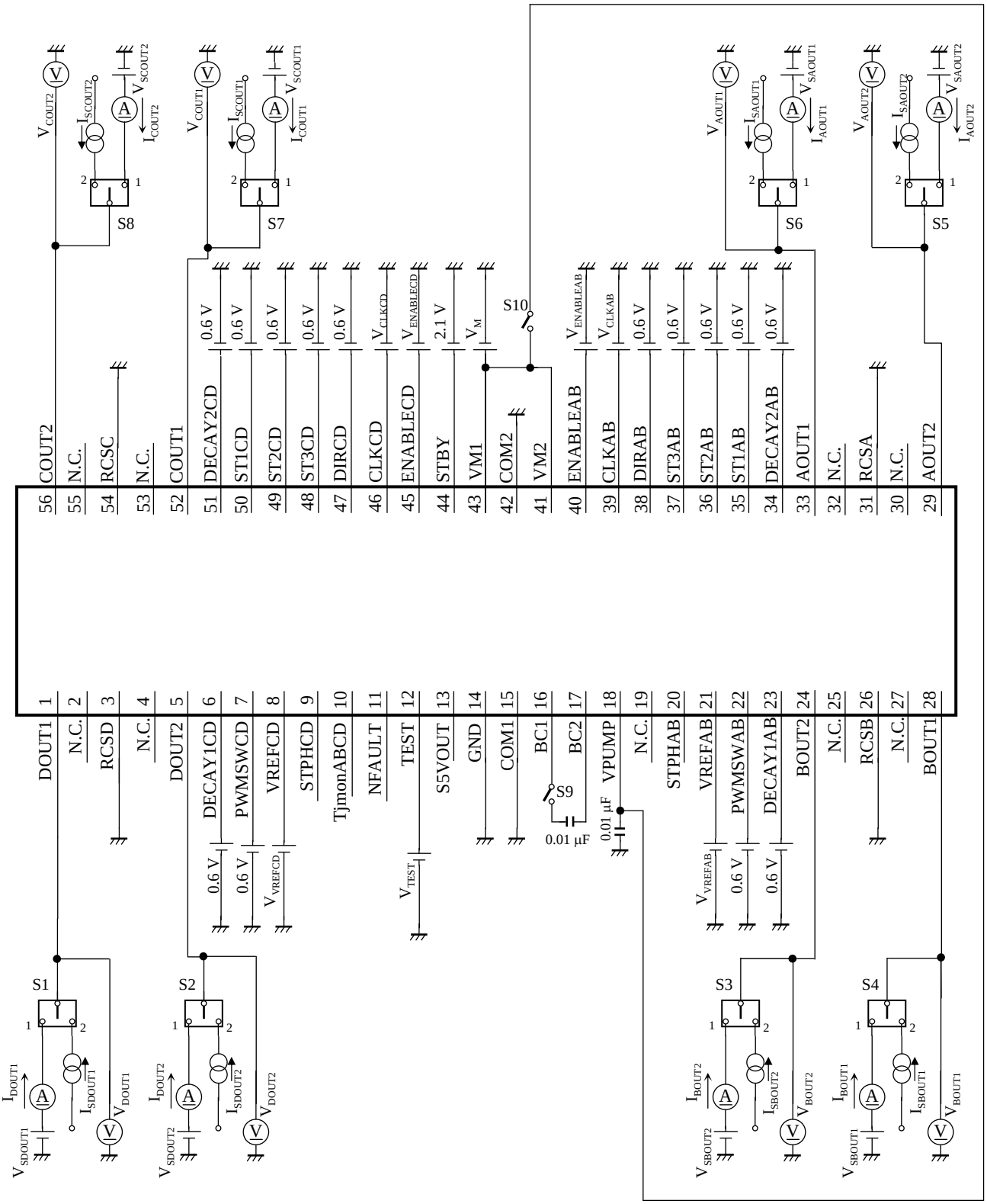
■ Test Circuit Diagram (continued)

2. Test Circuit 2



■ Electrical Characteristics Test Procedures

1. Test Circuit 1

C No.	Measuring pin	S1 to S8	S9	S10 to S12	S13 to S16	S17 to S20	V_{CLK} *1	V_{DECAY1} V_{DECAY2} *2	V_{STBY}	V_{ENABLE} *3	V_{PWMSW} *4	V_{RCS} *5	V_{DIR} *6	V_{ST1} V_{ST2} V_{ST3} *7	V_{TEST}	V_{VREF} *8	V_{VPUMP}	I_{S5VOUT}
9, 11	41, 43, 44	1	ON	1	1	—	0.6 V	0.6 V	2.1 V	0.6 V	0.6 V	0 V	0.6 V	0.6 V	0.6 V	5 V	Hi-Z	Hi-Z
10	41, 43	1	ON	1	1	—	0.6 V	0.6 V	0.6 V	0.6 V	0.6 V	0 V	0.6 V	0.6 V	0.6 V	5 V	Hi-Z	Hi-Z
12	13, 44	1	ON	1	1	—	0.6 V	0.6 V	0.6 V	2.1 V	0.6 V	0 V	0.6 V	0.6 V	0.6 V	5 V	Hi-Z	Hi-Z
49	13	1	ON	1	1	—	0.6 V	0.6 V	2.1 V	2.1 V	0.6 V	0 V	0.6 V	0.6 V	0.6 V	5 V	Hi-Z	Hi-Z
50	13	1	ON	1	1	—	0.6 V	0.6 V	2.1 V	2.1 V	0.6 V	0 V	0.6 V	0.6 V	0.6 V	5 V	Hi-Z	–7 mA
13, 17, 22, 27, 32, 36, 40, 57	6, 7, 12, 22, 23, 34 to 40, 44 to 51	1	ON	1	1	—	5 V	5 V	5 V	5 V	5 V	0 V	5 V	5 V	5 V	5 V	Hi-Z	Hi-Z
18, 23, 28, 33, 37, 41, 58	6, 7, 12, 22, 23, 34 to 40, 45 to 51	1	ON	1	1	—	0 V	0 V	5 V	0 V	0 V	0 V	0 V	0 V	0 V	5 V	Hi-Z	Hi-Z
14	44	1	ON	1	1	—	0 V	0 V	0 V	0 V	0 V	0 V	0 V	0 V	0 V	5 V	Hi-Z	Hi-Z
42	8, 21	1	ON	1	1	—	0 V	0 V	2.1 V	0 V	0 V	0 V	0 V	0 V	0 V	5 V	Hi-Z	Hi-Z
43	8, 21	1	ON	1	1	—	0 V	0 V	2.1 V	0 V	0 V	0 V	0 V	0 V	0 V	0 V	Hi-Z	Hi-Z
20, 21	33, 52, 40, 45	1	OFF	1	1	—	0.6 V	0.6 V	2.1 V	Sweep	0.6 V	0 V	0.6 V	0.6 V	0.6 V	5 V	29V	Hi-Z
48	29, 24, 56, 5, 3, 26, 31, 54	3	ON	1	1	2	0.6 V	0.6 V	2.1 V	2.1 V	0.6 V	0.475 V, 0.525 V	0.6 V	0.6 V	0.6 V	5 V	Hi-Z	Hi-Z
15, 16, 19	33, 29, 28, 24, 52, 56, 1, 5	2	ON	1	1	—	0.6 V / 2.1 V 50 kHz pulse	0.6 V	2.1 V	2.1 V	5 V	0 V	0.6 V	0.6 V	0.6 V	5 V	Hi-Z	Hi-Z
29	7, 22	1	ON	1	1	—	0 V	0 V	2.1 V	0 V	Hi-Z	0 V	0 V	0 V	0 V	0 V	Hi-Z	Hi-Z
55	9, 20	1	ON	2	1	—	Pulse input	0.6 V	2.1 V	2.1 V	0.6 V	0 V	0.6 V	0.6 V	4.0 V	5 V	Hi-Z	Hi-Z
56	9, 20	2	ON	2	1	—	Pulse input	0.6 V	2.1 V	2.1 V	1.7 V	0 V	0.6 V	2.1 V	0.6 V	5 V	Hi-Z	Hi-Z

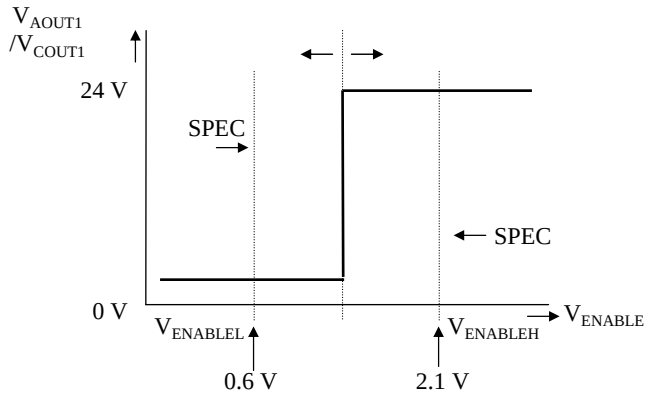
Notes) *1 : CLK represents CLKAB and CLKCD.
*2 : DECAY1 represents DECAY1AB and DECAY1CD.
DECAY2 represents DECAY2AB and DECAY2CD.
*3 : ENABLE represents ENABLEAB and ENABLECD.
*4 : PWMSW represents PWMSWAB and PWMSWCD.
*5 : RCS represents RCSA, RCSB, RCSC and RCSD.
*6 : DIR represents DIRAB and DIRCD.
*7 : ST1 represents ST1AB and ST1CD.
ST2 represents ST2AB and ST2CD.
ST3 represents ST3AB and ST3CD.
*8 : VREF represents VREFAB and VREFCD.

■ Electrical Characteristics Test Procedures (continued)

1. Test Circuit 1 (continued)

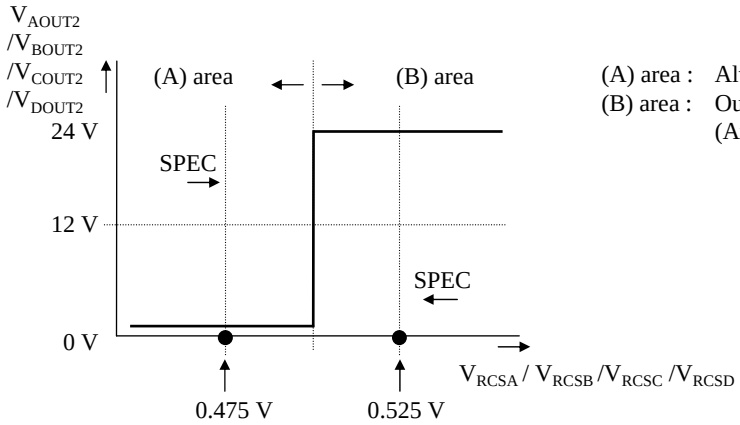
20) ENABLE High-level input voltage $V_{ENABLEH}$
21) ENABLE Low-level input voltage $V_{ENABLEL}$

Sweep ENABLE voltage, and check that V_{AOUT1} and V_{COUT1} switch as follows.



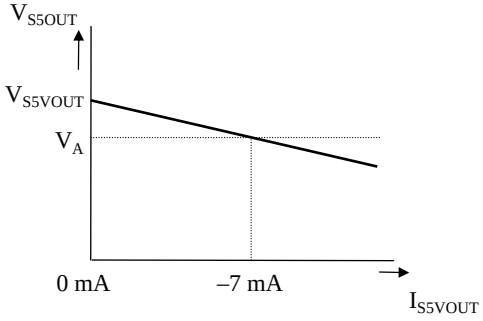
48) Comp threshold VT_{CMP}

Measure the voltages of V_{AOUT2}, V_{BOUT2}, V_{COUT2} and V_{DOUT2}. when input voltage is set to 0.475 V and 0.525 V respectively.



(A) area : Always output Low-level
(B) area : Output High-level as measurement value (Average)

50) Output impedance Z_{S5VOUT}



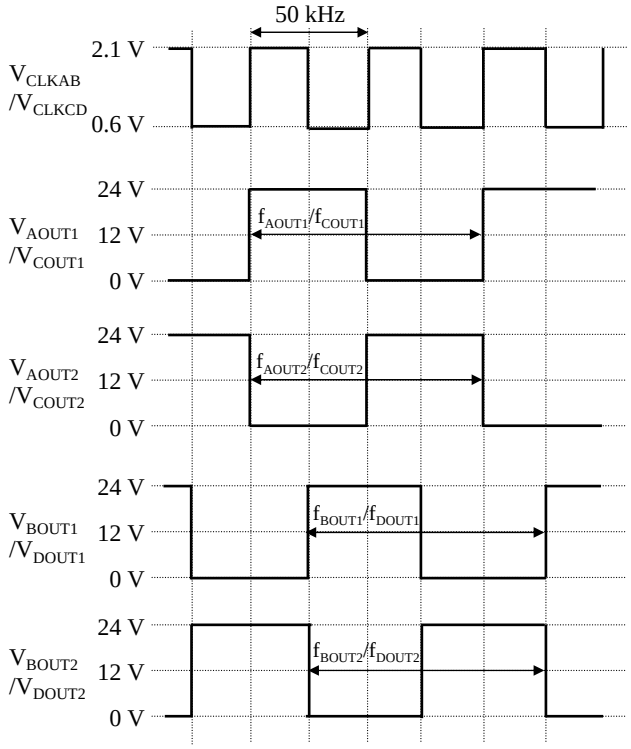
$$Z_{S5VOUT} = \frac{V_{S5VOUT} - V_A}{7\ mA}$$

■ Electrical Characteristics Test Procedures (continued)

1. Test Circuit 1 (continued)

15) CLK High-level input voltage V_{CLKH}
16) CLK Low-level input voltage V_{CLKL}
19) CLK maximum input frequency f_{CLK}

Input the pulse of 50 kHz as CLK as follows.
Low-level voltage = 0.6 V
High-level voltage = 2.1 V
When the frequency of V_{AOUT1}, V_{COUT1}, V_{AOUT2}, V_{COUT2}, V_{BOUT1}, V_{DOUT1}, V_{BOUT2} and V_{DOUT2} is 25 kHz, measure CLK High-level input voltage, CLK Low-level input voltage and CLK maximum input frequency.



55) TEST High-level input voltage V_{TESTH}
56) TEST Low-level input voltage V_{TESTL}

Check that the output status is as follows when Low-level input voltage (0.6 V) and High-level input voltage (4.0 V) are applied to TEST pin, Low-level / High-level input voltage to TEST pin.

Table Output status at TEST Low / High-level input voltage

Parameter	TEST pin voltage conditions	Status
TEST Low-level input voltage	0.6 V	STPH pin = Step detection output (Refer to page 44 for details.)
TEST High-level input voltage	4.0 V	STPH pin = Home Position output (Refer to page 40 to 43 for details.)

■ Electrical Characteristics Test Procedures (continued)

1. Test Circuit 1 (continued)

C No.	Measurement pin	S1 to S8	S9	S10 to S12	S13 to S16	S17 to S20	V_{CLK}	V_{DECAY1} V_{DECAY2}	V_{STBY}	V_{ENABLE}	V_{PWMSW}	V_{RCS}	V_{DIR}	V_{ST1} V_{ST2} V_{ST3}	V_{TEST}	V_{VREF}	V_{VPUMP}	I_{S5VOUT}
34, 35, 38, 39	33, 29, 28, 24, 52, 56, 1, 5, 35 to 38, 47 to 50	2	OFF	2	1	—	Pattern	Pattern	2.1 V	Pattern	Pattern	Pattern	Pattern	Pattern	Pattern	Pattern	30 V	Hi-Z
24, 25, 26, 44, 45, 46, 47	33, 29, 28, 24, 52, 56, 1, 5, 7, 22	3	ON	1	3	1	Pulse input	0.6 V	2.1 V	2.1 V	0.6 V 1.3 V 1.7 V 2.3 V	—	0.6 V	0.6 V	0.6 V	0.5 V	Hi-Z	Hi-Z
30, 31	33, 29, 28, 24, 52, 56, 1, 5, 6, 23, 34, 51	2	OFF	2	3	—	Pattern	Pattern	2.1 V	Pattern	Pattern	Pattern	Pattern	Pattern	Pattern	Pattern	30 V	Hi-Z

34) DIR High-level input voltage V_{DIRH}
35) DIR Low-level input voltage V_{DIRL}
38) ST1/ST2/ST3 High-level input voltage V_{STH}
39) ST1/ST2/ST3 Low-level input voltage V_{STL}

Check the logic related to the operation of each excitation mode in page 35 to 38 under the conditions that the input voltage of DIR, ST1, ST2 and ST3 is set as follows. Confirm Low-level / High-level of DIR, ST1, ST2 and ST3 by checking the logic.

DIR	ST1	ST2	ST3	Excitation mode
0.6 V	0.6 V	0.6 V	0.6 V	2-phase excitation drive (4-step sequence) / Forward
0.6 V	0.6 V	2.1 V	0.6 V	Half step drive (8-step sequence) / Forward
0.6 V	2.1 V	0.6 V	0.6 V	1-2 phase excitation drive (8-step sequence) / Forward
0.6 V	2.1 V	2.1 V	0.6 V	W1-2 phase excitation drive (16-step sequence) / Forward
0.6 V	0.6 V	2.1 V	2.1 V	2W1-2 phase excitation drive (32-step sequence) / Forward
2.1 V	0.6 V	0.6 V	0.6 V	2-phase excitation drive (4-step sequence) / Reverse
2.1 V	0.6 V	2.1 V	0.6 V	Half step drive (8-step sequence) / Reverse
2.1 V	2.1 V	0.6 V	0.6 V	1-2 phase excitation drive(8-step sequence) / Reverse
2.1 V	2.1 V	2.1 V	0.6 V	W1-2 phase excitation drive (16-step sequence) / Reverse
2.1 V	0.6 V	2.1 V	2.1 V	2W1-2 phase excitation drive (32-step sequence) / Reverse

■ Electrical Characteristics Test Procedures (continued)

1. Test Circuit 1 (continued)

24) PWMSW High-level input voltage V_{PWMSWH}
25) PWMSW Middle-level input voltage V_{PWMSWM}
26) PWMSW Low-level input voltage V_{PWMSWL}
44) PWM OFF time 1 T_{OFF1}
45) PWM OFF time 2 T_{OFF2}
46) PWM OFF time 3 T_{OFF3}
47) Pulse blanking time T_B

Each parameter is obtained by the timing chart of V_{AOUT1}, V_{BOUT1} , V_{COUT1}, V_{DOUT1}, V_{AOUT2},V_{BOUT2}, V_{COUT2} and V_{DOUT2} at VREF = 0.5 V.
The timing chart is shown as follows.
・For 24) to 26), 44) to 47), measure T_{OFF1}, T_{OFF2} and T_{OFF3} under the input conditions of PWMSW pin in the below chart.
・For 47), measure the Low-level interval of V_{AOUT1}, V_{BOUT1}, V_{COUT1} and V_{DOUT1} : T_B in the below chart.

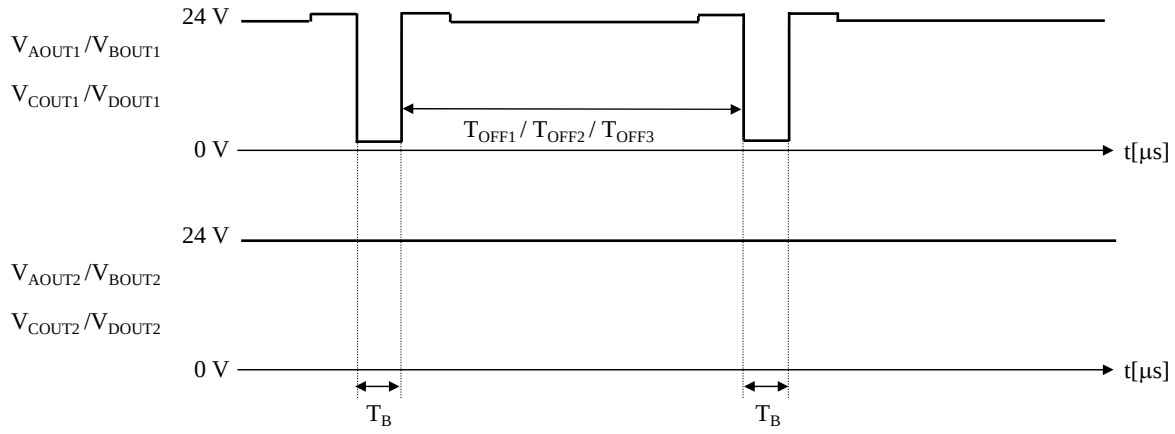


Table PWMSW input voltage vs. T_{OFF}

Input pin	Voltage conditions	Status
	V_{PWMSWH} / V_{PWMSWM} / V_{PWMSWL}	
PWMSW	0.6 V	T_{OFF1} = 28 µs
	1.3 V	T_{OFF3} = 8.1 µs
	1.7 V	T_{OFF3} = 8.1 µs
	2.3 V	T_{OFF2} = 15.2 µs

■ Electrical Characteristics Test Procedures (continued)

1. Test Circuit 1 (continued)

30) DECAY High-level input voltage V_{DECAYH}
31) DECAY Low-level input voltage V_{DECAYL}

Perform the logic test under the conditions that Low-level input voltage of DECAY1/DECAY2 is 0.6 V and High-level input voltage is 2.1 V.
The timing chart of V_{AOUT1}, V_{BOUT1} , V_{COUT1}, V_{DOUT1}, V_{AOUT2}, V_{BOUT2}, V_{COUT2} and V_{DOUT2} is as follows at the logic test.
Measure T_{DECAY} and T_{OFF-R}, and check Low-level / High-level input voltage of DECAY1/DECAY2.

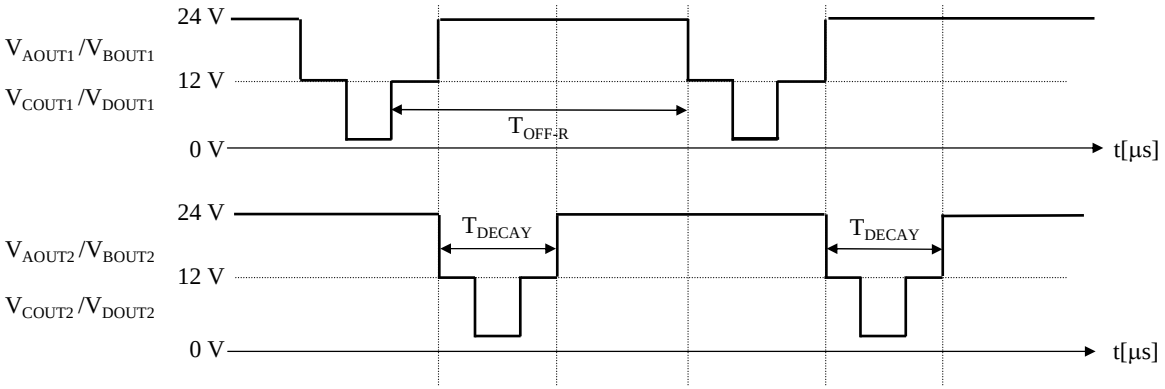


Table DECAY1/2 input voltage vs. Decay control

DECAY1	DECAY2	Decay control (T_{DECAY} / T_{OFF-R})
0.6 V	0.6 V	0% mode (Slow Decay)
0.6 V	2.1 V	25% mode
2.1 V	0.6 V	50% mode
2.1 V	2.1 V	100% mode

■ Electrical Characteristics Test Procedures (continued)

1. Test Circuit 1 (continued)

51) NFAULT pin output Low-level voltage $V_{NFAULTL}$

Input 1 mA to NFAULT pin under the condition that the output of NFAULT pin is Low, and measure the voltage of NFAULT pin.

52) NFAULT pin output leak current $I_{NFAULT(leak)}$

Input 5 V to NFAULT pin under the condition that the output of NFAULT pin is Hi-Z, measure the leak current.

53) STPH pin output Low-level voltage V_{STPHL}

Input 1 mA to STPH pin under the condition that the output of STPH pin is Low, measure the voltage of STPH pin.

54) STPH pin output leak current $I_{STPH (leak)}$

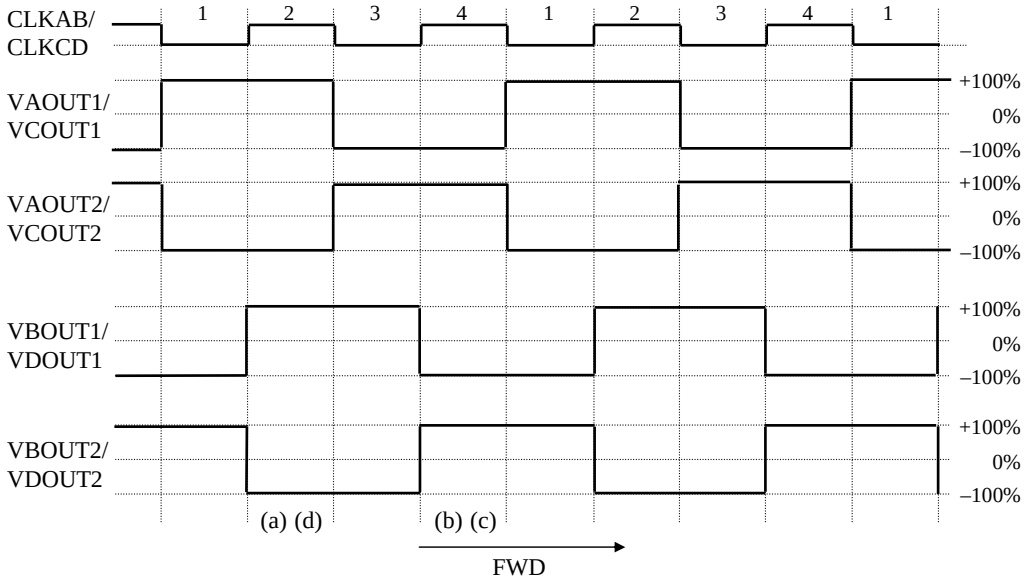
Input 5 V to STPH pin under the condition that the output of STPH pin is Hi-Z, measure the leak current.

■ Electrical Characteristics Test Procedures (continued)

2. Test Circuit 2

1) Output saturation voltage 1 High V_{OH1}
2) Output saturation voltage 1 Low V_{OL1}
3) Output saturation voltage 2 High V_{OH2}
4) Output saturation voltage 2 Low V_{OL2}

2-phase excitation drive (4-step sequence)
(ST1AB/ST1CD = Low, ST2AB/ST2CD = Low, ST3AB/ST3CD = Low), (DIRAB/DIRCD = Low)



Measure the output saturation voltage High and the output saturation voltage Low under the below conditions.

Measurement parameter	(a) B No.1/No.3	(b) B No.2/No.4	(c) B No.1/No.3	(d) B No.2/No.4
Applied pin	AOUT1/BOUT1 COUT1/DOUT1	AOUT1/BOUT1 COUT1/DOUT1	AOUT2/BOUT2 COUT2/DOUT2	AOUT2/BOUT2 COUT2/DOUT2
Measured voltage	V_{AOUT1}/V_{BOUT1} V_{COUT1}/V_{DOUT1}	V_{AOUT1}/V_{BOUT1} V_{COUT1}/V_{DOUT1}	V_{AOUT2}/V_{BOUT2} V_{COUT2}/V_{DOUT2}	V_{AOUT2}/V_{BOUT2} V_{COUT2}/V_{DOUT2}
Applied condition	I_{SAOUT1}/I_{SBOUT1} = –0.5 A I_{SCOUT1}/I_{SDOUT1} = –0.8 A	I_{SAOUT1}/I_{SBOUT1} = +0.5 A I_{SCOUT1}/I_{SDOUT1} = +0.8 A	I_{SAOUT2}/I_{SBOUT2} = –0.5 A I_{SCOUT2}/I_{SDOUT2} = –0.8 A	I_{SAOUT2}/I_{SBOUT2} = +0.5 A I_{SCOUT2}/I_{SDOUT2} = +0.8 A
S1 to S8	2	2	2	2
S9	ON	ON	ON	ON
S10	OFF	OFF	OFF	OFF
V_M	24 V	24 V	24 V	24 V
V_{VREFAB}/V_{VREFCD}	6 V	6 V	6 V	6 V
V_{TEST}	4 V	4 V	4 V	4 V
$V_{ENABLEAB}$ $/V_{ENABLECD}$	2.1 V	2.1 V	2.1 V	2.1 V

■ Electrical Characteristics Test Procedures (continued)

2. Test Circuit 2 (continued)

5) Flywheel diode forward voltage 1 V_{DI1}
6) Flywheel diode forward voltage 2 V_{DI2}

Measure the Flywheel diode forward voltage 1 and the Flywheel diode forward voltage 2 under the below conditions.

Measurement parameter	B No.5 (upper-side)	B No.5 (lower-side)	B No.6 (upper-side)	B No.6 (lower-side)
Applied pin	AOUT1/BOUT1 AOUT2/BOUT2	AOUT1/BOUT1 AOUT2/BOUT2	COUT1/DOUT1 COUT2/DOUT2	COUT1/DOUT1 COUT2/DOUT2
Measured voltage	V_{AOUT1}/V_{BOUT1} V_{AOUT2}/V_{BOUT2}	V_{AOUT1}/V_{BOUT1} V_{AOUT2}/V_{BOUT2}	V_{COUT1}/V_{DOUT1} V_{COUT2}/V_{DOUT2}	V_{COUT1}/V_{DOUT1} V_{COUT2}/V_{DOUT2}
Applied condition	I_{SAOUT1}/I_{SBOUT1} = +0.5 A I_{SAOUT2}/I_{SBOUT2} = +0.5 A	I_{SAOUT1}/I_{SBOUT1} = –0.5 A I_{SAOUT2}/I_{SBOUT2} = –0.5 A	I_{SCOUT1}/I_{SDOUT1} = +0.8 A I_{SCOUT2}/I_{SDOUT2} = +0.8 A	I_{SCOUT1}/I_{SDOUT1} = –0.8 A I_{SCOUT2}/I_{SDOUT2} = –0.8 A
S1 to S8	2	2	2	2
S9	ON	ON	ON	ON
S10	OFF	OFF	OFF	OFF
V_M	0 V	0 V	0 V	0 V
$V_{ENABLEAB}$ $/V_{ENABLECD}$	0.6 V	0.6 V	0.6 V	0.6 V

7) Upper-side output OFF current $I_{OUTOFF1}$

Measure the output OFF current ($I_{OUTOFF1}$) in each output pin under the below conditions.

8) Lower-side output OFF current $I_{OUTOFF2}$

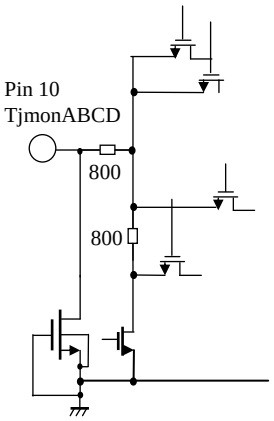
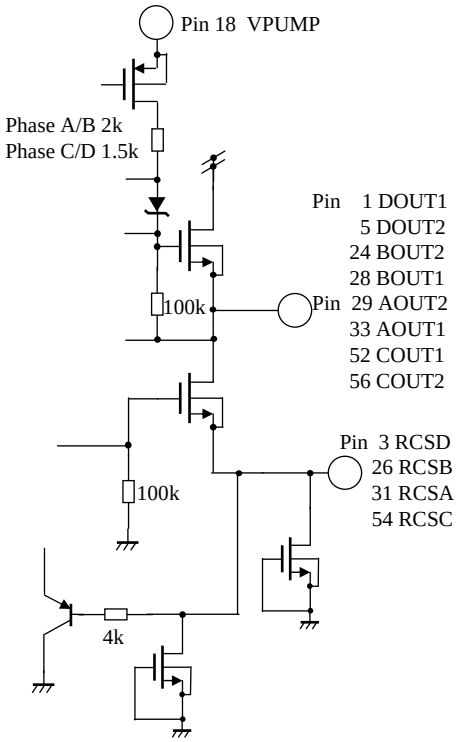
When the pattern is input to ENABLE pin as follows, and AOUT1, AOUT2, BOUT1, BOUT2, COUT1, COUT2, DOUT1 and DOUT2 output High, measure the output OFF current ($I_{OUTOFF2}$) in each output pin.

Measurement parameter	B No.7	B No.8
Applied pin Measurement current	AOUT1/AOUT2 BOUT1/BOUT2 COUT1/COUT2 DOUT1/DOUT2	AOUT1/AOUT2 BOUT1/BOUT2 COUT1/COUT2 DOUT1/DOUT2
Applied conditions	$V_{SAOUT1} = V_{SBOUT1} = V_{SCOUT1} = V_{SDOUT1}$ $= V_{SAOUT2} = V_{SBOUT2} = V_{SCOUT2} = V_{SDOUT2}$ = 0 V	$V_{SAOUT1} = V_{SBOUT1} = V_{SCOUT1} = V_{SDOUT1}$ $= V_{SAOUT2} = V_{SBOUT2} = V_{SCOUT2} = V_{SDOUT2}$ = 37 V
S1 to S8	1	1
S9	ON	OFF
S10	OFF	ON
V_M	37 V	37 V
V_{VREFAB}/V_{VREFCD}	5 V	5 V
V_{TEST}	0.6 V	Pattern
$V_{ENABLEAB}$ $/V_{ENABLECD}$	0.6 V	Pattern

■ Technical Data

1. I/O block circuit diagrams and pin function descriptions

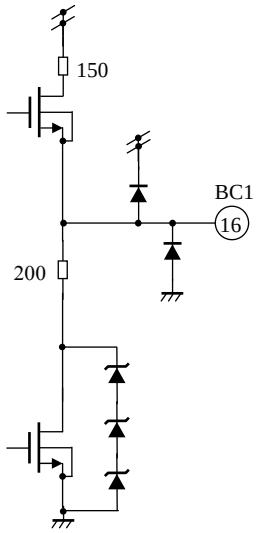
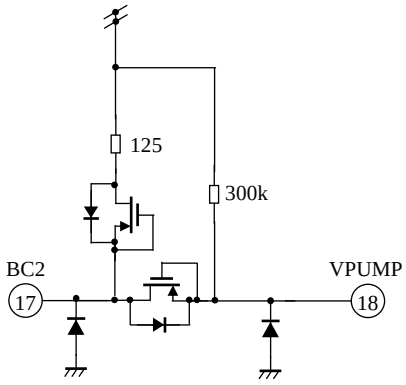
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
10	—		—	Pin10 : VBE monitor
1 3 5 24 26 28 29 31 33 52 54 56	—		—	Pin 1 : Phase D motor drive output 1 3 : Phase D motor current detection 5 : Phase D motor drive output 2 24 : Phase B motor drive output 2 26 : Phase B motor current detection 28 : Phase B motor drive output 1 29 : Phase A motor drive output 2 31 : Phase A motor current detection 33 : Phase A motor drive output 1 52 : Phase C motor drive output 1 54 : Phase C motor current detection 56 : Phase C motor drive output 2

■ Technical Data (continued)

1. I/O block circuit diagrams and pin function descriptions (continued)

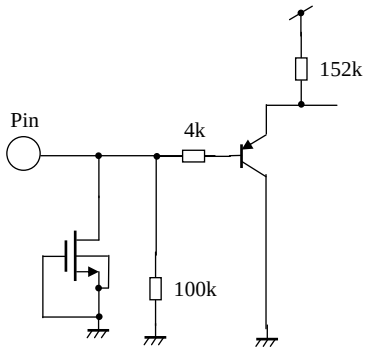
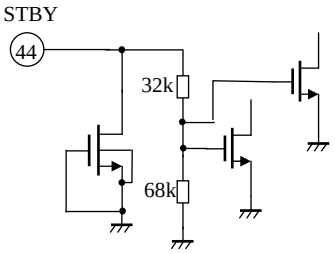
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
16	—		—	Pin 16 : Capacitor connection 1 for charge pump
17 18	—		—	Pin 17 : Capacitor connection 2 for charge pump 18 : Charge pump circuit output

■ Technical Data (continued)

1. I/O block circuit diagrams and pin function descriptions (continued)

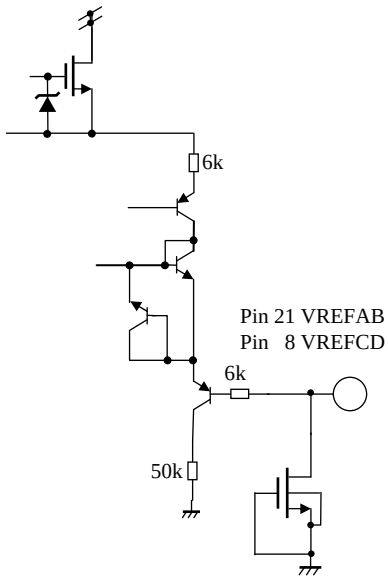
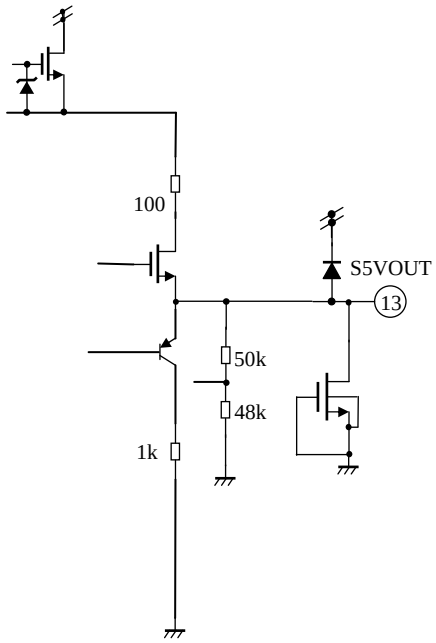
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
35 36 37 38 39 40 45 46 47 48 49 50	—	Pin 40 ENABLEAB, Pin 45 ENABLECD Pin 39 CLKAB, Pin 46 CLKCD Pin 37 ST3AB, Pin 48 ST3CD Pin 36 ST2AB, Pin 49 ST2CD Pin 35 ST1AB, Pin 50 ST1CD Pin 38 DIRAB, Pin 47 DIRCD 	100 kΩ	Pin 40, 45 : Enable / disable CTL Pin 39, 46 : Clock input Pin 37, 48 : Excitation selection 3 Pin 36, 49 : Excitation selection 2 Pin 35, 50 : Excitation selection 1 Pin 38, 47 : Rotation direction setup
44	—		100 kΩ	Pin 44 : Standby

■ Technical Data (continued)

1. I/O block circuit diagrams and pin function descriptions (continued)

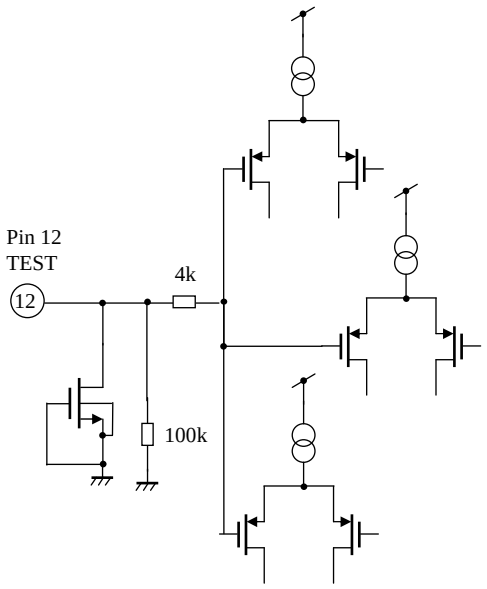
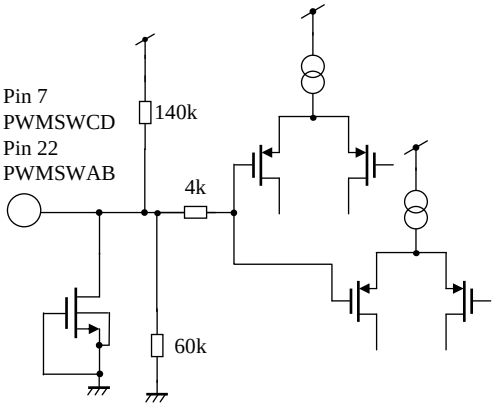
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
8 21	—		—	Pin 21, 8 : Torque reference voltage input
13	—		—	Pin 13 : Internal reference voltage (output 5 V)

■ Technical Data (continued)

1. I/O block circuit diagrams and pin function descriptions (continued)

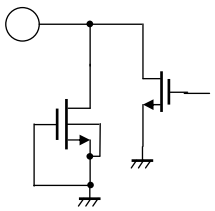
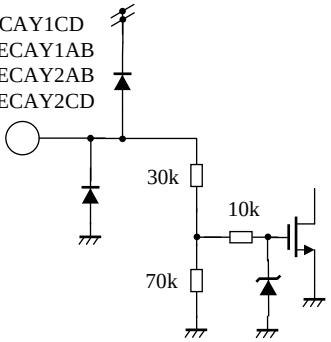
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
12	—		100 kΩ	Pin 12 : Test mode setup
7 22	—		—	Pin 7, 22 : PWM OFF period setup

■ Technical Data (continued)

1. I/O block circuit diagrams and pin function descriptions (continued)

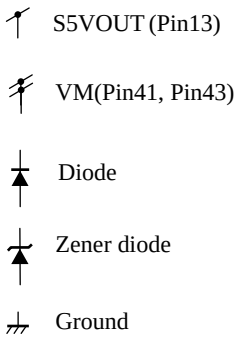
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
9 11 20	—	Pin 9 STPHCD Pin 11 NFAULT Pin 20 STPHAB 	—	Pin 9, 20 : Home Position / Step detection signal output Pin 11 : Abnormal detection output
6 23 34 51	—	Pin 6 DECAY1CD Pin 23 DECAY1AB Pin 34 DECAY2AB Pin 51 DECAY2CD 	100 kΩ	Pin 6, 23, 34, 51 : Mix DECAY setup

■ Technical Data (continued)

1. I/O block circuit diagrams and pin function descriptions (continued)

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
—	—		—	—

■ Technical Data (continued)

2. Control mode

Note) * is AB or CD.

1) Truth table (Excitation select)

ENABLE*	DIR*	ST1*	ST2*	ST3*	Output excitation mode	
Low	—	—	—	—	—	Output OFF
High	Low	Low	Low	Low	Phase B/D 90° delay to phase A/C	2-phase excitation drive (4-step sequence)
High	Low	Low	High	Low		Half step drive (8-step sequence)
High	Low	High	Low	Low		1-2 phase excitation drive (8-step sequence)
High	Low	High	High	Low		W1-2 phase excitation drive (16-step sequence)
High	Low	—	—	High		2W1-2 phase excitation drive (32-step sequence)
High	High	Low	Low	Low	Phase B/D 90° advance to phase A/C	2-phase excitation drive (4-step sequence)
High	High	Low	High	Low		Half step drive (8-step sequence)
High	High	High	Low	Low		1-2 phase excitation drive (8-step sequence)
High	High	High	High	Low		W1-2 phase excitation drive (16-step sequence)
High	High	—	—	High		2W1-2 phase excitation drive (32-step sequence)

2) Truth table (Control / Charge pump circuit)

STBY	ENABLE*	Control / Charge pump circuit	Output transistor
Low	—	OFF	All channel output : OFF
High (*3)	Low	ON	OFF (*4)
High (*3)	High	ON	ON

3) Truth table (PWM OFF period selection)

PWMSW*	PWM OFF period (*5)
Low	28.0 μs
Middle	8.1 μs
High	15.2 μs

4) Truth table (Decay selection)

DECAY1*	DECAY2*	Decay control (*6)
Low	Low	Slow Decay
Low	High	25%
High	Low	50%
High	High	100%

Note) The above rate is applied to Fast Decay every PWM OFF period.

5) Truth table (STPH output selection)

TEST	STPH* output
Low	STEP detection output
High	Home Position output

6) Truth table (NFAULT output)

TSD (*1)	OCP (*2)	NFAULT	Output transistor
Thermal shutdown protection start	—	Low	All channel output : OFF
—	Over-current detection start	Low	All channel output : OFF
Thermal shutdown protection stop	Over-current detection stop	Hi-Z	ON

Notes) *1 : TSD is a latch type protection

→ The protection operation starts at 150°C. (All motor outputs are turned off , and latched.) / The latch is released by Standby or UVLO.

*2 : OCP is a latch type protection

→ All motor outputs are turned off by over-current detection, and be latched. / The latch is released by Standby or UVLO. In addition, All motor outputs are turned off at under UVLO.

*3 : Input external signals to STBY pin in order to set STBY signal to High-level. Because, STBY pin cannot be set to High-level when it is connected to S5VOUT(Pin13).

*4 : The output transistors of AB/CD channel are controlled by ENABLEAB/CD respectively.

*5 : The PWM OFF intervals of AB/CD channel are set by PWMSWAB/CD respectively.

*6 : The Decay controls of AB/CD channel are set by DECAY1AB/CD (DECAY2AB/CD) respectively.

■ Technical Data (continued)

3. Each phase current value

1) 1-2 phase, W1-2 phase, 2W1-2 phase DIRAB / DIRCD = Low

Note) The definition of Phase A, B, C and D current "100%" : (VREFAB(VREFCD) × 0.1) / Motor current detection resistance

1-2 phase (8-Step)	W1-2 phase (16- Step)	2W1-2 phase (32-Step)	A/C phase current (%)	B/D phase current (%)
1	1	1	70.7	–70.7
—	—	2	83.2	–55.6
—	2	3	92.4	–38.3
—	—	4	98.1	–19.5
2	3	5	100	0
—	—	6	98.1	19.5
—	4	7	92.4	38.3
—	—	8	83.2	55.6
3	5	9	70.7	70.7
—	—	10	55.6	83.2
—	6	11	38.3	92.4
—	—	12	19.5	98.1
4	7	13	0	100
—	—	14	–19.5	98.1
—	8	15	–38.3	92.4
—	—	16	–55.6	83.2
5	9	17	–70.7	70.7
—	—	18	–83.2	55.6
—	10	19	–92.4	38.3
—	—	20	–98.1	19.5
6	11	21	–100	0
—	—	22	–98.1	–19.5
—	12	23	–92.4	–38.3
—	—	24	–83.2	–55.6
7	13	25	–70.7	–70.7
—	—	26	–55.6	–83.2
—	14	27	–38.3	–92.4
—	—	28	–19.5	–98.1
8	15	29	0	–100
—	—	30	19.5	–98.1
—	16	31	38.3	–92.4
—	—	32	55.6	–83.2

■ Technical Data (continued)

3. Each phase current value (continued)

2) 1-2 phase, W1-2 phase, 2W1-2 phase DIRAB / DIRCD = High

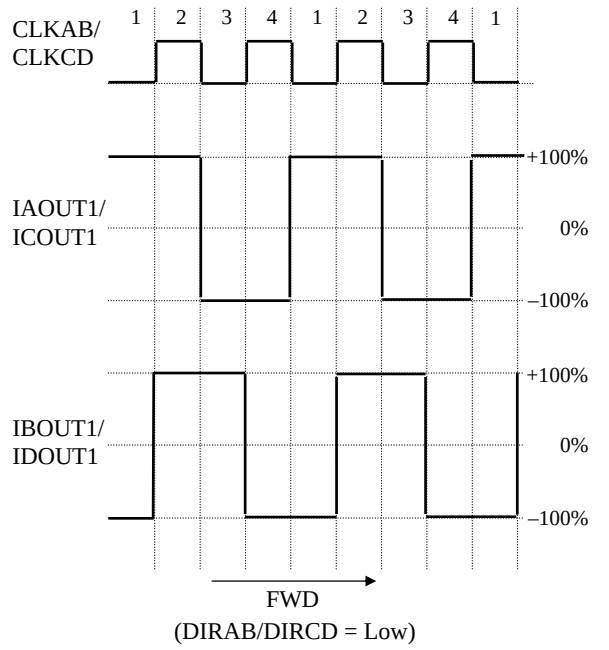
Note) The definition of Phase A, B, C and D current "100%" : (VREFAB(VREFCD) ×0.1) / Motor current detection resistance

1-2 phase (8-Step)	W1-2 phase (16-Step)	2W1-2 phase (32-Step)	A/C phase current (%)	B/D phase current (%)
1	1	1	70.7	–70.7
—	—	2	55.6	–83.2
—	2	3	38.3	–92.4
—	—	4	19.5	–98.1
2	3	5	0	–100
—	—	6	–19.5	–98.1
—	4	7	–38.3	–92.4
—	—	8	–55.6	–83.2
3	5	9	–70.7	–70.7
—	—	10	–83.2	–55.6
—	6	11	–92.4	–38.3
—	—	12	–98.1	–19.5
4	7	13	–100	0
—	—	14	–98.1	19.5
—	8	15	–92.4	38.3
—	—	16	–83.2	55.6
5	9	17	–70.7	70.7
—	—	18	–55.6	83.2
—	10	19	–38.3	92.4
—	—	20	–19.5	98.1
6	11	21	0	100
—	—	22	19.5	98.1
—	12	23	38.3	92.4
—	—	24	55.6	83.2
7	13	25	70.7	70.7
—	—	26	83.2	55.6
—	14	27	92.4	38.3
—	—	28	98.1	19.5
8	15	29	100	0
—	—	30	98.1	–19.5
—	16	31	92.4	–38.3
—	—	32	83.2	–55.6

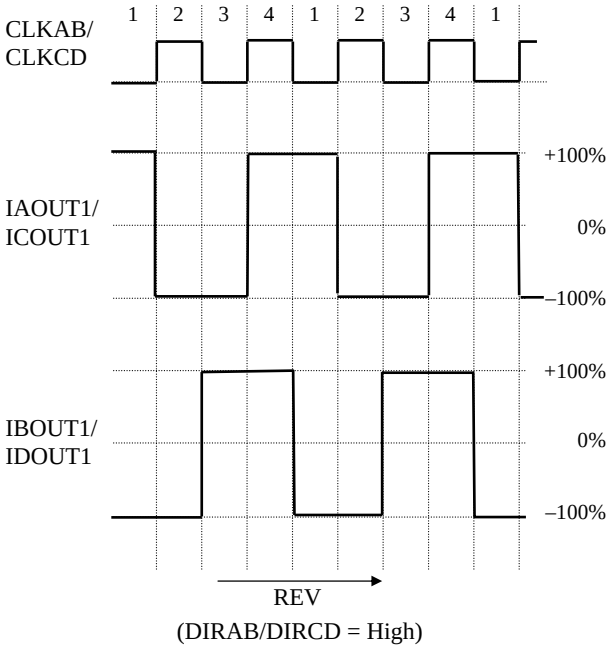
■ Technical Data (continued)

4. Each phase current value (Timing chart)

1) 2-phase excitation drive (4-step sequence)
(ST1AB/ST1CD = Low, ST2AB/ST2CD = Low, ST3AB/ST3CD = Low)

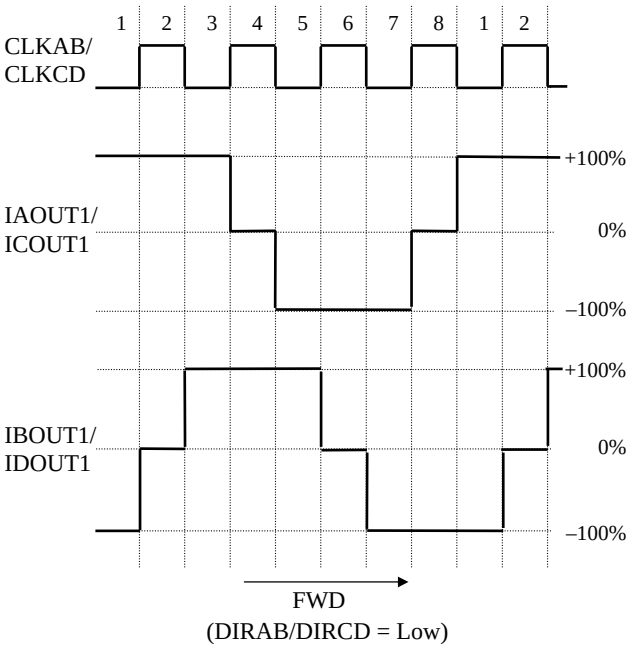


(DIRAB/DIRCD = Low)

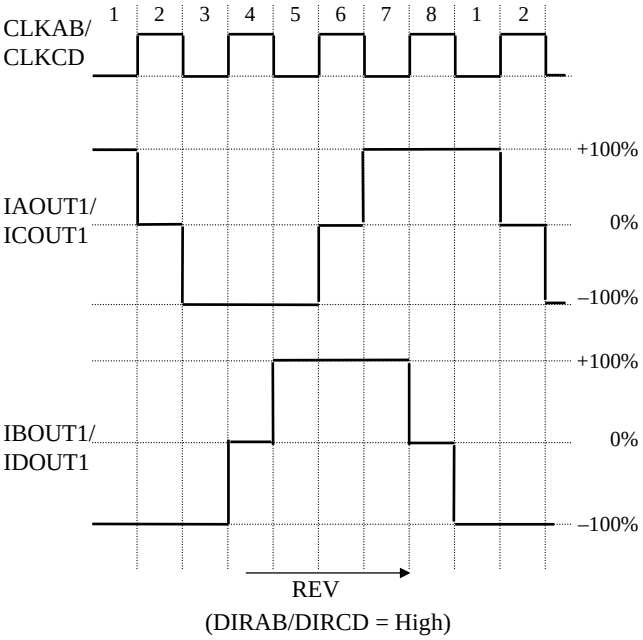


(DIRAB/DIRCD = High)

2) Half step drive (8-step sequence)
(ST1AB/ST1CD = Low, ST2AB/ST2CD = High, ST3AB/ST3CD = Low)



(DIRAB/DIRCD = Low)

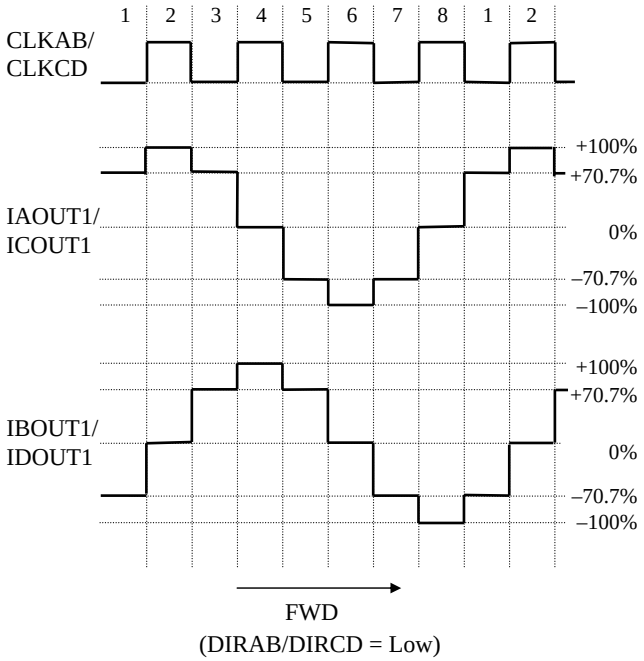


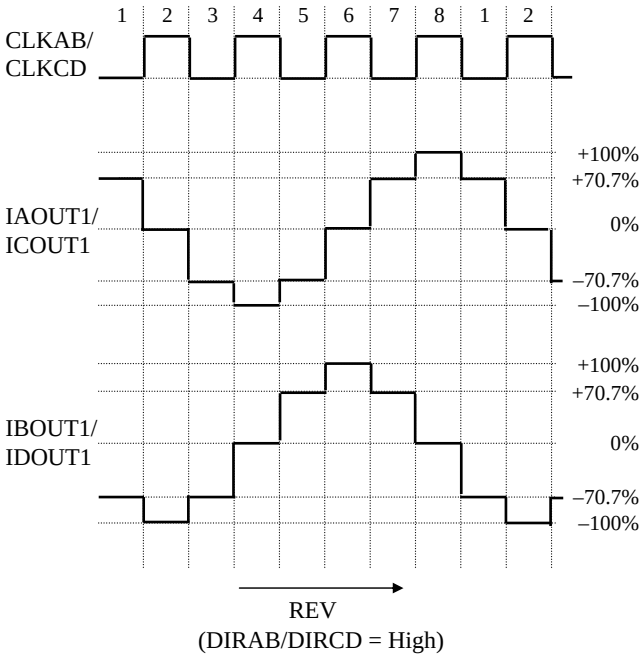
(DIRAB/DIRCD = High)

■ Technical Data (continued)

4. Each phase current value (Timing chart) (continued)

3) 1-2-phase excitation (8-step sequence)
(ST1AB/ST1CD = High, ST2AB/ST2CD = Low, ST3AB/ST3CD = Low)

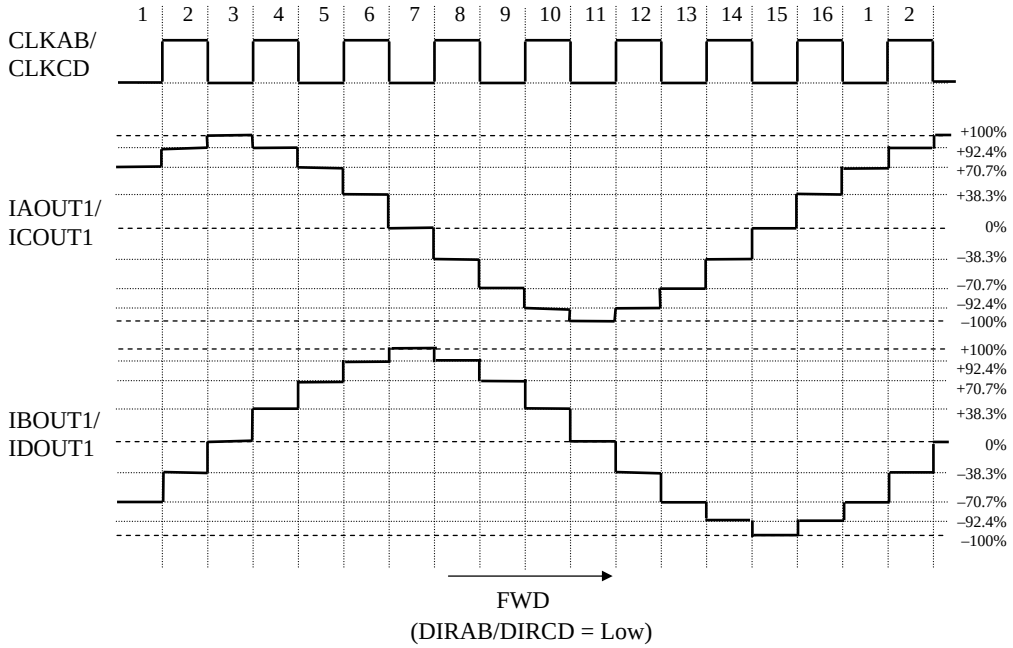




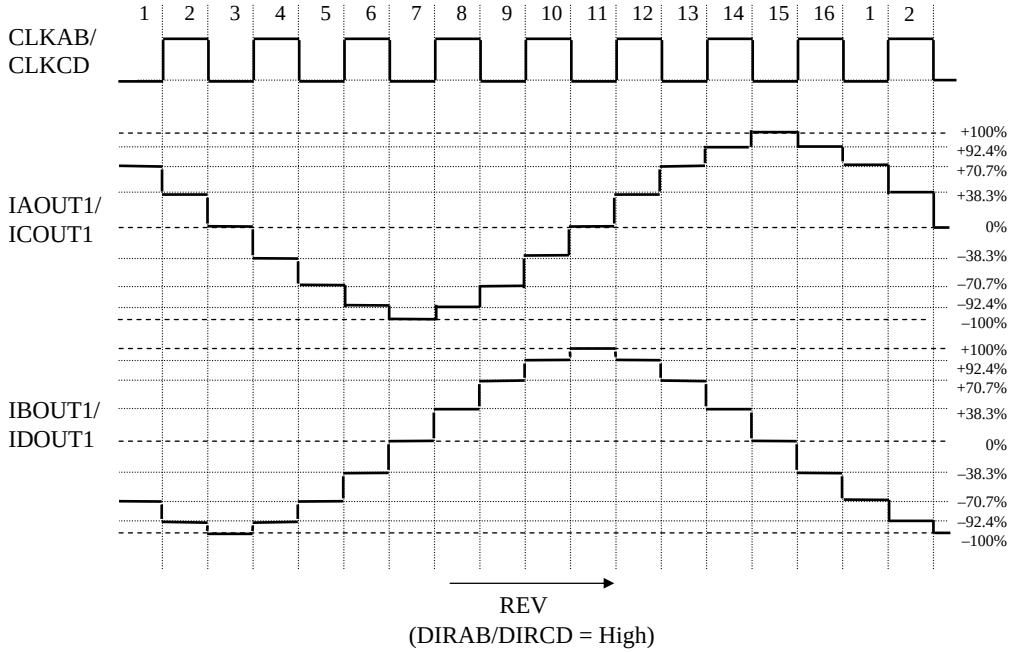
■ Technical Data (continued)

4. Each phase current value (Timing chart) (continued)

4) W1-2-phase excitation (16-step sequence)
(ST1AB/ST1CD = High, ST2AB/ST2CD = High, ST3AB/ST3CD = Low)



(DIRAB/DIRCD = Low)

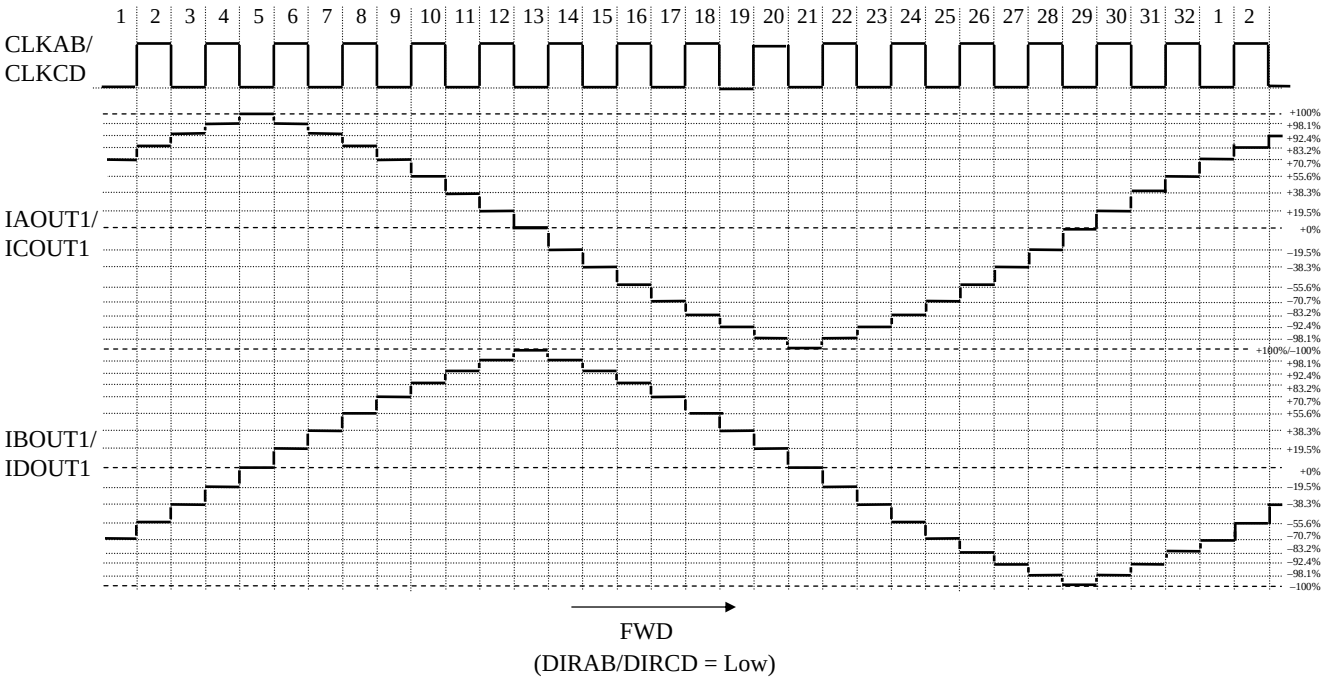


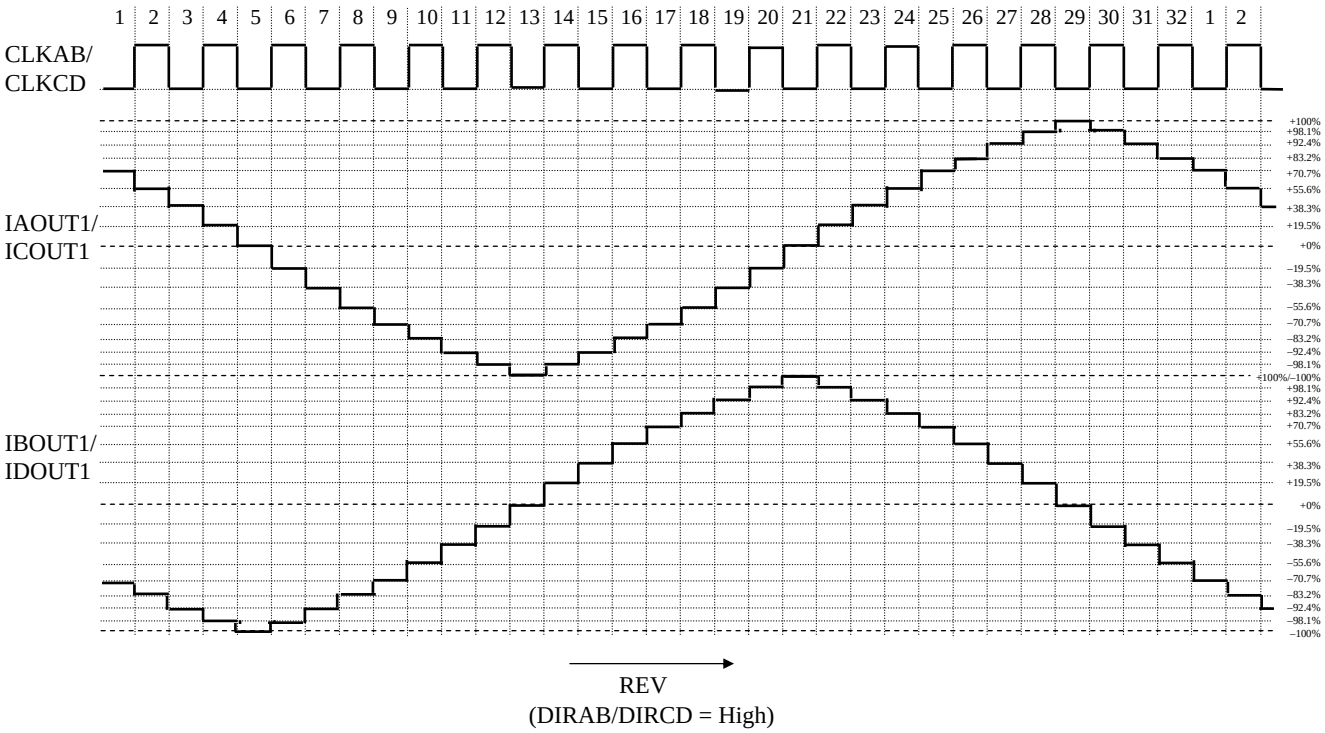
(DIRAB/DIRCD = High)

■ Technical Data (continued)

4. Each phase current value (Timing chart) (continued)

5) 2W1-2-phase excitation (32-step sequence)
(ST3AB/ST3CD = High)

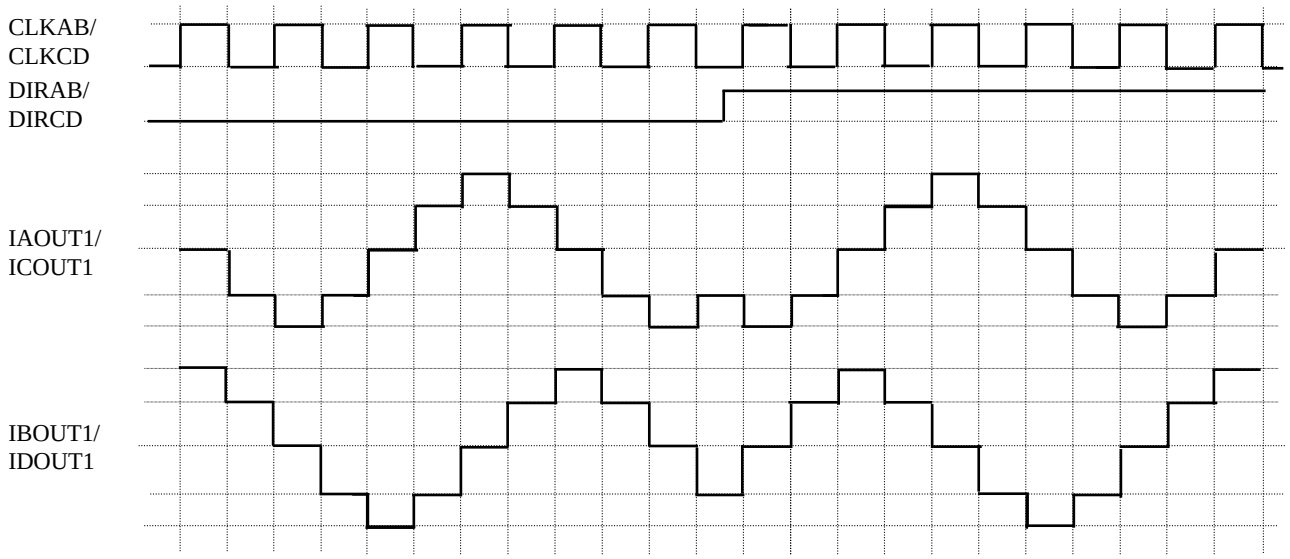




■ Technical Data (continued)

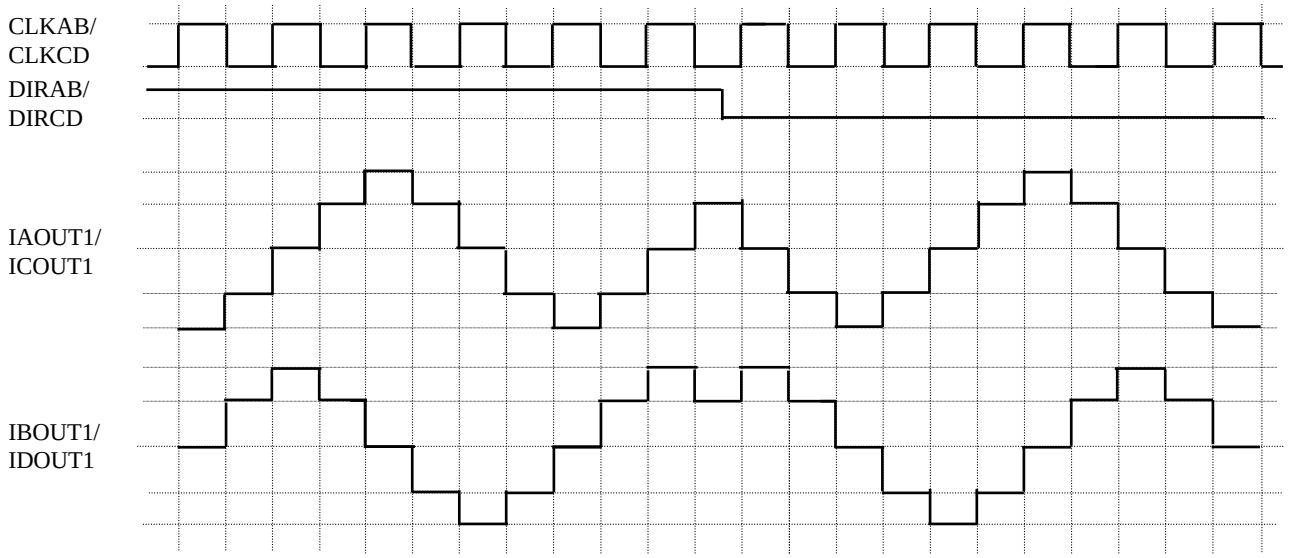
5. Timing chart when DIR switches

(Example 1) Timing chart at 1-2-phase excitation (DIRAB/DIRCD : Low → High)



When DIRAB(DIRCD) switches,
the state before switching is kept and operates continuously.

(Example 2) Timing chart at 1-2-phase excitation (DIRAB/DIRCD : High → Low)



When DIRAB(DIRCD) switches,
the state before switching is kept and operates continuously.

■ Technical Data (continued)

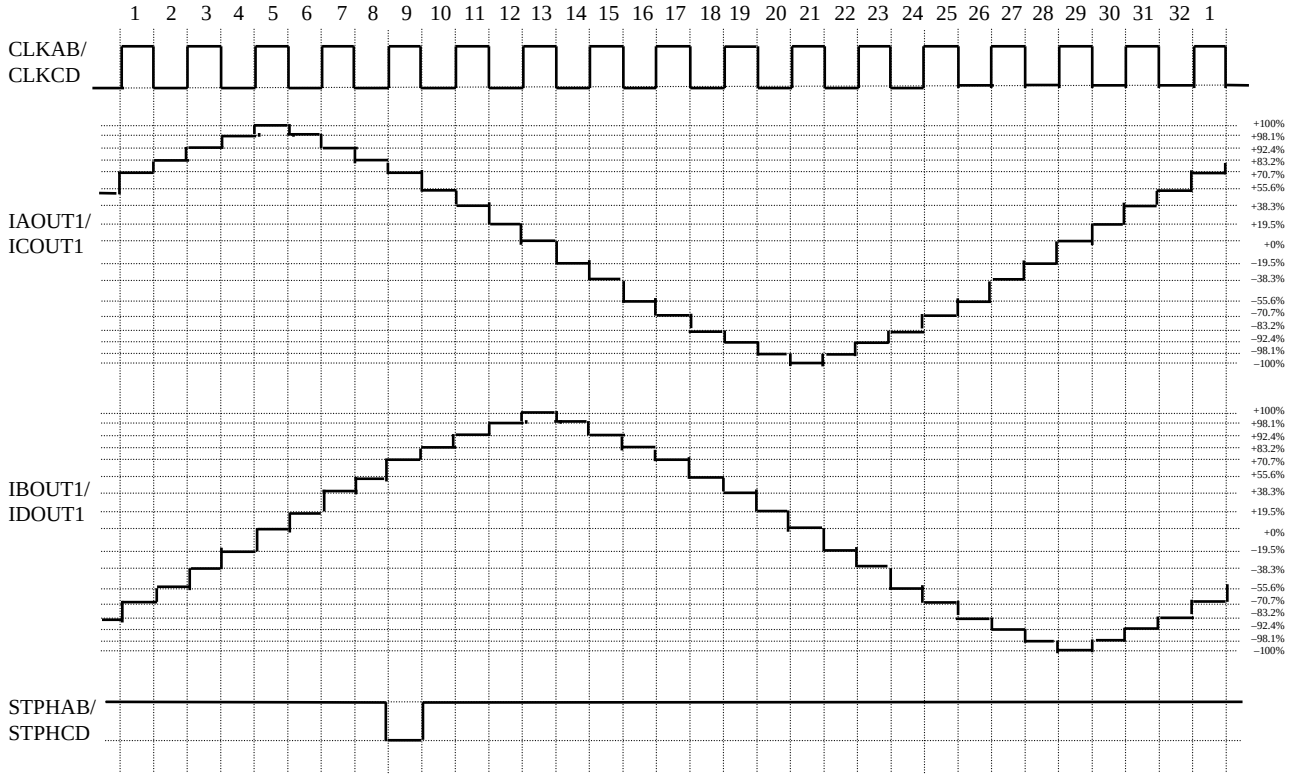
6. Home Position function (TEST = High)

This LSI has built-in Home Position function to reduce the displacement of motor current state at the change of excitation mode during motor drive. Low-level voltage is output to STPHAB pin and STPHCD pin at the timing when the displacement of motor current state doesn't occur at the change of excitation mode. The timing when Low-level voltage is output to STPHAB pin and STPHCD pin is as follows. The Home Position function becomes valid by setting TEST pin to High.

Connect pull-up resistor to power supply (recommendation : S5VOUT), because STPHAB pin and STPHCD pin are composed by open drain circuit. The recommended value of pull-up resistor is 10 kΩ.

• Home Position output timing chart (DIRAB / DIRCD = Low)

1) 2W1-2-phase excitation

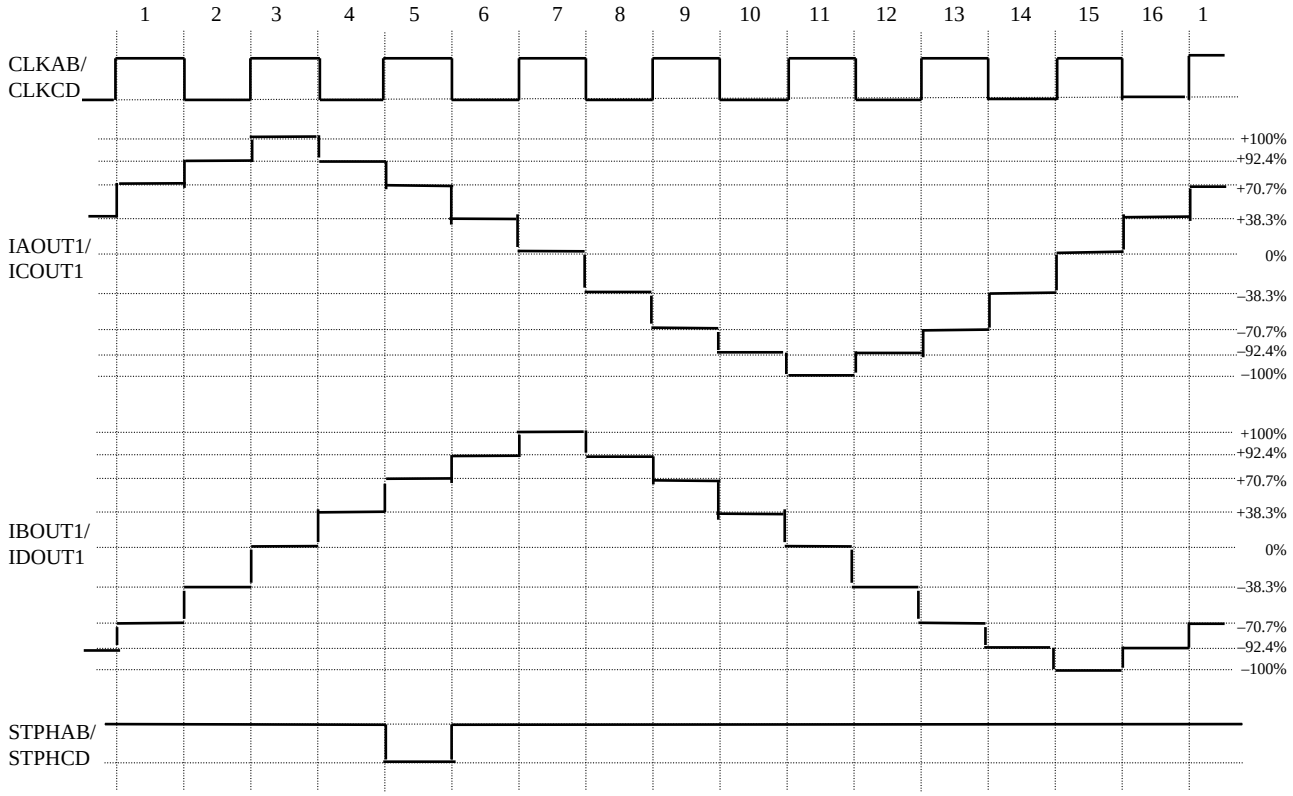


■ Technical Data (continued)

6. Home Position function (TEST = High) (continued)

- Home Position output timing chart (DIRAB / DIRCD = Low) (continued)

2) W1-2-phase excitation

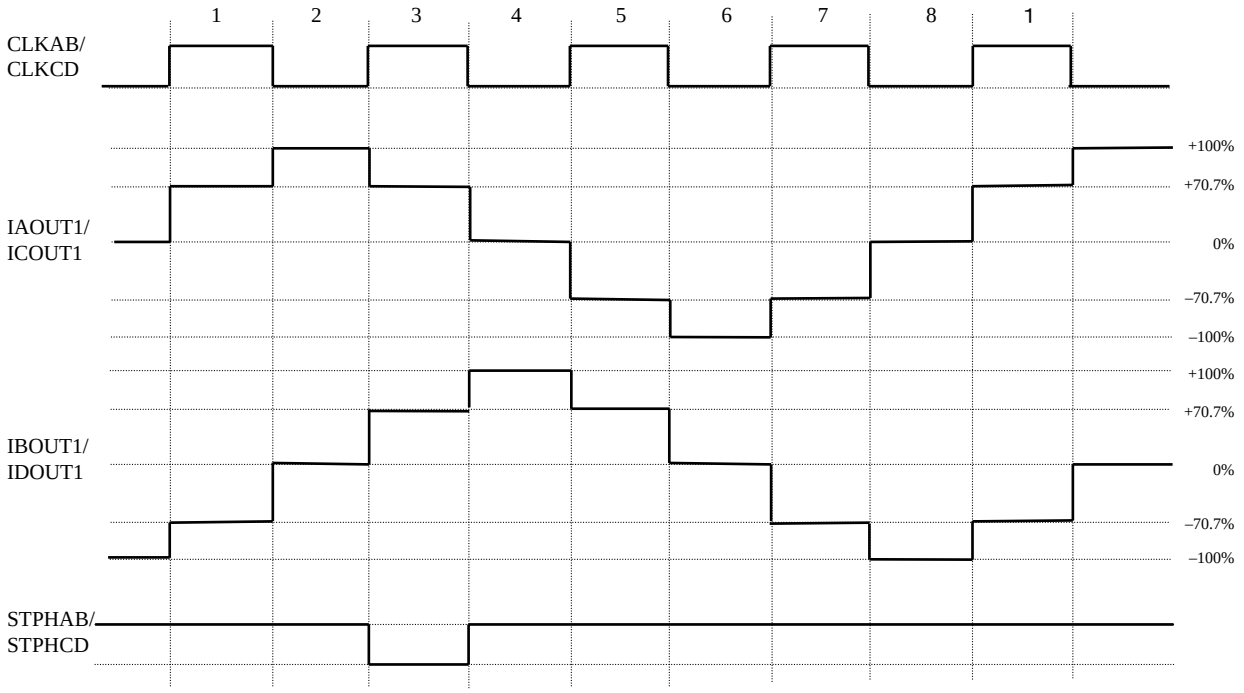


■ Technical Data (continued)

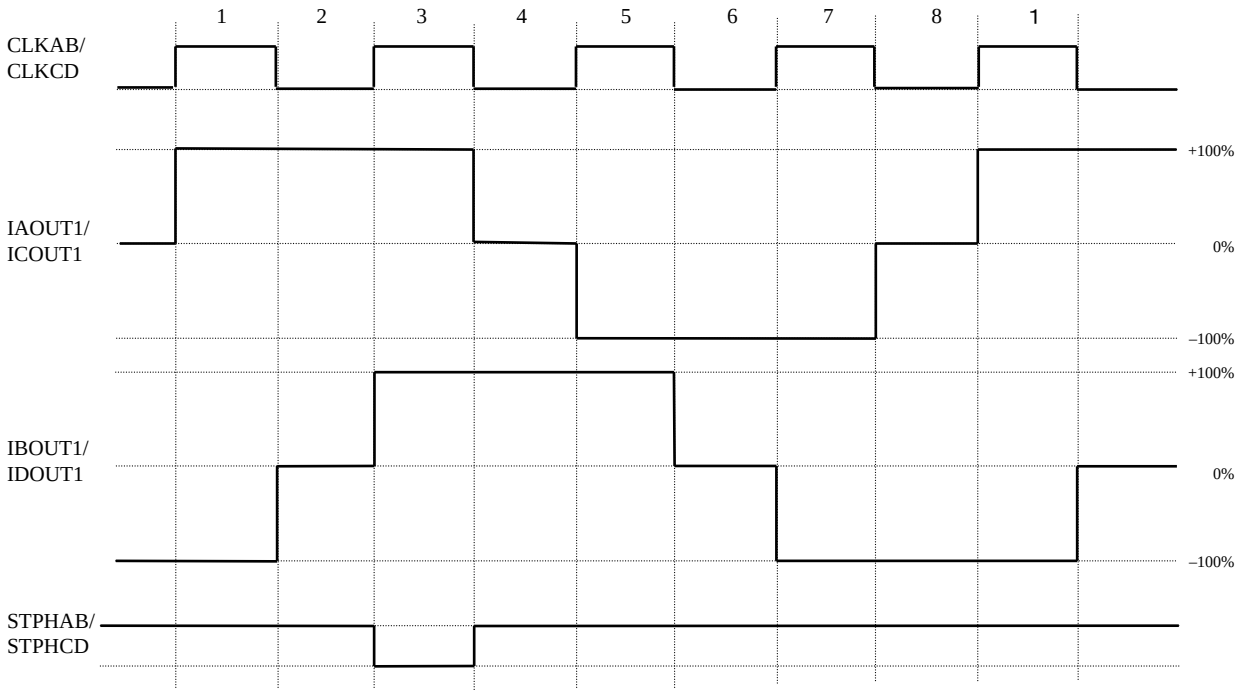
6. Home Position function (TEST = High) (continued)

- Home Position output timing chart (DIRAB / DIRCD = Low) (continued)

3) 1-2-phase excitation



4) Half step

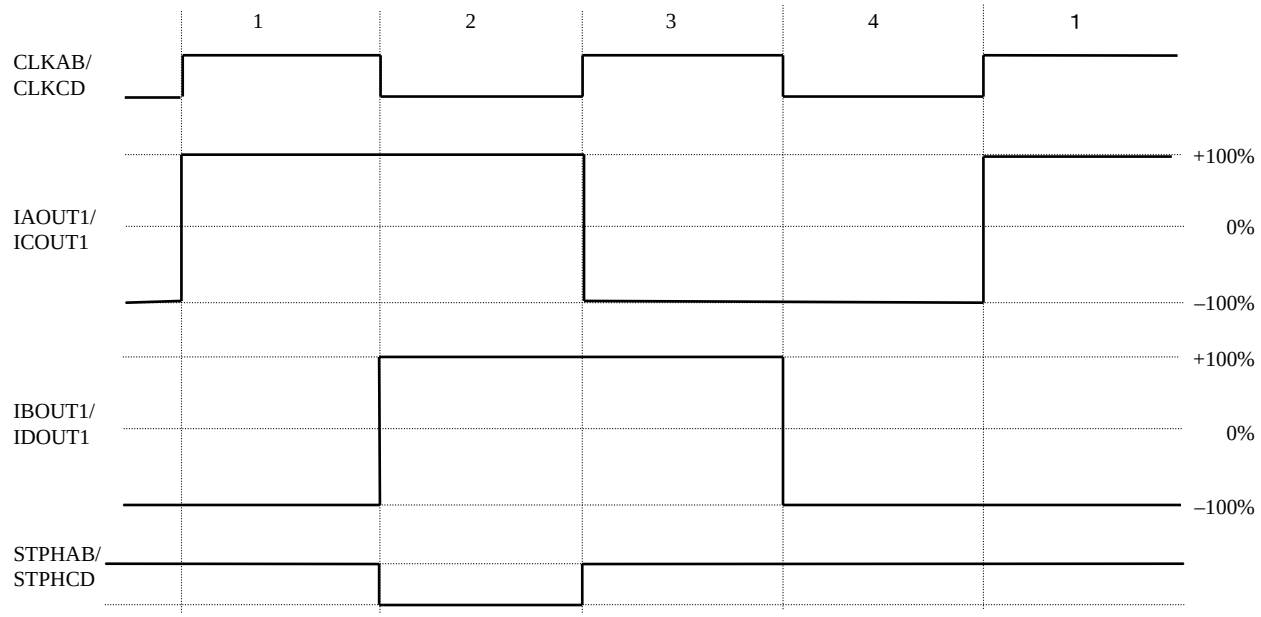


■ Technical Data (continued)

6. Home Position function (TEST = High) (continued)

- Home Position output timing chart (DIRAB / DIRCD = Low) (continued)

5) 2-phase excitation



■Technical Data (continued)

7. STEP detection output function (TEST = Low)

Whenever edges signal is input into clock input pins, this IC outputs Low pulse signal from step detection output pins. The Low pulse width depend on each excitation mode. Refer to the below table. The STEP detection function becomes valid by setting TEST pin to Low. Connect pull-up resistor to supply voltage (Recommendation : S5VOUT), because STPHAB pin and STPHCD pin are composed by open drain circuit. The recommended value of pull-up resistor is 10 kΩ.

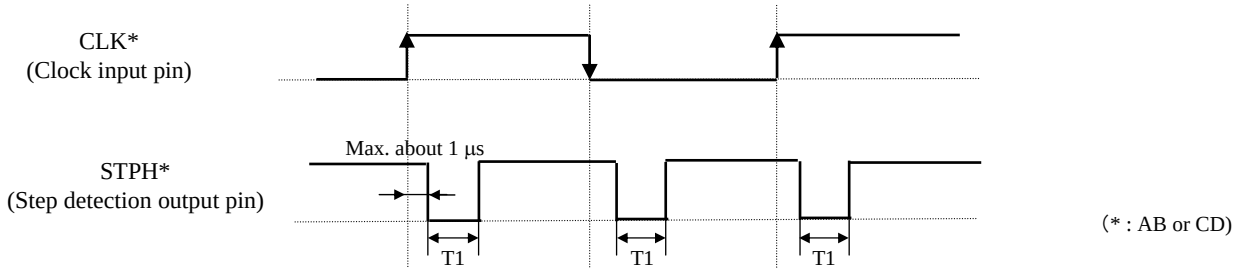


Table Step detection output pulse width

	2-phase excitation	Half step / 1-2 phase excitation	W1-2-phase excitation	2W1-2-phase excitation
Pulse width (T1)	About 20 µs	About 20 µs	About 10 µs	About 5 µs

8. Over-current protection function

This IC has over-current protection (OCP) circuit to protect from the ground-fault etc. of the motor output. When motor current more than setting value flows to power MOS for about 3.8 µs (Typ.) due to the ground-fault, all motor outputs are turned OFF by latch operation. OCP is canceled by STBY = Low or UVLO (Under-voltage lockout) operation. However, the OCP circuit do not guaranteed the protection circuit of set. Therefore, do not use the OCP function of this IC to protect a set. Note that this IC might break before the protection function operates when it instantaneously exceeds the safe operation area and the maximum rating. When the inductor element is large due to the length of wiring at ground-fault, note that this IC might break. Because the motor output voltage falls on a negative voltage or excessively rises after motor current excessively flows to motor outputs. The setup current of the OCP (reference) is as follows.

Table Over-current protection setup current (Typ. value)

	A/Bch motor output	C/Dch motor output
Setup current	2.2 A	3.3 A

9. About inputting the supply voltage to IF pins when VM power supply is not applied.

This IC does the measures of error for inputting voltage to IF pins when VM power supply is not applied.
IF pin : ENABLE*, DIR*, ST1*, ST2*, ST3*, CLK*, STBY, VREF* (* : AB or CD)
Therefore, this IC doesn't break and it doesn't cause error operation by the input voltage to the IF pins when VM supply voltage is not supplied.

■ Usage Notes

1. Special attention and precaution in using

1) This IC is intended to be used for general electronic equipment [Stepping motor drive].
Consult our sales staff in advance for information on the following applications:
・ Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this IC may directly jeopardize life or harm the human body.
・ Any applications other than the standard applications intended.
(1) Space appliance (such as artificial satellite, and rocket)
(2) Traffic control equipment (such as for automobile, airplane, train, and ship)
(3) Medical equipment for life support
(4) Submarine transponder
(5) Control equipment for power plant
(6) Disaster prevention and security device
(7) Weapon
(8) Others : Applications of which reliability equivalent to (1) to (7) is required
It is to be understood that our company shall not be held responsible for any damage incurred as a result of or in connection with your using the IC described in this book for any special application, unless our company agrees to your using the IC in this book for any special application.

2) Pay attention to the direction of LSI. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might smoke or ignite.

3) Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.

4) Perform a visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as a solder-bridge between the pins of the semiconductor device. Also, perform a full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.

5) Take notice in the use of this product that it might break or occasionally smoke when an abnormal state occurs such as output pin-V_M short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short) .
Especially, for the pins below, take notice Power supply fault, Ground fault, short to motor current detection pin, load short and short between the pin.
・ Motor drive output pin (Pin 1, 5, 24, 28, 29, 33, 52, 56)
・ Motor current detection pin (Pin 3, 26, 31, 54)
・ Charge pump circuit pin (Pin 16, 17, 18)
・ Power supply (Pin 41, 43)
And, safety measures such as an installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply.

6) When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

7) When using the LSI for new models, verify the safety including the long-term reliability for each product.

8) When the application system is designed by using this LSI, be sure to confirm notes in this book.
Be sure to read the notes to descriptions and the usage notes in the book.

9) Connect the metallic plate (fin) on the back side of the IC with the GND potential. The thermal resistance and the electrical characteristics are guaranteed only when the metallic plate (fin) is connected with the GND potential.

10) Confirm characteristics fully when using the LSI.
Secure adequate margin after considering variation of external part and this IC including not only static characteristics but transient characteristics. Especially, Pay attention that abnormal current or voltage must not be applied to external parts because the pins (Pin 1, 5, 16, 17, 18, 24, 28, 29, 33, 52, 56) output high current or voltage.

■ Usage Notes (continued)

2. Notes of Power LSI.

1) Design the heat radiation with sufficient margin so that Power dissipation must not be exceeded base on the conditions of power supply voltage, load and ambient temperature.
(It is recommended to design to set connective parts to 70% to 80% of maximum rating)
2) The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.
Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VM short (Power supply fault), or output pin to GND short (Ground fault), the LSI might be damaged before the thermal protection circuit could operate.
3) Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the device might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.
4) The product which has specified ASO (Area of Safe Operation) should be operated in ASO.
5) Verify the risks which might be caused by malfunctions of external parts.
6) Set capacitance value between VPUMP and GND so that VPUMP (Pin 18) must not exceed 43 V transiently at the time of motor standby to motor start.
7) This IC employs a PWM drive method that switches the high-current output of the output transistor. Therefore, the IC is apt to generate noise that may cause the IC to malfunction or have fatal damage. To prevent these problems, the power supply must be stable enough. Therefore, the capacitance between the S5VOUT and GND pins must be 0.1 μF and the one between the VM and GND pins must be a minimum of 47 μF and as close as possible to the IC so that PWM noise will not cause the IC to malfunction or have fatal damage.

■ Usage Notes (continued)

3. Notes of this IC

1) Pulse blanking time

This IC has pulse blanking time (0.7 μs/Typ.value) to prevent erroneous current detection caused by noise. Therefore, the motor current value will not be less than current determined by pulse blanking time. Pay attention at the time of low current control. The relation between pulse blanking time and minimum current value is shown as Chart 1. In addition, increase-decrease of motor current value is determined by L value, wire wound resistance, induced voltage and PWM on Duty inside a motor.

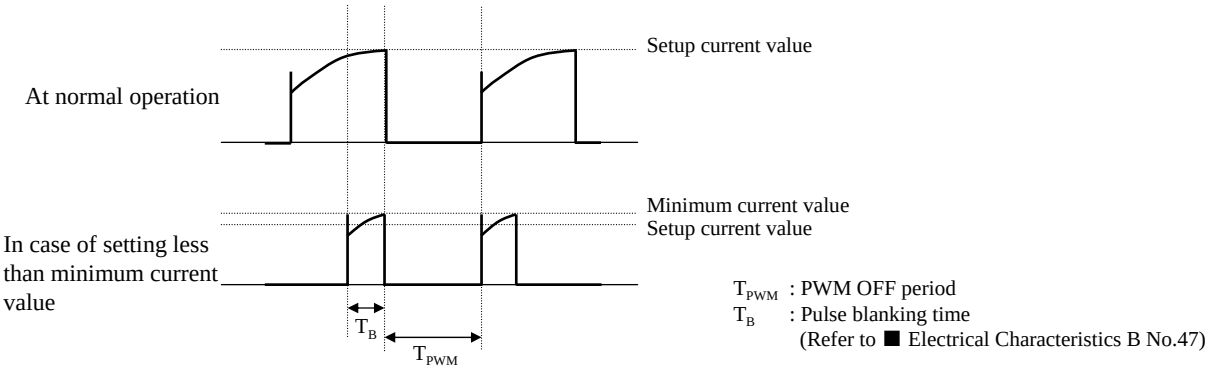


Chart 1. RCS current waveform

2) VREF voltage

When VREF* voltage is set to Low-level, erroneous detection of current might be caused by noise because threshold of motor current detection comparator becomes low (= VREF/10 × motor current ratio [%] (Refer to Page 33, 34). Use this IC after confirming no misdetection with setup VREF* voltage.

If VREF* pin is open, input voltage might be irregular and rise, a large current might flow to the output. Therefore do not use on condition that VREF* pin is open.

(* : AB or CD)

3) Notes on interface

Absolute maximum of Pin 6 to 8, Pin 12, Pin 21 to 23, Pin 34 to 40 and Pin 44 to 51 is –0.3 V to 6 V. When the setup current for a motor is large and lead line of GND is long, GND pin potential might rise. Take notice that interface pin potential is negative to difference in potential between GND pin reference and interface pin in spite of inputting 0 V to the interface pin. At that time, pay attention allowable voltage range must not be exceeded.

4) Notes on test mode

When inputting voltage of above 0.6 V and below 4.0 V to TEST (Pin 12), this LSI might become test mode.
When disturbance noise etc. makes this LSI test mode, motor might not operate normally. Therefore, use this LSI on condition that TEST pin is shorted to GND or S5VOUT at normal motor operation.

■ Usage Notes (continued)

3. Notes of this IC (continued)

5) Notes on Standby mode release / Under-voltage lockout release

This LSI has all motor outputs OFF period of about 100 μs (typ) owing to release of Standby and UVLO (Refer to the below figure).

This is why restart from Standby and UVLO after charge pump voltage rises sufficiently because charge pump operation stops at Standby and UVLO.

When the charge pump voltage does not rise sufficiently during all motor outputs OFF period due to that capacitance between VPUMP and GND becomes large etc., the IC might overheat and it might not operate normally. In this case, release Standby and UVLO at ENABLE = Low-level, and restart at ENABLE = High-level after the charge pump voltage rises sufficiently.

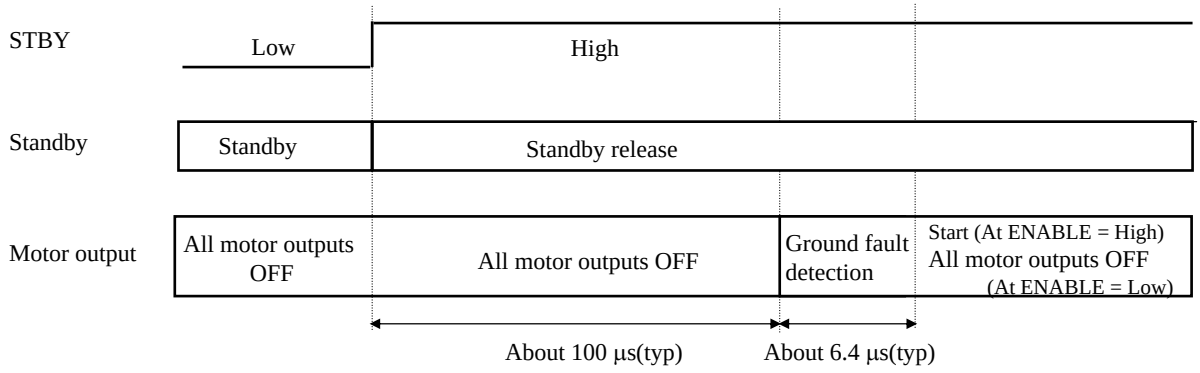
Moreover, take notice that state of motor current becomes default position at Standby and UVLO operation following as 3. Notes of this IC No.6.

After all motor outputs OFF period, the ground-fault detection period is set to about 6.4 μs in order to detect the ground-fault of motor output before motor is turned on.

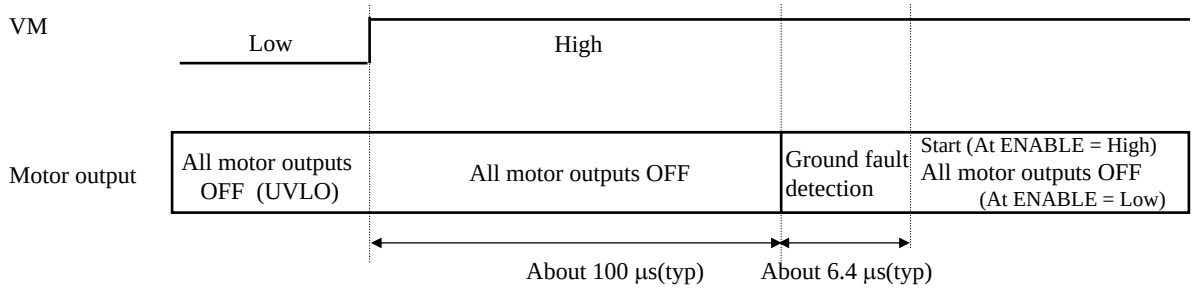
All the upper side power MOS are turned on during the above ground fault detection period, and then whether the ground-fault occurs or not is checked. (Refer to the following contents.)

If the ground-fault is detected at that time, all motor outputs are turned off, and motor drive stops.

【At Standby release】



【At under-voltage lockout release】



■ Usage Notes (continued)

3. Notes of this IC (continued)

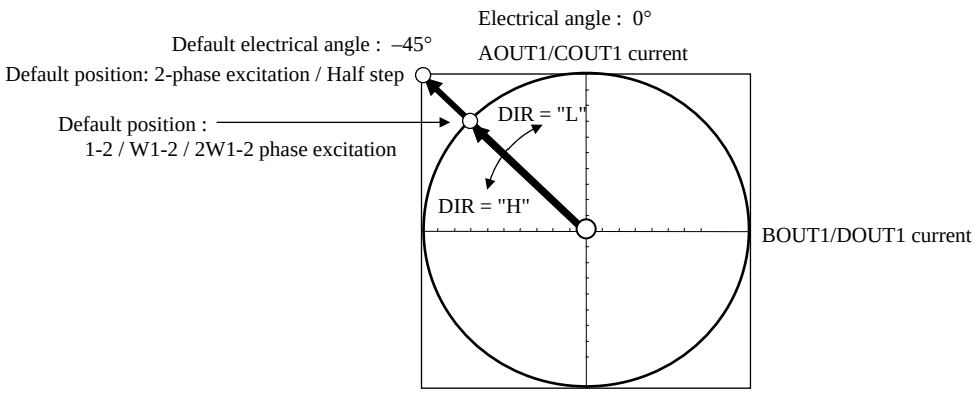
6) Default of motor current state

The defaults of motor current state after the releases of UVLO and standby in each excitation mode are as follows.

Table Default position of each excitation mode

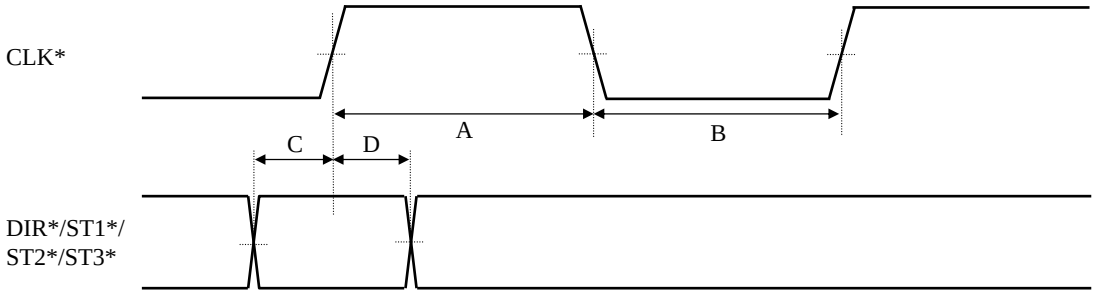
Excitation mode	Default electrical angle*
2-phase excitation (4-step)	–45°
Half step (8-step)	–45°
1-2 phase excitation (8-step)	–45°
W1-2 phase excitation (16-step)	–45°
2W1-2 phase excitation (32-step)	–45°

*Definition of electric angle
Electric angle is defined as 0° on the conditions of AOUT1/COUT1 current = 100% and BOUT1/DOUT1 current = 0%.
It is defined at DIR = Low as "+" direction.
It is defined at DIR = High as "–" direction.



7) CLK* input signal and DIR* input signal

The set/hold time of CLK* and DIR* input signals, CLK* input minimum pulse width (High/Low) are as follows.
Input signals after securing set/hold time.



Period	Contents	Time
A	CLK* input minimum pulse width (High)	10 μs or more
B	CLK* input minimum pulse width (Low)	10 μs or more
C	DIR*/ST1*/ST2*/ST3* set time	2 μs or more
D	DIR*/ST1*/ST2*/ST3* hold time	2 μs or more

* : AB or CD

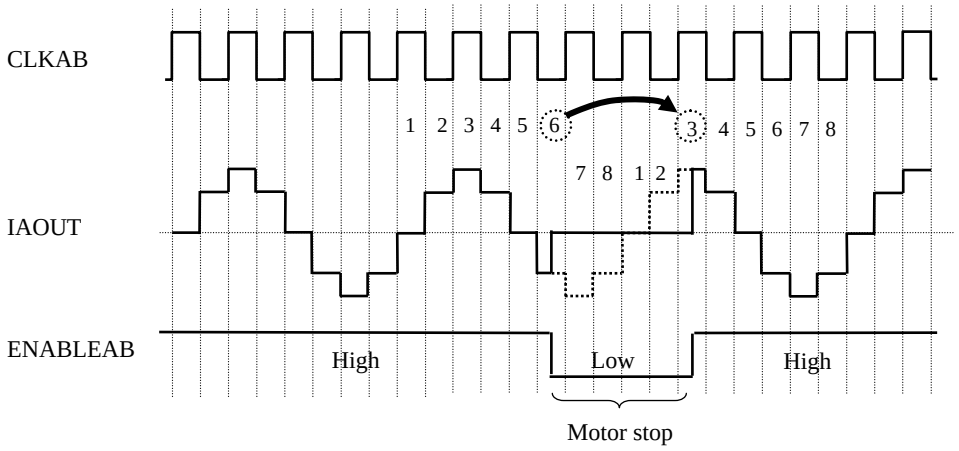
■ Usage Notes (continued)

3. Notes of this IC (continued)

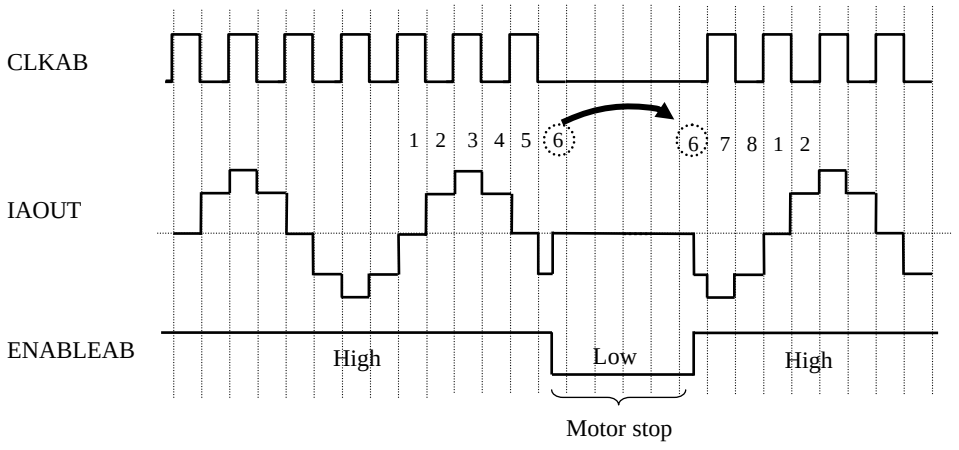
8) CLK input at ENABLE = Low

As the below figure (Ex. 1-2 phase excitation), when inputting CLKAB at the time of motor stop and ENABLEAB = Low (all motor outputs OFF → Motor current = 0 A), the setup value of motor current will proceed at CLKAB input. Therefore, in case of restart at ENABLEAB = High, take notice that the position of restart is where the current state just before motor stop gains CLKAB input. For IBOUT, ICOUT and IDOUT, the operation is same as the below.

Example) 1-2 phase excitation



In spite of stop at state[6] , because CLKAB is input at ENABLEAB = Low, the motor will restart after ENABLEAB = High at state [3].



In spite of stop at state [6] , because CLKAB is not input at ENABLEAB = Low, the motor will restart after ENABLE AB= High at state [6] just before stop.

■ Usage Notes (continued)

3. Notes of this IC (continued)

9) Notes on RCS line

Take consideration in the below figure and the points and design PCB pattern.

(1) Point 1

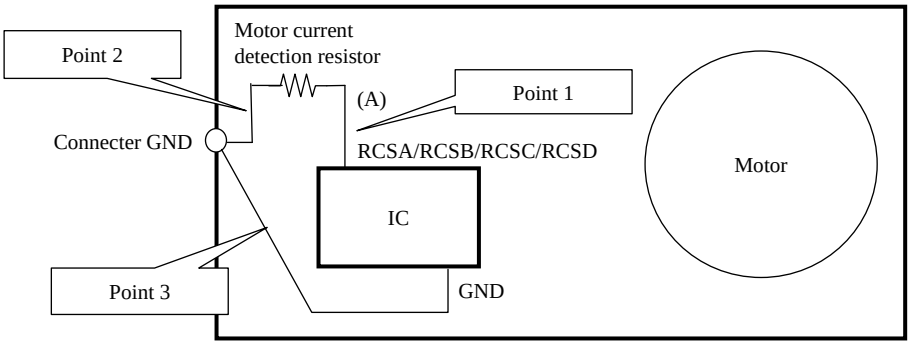
Design so that the wiring to the current detection pin (RCSA/RCSB/RCSC/RCSD pin) of this IC is thick and short to lower impedance. This is why current can not be detected correctly owing to wiring impedance and current might not be supplied to a motor sufficiently.

(2) Point 2

Design so that the wiring between current detection resister and connecter GND (the below figure Point 2) is thick and short to lower impedance. As the same as Point 1, sufficient current might not be supplied due to wiring impedance. In addition, if there is a common impedance on the side of GND of RCSA/RCSB/RCSC/RCSD, peak detection might be erroneous detection. Therefore, install the wiring on the side of GND of RCSA/RCSB/RCSC/RCSD independently.

(3) Point 3

Connect GND pin of this IC to the connecter on PCB independently. Separate the wiring removed current detection resister of large current line (Point 2) from GND wiring and make these wirings one-point shorted at the connecter as the below figure. That can make fluctuation of GND minimum.



10) A high current flows into the IC. Therefore, the common impedance of PCB can not be ignored. Take the following points into consideration and design the PCB pattern for a motor. Because the wiring connecting to VM1 (Pin 43) and VM2 (Pin 41)of this IC is high-current, it is easy to generate noise at time of switching by wiring L. That might cause malfunction and destruction (Figure 1). As Figure 2, the escape way of the noise is secured by connecting a capacitor to the connector close to the VM pin of the IC. This makes it possible to suppress the fluctuation of direct VM pin voltage of the IC. Make the setting as shown in Figure 2 as much as possible.

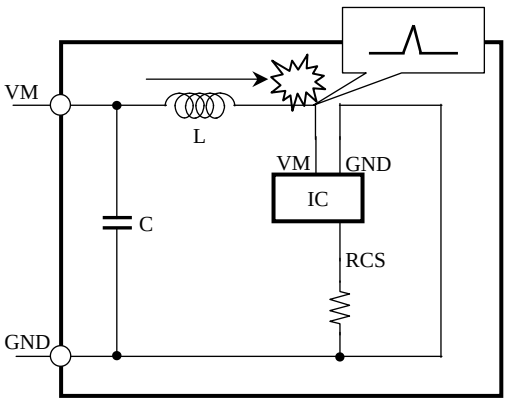


Figure 1. No recommended pattern

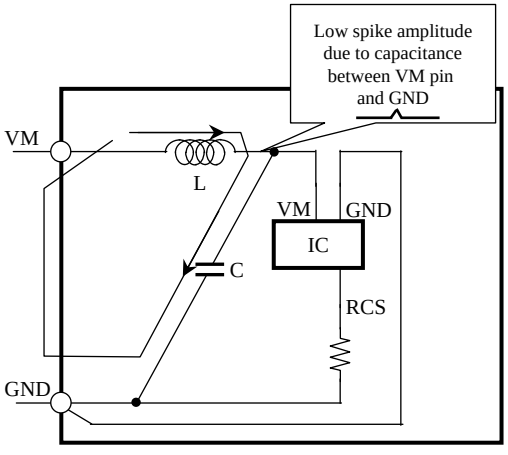


Figure 2. Recommended pattern

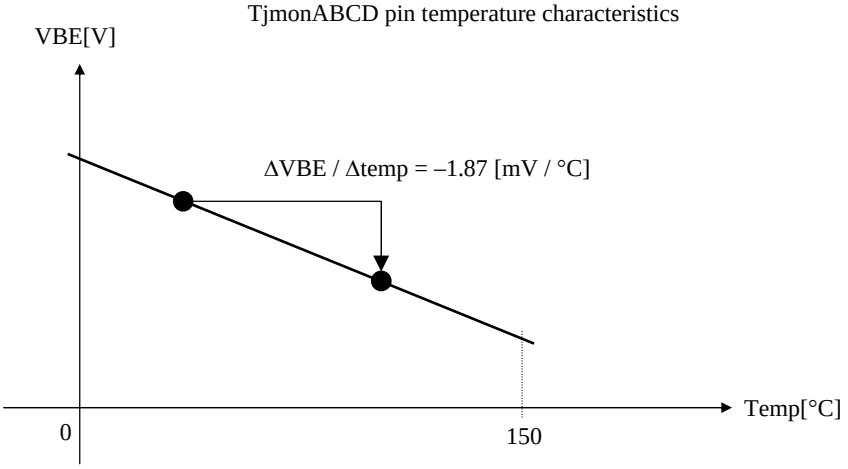
■ Usage Notes (continued)

3. Notes of this IC (continued)

11) IC junction temperature

In case of measuring chip temperature of this IC, measure the voltage of TjmonABCD pin (Pin 10) and estimate the chip temperature from the data below. However, because this data is technical reference data, conduct a sufficient reliability test of the IC and evaluate the product with the IC incorporated.

TjmonABCD pin temperature characteristics



12) Power-on and Supply voltage change

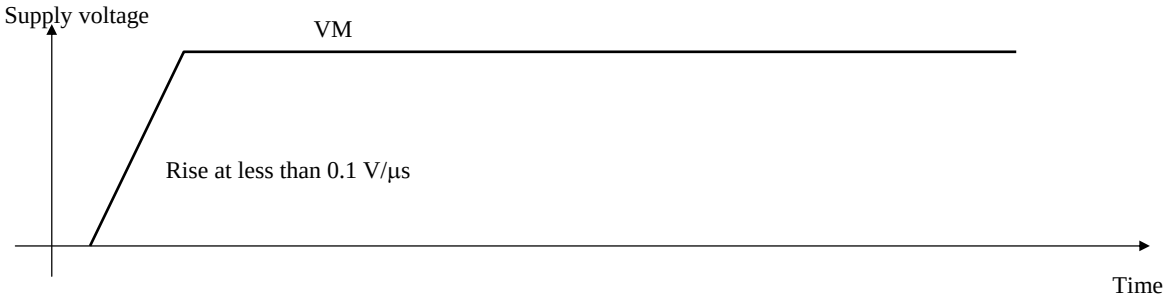
When supplying to VM pin (Pin 41, 43) or raising supply voltage, set the rise speed of VM voltage to less than 0.1 V/μs . If the rise speed of supply voltage is too rapid, it might cause error of operation and destruction of the IC. If the rise speed of VM voltage is more rapid than 0.1V/us, conduct a sufficient reliability test and also check a sufficient evaluation for a product.

In addition, rise the VM supply voltage in an ENABLE = Low state when change VM supply voltage from low voltage to high voltage within the operating supply voltage range.

Since there is not the all motor outputs OFF period shown in 3. Notes of this IC 5) (page 48) for the supply voltage change within the operating supply voltage range, the VPUMP voltage is in a low voltage state due to not following to VM supply voltage change enough, and this IC might not operate normally.

Therefore, restart this IC by setting ENABLE to High after the VPUMP voltage rises enough.

In addition, it is recommended to fall VM voltage in motor stop state (ENABLEAB/CD = Low or STBY = Low) for the stable fall of supply voltage.



13) Pins to set mode

- As for the High/Low setting of DECAY1AB, DECAY2AB, DECAY1CD, DECAY2CD, PWMSWAB and PWMSWCD, it is recommended to short to GND or S5VOUT. If the above pins are high-impedance such as open, note that this IC might not operate normally because it easily influences the noise
- PWMSWAB/CD can be set to Middle by setting PWMSWAB/CD to Open. However, it might occur the error of operation due to the noise. In case, connect the capacity of 0.01 μF or more between PWMSWAB/CD and GND .

Package Standards

Package Code	HSOP056-P-0300B

Semiconductor Company
Panasonic Corporation

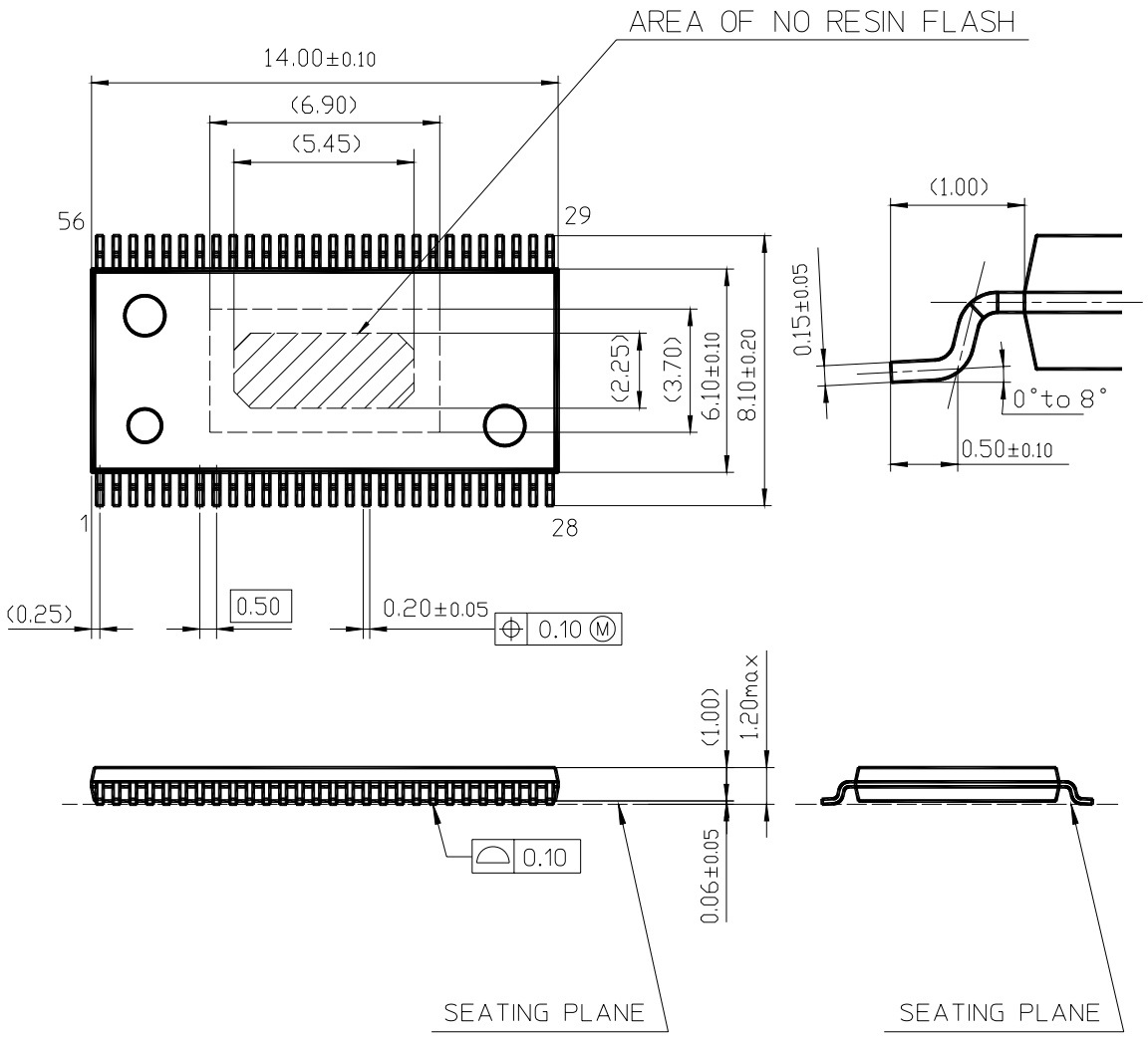
Established by	Applied by	Checked by	Prepared by
H.Shidooka	H.Yoshida	M.Okajima	M.Itoh

Established: 2009-06-05
Revised : -

1. Outline Drawing

Unit:mm

Package Code : HSOP056-P-0300B



Body Material	: Epoxy Resin
Lead Material	: Cu Alloy
Lead Finish Method	: Pd Plating

Established	Revised
-	-

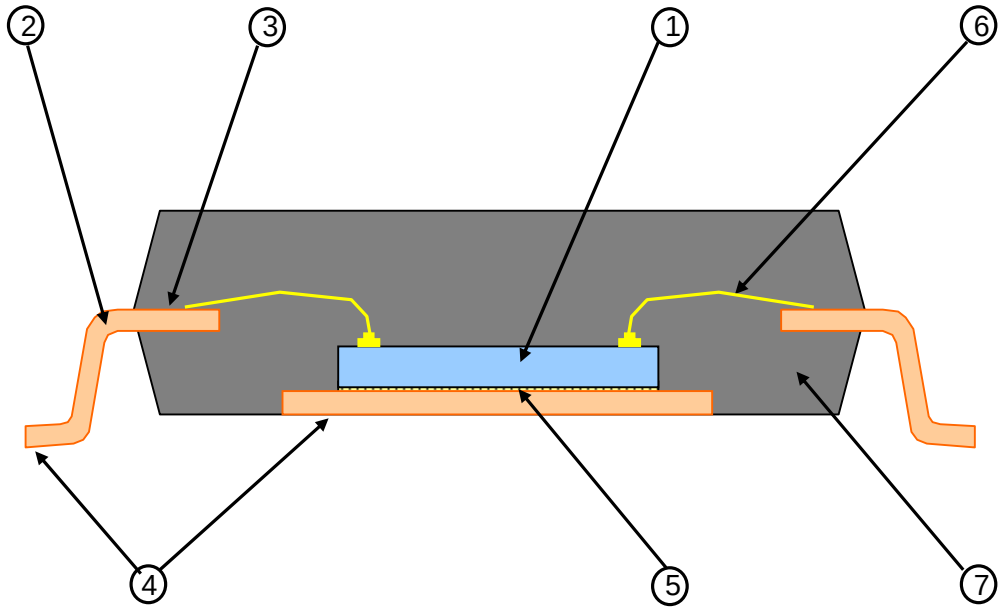
Semiconductor Company, Panasonic Corporation

Established: 2009-06-05
Revised : -

2. Package Structure (Technical Report : Reference Value)

Package Code : HSOP056-P-0300B

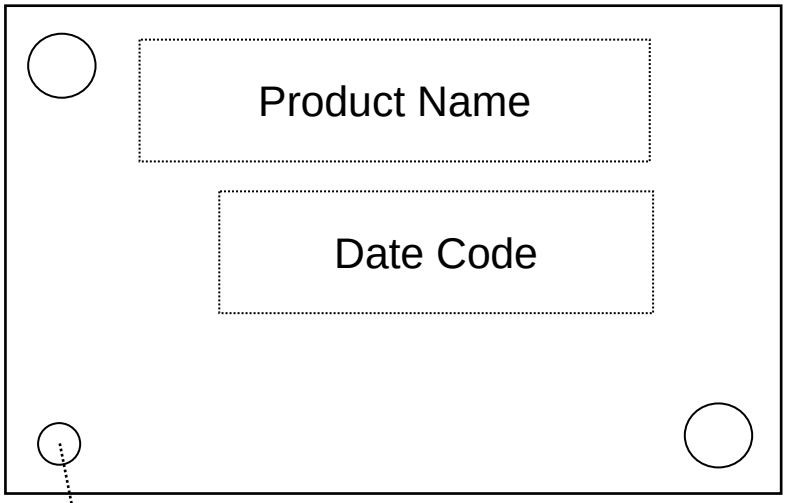
Chip Material		Si	①
Leadframe material		Cu alloy	②
Inner lead surface		Pd plating	③
Outer lead surface		Pd plating	④
Chip mount	Method	Resin adhesive method	⑤
	Material	Adhesive material	
Wirebond	Method	Thermo-compression bonding	⑥
	Material	Au	
Molding	Method	Transfer molding	⑦
	Material	Epoxy resin	
Mass		250 mg	



Established: 2009-06-05
Revised : -

3. Mark Layout

Package Code : HSOP056-P-0300B

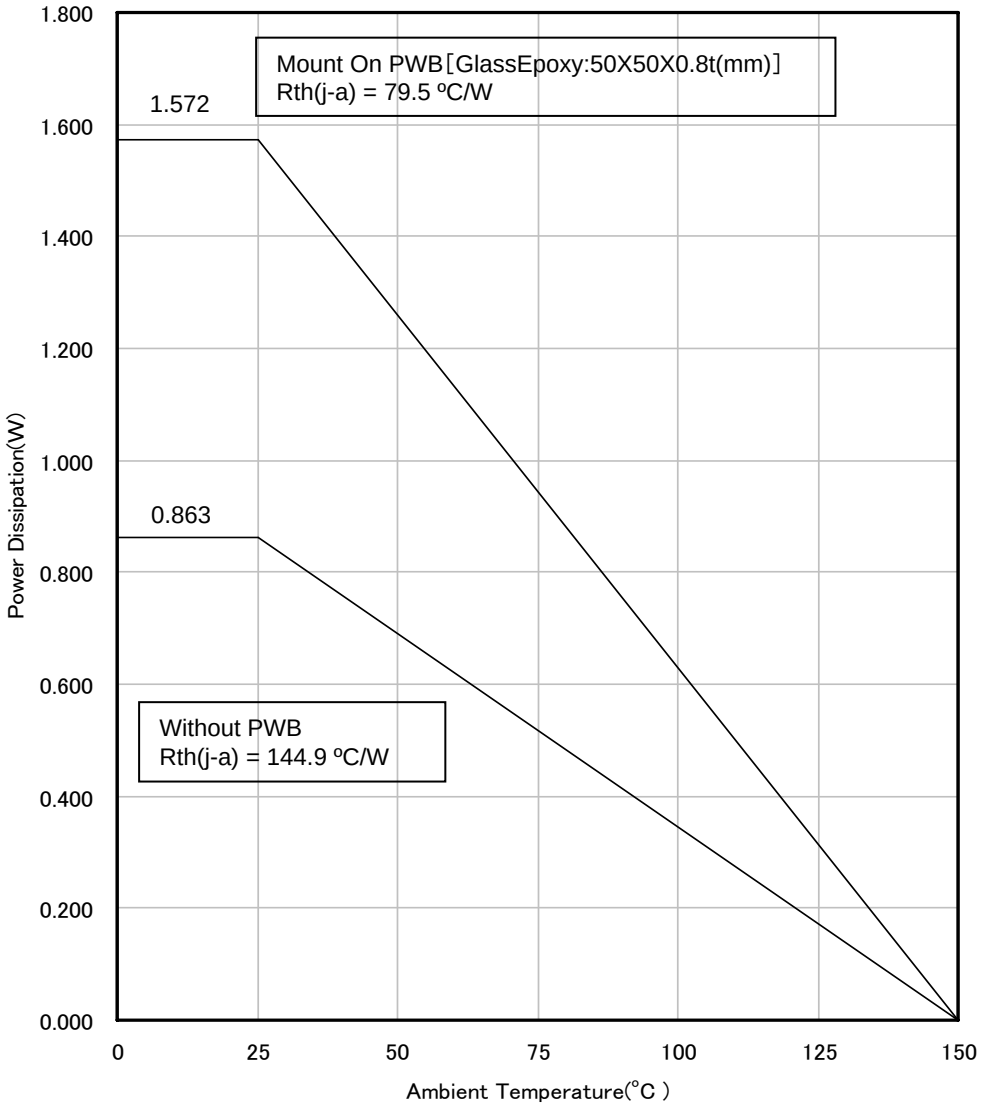


1-pin direction

Established: 2009-06-05
Revised : -

4. Power Dissipation (Technical Report)

Package Code : HSOP056-P-0300B



Established: 2009-06-05
Revised : -

5. Power Dissipation (Supplementary Explanation)

[Experiment environment]

Power Dissipation（Technical Report）is a result in the experiment environment of SEMI standard conformity. （Ambient air temperature (Ta) is 25 degrees C）

[Supplementary information of PWB to be used for measurement]

The supplement of PWB information for Power Dissipation data (Technical Report）are shown below.

Indication	Total Layer	Resin Material
Glass-Epoxy	1-layer	FR-4
4-layer	4-layer	FR-4

[Notes about Power Dissipation（Thermal Resistance）]

Power Dissipation values（Thermal Resistance）depend on the conditions of the surroundings, such as specification of PWB and a mounting condition , and a ambient temperature. (Power Dissipation (Thermal Resistance) is not a fixed value.)

The Power Dissipation value（Technical Report）is the experiment result in specific conditions (evaluation environment of SEMI standard conformity) ,and keep in mind that Power Dissipation values (Thermal resistance) depend on circumference conditions and also change.

[Definition of each temperature and thermal resistance]

Ta ：Ambient air temperature

※The temperature of the air is defined at the position where the convection, radiation, etc. don't affect the temperature value, and it's separated from the heating elements.

Tc ：It's the temperature near the center of a package surface. The package surface is defined at the opposite side if the PWB.

Tj ：Semiconductor element surface temperature (Junction temperature.)

Rth(j-c)：The thermal resistance (difference of temperature of per 1 Watts) between a semiconductor element junction part and the package surface

Rth(c-a)：The thermal resistance (difference of temperature of per 1 Watts) between the package surface and the ambient air

Rth(j-a)：The thermal resistance (difference of temperature of per 1 Watts) between a semiconductor element junction part and the ambient air

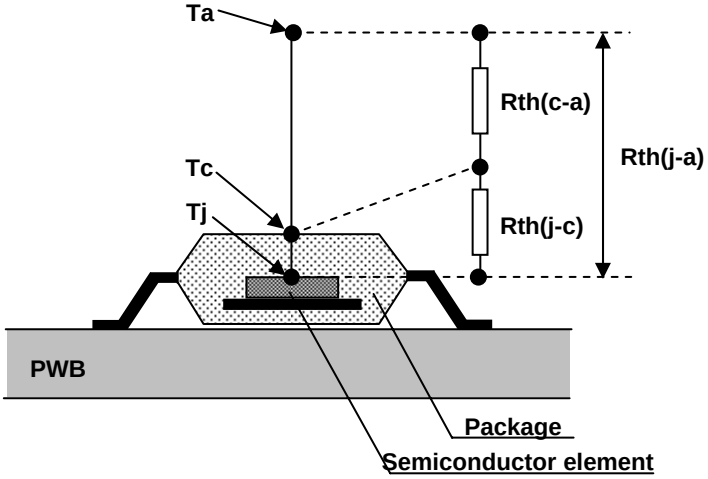


Fig1. Definition image

[Definition formula]

$$Tj=\{Rth(j-c)+Rth(c-a)\}\times P+Ta$$

$$=Rth(j-a)\times P+Ta$$

$$Rth(j-c)=\frac{Tj-Tc}{P}\ (℃/W)$$

$$Rth(c-a)=\frac{Tc-Ta}{P}\ (℃/W)$$

$$Rth(j-a)=\frac{Tj-Ta}{P}\ (℃/W)$$

$$=Rth(j-c)+Rth(c-a)$$

P:power(W)

Established: 2009-06-05
Revised : -

	Recommended Soldering Conditions	Total pages	page
		2	1

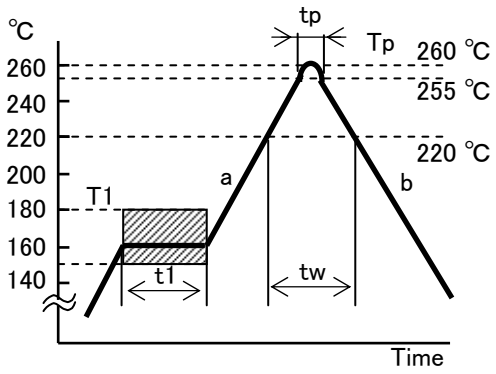
Product name : AN44071A-VF
Package : HSOP056-P-0300B

1. Recommended Soldering Conditions

In case that the semiconductor packages are mounted on the PCB, the soldering should be performed under the following conditions.

① Reflow soldering

Reflow peak temp. :	max. 260 ℃



No.	mark	contents	value
1	T1	Pre-heating temp.	150 ℃～180 ℃
2	t1	Pre-heating temp. hold time	60 s～120 s
3	a	Rising rate	2 ℃/s～5 ℃/s
4	Tp	Peak temp.	255 ℃+5 ℃、-0 ℃
5	tp	Peak temp. hold time	10 s±3 s
6	tw	High temp. region hold time	within 60 s (≧220 ℃)
7	b	Down rate	2 ℃/s～5 ℃/s
8	-	Number of reflow	within 2 times

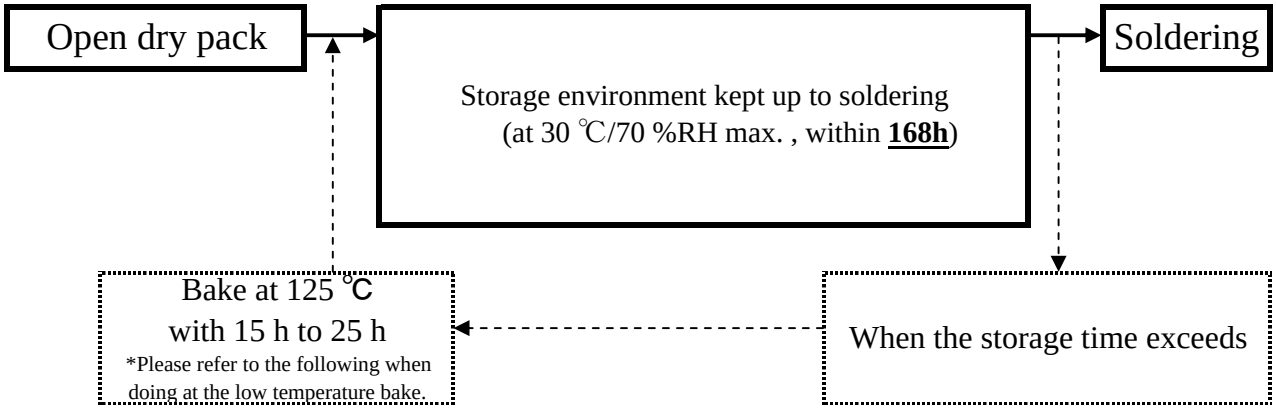
＊Peak temperature : less than 260 ℃
＊Temperature is measured at package surface point

② Wave soldering (Flow soldering)
＊Temp. of solder : 260 ℃ or less
＊Soak time : within 5 s
＊Number of flow : only 1 time

③ Manual soldering
＊Iron Temperature : 350 ℃ or less (Device lead temperature : 270 ℃、10 s max.)
＊Soldering time : within 3 s
＊Number of manual soldering : only 1 time

2012/3/6		
Prepared	Revised	

2. Storage environment after dry pack opening



※ Because the taping and the magazine materials are not the heat-resistant materials, the bake at 125℃ cannot be done.
Therefore, please solder everything or control everything in the rule time.
Please keep them in an equal environment with the moisture-proof packaging or dry box.
(Temperature: room temperature, relative humidity: 30% or less.)
To control storage time, when bake in the taping and the magazine is necessary, it is necessary for each type to set a bake condition. Please inquire of our company.

☆ **AN44071A-VF limitation, low temperature bake condition : 40 ℃ / 25 %RH or less / 192 h**

3. Note

① Storage environment conditions: keep the following conditions Ta=5 ℃～30 ℃、RH=30 %～70 %.

② Storage period before opening dry pack shall be 1year from a shipping day under Ta=5 ℃～30 ℃、RH=30 %～70 %. When the storage exceeds, Bake at 125 ℃ with 15 h to 25 h.

③ Baking cycle should be only one time.
Please be cautious of solderability at baking.

④ In case that use reflow two times, 2nd reflow must be finished within **168 hours.**

⑤ Remove flux sufficiently from product in the washing process.
(Flux : Chlorineless rosin flux is recommended.)

⑥ In case that use ultrasonic for product washing,
There is the possibility that the resonance may occur due to the frequency and shape of PCB.
It may be affected to the strength of lead. Please be cautious of this matter.

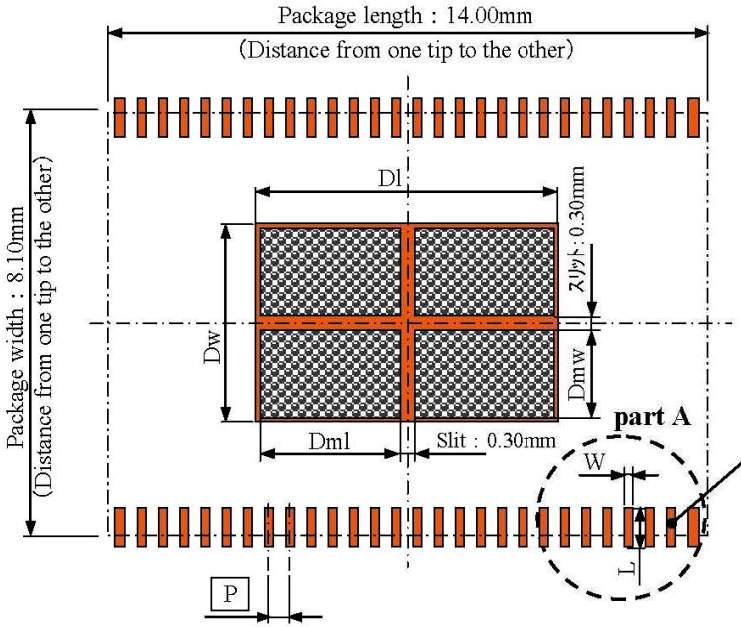
PCB & Mask spec. for HSOP-56pin

Assembly Technology Center
Semiconductor Company
Panasonic Corporation

Reference

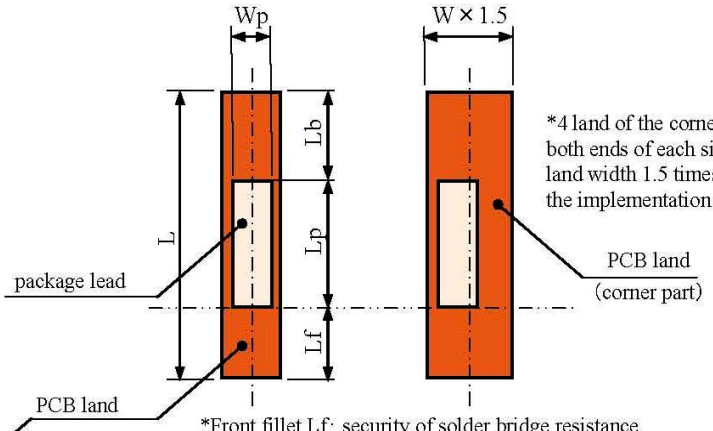
【Whole PCB land figure】

(Reference figure) Package code : HSOP056-P-0300 (0.50mmP/56pin)

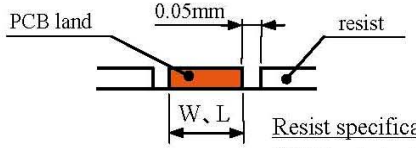


【Expansion of part A】

<Layout of PCB land and package land>



【PCB land cross-sectional figure】



Metal mask thickness
: 0.13～0.15mmt

Resist specifications : Normal resist (NSMD)
(PCB land size + 0.10mm (One side + 0.05mm))

■List of recommended dimensions for QFP

Terminal pitch P	Package lead			PCB land					Metal mask opening (Unit: mm)		
	Width Wp	Length Lp	Diepad size Dpl×Dpw	Width W	Length L	Front fillet Lf	Back fillet Lb	Diepad Dl × Dw	Width Wm	Length Lm	Diepad size Dml×Dmw
0.50mmP	0.20	0.50	6.90×3.70	0.30	1.20～1.40	0.30～0.40	0.40～0.50	7.00×3.80	Same as the PCB land		3.30×1.70×4 (Width of slit 0.30)

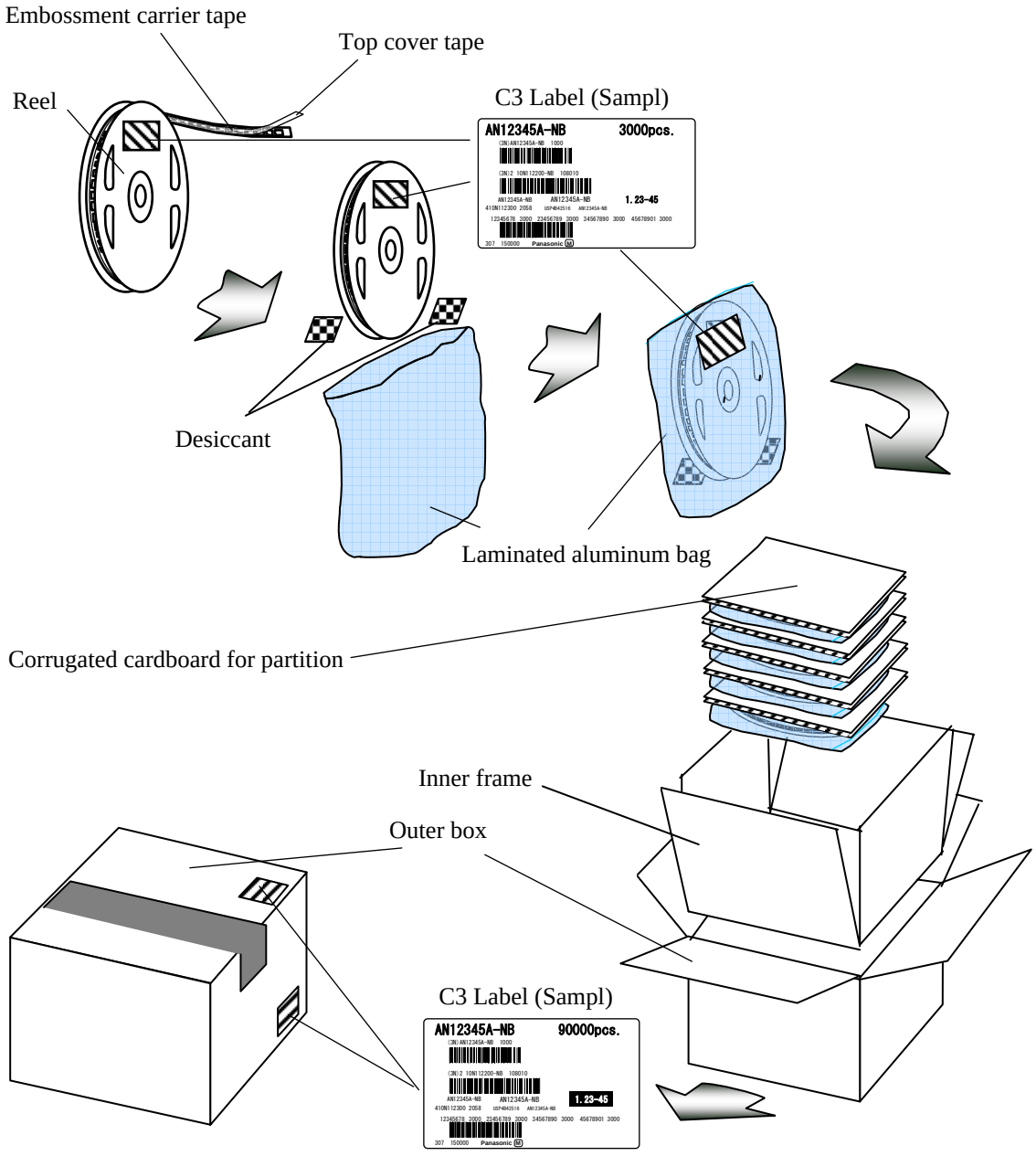
*The above size is calculated based on the experiment results by Matsushita Electric Industrial Co., Ltd., and is not intended as a guarantee of mounting reliability. Mounting reliability can vary depending on factors such as the equipment specifications and conditions, material specifications and properties, and environmental conditions. To ensure satisfactory results, your company should evaluate and confirm actual mounting performance.

Recommended Land Pattern

Total pages 1
page 1

Specifications of packing by the embossment tape

(Specifications for dampproof packing of the reel without the inner carton)



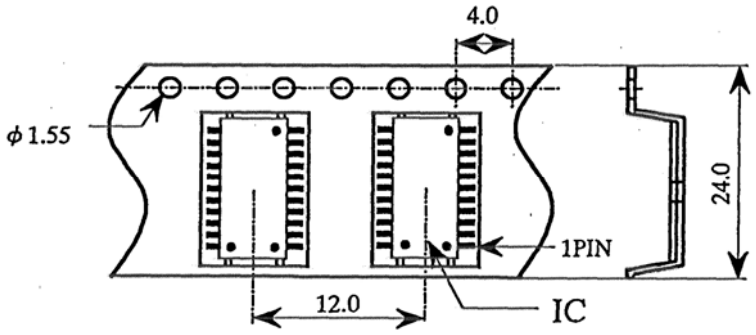
Package : HSOP056-P-0300B

Unit : mm

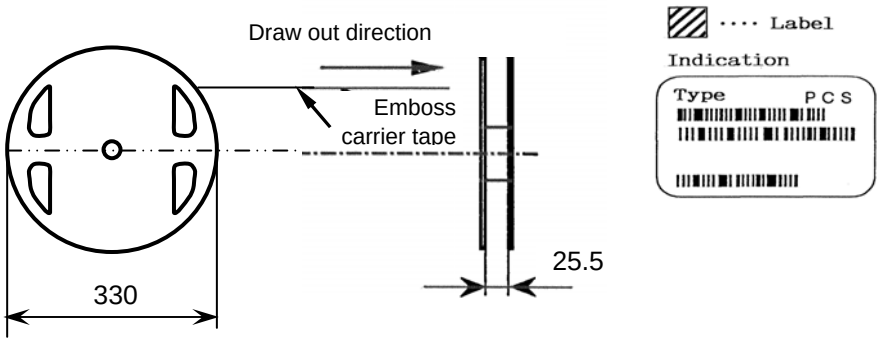
1 Packing

1) Tape

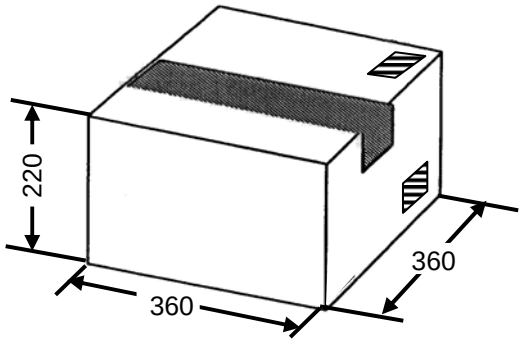
V F



2) Reel



3) Packing case

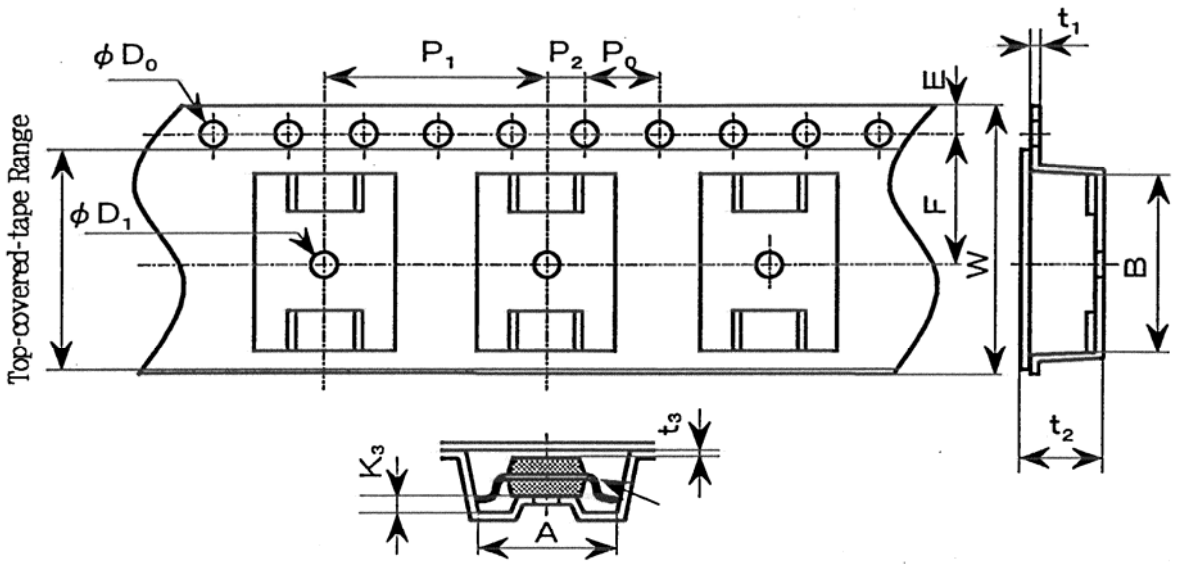


2 Packing quantity

Form	IC quantity	Contents
Reel	3000 Pcs	Reel × 1Pcs
Packing case	15000 Pcs	Reel × 5Pcs

Package : HSOP056-P-0300B

Unit : mm



Unit : mm

Dimensions & Tolerance					
W	A	B	E	F	P₁
24.0±0.3	8.7±0.1	14.5±0.1	1.75±0.1	11.5±0.1	12.0±0.1
P₂	Po	φ D₁	φ Do	t₁	t₂
2.0±0.1	4.0±0.1	2.05±0.05	1.55±0.05	0.3±0.05	1.9max
t₃	K₁				
(0.1)	(0.3)				

Panasonic

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Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001
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Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

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http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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