Energy Metering IC with Pulse Output

Data Sheet

ADE7755

FEATURES

High accuracy, surpasses 50 Hz/60 Hz IEC 687/IEC 1036
Less than 0.1% error over a dynamic range of 500 to 1
Supplies active power on the frequency outputs, F1 and F2
High frequency output CF is intended for calibration and supplies instantaneous active power
Synchronous CF and F1/F2 outputs
Logic output REVP provides information regarding the sign of the active power
Direct drive for electromechanical counters and 2-phase stepper motors (F1 and F2)
Programmable gain amplifier (PGA) in the current channel facilitates usage of small shunts and burden resistors
Proprietary ADCs and DSPs provide high accuracy over large variations in environmental conditions and time
On-chip power supply monitoring
On-chip creep protection (no load threshold)
On-chip reference 2.5 V ± 8% (30 ppm/°C typical) with external overdrive capability
Single 5 V supply, low power (15 mW typical)
Low cost CMOS process

GENERAL DESCRIPTION

The ADE7755 is a high accuracy electrical energy measurement IC. The part specifications surpass the accuracy requirements as quoted in the IEC 1036 standard.

The only analog circuitry used in the ADE7755 is in the ADCs and reference circuit. All other signal processing (for example, multiplication and filtering) is carried out in the digital domain. This approach provides superior stability and accuracy over extremes in environmental conditions and over time.

The ADE7755 supplies average active power information on the low frequency outputs, F1 and F2. These logic outputs can be used to directly drive an electromechanical counter or interface to an MCU. The CF logic output gives instantaneous active power information. This output is intended to be used for calibration purposes or for interfacing to an MCU.

The ADE7755 includes a power supply monitoring circuit on the AV_{DD} supply pin. The ADE7755 remains in a reset condition until the supply voltage on AV_{DD} reaches 4 V. If the supply falls below 4 V, the ADE7755 resets and no pulse is issued on F1, F2, and CF.

Internal phase matching circuitry ensures that the voltage and current channels are phase matched whether the HPF in Channel 1 is on or off. An internal no load threshold ensures that the ADE7755 does not exhibit any creep when there is no load.

The ADE7755 is available in a 24-lead SSOP package.

FUNCTIONAL BLOCK DIAGRAM

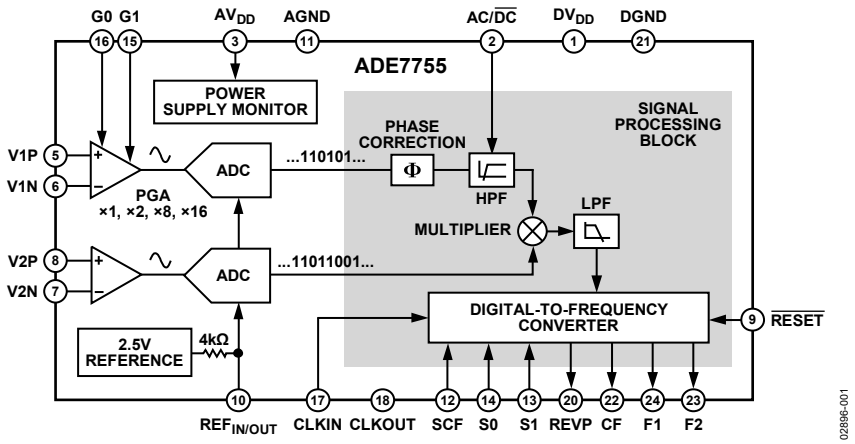

Figure 1.

[1] U.S. Patents 5,745,323; 5,760,617; 5,862,069; and 5,872,469.

Rev. B Document Feedback

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5/2002—Revision 0: Initial Version

SPECIFICATIONS

AV_{DD} = DV_{DD} = 5 V ± 5%, AGND = DGND = 0 V, on-chip reference, CLKIN = 3.58 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ACCURACY[1, 2]					
Measurement Error[1] on Channel 1					Channel 2 with full-scale signal (±660 mV), 25°C
Gain = 1		0.1		% reading	Over a dynamic range of 500 to 1
Gain = 2		0.1		% reading	Over a dynamic range of 500 to 1
Gain = 8		0.1		% reading	Over a dynamic range of 500 to 1
Gain = 16		0.1		% reading	Over a dynamic range of 500 to 1
Phase Error[1] Between Channels					Line frequency = 45 Hz to 65 Hz
V1 Phase Lead 37° (PF = 0.8 Capacitive)			±0.1	Degrees	AC/$\overline{DC}$ = 0 and AC/$\overline{DC}$ = 1
V1 Phase Lag 60° (PF = 0.5 Inductive)			±0.1	Degrees	AC/$\overline{DC}$ = 0 and AC/$\overline{DC}$ = 1
AC Power Supply Rejection[1]					AC/$\overline{DC}$ = 1, S0 = S1 = 1, G0 = G1 = 0
Output Frequency Variation (CF)		0.2		% reading	V1 = 100 mV rms, V2 = 100 mV rms @ 50 Hz, ripple on AV_{DD} of 200 mV rms @ 100 Hz
DC Power Supply Rejection[1]					AC/$\overline{DC}$ = 1, S0 = S1 = 1, G0 = G1 = 0
Output Frequency Variation (CF)		±0.3		% reading	V1 = 100 mV rms, V2 = 100 mV rms, AV_{DD} = DV_{DD} = 5 V ± 250 mV
ANALOG INPUTS					See the Analog Inputs section
Maximum Signal Levels			±1	V	V1P, V1N, V2N, and V2P to AGND
Input Impedance (DC)	390			kΩ	CLKIN = 3.58 MHz
−3 dB Bandwidth		14		kHz	CLKIN/256, CLKIN = 3.58 MHz
ADC Offset Error[1, 2]			±25	mV	Gain = 1[1, 2]
Gain Error[1]		±7		% ideal	External 2.5 V reference, gain = 1
					V1 = 470 mV dc, V2 = 660 mV dc
Gain Error Match[1]		±0.2		% ideal	External 2.5 V reference
REFERENCE INPUT					
$REF_{IN/OUT}$ Input Voltage Range			2.7	V	2.5 V + 8%
	2.3			V	2.5 V − 8%
Input Impedance	3.2			kΩ	
Input Capacitance			10	pF	
ON-CHIP REFERENCE					Nominal 2.5 V
Reference Error			±200	mV	
Temperature Coefficient		±30		ppm/°C	
CLKIN					Note all specifications for CLKIN of 3.58 MHz
Input Clock Frequency			4	MHz	
	1			MHz	
LOGIC INPUTS[3]					
SCF, S0, S1, AC/$\overline{DC}$, $\overline{RESET}$, G0, and G1					
Input High Voltage, V_{INH}	2.4			V	DV_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}			0.8	V	DV_{DD} = 5 V ± 5%
Input Current, I_{IN}			±3	μA	Typically 10 nA, V_{IN} = 0 V to DV_{DD}
Input Capacitance, C_{IN}			10	pF	
LOGIC OUTPUTS[3]					
F1 and F2					
Output High Voltage, V_{OH}	4.5			V	I_{SOURCE} = 10 mA, DV_{DD} = 5 V
Output Low Voltage, V_{OL}			0.5	V	I_{SINK} = 10 mA, DV_{DD} = 5 V
CF and REVP					
Output High Voltage, V_{OH}	4			V	I_{SOURCE} = 5 mA, DV_{DD} = 5 V
Output Low Voltage, V_{OL}			0.5	V	I_{SINK} = 5 mA, DV_{DD} = 5 V

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY					For specified performance
AV_{DD}	4.75			V	5 V – 5%
			5.25	V	5 V + 5%
DV_{DD}	4.75			V	5 V – 5%
			5.25	V	5 V + 5%
AI_{DD}			3	mA	Typically 2 mA
DI_{DD}			2.5	mA	Typically 1.5 mA

[1] See the Terminology section.
[2] See the Typical Performance Characteristics section for the plots.
[3] Sample tested during initial release and after any redesign or process change that may affect this parameter.

TIMING CHARACTERISTICS

$AV_{DD} = DV_{DD} = 5$ V ± 5%, AGND = DGND = 0 V, on-chip reference, CLKIN = 3.58 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C.

Table 2.

Parameter[1, 2]	Specification	Unit	Test Conditions/Comments
t_1[3]	275	ms	F1 and F2 pulse width (logic low)
t_2	See Table 7	sec	Output pulse period; see the Transfer Function section
t_3	1/2 t_2	sec	Time between F1 falling edge and F2 falling edge
t_4[3, 4]	90	ms	CF pulse width (logic high)
t_5	See Table 8	sec	CF pulse period; see the Transfer Function section
t_6	CLKIN/4	sec	Minimum time between F1 and F2 pulse

[1] Sample tested during initial release and after any redesign or process change that may affect this parameter.
[2] See Figure 2.
[3] The pulse widths of F1, F2, and CF are not fixed for higher output frequencies. See the Frequency Outputs section.
[4] The CF pulse is always 18 µs in the high frequency mode. See the Frequency Outputs section and Table 8.

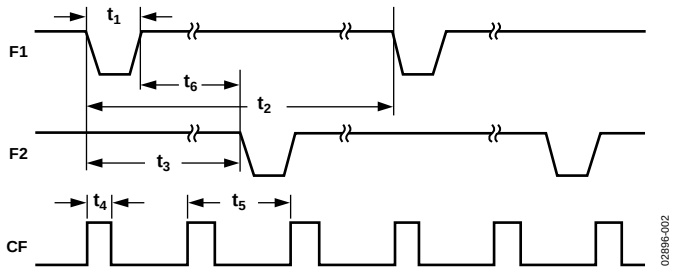


Figure 2. Timing Diagram for Frequency Outputs

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AV_{DD} to AGND	−0.3 V to +7 V
DV_{DD} to DGND	−0.3 V to +7 V
DV_{DD} to AV_{DD}	−0.3 V to +0.3 V
Analog Input Voltage to AGND	
V1P, V1N, V2P, and V2N	−6 V to +6 V
Reference Input Voltage to AGND	−0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to DGND	−0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to DGND	−0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range	
Industrial	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
24-Lead SSOP, Power Dissipation	450 mW
θ_{JA} Thermal Impedance	112°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

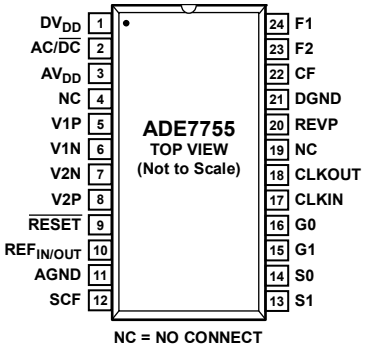


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	DV_{DD}	Digital Power Supply. This pin provides the supply voltage for the digital circuitry in the ADE7755. The supply voltage should be maintained at 5 V ± 5% for specified operation. This pin should be decoupled with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.
2	AC/$\overline{DC}$	High-Pass Filter Select. This logic input is used to enable the HPF in Channel 1 (current channel). A Logic 1 on this pin enables the HPF. The associated phase response of this filter is internally compensated over a frequency range of 45 Hz to 1 kHz. The HPF should be enabled in power metering applications.
3	AV_{DD}	Analog Power Supply. This pin provides the supply voltage for the analog circuitry in the ADE7755. The supply should be maintained at 5 V ± 5% for specified operation. Every effort should be made to minimize power supply ripple and noise at this pin by the use of proper decoupling. This pin should be decoupled to AGND with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.
4, 19	NC	No Connect.
5, 6	V1P, V1N	Analog Inputs for Channel 1 (Current Channel). These inputs are fully differential voltage inputs with a maximum differential signal level of ±470 mV for specified operation. Channel 1 also has a PGA, and the gain selections are outlined in Table 5. The maximum signal level at these pins is ±1 V with respect to AGND. Both inputs have internal ESD protection circuitry. An overvoltage of ±6 V can be sustained on these inputs without risk of permanent damage.
7, 8	V2N, V2P	Negative and Positive Inputs for Channel 2 (Voltage Channel). These inputs provide a fully differential input pair with a maximum differential input voltage of ±660 mV for specified operation. The maximum signal level at these pins is ±1 V with respect to AGND. Both inputs have internal ESD protection circuitry, and an overvoltage of ±6 V can be sustained on these inputs without risk of permanent damage.
9	$\overline{RESET}$	Reset Pin. A logic low on this pin holds the ADCs and digital circuitry in a reset condition. Bringing this pin logic low clears the ADE7755 internal registers.
10	$REF_{IN/OUT}$	This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 2.5 V ± 8% and a typical temperature coefficient of 30 ppm/°C. An external reference source may also be connected at this pin. In either case, this pin should be decoupled to AGND with a 1 µF ceramic capacitor and a 100 nF ceramic capacitor.
11	AGND	This pin provides the ground reference for the analog circuitry in the ADE7755, that is, the ADCs and reference. This pin should be tied to the analog ground plane of the PCB. The analog ground plane is the ground reference for all analog circuitry, for example, antialiasing filters and current and voltage transducers. For good noise suppression, the analog ground plane should be connected to the digital ground plane at one point only. A star ground configuration helps to keep noisy digital currents away from the analog circuits.
12	SCF	Select Calibration Frequency. This logic input is used to select the frequency on the calibration output, CF. Table 8 shows how the calibration frequencies are selected.
13, 14	S1, S0	These logic inputs are used to select one of four possible frequencies for the digital-to-frequency conversion. This offers the designer greater flexibility when designing the energy meter. See the Selecting a Frequency for an Energy Meter Application section.
15, 16	G1, G0	These logic inputs are used to select one of four possible gains for Channel 1, that is, V1. The possible gains are 1, 2, 8, and 16. See the Analog Inputs section.

Pin No.	Mnemonic	Description
17	CLKIN	An external clock can be provided at this logic input. Alternatively, a parallel resonant AT crystal can be connected across CLKIN and CLKOUT to provide a clock source for the ADE7755. The clock frequency for specified operation is 3.579545 MHz. Crystal load capacitance of between 22 pF and 33 pF (ceramic) should be used with the gate oscillator circuit.
18	CLKOUT	A crystal can be connected across this pin and CLKIN to provide a clock source for the ADE7755. The CLKOUT pin can drive one CMOS load when an external clock is supplied at CLKIN or by the gate oscillator circuit.
20	REVP	This logic output goes logic high when negative power is detected, that is, when the phase angle between the voltage and current signals is greater than 90°. This output is not latched and is reset when positive power is detected again. The output goes high or low at the same time that a pulse is issued on CF.
21	DGND	This pin provides the ground reference for digital circuitry in the ADE7755, that is, the multiplier, filters, and digital-to-frequency converter. This pin should be tied to the digital ground plane of the PCB. The digital ground plane is the ground reference for all digital circuitry, for example, counters (mechanical and digital), MCUs, and indicator LEDs. For good noise suppression, the analog ground plane should be connected to the digital ground plane at one point only, for example, a star ground.
22	CF	Calibration Frequency Logic Output. The CF logic output gives instantaneous active power information. This output is intended to be used for calibration purposes. Also, see the SCF pin description.
23, 24	F2, F1	Low Frequency Logic Outputs. F1 and F2 supply average active power information. The logic outputs can be used to directly drive electromechanical counters and 2-phase stepper motors. See the Transfer Function section.

TYPICAL PERFORMANCE CHARACTERISTICS

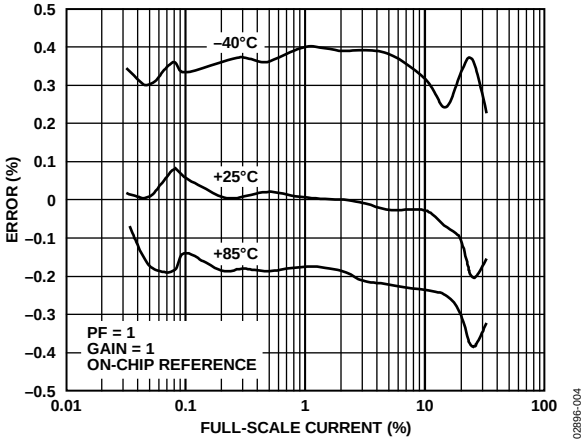


Figure 4. Error as a % of Reading (Gain = 1)

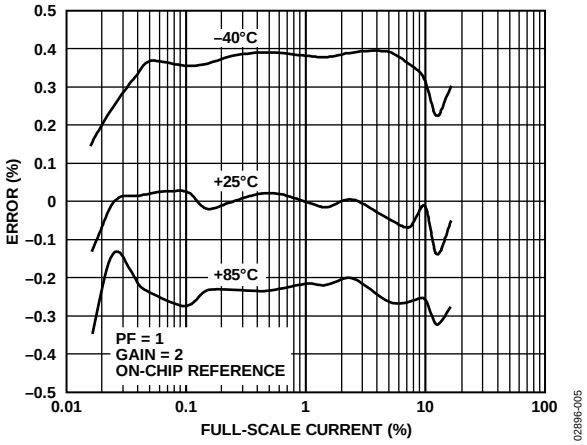


Figure 5. Error as a % of Reading (Gain = 2)

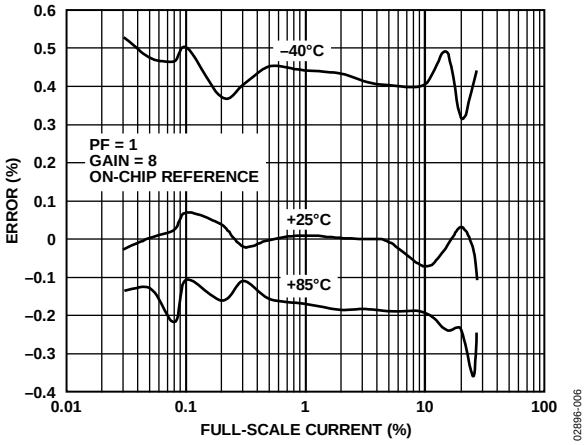


Figure 6. Error as a % of Reading (Gain = 8)

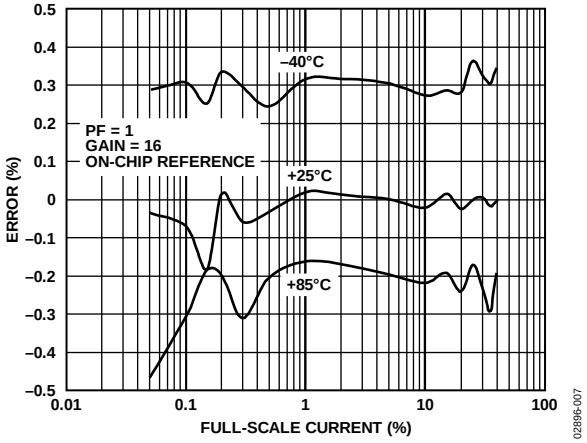


Figure 7. Error as a % of Reading (Gain = 16)

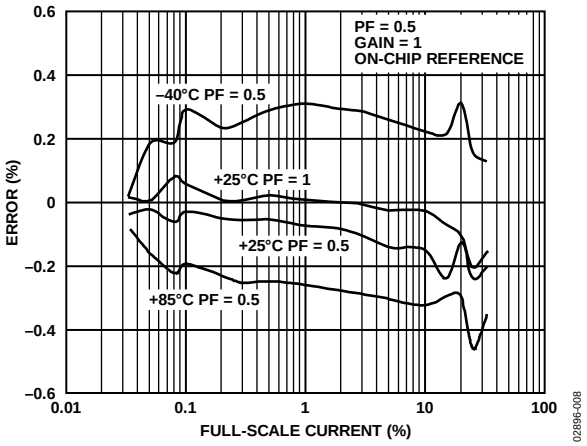


Figure 8. Error as a % of Reading (Gain = 1)

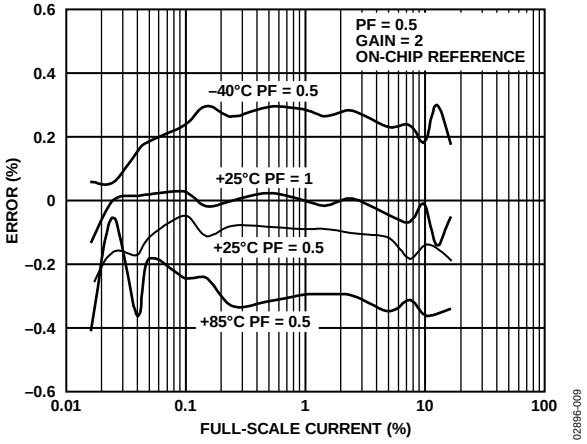


Figure 9. Error as a % of Reading (Gain = 2)

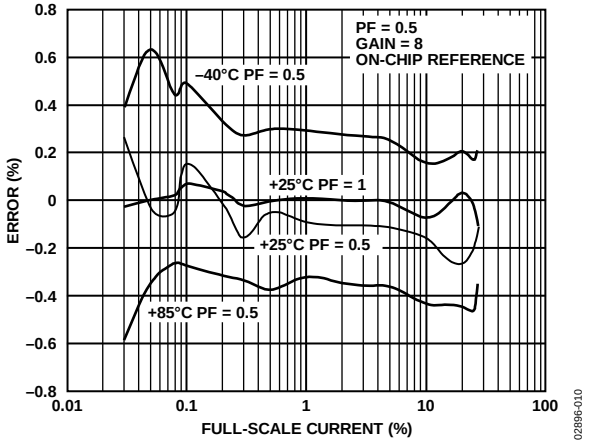


Figure 10. Error as a % of Reading (Gain = 8)

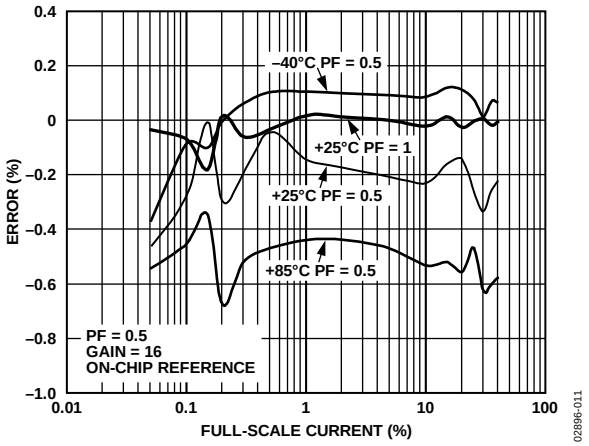


Figure 11. Error as a % of Reading (Gain = 16)

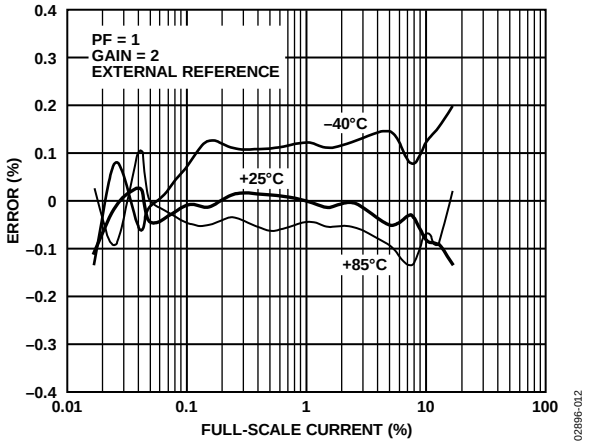


Figure 12. Error as a % of Reading over Temperature with an External Reference (Gain = 2)

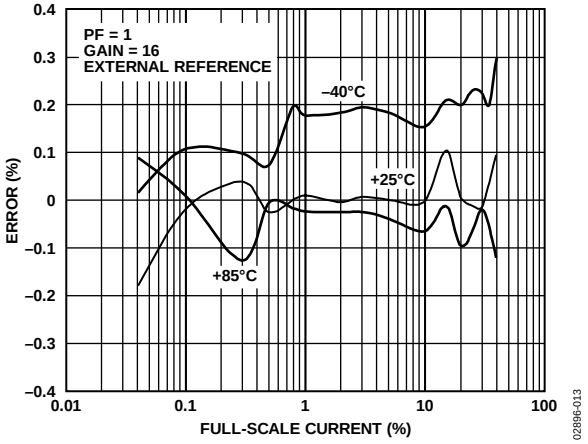


Figure 13. Error as a % of Reading over Temperature with an External Reference (Gain = 16)

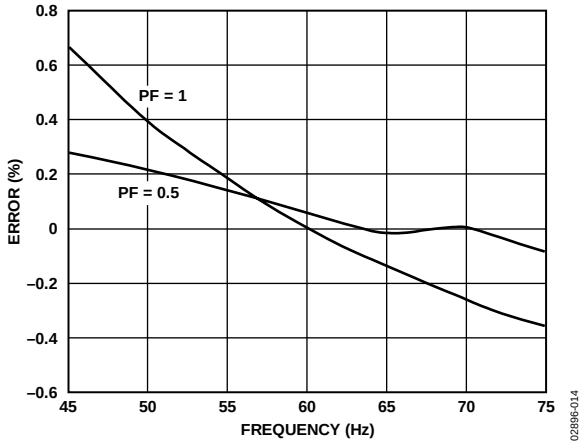


Figure 14. Error as a % of Reading over Frequency

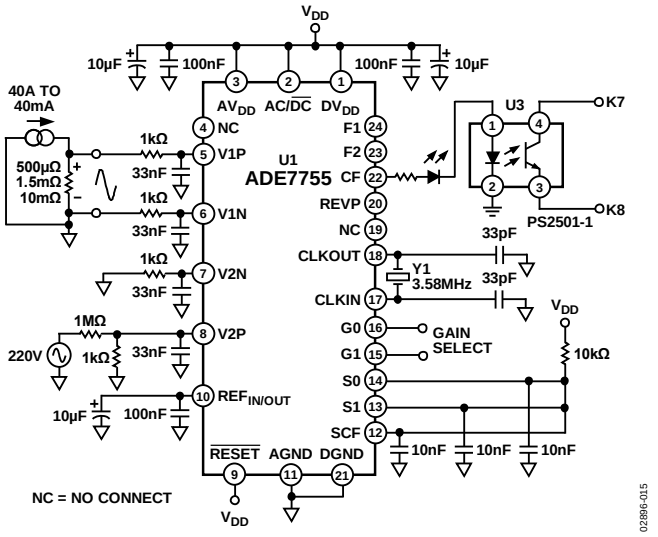


Figure 15. Test Circuit for Performance Curves

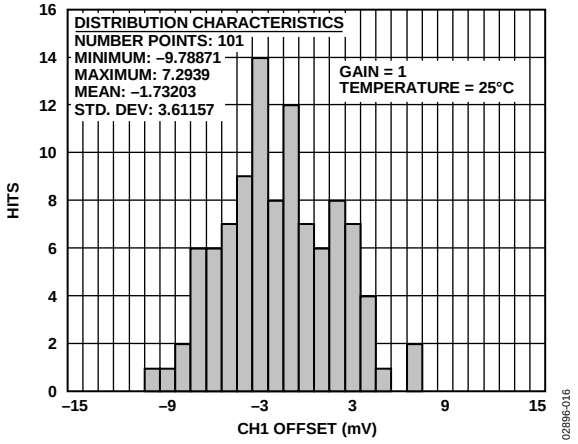


Figure 16. Channel 1 Offset Distribution (Gain = 1)

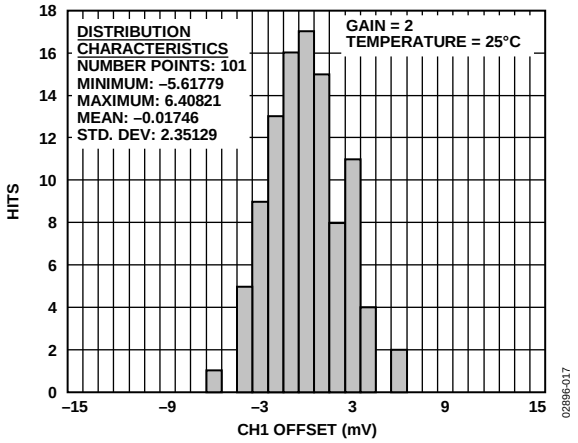


Figure 17. Channel 1 Offset Distribution (Gain = 2)

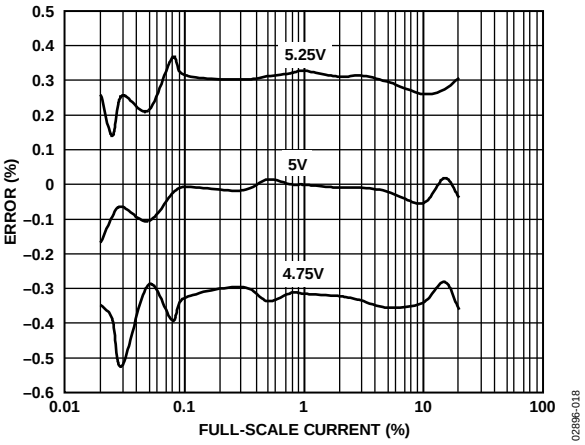


Figure 18. PSR with Internal Reference (Gain = 16)

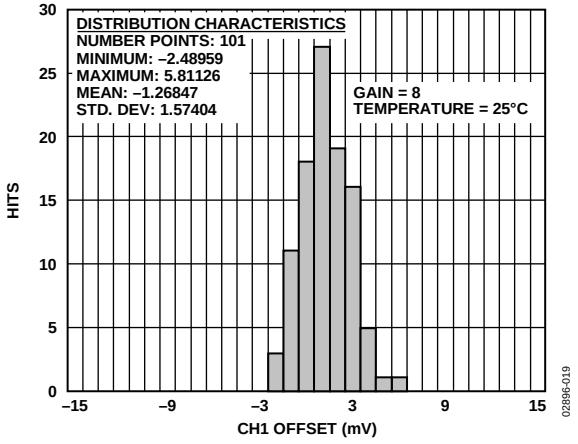


Figure 19. Channel 1 Offset Distribution (Gain = 8)

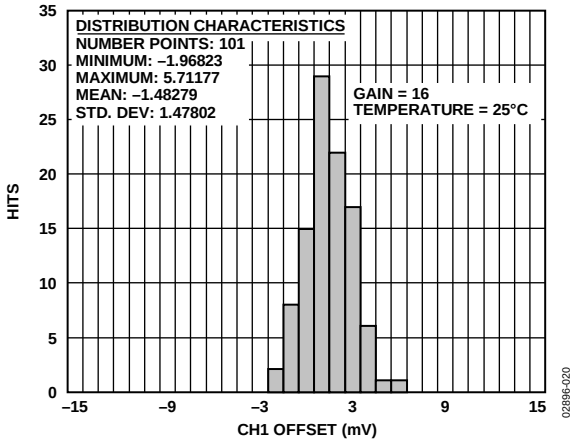


Figure 20. Channel 1 Offset Distribution (Gain = 16)

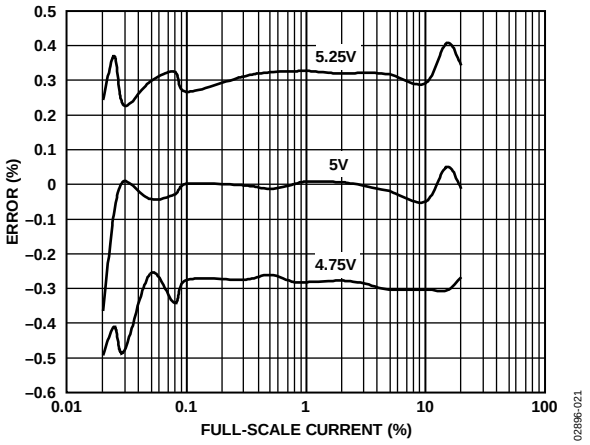


Figure 21. PSR with External Reference (Gain = 16)

TERMINOLOGY

Measurement Error
The error associated with the energy measurement made by the ADE7755 is defined by the following formula:

$$Percentage\ Error = \frac{Energy\ Registered\ by\ the\ ADE7755 - True\ Energy}{True\ Energy} \times 100\%$$

Phase Error Between Channels
The high-pass filter (HPF) in Channel 1 has a phase lead response. To offset this phase response and equalize the phase response between channels, a phase compensation network is also placed in Channel 1. The phase compensation network matches the phase to within ±0.1° over a range of 45 Hz to 65 Hz and ±0.2° over a range of 40 Hz to 1 kHz. See Figure 30 and Figure 31.

Power Supply Rejection (PSR)
The PSR quantifies the ADE7755 measurement error as a percentage of the reading when the power supplies are varied.

For the ac PSR measurement, a reading at nominal supplies (5 V) is taken. A 200 mV rms/100 Hz signal is then introduced onto the supplies and a second reading is obtained under the same input signal levels. Any error introduced is expressed as a percentage of the reading (see the Measurement Error definition).

For the dc PSR measurement, a reading at nominal supplies (5 V) is taken. The supplies are then varied ±5% and a second reading is obtained with the same input signal levels. Any error introduced is again expressed as a percentage of the reading.

ADC Offset Error
The ADC offset error refers to the dc offset associated with the analog inputs to the ADCs. It means that with the analog inputs connected to AGND, the ADCs still see a small dc signal (offset). The offset decreases with increasing gain in Channel 1. This specification is measured at a gain of 1. At a gain of 16, the dc offset is typically less than 1 mV. However, when the HPF is switched on, the offset is removed from the current channel, and the power calculation is not affected by this offset.

Gain Error
The gain error of the ADE7755 is defined as the difference between the measured output frequency (minus the offset) and the ideal output frequency. It is measured with a gain of 1 in Channel 1. The difference is expressed as a percentage of the ideal frequency. The ideal frequency is obtained from the ADE7755 transfer function (see the Transfer Function section).

Gain Error Match
The gain error match is defined as the gain error (minus the offset) obtained when switching between a gain of 1 and a gain of 2, 8, or 16. It is expressed as a percentage of the output frequency obtained under a gain of 1. This gives the gain error observed when the gain selection is changed from 1 to 2, 8, or 16.

THEORY OF OPERATION

The two ADCs of the ADE7755 digitize the voltage signals from the current and voltage transducers. These ADCs are 16-bit, second-order Σ-Δ with an oversampling rate of 900 kHz. This analog input structure greatly simplifies transducer interfacing by providing a wide dynamic range for direct connection to the transducer and also by simplifying the antialiasing filter design. A programmable gain stage in the current channel further facilitates easy transducer interfacing. A high-pass filter in the current channel removes any dc components from the current signal. This removal eliminates any inaccuracies in the active power calculation due to offsets in the voltage or current signals (see the HPF and Offset Effects section).

The active power calculation is derived from the instantaneous power signal. The instantaneous power signal is generated by a direct multiplication of the current and voltage signals. To extract the active power component (that is, the dc component), the instantaneous power signal is low-pass filtered. Figure 22 illustrates the instantaneous active power signal and shows how the active power information can be extracted by low-pass filtering the instantaneous power signal. This scheme correctly calculates active power for nonsinusoidal current and voltage waveforms at all power factors. All signal processing is carried out in the digital domain for superior stability over temperature and time.

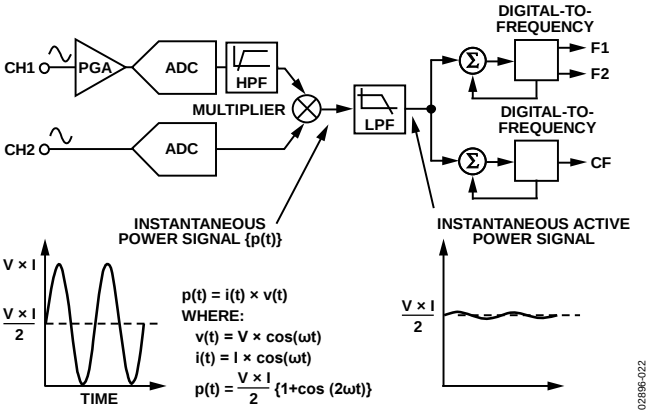


Figure 22. Signal Processing Block Diagram

The low frequency output of the ADE7755 is generated by accumulating this active power information. This low frequency inherently means a long accumulation time between output pulses. The output frequency is therefore proportional to the average active power. This average active power information can, in turn, be accumulated (for example, by a counter) to generate active energy information. Because of its high output frequency and shorter integration time, the calibration frequency (CF) output is proportional to the instantaneous active power. This is useful for system calibration purposes that take place under steady load conditions.

POWER FACTOR CONSIDERATIONS

The method used to extract the active power information from the instantaneous power signal (that is, by low-pass filtering) is valid even when the voltage and current signals are not in phase. Figure 23 displays the unity power factor condition and a displacement power factor (DPF) = 0.5, that is, current signal lagging the voltage by 60°. Assuming that the voltage and current waveforms are sinusoidal, the active power component of the instantaneous power signal (that is, the dc term) is given by

$$\left(\frac{V \times I}{2}\right) \times \cos(60°)$$

This is the correct active power calculation.

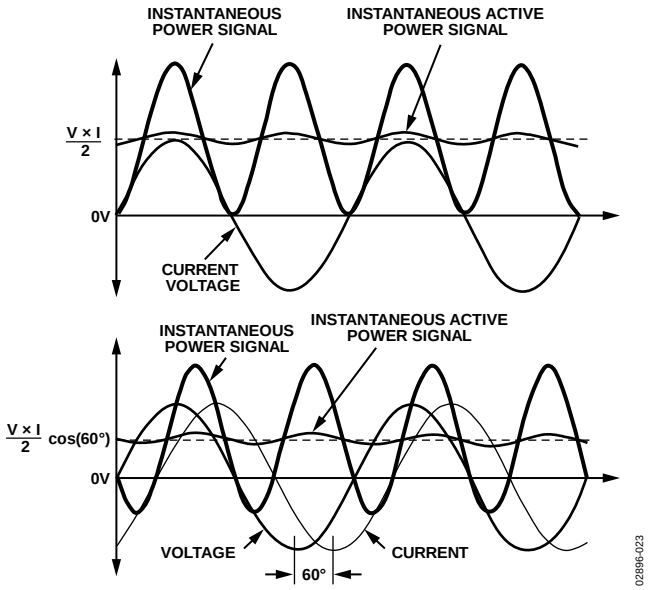


Figure 23. DC Component of Instantaneous Power Signal Conveys Active Power Information PF < 1

NONSINUSOIDAL VOLTAGE AND CURRENT

The active power calculation method also holds true for non-sinusoidal current and voltage waveforms. All voltage and current waveforms in practical applications have some harmonic content. Using the Fourier Transform operation, instantaneous voltage and current waveforms can be expressed in terms of their harmonic content.

$$v(t) = V_O + \sqrt{2} \times \sum_{h \neq 0}^{\infty} V_h \times \sin\left(h\omega t + a_h\right) \quad (1)$$

where:
$v(t)$ is the instantaneous voltage.
V_O is the average voltage value.
V_h is the rms value of the voltage harmonic, h.
a_h is the phase angle of the voltage harmonic.

$$i(t) = I_O + \sqrt{2} \times \sum_{h \neq 0}^{\infty} I_h \times \sin(h\omega t + \beta_h) \quad (2)$$

where:
$i(t)$ is the instantaneous current.
I_O is the current dc component.
I_h is the rms value of the current harmonic, h.
β_h is the phase angle of the current harmonic.

Using Equation 1 and Equation 2, the active power (P) can be expressed in terms of its fundamental active power (P1) and harmonic active power (P_H).

$$P = P_1 + P_H \quad (3)$$

where:
P_1 is the active power of the fundamental component:

$$P_1 = V_1 \times I_1 \cos\Phi_1$$
$$\Phi_1 = \alpha_1 - \beta_1$$

and

P_H is the active power of all harmonic components:

$$P_H = \sum_{h \neq 1}^{\infty} V_h \times I_h \cos\Phi_h$$

$$\Phi_h = \alpha_h - \beta_h$$

A harmonic active power component is generated for every harmonic, provided that the harmonic is present in both the voltage and current waveforms. The power factor calculation previously shown is accurate in the case of a pure sinusoid; therefore, the harmonic active power must also correctly account for the power factor because it is made up of a series of pure sinusoids.

Note that the input bandwidth of the analog inputs is 14 kHz with a master clock frequency of 3.5795 MHz.

ANALOG INPUTS

Channel 1 (Current Channel)

The voltage output from the current transducer is connected to the ADE7755 at Channel 1. Channel 1 is a fully differential voltage input. V1P is the positive input with respect to V1N.

The maximum peak differential signal on Channel 1 should be less than ±470 mV (330 mV rms for a pure sinusoidal signal) for specified operation. Note that Channel 1 has a programmable gain amplifier (PGA) with user-selectable gain of 1, 2, 8, or 16 (see Table 5). These gains facilitate easy transducer interfacing.

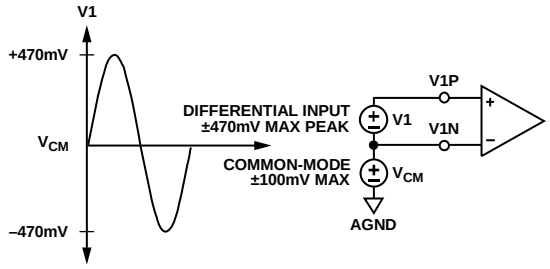


Figure 24. Maximum Signal Levels, Channel 1, Gain = 1

Figure 24 illustrates the maximum signal levels on V1P and V1N. The maximum differential voltage is ±470 mV divided by the gain selection. The differential voltage signal on the inputs must be referenced to a common mode, for example, AGND. The maximum common-mode signal is ±100 mV, as shown in Figure 24.

Table 5. Gain Selection for Channel 1

G1	G0	Gain	Maximum Differential Signal (mV)
0	0	1	±470
0	1	2	±235
1	0	8	±60
1	1	16	±30

Channel 2 (Voltage Channel)

The output of the line voltage transducer is connected to the ADE7755 at this analog input. Channel 2 is a fully differential voltage input. The maximum peak differential signal on Channel 2 is ±660 mV. Figure 25 illustrates the maximum signal levels that can be connected to Channel 2 of the ADE7755.

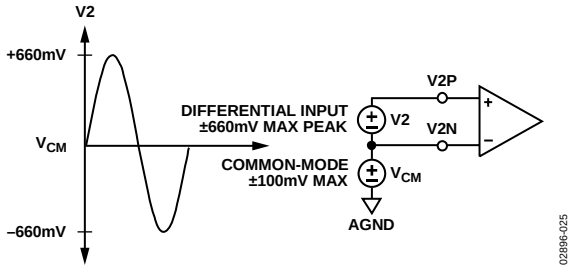


Figure 25. Maximum Signal Levels, Channel 2

Channel 2 must be driven from a common-mode voltage, that is, the differential voltage signal on the input must be referenced to a common mode (usually AGND). The analog inputs of the ADE7755 can be driven with common-mode voltages of up to 100 mV with respect to AGND. However, best results are achieved using a common mode equal to AGND.

TYPICAL CONNECTION DIAGRAMS

Figure 26 shows a typical connection diagram for Channel 1. A current transformer (CT) is the current transducer selected for this example. Note that the common-mode voltage for Channel 1 is AGND and is derived by center-tapping the burden resistor to AGND. This provides the complementary analog input signals for V1P and V1N. The CT turns ratio and burden resistor Rb are selected to give a peak differential voltage of ±470 mV/gain at maximum load.

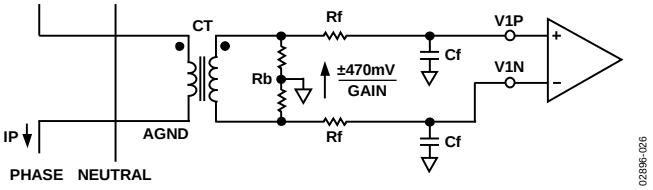


Figure 26. Typical Connection for Channel 1

Figure 27 shows two typical connections for Channel 2. The first option uses a potential transformer (PT) to provide complete isolation from the power line. In the second option, the ADE7755 is biased around the neutral wire, and a resistor divider provides a voltage signal that is proportional to the line voltage. Adjusting the ratio of Ra, Rb, and VR is also a convenient way of carrying out a gain calibration on the meter.

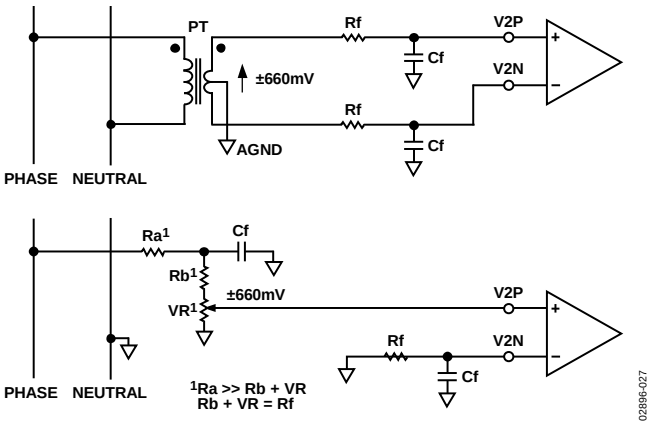


Figure 27. Typical Connections for Channel 2

POWER SUPPLY MONITOR

The ADE7755 contains an on-chip power supply monitor. The analog supply (AV_{DD}) is continuously monitored by the ADE7755. If the supply is less than 4 V ± 5%, the ADE7755 resets. This is useful to ensure correct device startup at power-up and power-down. The power supply monitor has built-in hysteresis and filtering. These features give a high degree of immunity to false triggering due to noisy supplies.

In Figure 28, the trigger level is nominally set at 4 V. The tolerance on this trigger level is about ±5%. The power supply and decoupling for the part should be such that the ripple at AV_{DD} does not exceed 5 V ± 5%, as specified for normal operation.

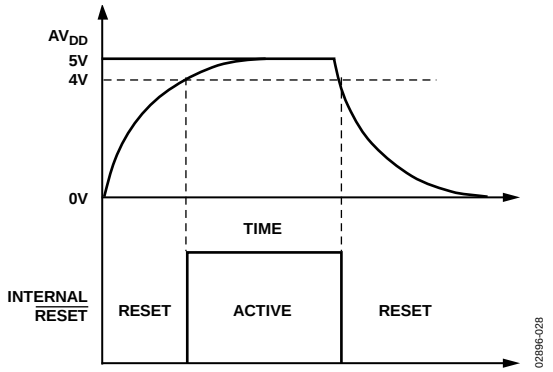


Figure 28. On-Chip Power Supply Monitor

HPF and Offset Effects

Figure 29 shows the effect of offsets on the active power calculation. An offset on Channel 1 and Channel 2 contributes a dc component after multiplication. Because the dc component is extracted by the LPF, it accumulates as active power. If not properly filtered, dc offsets introduce error to the energy accumulation. This problem is easily avoided by enabling the HPF (that is, the AC/$\overline{\text{DC}}$ pin is set to logic high) in Channel 1. By removing the offset from at least one channel, no error component can be generated at dc by the multiplication. Error terms at cos(ωt) are removed by the LPF and the digital-to-frequency conversion (see the Digital-to-Frequency Conversion section).

$$\{V\cos(\omega t) + V_{OS}\} \times \{I\cos(\omega t) + I_{OS}\} =$$

$$\frac{V \times I}{2} + V_{OS} \times I_{OS} + V_{OS} \times I\cos(\omega t) + I_{OS} \times V\cos(\omega t) +$$

$$\frac{V \times I}{2} \times \cos(2\omega t)$$

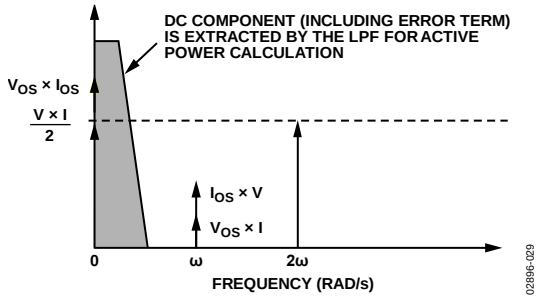


Figure 29. Effect of Channel Offset on the Active Power Calculation

The HPF in Channel 1 has an associated phase response that is compensated for on chip. The phase compensation is activated when the HPF is enabled and is disabled when the HPF is not activated. Figure 30 and Figure 31 show the phase error between channels with the compensation network activated. The ADE7755 is phase compensated up to 1 kHz, as shown. This ensures correct active harmonic power calculation even at low power factors.

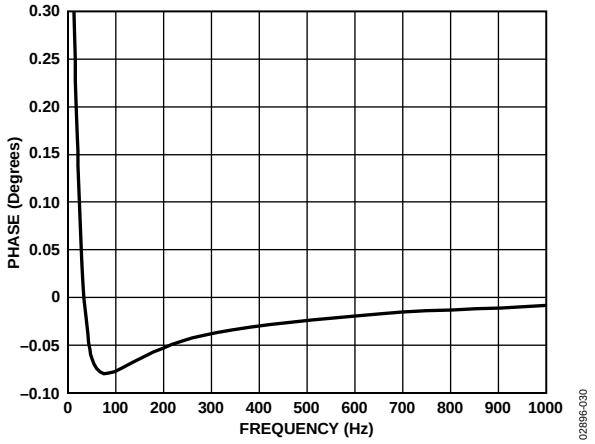


Figure 30. Phase Error Between Channels (0 Hz to 1 kHz)

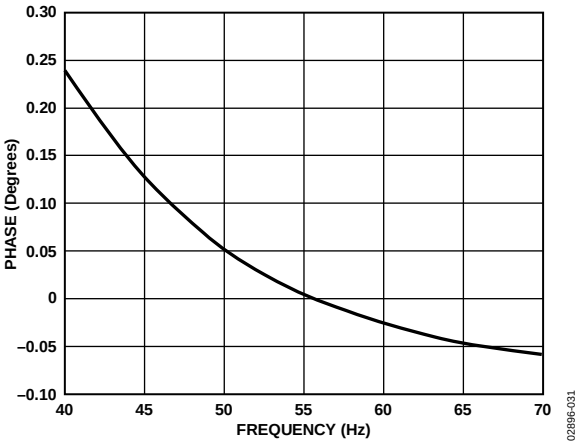


Figure 31. Phase Error Between Channels (40 Hz to 70 Hz)

DIGITAL-TO-FREQUENCY CONVERSION

The digital output of the low-pass filter after multiplication contains the active power information. However, because this LPF is not an ideal brick-wall filter implementation, the output signal also contains attenuated components at the line frequency and its harmonics, that is, cos(hωt) where h = 1, 2, 3, and so on.

The magnitude response of the filter is given by

$$|H(f)| = \frac{1}{1 + (f/8.9\,\text{Hz})} \quad (4)$$

For a line frequency of 50 Hz, the filter gives an attenuation of the 2ω (100 Hz) component of approximately −22 dB. The dominating harmonic is at twice the line frequency, that is, cos(2 ωt), which is due to the instantaneous power signal.

Figure 32 shows the instantaneous active power signal at the output of the LPF, which still contains a significant amount of instantaneous power information, that is, cos(2 ωt). This signal is then passed to the digital-to-frequency converter where it is integrated (accumulated) over time to produce an output frequency. This accumulation of the signal suppresses or averages out any non-dc components in the instantaneous active power signal. The average value of a sinusoidal signal is 0. Therefore, the frequency generated by the ADE7755 is proportional to the average active power. Figure 32 shows the digital-to-frequency conversion for steady load conditions, that is, constant voltage and current.

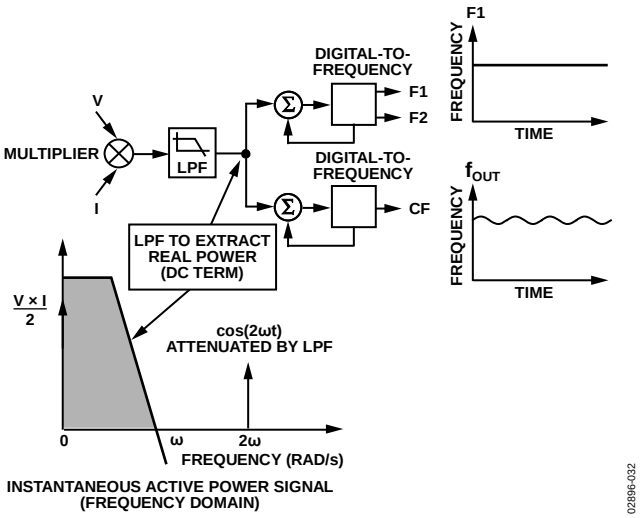


Figure 32. Active Power-to-Frequency Conversion

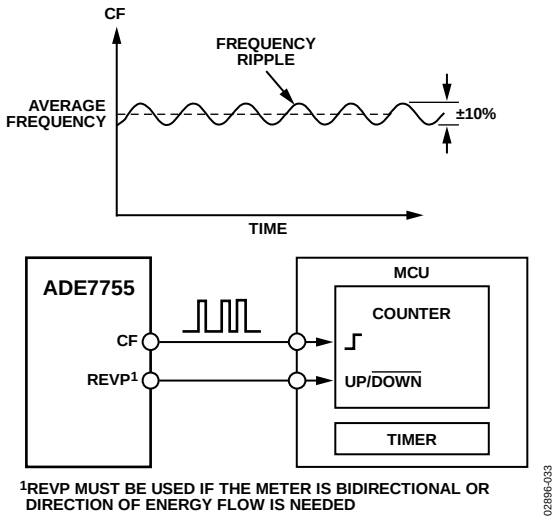


Figure 33. Interfacing the ADE7755 to an MCU

As can be seen in Figure 32, the frequency output CF varies over time, even under steady load conditions. This frequency variation is primarily due to the cos(2 ωt) component in the instantaneous active power signal. The output frequency on CF can be up to 2048 times higher than the frequency on F1 and F2. This higher output frequency is generated by accumulating the instantaneous active power signal over a much shorter time while converting it to a frequency. This shorter accumulation period means less averaging of the cos(2 ωt) component. Consequently, some of this instantaneous power signal passes through the digital-to-frequency conversion, which is not a problem in the application. When CF is used for calibration purposes, the frequency should be averaged by the frequency counter. This averaging operation removes any ripple. If CF is measuring energy, for example, in a microprocessor-based application, the CF output should also be averaged to calculate power. Because the outputs, F1 and F2, operate at a much lower frequency, more averaging of the instantaneous active power signal is carried out. The result is a greatly attenuated sinusoidal content and a virtually ripple-free frequency output.

INTERFACING THE ADE7755 TO A MICROCONTROLLER FOR ENERGY MEASUREMENT

The easiest way to interface the ADE7755 to a microcontroller is to use the CF high frequency output with the output frequency scaling set to 2048 × F1, F2. This is done by setting SCF = 0 and S0 = S1 = 1 (see Table 8). With full-scale ac signals on the analog inputs, the output frequency on CF is approximately 5.5 kHz. Figure 33 illustrates one scheme that can be used to digitize the output frequency and carry out the necessary averaging described in the Digital-to-Frequency Conversion section.

As shown in Figure 33, the frequency output CF is connected to an MCU counter or port, which counts the number of pulses in a given integration time that is determined by an MCU internal timer. The average power proportional to the average frequency is given by

$$Average\ Frequency = Average\ Active\ Power = \frac{Counter}{Timer}$$

The energy consumed during an integration period is given by

$$Energy = Average\ \ Power \times Time = \frac{Counter}{Time} \times Time = Counter$$

For the purpose of calibration, this integration time can be 10 seconds to 20 seconds to accumulate enough pulses to ensure correct averaging of the frequency. In normal operation, the integration time can be reduced to 1 second or 2 seconds depending, for example, on the required update rate of a display. With shorter integration times on the MCU, the amount of energy in each update may still have some small amount of ripple, even under steady load conditions. However, over a minute or more, the measured energy has no ripple.

POWER MEASUREMENT CONSIDERATIONS

Calculating and displaying power information always has some associated ripple that depends on the integration period used in the MCU to determine average power and also the load. For example, at light loads, the output frequency can be 10 Hz. With an integration period of 2 seconds, only about 20 pulses are counted. The possibility of missing one pulse always exists because the ADE7755 output frequency is running asynchronously to the MCU timer. This possibility results in a 1-in-20 (or 5%) error in the power measurement.

TRANSFER FUNCTION

Frequency Outputs F1 and F2

The ADE7755 calculates the product of two voltage signals (on Channel 1 and Channel 2) and then low-pass filters this product to extract active power information. This active power information is then converted to a frequency. The frequency information is output on F1 and F2 in the form of active low pulses. The pulse rate at these outputs is relatively low, for example, 0.34 Hz maximum for ac signals with S0 = S1 = 0 (see Table 7). This means that the frequency at these outputs is generated from active power information accumulated over a relatively long time. The result is an output frequency that is proportional to the average active power. The averaging of the active power signal is implicit to the digital-to-frequency conversion. The output frequency or pulse rate is related to the input voltage signals by the following equation:

$$Freq = \frac{8.06 \times V1 \times V2 \times Gain \times f_i}{V_{REF}{}^2}$$

where:
Freq = output frequency on F1 and F2 (Hz).
V1 = differential rms voltage signal on Channel 1 (volts).
V2 = differential rms voltage signal on Channel 2 (volts).
Gain = 1, 2, 8, or 16, depending on the PGA gain selection made using logic inputs G0 and G1.
V_{REF} = the reference voltage (2.5 V ± 8%) (volts).
f_i = one of the four possible frequencies (f_1, f_2, f_3, or f_4) selected by using the logic inputs S0 and S1, see Table 6.

Table 6. f_1, f_2, f_3, and f_4 Frequency Selection

S1	S0	f_1, f_2, f_3, and f_4 (Hz)	XTAL/CLKIN[1]
0	0	f_1 = 1.7	3.579 MHz/2^{21}
0	1	f_2 = 3.4	3.579 MHz/2^{20}
1	0	f_3 = 6.8	3.579 MHz/2^{19}
1	1	f_4 = 13.6	3.579 MHz/2^{18}

[1] f_1, f_2, f_3, or f_4 is a binary fraction of the master clock and, therefore, varies if the specified CLKIN frequency is altered.

Example 1

If full-scale differential dc voltages of +470 mV and −660 mV are applied to V1 and V2, respectively (470 mV is the maximum differential voltage that can be connected to Channel 1, and 660 mV is the maximum differential voltage that can be connected to Channel 2), the expected output frequency is calculated as follows:

$$Freq = \frac{8.06 \times V1 \times V2 \times Gain \times f_i}{V_{REF}{}^2}$$

where:
Gain = 1, G0 = G1 = 0.
f_i = f_1 = 1.7 Hz, S0 = S1 = 0.
V1 = +470 mV dc = 0.47 V (rms of dc = dc).
V2 = −660 mV dc = 0.66 V (rms of dc = |dc|).
V_{REF} = 2.5 V (nominal reference value).

If the on-chip reference is used, actual output frequencies may vary from device to device due to a reference tolerance of ±8%.

Example 2

In this example, with ac voltages of ±470 mV peak applied to V1 and ±660 mV peak applied to V2, the expected output frequency is calculated as follows:

$$Freq = \frac{8.06 \times 0.47 \times 0.66 \times 1 \times 1.7}{\sqrt{2} \times \sqrt{2} \times 2.5^2} = 0.34$$

where:
Gain = 1, G0 = G1 = 0.
f_i = f_1 = 1.7 Hz, S0 = S1 = 0.
V1 = rms of 470 mV peak ac = 0.47/√2 V.
V2 = rms of 660 mV peak ac = 0.66/√2 V.
V_{REF} = 2.5 V (nominal reference value).

If the on-chip reference is used, actual output frequencies may vary from device to device due to a reference tolerance of ±8%.

As can be seen from these two example calculations, the maximum output frequency for ac inputs is always half that for dc input signals. Table 7 shows a complete listing of all the maximum output frequencies.

Table 7. Maximum Output Frequency on F1 and F2

S1	S0	Maximum Frequency for DC Inputs (Hz)	Maximum Frequency for AC Inputs (Hz)
0	0	0.68	0.34
0	1	1.36	0.68
1	0	2.72	1.36
1	1	5.44	2.72

Frequency Output CF

The pulse output CF is intended for use during calibration. The output pulse rate on CF can be up to 2048 times the pulse rate on F1 and F2. The lower the f_i frequency selected (i = 1, 2, 3, or 4), the higher the CF scaling (except for the high frequency mode SCF = 0, S1 = S0 = 1). Table 8 shows how the two frequencies are related, depending on the state of the logic inputs, S0, S1, and SCF. Because of its relatively high pulse rate, the frequency at CF is proportional to the instantaneous active power. As is the case with F1 and F2, the frequency is derived from the output of the low-pass filter after multiplication. However, because the output frequency is high, this active power information is accumulated over a much shorter time. Therefore, less averaging is carried out in the digital-to-frequency conversion. With much less averaging of the active power signal, the CF output is much more responsive to power fluctuations (see the signal processing block diagram in Figure 22).

Table 8. Maximum Output Frequency on CF

SCF	S1	S0	f_1, f_2, f_3, and f_4 (Hz)	CF Maximum for AC Signals
1	0	0	f_1 = 1.7	128 × F1, F2 = 43.52 Hz
0	0	0	f_1 = 1.7	64 × F1, F2 = 21.76 Hz
1	0	1	f_2 = 3.4	64 × F1, F2 = 43.52 Hz
0	0	1	f_2 = 3.4	32 × F1, F2 = 21.76 Hz
1	1	0	f_3 = 6.8	32 × F1, F2 = 43.52 Hz
0	1	0	f_3 = 6.8	16 × F1, F2 = 21.76 Hz
1	1	1	f_4 = 13.6	16 × F1, F2 = 43.52 Hz
0	1	1	f_4 = 13.6	2048 × F1, F2 = 5.57 kHz

SELECTING A FREQUENCY FOR AN ENERGY METER APPLICATION

As shown in Table 6, the user can select one of four frequencies. This frequency selection determines the maximum frequency on F1 and F2. These outputs are intended to be used to drive the energy register (electromechanical or other). Because only four different output frequencies can be selected, the available frequency selection has been optimized for a meter constant of 100 imp/kWh with a maximum current between 10 A and 120 A. Table 9 shows the output frequency for several maximum currents (I_{MAX}) with a line voltage of 220 V. In all cases, the meter constant is 100 imp/kWh.

Table 9. F1 and F2 Frequency at 100 imp/kWh

I_{MAX} (A)	F1 and F2 (Hz)
12.5	0.076
25	0.153
40	0.244
60	0.367
80	0.489
120	0.733

The f_i frequencies (i = 1, 2, 3, or 4) allow complete coverage of this range of output frequencies on F1 and F2. When designing an energy meter, the nominal design voltage on Channel 2 (voltage) should be set to half scale to allow for calibration of the meter constant. The current channel should also be no more than half scale when the meter sees maximum load. This allows overcurrent signals and signals with high crest factors to be accommodated. Table 10 shows the output frequency on F1 and F2 when both analog inputs are half scale. The frequencies listed in Table 10 align well with those listed in Table 9 for maximum load.

Table 10. F1 and F2 Frequency with Half-Scale AC Inputs

S1	S0	f_1, f_2, f_3, and f_4 (Hz)	F1 and F2 Frequency on CH1 and CH2 Half-Scale AC Inputs (Hz)
0	0	f_1 = 1.7	0.085
0	1	f_2 = 3.4	0.17
1	0	f_3 = 6.8	0.34
1	1	f_4 = 13.6	0.68

When selecting a suitable f_i frequency (i = 1, 2, 3, or 4) for a meter design, the frequency output at I_{MAX} (maximum load) with a meter constant of 100 imp/kWh should be compared with Column 4 of Table 10. The frequency that is closest in Table 10 determines the best choice of f_i frequency (i = 1, 2, 3, or 4). For example, if a meter with a maximum current of 25 A is being designed, the output frequency on F1 and F2 with a meter constant of 100 imp/kWh is 0.153 Hz at 25 A and 220 V (from Table 9). Table 10, the closest frequency to 0.153 Hz in Column 4, is 0.17 Hz. Therefore, f_2 (3.4 Hz, see Table 6) is selected for this design.

FREQUENCY OUTPUTS

Figure 2 shows a timing diagram for the various frequency outputs. The F1 and F2 outputs are the low frequency outputs that can be used to directly drive a stepper motor or electromechanical impulse counter. The F1 and F2 outputs provide two alternating low going pulses. The pulse width (t_1) is set at 275 ms, and the time between the falling edges of F1 and F2 (t_3) is approximately half the period of F1 (t_2). If, however, the period of F1 and F2 falls below 550 ms (1.81 Hz), the pulse width of F1 and F2 is set to half of their period. The maximum output frequencies for F1 and F2 are shown in Table 7.

The high frequency CF output is intended to be used for communications and calibration purposes. CF produces a 90 ms wide active high pulse (t_4) at a frequency proportional to active power. The CF output frequencies are listed in Table 8. As in the case of F1 and F2, if the period of CF (t_5) falls below 180 ms, the CF pulse width is set to half the period. For example, if the CF frequency is 20 Hz, the CF pulse width is 25 ms.

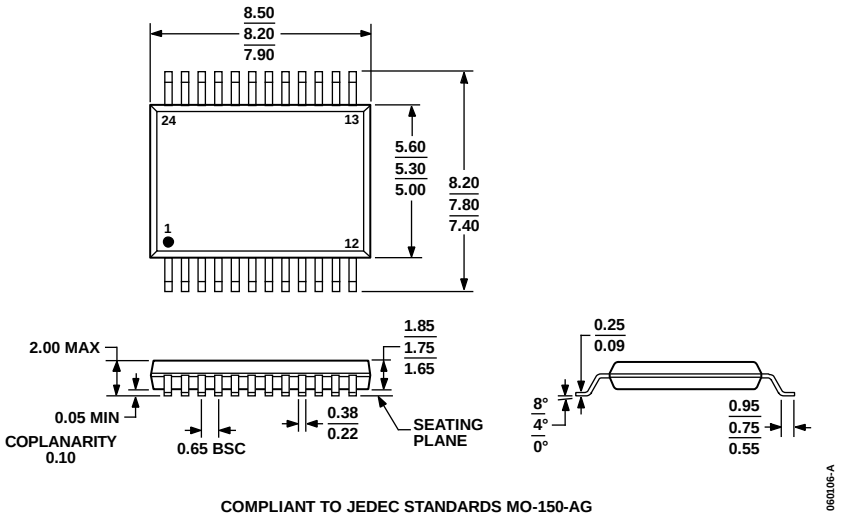
When the high frequency mode is selected (that is, SCF = 0, S1 = S0 = 1), the CF pulse width is fixed at 18 µs. Therefore, t_4 is always 18 µs, regardless of the output frequency on CF.

NO LOAD THRESHOLD

The ADE7755 also includes a no load threshold and start-up current feature that eliminates any creep effects in the meter. The ADE7755 is designed to issue a minimum output frequency in all modes except when SCF = 0 and S1 = S0 = 1. The no load detection threshold is disabled in this output mode to accommodate specialized application of the ADE7755. Any load generating a frequency lower than this minimum frequency will not cause a pulse to be issued on F1, F2, or CF. The minimum output frequency is given as 0.0014% of the full-scale output frequency for each of the f_i frequencies (i = 1, 2, 3, or 4), see Table 6.

For example, in an energy meter with a meter constant of 100 imp/kWh on F1 and F2 using f_2 (3.4 Hz), the maximum output frequency at F1 or F2 is 0.0014% of 3.4 Hz or 4.76×10^{-5} Hz. This is 3.05×10^{-3} Hz at CF (64 × F1 Hz). In this example, the no load threshold is equivalent to 1.7 W of the load or a start-up current of 8 mA at 220 V. IEC 1036 states that the meter must start up with a load current equal to or less than 0.4% Ib. For a 5 A (Ib) meter, 0.4% Ib is equivalent to 20 mA. The start-up current of this design therefore satisfies the IEC requirement. As illustrated in this example, the choice of f_i frequency (i = 1, 2, 3, or 4) and the ratio of the stepper motor display determine the start-up current.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-150-AG

Figure 34. 24-Lead Shrink Small Outline Package [SSOP]
(RS-24)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADE7755ARSZ	−40°C to +85°C	24-Lead Shrink Small Outline Package [SSOP]	RS-24
ADE7755ARSZRL	−40°C to +85°C	24-Lead Shrink Small Outline Package [SSOP], 13″ Tape and Reel	RS-24

[1] Z = RoHS Compliant Part.

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