



PSMN059-150Y

N-channel TrenchMOS SiliconMAX standard level FET

3 October 2013

Product data sheet

1. General description

SiliconMAX standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

2. Features and benefits

- Higher operating power due to low thermal resistance
- Suitable for high frequency applications due to fast switching characteristics

3. Applications

- Class D amplifier
- DC-to-DC converters
- Motion control
- Switched-mode power supplies

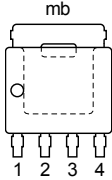
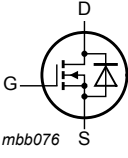
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$	-	-	150	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; Fig. 1 ; Fig. 3	-	-	43	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 2	-	-	113	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 12\text{ A}$; $T_j = 25\text{ °C}$; Fig. 9 ; Fig. 10	-	46	59	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 10\text{ V}$; $I_D = 12\text{ A}$; $V_{DS} = 75\text{ V}$; Fig. 11 ; Fig. 12	-	9.1	-	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LFPAK56; Power-SO8 (SOT669)	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN059-150Y	LFPAK56; Power-SO8	Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN059-150Y	059150

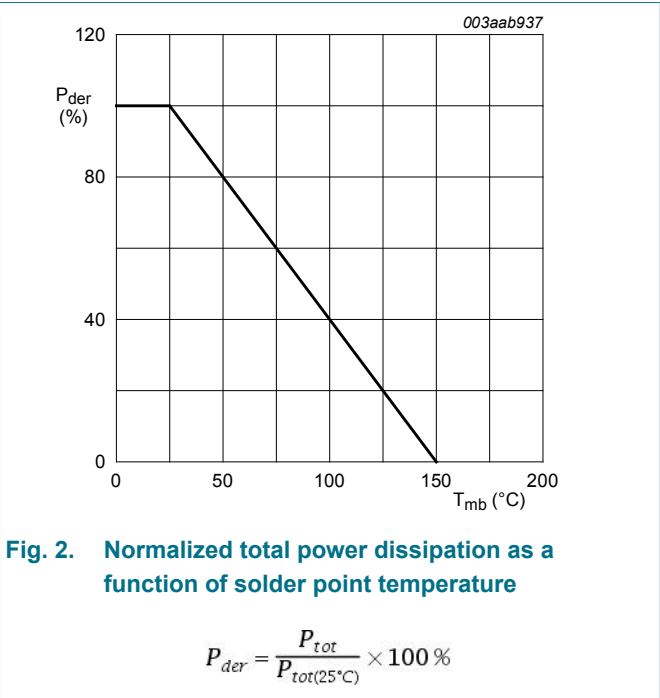
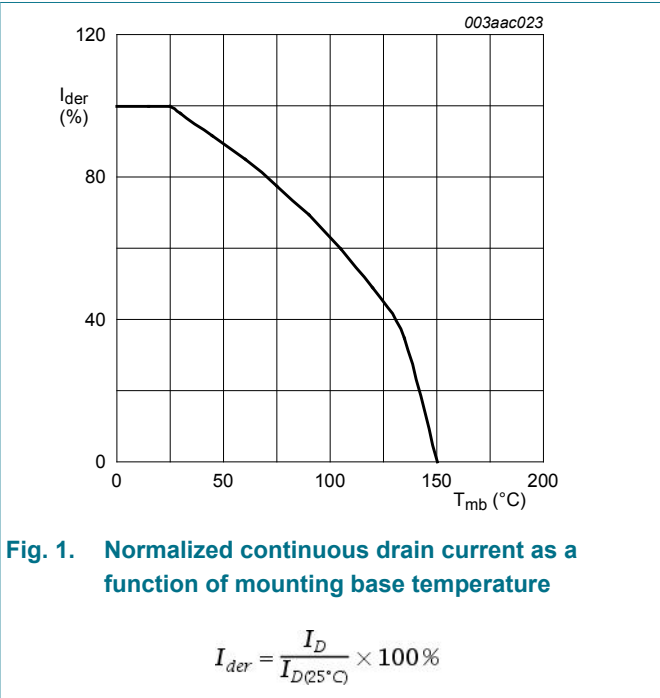
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ }^{\circ}\text{C}$; $T_j \leq 150\text{ }^{\circ}\text{C}$	-	150	V
V_{DGR}	drain-gate voltage	$T_j \geq 25\text{ }^{\circ}\text{C}$; $T_j \leq 150\text{ }^{\circ}\text{C}$; $R_{GS} = 20\text{ }\Omega$	-	150	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ }^{\circ}\text{C}$; Fig. 1 ; Fig. 3	-	43	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ }^{\circ}\text{C}$; Fig. 1	-	27.7	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ }^{\circ}\text{C}$; Fig. 3	-	129	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ }^{\circ}\text{C}$; Fig. 2	-	113	W
T_{stg}	storage temperature		-55	150	$^{\circ}\text{C}$

Symbol	Parameter	Conditions		Min	Max	Unit
T _j	junction temperature			-55	150	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C		-	52	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	208	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(init)} = 25 °C; I _D = 12.1 A; V _{sup} ≤ 150 V; unclamped; t _p = 0.21 ms; R _{GS} = 50 Ω		-	255	mJ



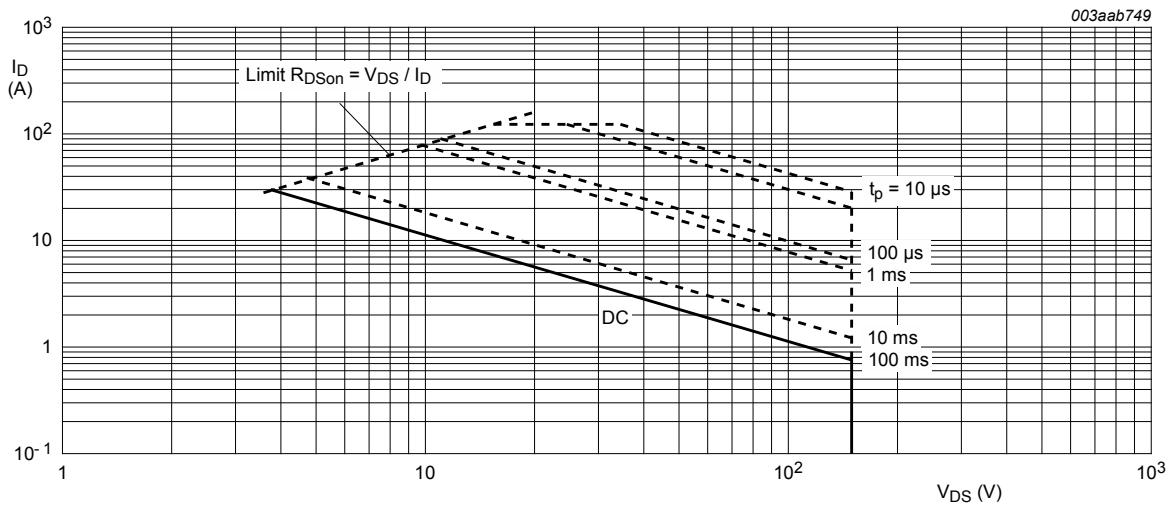


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^\circ C; I_{DM}$ is single pulse

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	mounted on a printed-circuit board; vertical in still air; Fig. 4	-	-	1.1	K/W

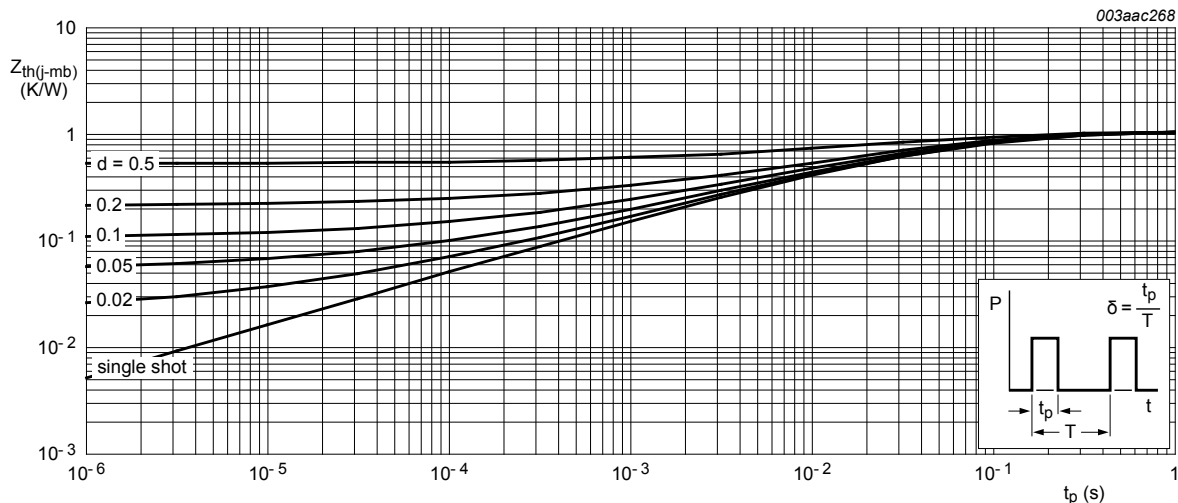


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C		150	-	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _j = -55 °C		133	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C; Fig. 7 ; Fig. 8		2	3	4	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 150 °C; Fig. 7 ; Fig. 8		1	-	-	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = -55 °C; Fig. 7 ; Fig. 8		-	-	4.4	V
I _{DSS}	drain leakage current	V _{DS} = 120 V; V _{GS} = 0 V; T _j = 25 °C		-	-	1	μA
		V _{DS} = 120 V; V _{GS} = 0 V; T _j = 150 °C		-	-	100	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C		-	-	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C		-	-	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 12 A; T _j = 25 °C; Fig. 9 ; Fig. 10		-	46	59	mΩ
		V _{GS} = 10 V; I _D = 12 A; T _j = 150 °C; Fig. 9 ; Fig. 10		-	101	135	mΩ
R _G	gate resistance	f = 1 MHz		-	1.1	-	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	I _D = 12 A; V _{DS} = 75 V; V _{GS} = 10 V; Fig. 11 ; Fig. 12		-	27.9	-	nC
Q _{GS}	gate-source charge			-	6.3	-	nC
Q _{GD}	gate-drain charge			-	9.1	-	nC
V _{GS(pl)}	gate-source plateau voltage	I _D = 12 A; V _{DS} = 75 V; Fig. 11 ; Fig. 12		-	4.8	-	V
C _{iss}	input capacitance	V _{DS} = 30 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; Fig. 13		-	1529	-	pF
C _{oss}	output capacitance			-	208	-	pF
C _{rss}	reverse transfer capacitance			-	66	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 75 V; R _L = 3 Ω; V _{GS} = 10 V; R _{G(ext)} = 5.6 Ω		-	14.2	-	ns
t _r	rise time			-	42	-	ns
t _{d(off)}	turn-off delay time			-	54.2	-	ns
t _f	fall time			-	11.1	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 12 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 14		-	0.9	1.2	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{rr}	reverse recovery time	$I_S = 12\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 30\text{ V}$	-	67	-	ns
Q_r	recovered charge	$I_S = 12\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$	-	226	-	nC

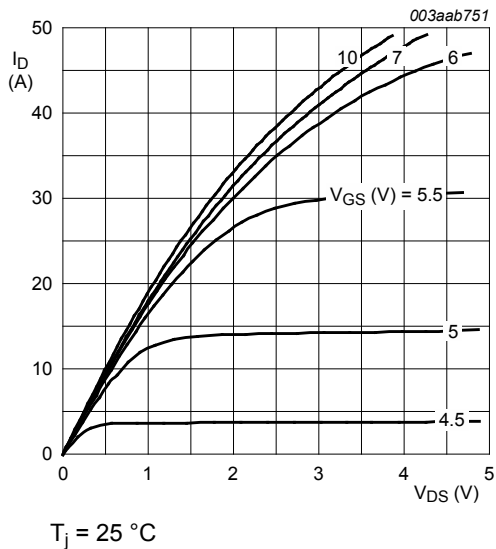


Fig. 5. Output characteristics: drain current as a function of drain-source voltage; typical values

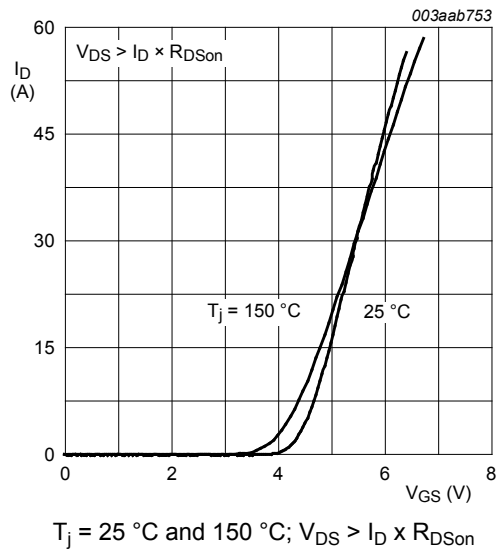


Fig. 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

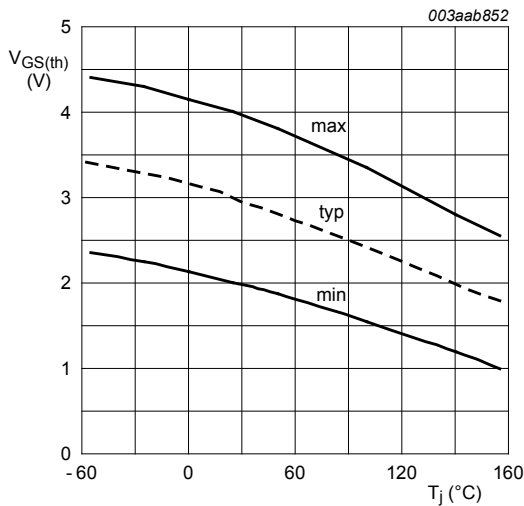


Fig. 7. Gate-source threshold voltage as a function of junction temperature

$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

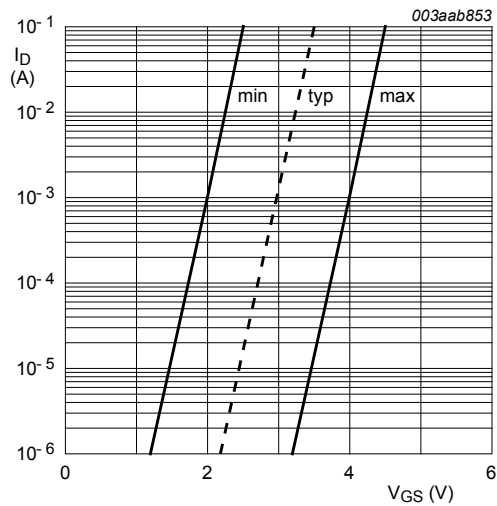


Fig. 8. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25\text{ °C}; V_{DS} = 5\text{ V}$

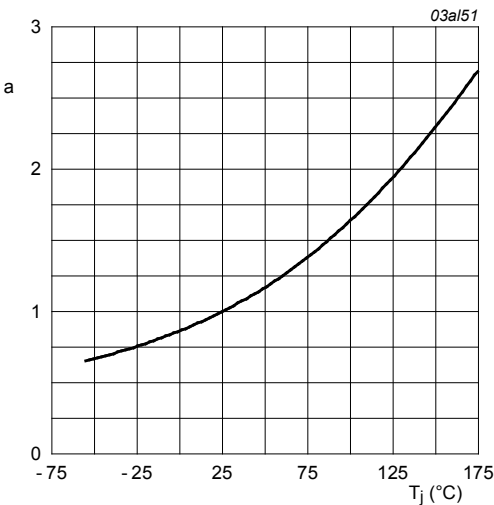


Fig. 9. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}\text{C})}}$$

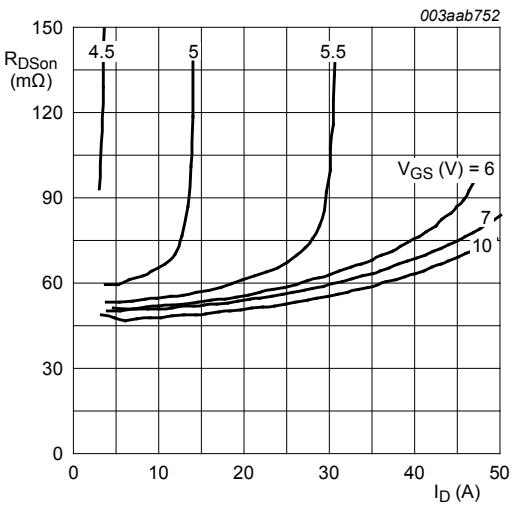


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

$$T_j = 25^{\circ}\text{C}$$

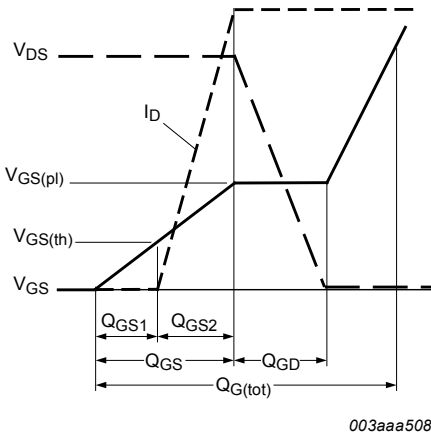


Fig. 11. Gate charge waveform definitions

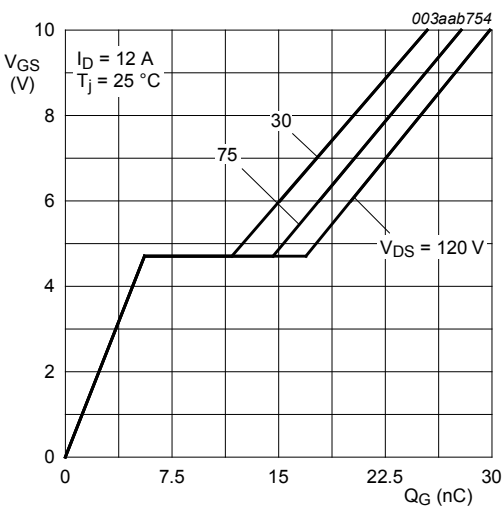


Fig. 12. Gate-source voltage as a function of gate charge; typical values

$$I_D = 12\text{ A}; V_{DS} = 30, 75 \text{ and } 120\text{ V}$$

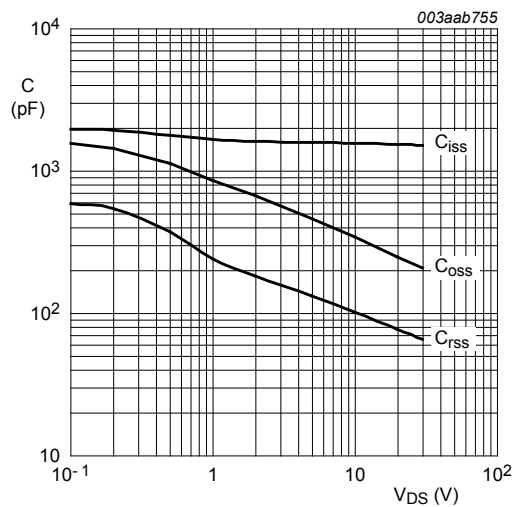


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0V; f = 1MHz$

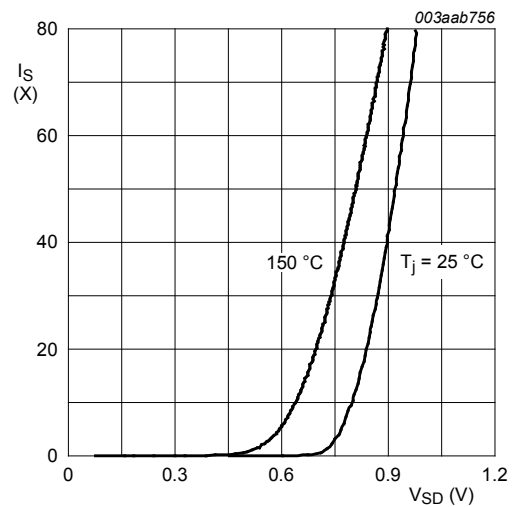


Fig. 14. Source current as a function of source-drain voltage; typical values

$T_j = 25^{\circ}C \text{ and } 150^{\circ}C; V_{GS} = 0V$

11. Package outline

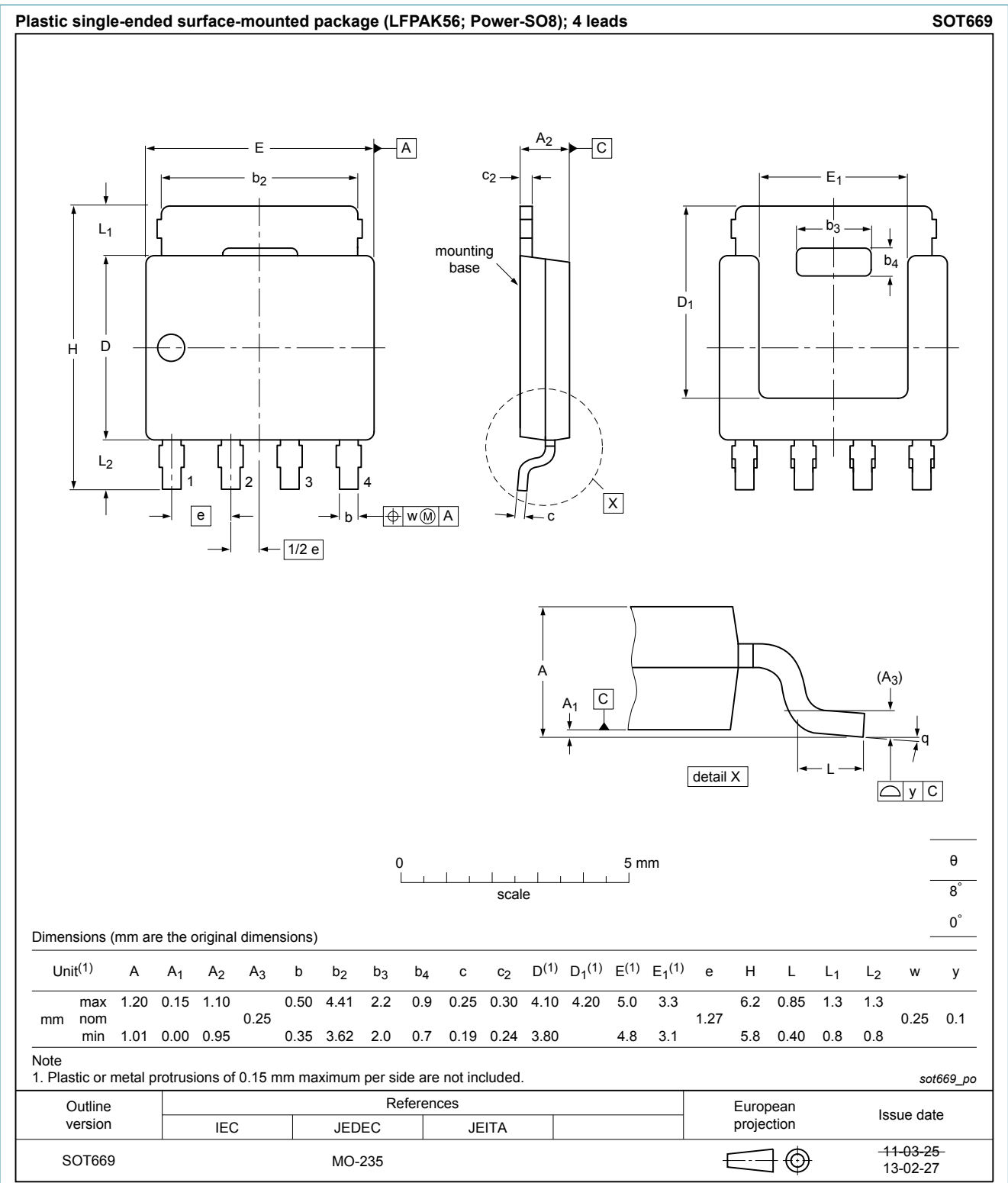


Fig. 15. Package outline LPAK56; Power-SO8 (SOT669)

12. Legal information

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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