# 74AHC374-Q100; 74AHCT374-Q100

Octal D-type flip-flop; positive edge-trigger; 3-state

Rev. 1 — 11 March 2014

Product data sheet

### 1. General description

The 74AHC374-Q100; 74AHCT374-Q100 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7-A.

The 74AHC374-Q100; 74AHCT374-Q100 comprises eight D-type flip-flops featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A clock input (CP) and an output enable input (OE) are common to all flip-flops.

The eight flip-flops will store the state of their individual D inputs that meet the set-up and hold times requirements for the LOW-to-HIGH CP transition.

When  $\overline{OE}$  is LOW the content of the eight flip-flops is available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high-impedance OFF-state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

#### 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - ◆ Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Inputs accept voltages higher than V<sub>CC</sub>
- Common 3-state output enable input
- Input levels:
  - ◆ For 74AHC374-Q100: CMOS level
  - ♦ For 74AHCT374-Q100: TTL level
- ESD protection:
  - ◆ MIL-STD-883, method 3015 exceeds 2000 V
  - HBM JESD22-A114F exceeds 2000 V
  - ♦ MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0  $\Omega$ )
- Multiple package options

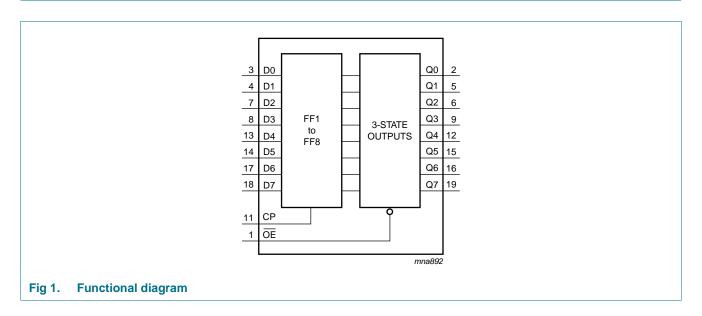


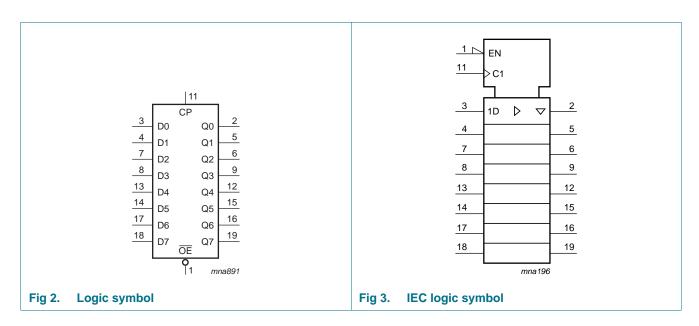
### 3. Ordering information

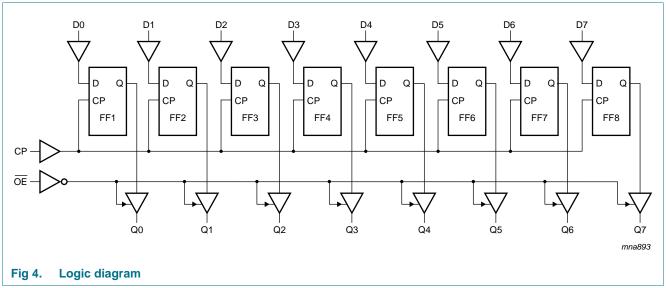
Table 1. Ordering information

Type number	Package	Package								
	Temperature range	Name	Description	Version						
74AHC374-Q100										
74AHC374D-Q100	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1						
74AHC374PW-Q100	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1						
74AHCT374-Q100				1						
74AHCT374D-Q100	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1						
74AHCT374PW-Q100	–40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1						

### 4. Functional diagram

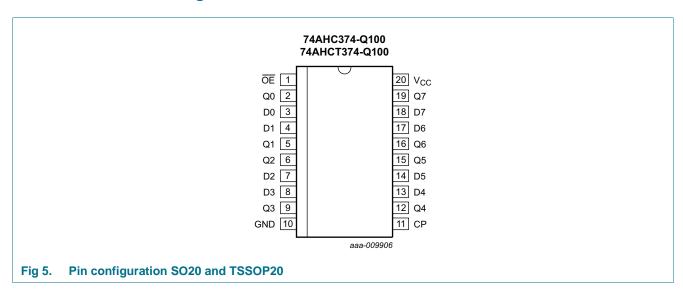






### 5. Pinning information

#### 5.1 Pinning



#### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
ŌĒ	1	3-state output enable input (active LOW)
Q0	2	3-state flip-flop output
D0	3	data input
D1	4	data input
Q1	5	3-state flip-flop output
Q2	6	3-state flip-flop output
D2	7	data input
D3	8	data input
Q3	9	3-state flip-flop output
GND	10	ground (0 V)
СР	11	clock input (LOW-to-HIGH, edge triggered)
Q4	12	3-state flip-flop output
D4	13	data input
D5	14	data input
Q5	15	3-state flip-flop output
Q6	16	3-state flip-flop output
D6	17	data input
D7	18	data input
Q7	19	3-state flip-flop output
V <sub>CC</sub>	20	supply voltage

### 6. Functional description

#### Table 3. Function table[1]

Operating mode	Control		Input	Internal	Output
	OE	СР	Dn	flip-flop	Q0 to Q7
Load and read register	L	1	I	L	L
	L	1	h	Н	Н
Load register and disable outputs	Н	1	I	L	Z
	Н	1	h	Н	Z

<sup>[1]</sup> H = HIGH voltage level;

h = HIGH voltage level one setup time prior to the LOW-to-HIGH CP transition;

L = LOW voltage level;

I = LOW voltage level one setup time prior to the LOW-to-HIGH CP transition;

↑ = LOW-to-HIGH CP transition;

Z = high-impedance OFF-state.

### 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>CC</sub>	supply voltage			-0.5	+7.0	V
VI	input voltage			-0.5	+7.0	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V	<u>[1]</u>	-20	-	mA
I <sub>OK</sub>	output clamping current	$V_O < -0.5 \text{ V or } V_O > V_{CC} + 0.5 \text{ V}$	<u>[1]</u>	-20	+20	mA
I <sub>O</sub>	output current	$V_{O} = -0.5 \text{ V to } (V_{CC} + 0.5 \text{ V})$		-25	+25	mA
I <sub>CC</sub>	supply current			-	+75	mA
$I_{GND}$	ground current			<b>−75</b>	-	mA
T <sub>stg</sub>	storage temperature			-65	+150	°C
P <sub>tot</sub>	total power dissipation	$T_{amb} = -40  ^{\circ}\text{C} \text{ to } +125  ^{\circ}\text{C}$	[2]	-	500	mW

<sup>[1]</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>[2]</sup> For SO20 packages: above 70 °C the value of  $P_{tot}$  derates linearly at 8 mW/K. For TSSOP20 packages: above 60 °C the value of  $P_{tot}$  derates linearly at 5.5 mW/K.

### 8. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
74AHC3	74-Q100					
V <sub>CC</sub>	supply voltage		2.0	5.0	5.5	V
VI	input voltage		0	-	5.5	V
Vo	output voltage		0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	-	-	100	ns/V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	20	ns/V
74AHCT	374-Q100		'			
V <sub>CC</sub>	supply voltage		4.5	5.0	5.5	V
VI	input voltage		0	-	5.5	V
Vo	output voltage		0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	20	ns/V

### 9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C	;	-40 °C t	o +85 °C	-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
74AHC3	74-Q100									<u>'</u>
V <sub>IH</sub>	HIGH-level	V <sub>CC</sub> = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
	input voltage	V <sub>CC</sub> = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V <sub>CC</sub> = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V <sub>CC</sub> = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V <sub>CC</sub> = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V <sub>OH</sub> HIGH-level	$V_I = V_{IH}$ or $V_{IL}$									
	output voltage	$I_{O} = -50 \mu A; V_{CC} = 2.0 V$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_{O} = -50 \mu A; V_{CC} = 3.0 V$	2.9	3.0	-	2.9	-	2.9	-	V
		$I_{O} = -50 \mu A; V_{CC} = 4.5 V$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_{O} = -4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.58	-	-	2.48	-	2.40	-	V
		$I_{O} = -8.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.94	-	-	3.80	-	3.70	-	V
V <sub>OL</sub>	LOW-level	$V_I = V_{IH}$ or $V_{IL}$								
	output voltage	$I_O = 50 \mu A; V_{CC} = 2.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50 \mu A; V_{CC} = 3.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50 \mu A; V_{CC} = 4.5 V$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.36	-	0.44	-	0.55	V
		$I_O = 8.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	-	0.36	-	0.44	-	0.55	V

 Table 6.
 Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C	;	–40 °C t	o +85 °C	–40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
l <sub>l</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μΑ
I <sub>OZ</sub>	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_O = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±0.25	-	±2.5	-	±10.0	μΑ
I <sub>CC</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	4.0	-	40	-	80	μΑ
Cı	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	-	10	-	10	pF
Co	output capacitance		-	4	-	-	-	-	-	pF
74AHCT	374-Q100									
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
$V_{IL}$	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	I <sub>O</sub> = -50 μA	4.4	4.5	-	4.4	-	4.4	-	V
		$I_{O} = -8.0 \text{ mA}$	3.94	-	-	3.80	-	3.70	-	V
$V_{OL}$	LOW-level	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	Ι <sub>Ο</sub> = 50 μΑ	-	0	0.1	-	0.1	-	0.1	V
		$I_{O} = 8.0 \text{ mA}$	-	-	0.36	-	0.44	-	0.55	V
l <sub>l</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μΑ
I <sub>OZ</sub>	OFF-state output current	$\begin{aligned} &V_{I} = V_{IH} \text{ or } V_{IL}; \\ &V_{O} = V_{CC} \text{ or GND per input} \\ &\text{pin; other inputs at} \\ &V_{CC} \text{ or GND; } I_{O} = 0 \text{ A;} \\ &V_{CC} = 5.5 \text{ V} \end{aligned}$	-	-	±0.25	-	±2.5	-	±10.0	μА
I <sub>CC</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	4.0	-	40	-	80	μΑ
Δl <sub>CC</sub>	additional supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V}$ ; other pins at $V_{CC}$ or GND; $I_O = 0 \text{ A}$ ; $V_{CC} = 4.5 \text{ V}$ to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
Cı	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	-	10	-	10	pF
Co	output capacitance		-	4	-	-	-	-	-	pF

### 10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 9.

Symbol	Parameter	Conditions			25 °C		-40 °C t	o +85 °C	-40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	Min	Max	
74AHC3	74-Q100						I	-	1		1
t <sub>pd</sub>	propagation delay	CP to Qn; see Figure 6 and Figure 8	[2]								
		V <sub>CC</sub> = 3.0 V to 3.6 V									
		C <sub>L</sub> = 15 pF		-	6.4	12.7	1.0	15.0	1.0	16.0	ns
		C <sub>L</sub> = 50 pF		-	8.4	16.2	1.0	18.5	1.0	20.5	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V									
		C <sub>L</sub> = 15 pF		-	4.4	8.1	1.0	9.5	1.0	10.0	ns
		C <sub>L</sub> = 50 pF		-	5.7	10.1	1.0	11.5	1.0	12.5	ns
t <sub>en</sub>	enable time	OE to Qn; see Figure 7	[3]								
		V <sub>CC</sub> = 3.0 V to 3.6 V									
		C <sub>L</sub> = 15 pF		-	5.5	11.0	1.0	13.0	1.0	14.0	ns
		C <sub>L</sub> = 50 pF		-	7.3	14.5	1.0	16.5	1.0	18.0	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V									
		C <sub>L</sub> = 15 pF		-	3.9	7.6	1.0	9.0	1.0	9.5	ns
		C <sub>L</sub> = 50 pF		-	5.2	9.6	1.0	11.0	1.0	12.0	ns
t <sub>dis</sub>	disable time	OE to Qn; see Figure 7	[4]								
		V <sub>CC</sub> = 3.0 V to 3.6 V									
		C <sub>L</sub> = 15 pF		-	5.6	10.5	1.0	12.5	1.0	13.0	ns
		C <sub>L</sub> = 50 pF		-	9.4	14.0	1.0	16.0	1.0	17.5	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V									
		C <sub>L</sub> = 15 pF		-	4.2	6.8	1.0	8.0	1.0	8.5	ns
		C <sub>L</sub> = 50 pF		-	6.4	8.8	1.0	10.0	1.0	11.0	ns
f <sub>max</sub>	maximum	see Figure 6									
	frequency	V <sub>CC</sub> = 3.0 V to 3.6 V									
		C <sub>L</sub> = 15 pF		80	130	-	70	-	70	-	MHz
		C <sub>L</sub> = 50 pF		55	85	-	50	-	50	-	MHz
		V <sub>CC</sub> = 4.5 V to 5.5 V									
		C <sub>L</sub> = 15 pF		130	185	-	110	-	110	-	MHz
		C <sub>L</sub> = 50 pF		85	120	-	75	-	75	-	MHz
t <sub>W</sub>	pulse width	CP HIGH or LOW; see Figure 6									
		V <sub>CC</sub> = 3.0 V to 3.6 V		5.0	-	-	5.5	-	5.5	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V		5.0	-	-	5.0	-	5.0	-	ns
t <sub>su</sub>	set-up time	Dn to CP; see Figure 8									
		V <sub>CC</sub> = 3.0 V to 3.6 V		4.5	-	-	4.0	-	4.0	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V		3.0	-	-	3.0	-	3.0	-	ns

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 Table 7.
 Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 9.

Symbol	Parameter	Conditions			25 °C		-40 °C to	o +85 °C	-40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	Min	Max	
t <sub>h</sub>	hold time	Dn to CP; see Figure 8									
		V <sub>CC</sub> = 3.0 V to 3.6 V		2.0	-	-	2.0	-	2.0	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V		2.0	-	-	2.0	-	2.0	-	ns
C <sub>PD</sub>	power dissipation capacitance	$f_i = 1 \text{ MHz}; V_I = \text{GND to } V_{CC}$	5]	-	10	-	-	-	-	-	pF
74AHCT	374-Q100; V <sub>C</sub>	<sub>C</sub> = 4.5 V to 5.5 V								1	
t <sub>pd</sub>	propagation delay	CP to Qn; see Figure 6 and Figure 8	2]								
		C <sub>L</sub> = 15 pF		-	4.3	9.4	1.0	10.5	1.0	12.0	ns
		C <sub>L</sub> = 50 pF		-	5.6	10.4	1.0	11.5	1.0	13.0	ns
t <sub>en</sub>	enable time	OE to Qn; see Figure 7	3]								
		C <sub>L</sub> = 15 pF		-	3.5	10.2	1.0	11.5	1.0	13.0	ns
		C <sub>L</sub> = 50 pF		-	4.8	11.2	1.0	12.5	1.0	14.0	ns
t <sub>dis</sub>	disable time	OE to Qn; see Figure 7	4]								
		C <sub>L</sub> = 15 pF		-	3.6	10.2	1.0	11.0	1.0	13.0	ns
		C <sub>L</sub> = 50 pF		-	5.7	11.2	1.0	12.0	1.0	14.0	ns
f <sub>max</sub>	maximum	see Figure 6									
	frequency	C <sub>L</sub> = 15 pF		90	140	-	80	-	80	-	MHz
		C <sub>L</sub> = 50 pF		85	130	-	75	-	75	-	MHz
t <sub>W</sub>	pulse width	CP HIGH or LOW; see Figure 6		6.5	-	-	6.5	-	6.5	-	ns
t <sub>su</sub>	set-up time	Dn to CP; see Figure 8		2.5	-	-	2.5	-	2.5	-	ns
t <sub>h</sub>	hold time	Dn to CP; see Figure 8		2.5	-	-	2.5	-	2.5	-	ns
C <sub>PD</sub>	power dissipation capacitance	$f_i = 1 \text{ MHz}; V_I = \text{GND to } V_{CC}$	5]	-	12	-	-	-	-	-	pF

- [1] Typical values are measured at nominal supply voltage ( $V_{CC} = 3.3 \text{ V}$  and  $V_{CC} = 5.0 \text{ V}$ ).
- [2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .
- [3]  $t_{en}$  is the same as  $t_{PZH}$  and  $t_{PZL}$ .
- [4]  $t_{dis}$  is the same as  $t_{PHZ}$  and  $t_{PLZ}$ .
- [5]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ).

 $P_D = C_{PD} \times V_{CC}{}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}{}^2 \times f_o) \text{ where:}$ 

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

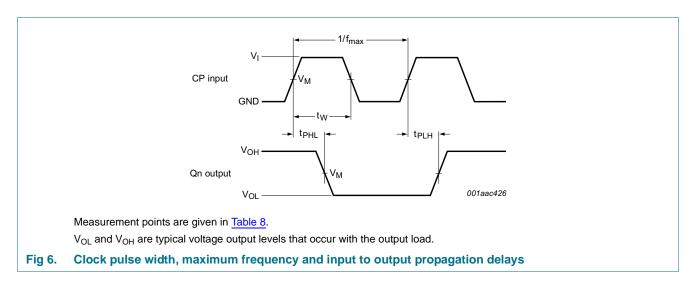
C<sub>L</sub> = output load capacitance in pF;

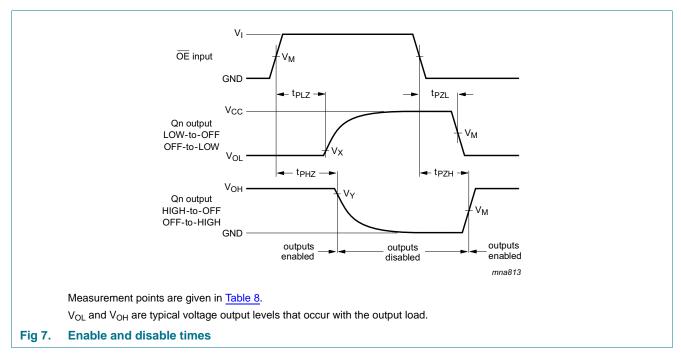
V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;

 $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

#### 10.1 Waveforms





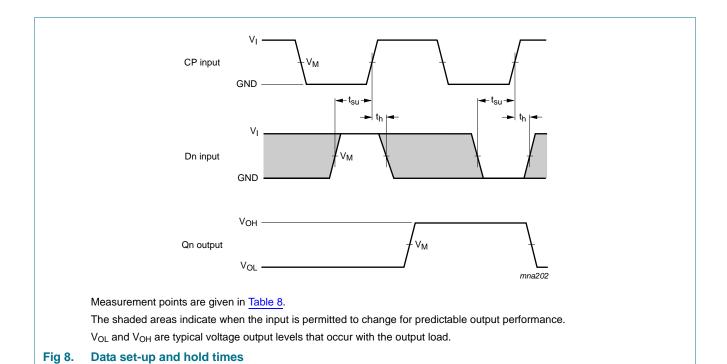
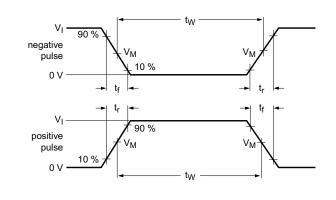
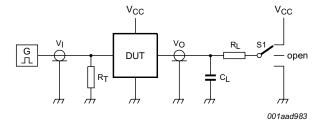


Table 8. Measurement points

Туре	Input	Output					
	V <sub>M</sub>	V <sub>M</sub>	V <sub>X</sub>	V <sub>Y</sub>			
74AHC374-Q100	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V <sub>OL</sub> + 0.3 V	V <sub>OH</sub> – 0.3 V			
74AHCT374-Q100	1.5 V	$0.5 \times V_{CC}$	V <sub>OL</sub> + 0.3 V	V <sub>OH</sub> – 0.3 V			





Test data is given in Table 9.

Definitions test circuit:

 $R_T$  = termination resistance should be equal to output impedance  $Z_0$  of the pulse generator.

C<sub>L</sub> = load capacitance including jig and probe capacitance.

 $R_L$  = load resistance.

S1 = test selection switch.

Fig 9. Test circuit for measuring switching times

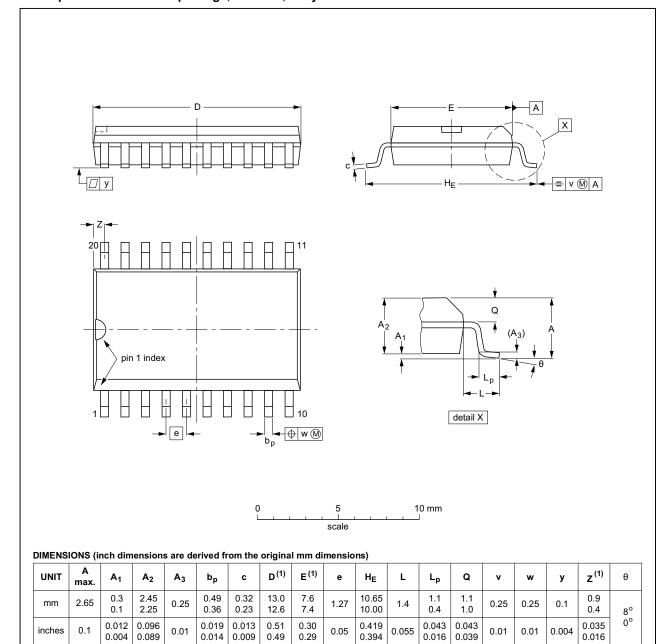
Table 9. Test data

Туре	Input		Load	S1 position	
	V <sub>I</sub>	t <sub>r</sub> , t <sub>f</sub>	C <sub>L</sub>	R <sub>L</sub>	t <sub>PHL</sub> , t <sub>PLH</sub>
74AHC374-Q100	V <sub>CC</sub>	≤ 3.0 ns	15 pF, 50 pF	1 kΩ	open
74AHCT374-Q100	3.0 V	≤ 3.0 ns	15 pF, 50 pF	1 kΩ	open

### 11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



#### Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE		REFER	RENCES	EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE	
SOT163-1	075E04	MS-013			<del>99-12-27</del> 03-02-19	

Fig 10. Package outline SOT163-1 (SO20)

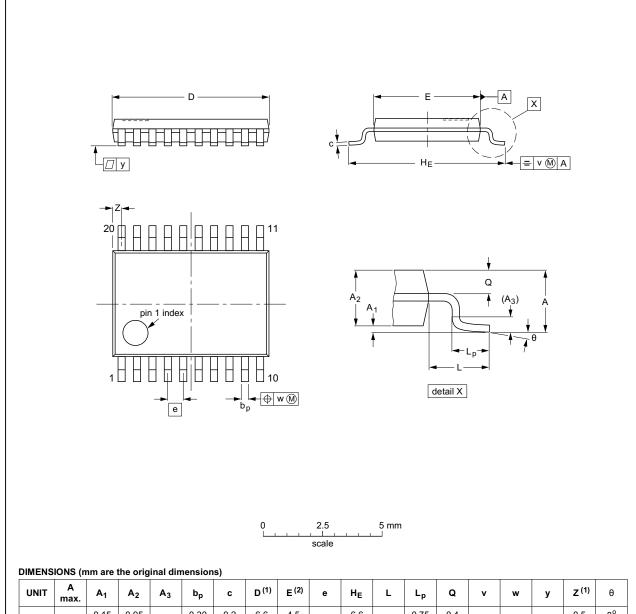
74AHC\_AHCT374\_Q100

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#### TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	<b>A</b> <sub>3</sub>	bp	С	D <sup>(1)</sup>	E (2)	е	HE	L	Lp	Q	٧	w	у	Z <sup>(1)</sup>	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

#### Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

		EUROPEAN	ISSUE DATE			
IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
	MO-153				<del>99-12-27</del> 03-02-19	
_	IEC				IEC JEDEC JEHA	

Fig 11. Package outline SOT360-1 (TSSOP20)

74AHC\_AHCT374\_Q100

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### 12. Abbreviations

#### Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MIL	Military
MM	Machine Model

### 13. Revision history

#### Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT374_Q100 v.1	20140311	Product data sheet	-	-

### 14. Legal information

#### 14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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#### **NXP Semiconductors**

# 74AHC374-Q100; 74AHCT374-Q100

Octal D-type flip-flop; positive edge-trigger; 3-state

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Octal D-type flip-flop; positive edge-trigger; 3-state

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