

High Isolation SPDT SWITCH

■ GENERAL DESCRIPTION

The NJG1697EM1 is a 1bit control GaAs high isolation SPDT switch MMIC. The NJG1697EM1 features very high isolation and low control voltage. It has integrated DC blocking capacitor at PC port.

It has integrated ESD protection circuits the IC to achieve high ESD tolerance.

The small and thin 6-pin DFN6-M1 package is adopted.

■ PACKAGE OUTLINE



NJG1697EM1

■ APPLICATIONS

Multi-mode 2G/3G and LTE application receive system

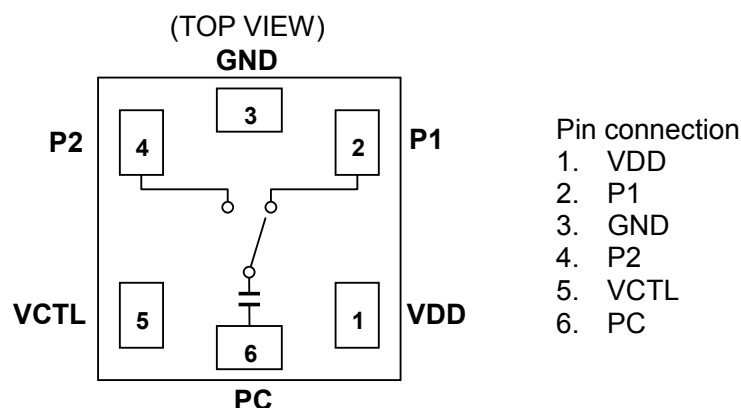
Pre PA switching, reception bands switching applications

General purpose switching applications

■ FEATURES

- Low voltage logic control $V_{CTL(H)}=1.8V$ typ.
- Low voltage operation $V_{DD}=2.7V$ typ.
- High isolation
 - 50dB typ. @f=1.0GHz, $P_{IN}=0dBm$
 - 48dB typ. @f=2.0GHz, $P_{IN}=0dBm$
 - 43dB typ. @f=2.7GHz, $P_{IN}=0dBm$
- Low insertion loss
 - 0.45dB typ. @f=1.0GHz, $P_{IN}=0dBm$
 - 0.50dB typ. @f=2.0GHz, $P_{IN}=0dBm$
 - 0.55dB typ. @f=2.7GHz, $P_{IN}=0dBm$
- Ultra small & ultra thin package DFN6-M1 Package (Package size: 1.0 x 1.0 x 0.38mm)
- RoHS compliant and Halogen Free, MSL1

■ PIN CONFIGURATION



■ TRUTH TABLE

"H"= $V_{CTL(H)}$, "L"= $V_{CTL(L)}$

ON PATH	VCTL
PC-P1	H
PC-P2	L

NOTE: Please note that any information on this datasheet will be subject to change.

■ ABSOLUTE MAXIMUM RATINGS

($T_a=+25^{\circ}\text{C}$, $Z_s=Z_i=50\Omega$)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNITS
RF Input Power	P_{IN}	$V_{DD}=2.7\text{V}$	28	dBm
Supply Voltage	V_{DD}	VDD terminal	5.0	V
Control Voltage	V_{CTL}	VCTL terminal	5.0	V
Power Dissipation	P_D	Four-layer FR4 PCB with through-hole (114.3×76.2mm), $T_j=150^{\circ}\text{C}$	440	mW
Operating Temperature	T_{opr}		-40~+90	$^{\circ}\text{C}$
Storage Temperature	T_{stg}		-55~+150	$^{\circ}\text{C}$

■ ELECTRICAL CHARACTERISTICS1 (DC CHARACTERISTICS)

(General conditions: $T_a=+25^{\circ}\text{C}$, $Z_s=Z_l=50\Omega$, $V_{DD}=2.7\text{V}$, $V_{CTL(L)}=0\text{V}$, $V_{CTL(H)}=1.8\text{V}$, with application circuit)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}	VDD terminal	1.5	2.7	4.5	V
Operating Current	I_{DD}		-	15	30	μA
Control Voltage (LOW)	$V_{CTL(L)}$	VCTL terminal	0	0	0.45	V
Control Voltage (HIGH)	$V_{CTL(H)}$	VCTL terminal	1.35	1.8	4.5	V
Control Current	I_{CTL}	$V_{CTL(H)}=1.8\text{V}$	-	5	10	μA

■ ELECTRICAL CHARACTERISTICS2 (RF CHARACTERISTICS)

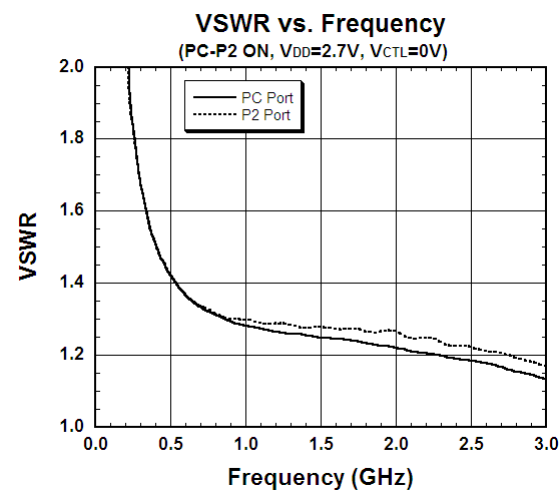
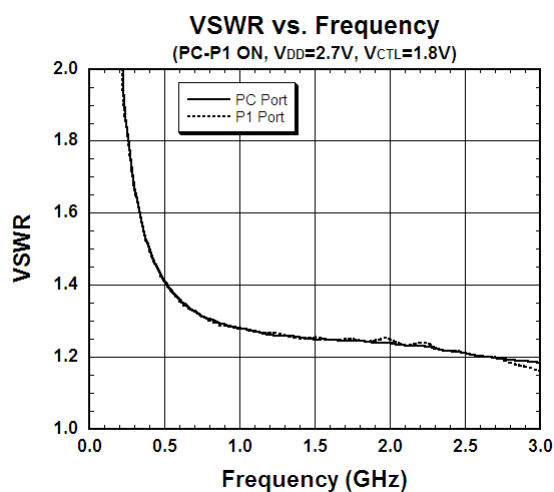
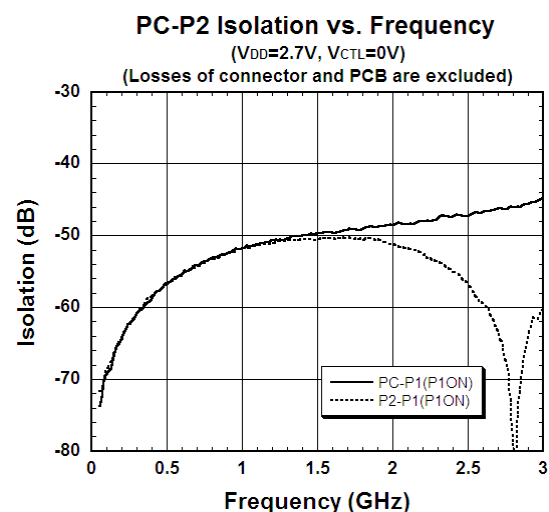
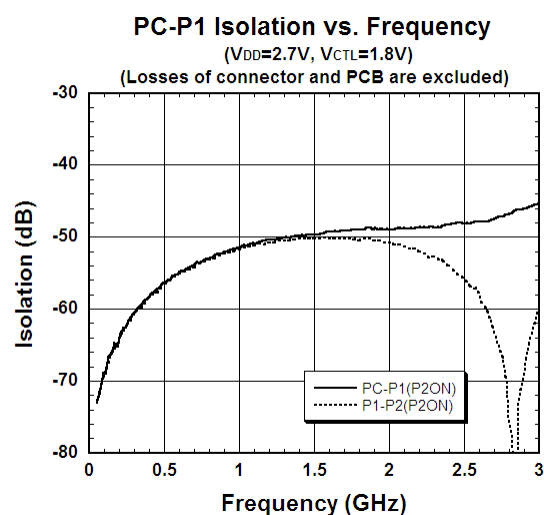
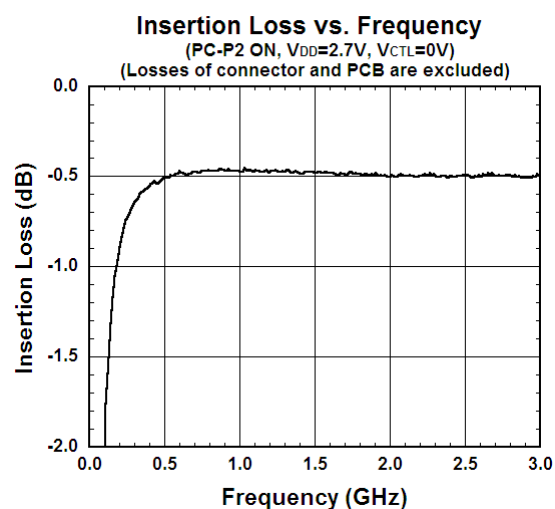
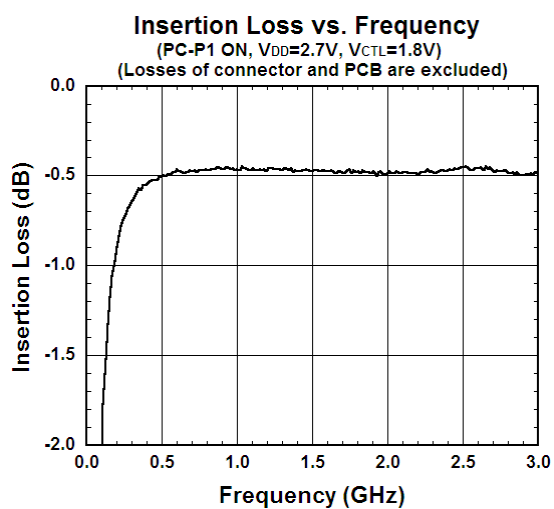
(General conditions: $T_a=+25^{\circ}\text{C}$, $Z_s=Z_l=50\Omega$, $V_{DD}=2.7\text{V}$, $V_{CTL(L)}=0\text{V}$, $V_{CTL(H)}=1.8\text{V}$, with application circuit)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Insertion Loss 1	LOSS1	$f=0.5\text{GHz}$, $P_{IN}=0\text{dBm}$	-	0.55	0.75	dB
Insertion Loss 2	LOSS2	$f=1.0\text{GHz}$, $P_{IN}=0\text{dBm}$	-	0.45	0.65	dB
Insertion Loss 3	LOSS3	$f=2.0\text{GHz}$, $P_{IN}=0\text{dBm}$	-	0.50	0.70	dB
Insertion Loss 4	LOSS4	$f=2.7\text{GHz}$, $P_{IN}=0\text{dBm}$	-	0.55	0.75	dB
Isolation 1	ISL1	PC-P1, P2 $f=0.5\text{GHz}$, $P_{IN}=0\text{dBm}$	50	55	-	dB
Isolation 2	ISL2	PC-P1, P2 $f=1.0\text{GHz}$, $P_{IN}=0\text{dBm}$	45	50	-	dB
Isolation 3	ISL3	PC-P1, P2 $f=2.0\text{GHz}$, $P_{IN}=0\text{dBm}$	45	48	-	dB
Isolation 4	ISL4	PC-P1, P2 $f=2.7\text{GHz}$, $P_{IN}=0\text{dBm}$	40	43	-	dB
Input power at 0.2dB Compression Point	$P_{-0.2\text{dB}}$	$f=2.0\text{GHz}$	18	22	-	dBm
VSWR	VSWR	$f=2.0\text{GHz}$, On port	-	1.3	1.5	-
Switching time	T_{SW}	50% V_{CTL} to 10/90% RF	-	2	5	μs

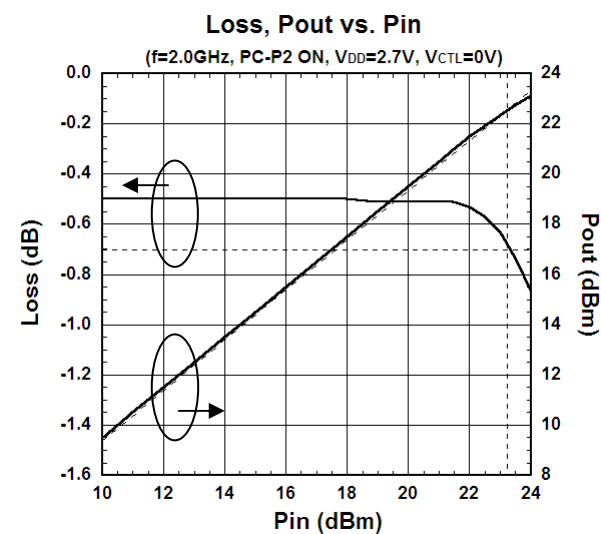
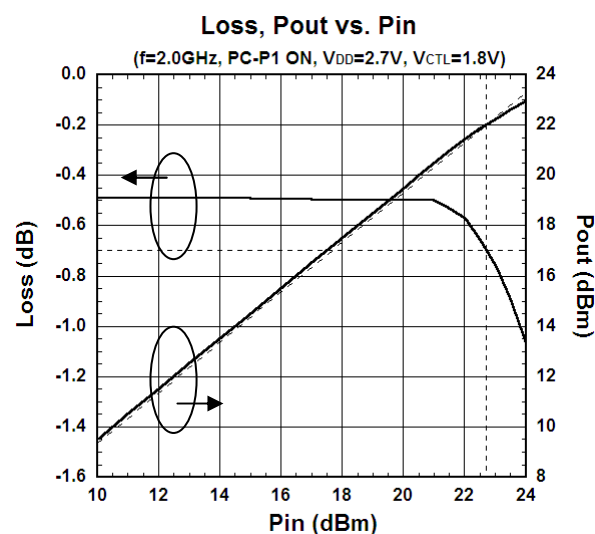
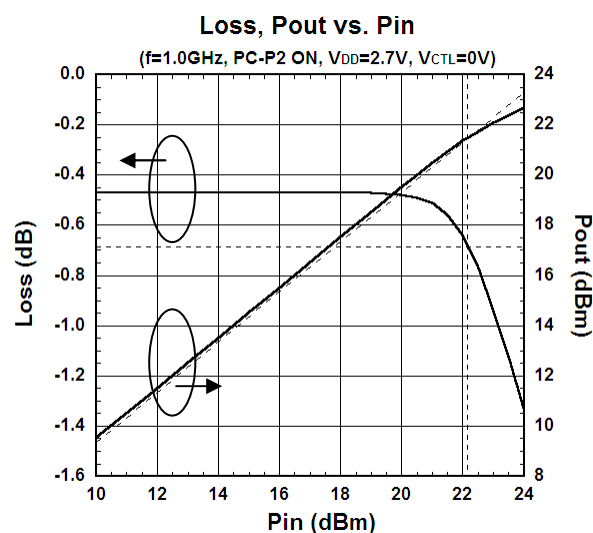
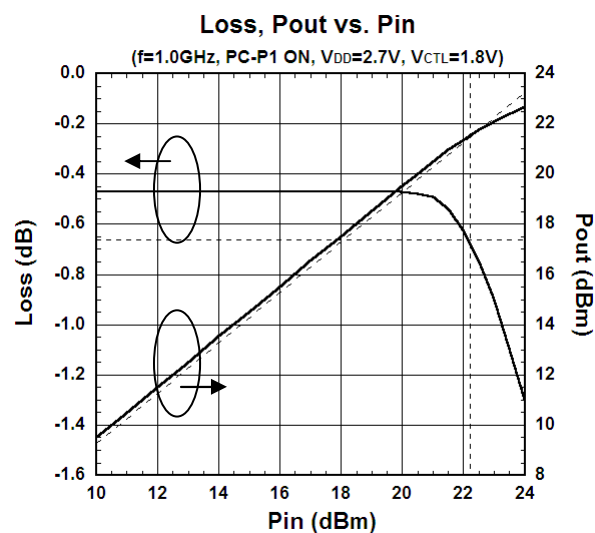
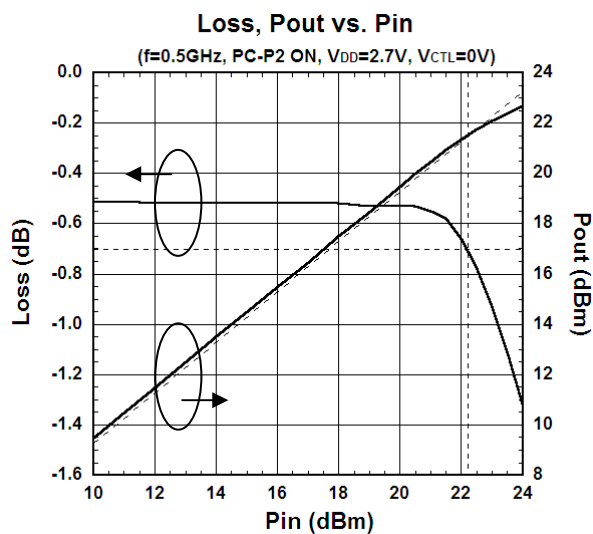
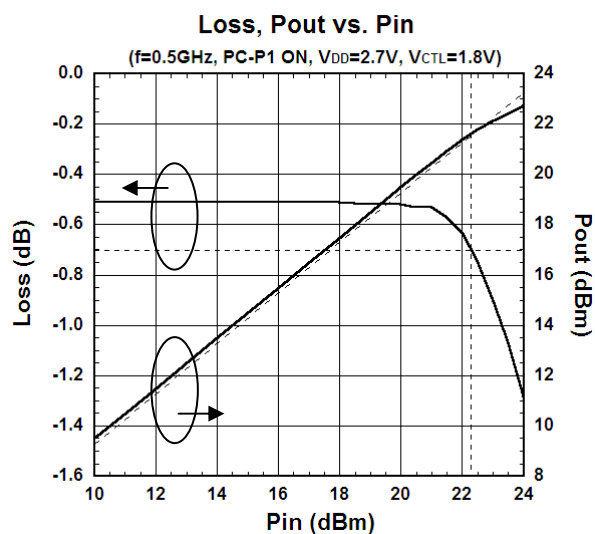
■ TERMINAL INFORMATION

No.	SYMBOL	DESCRIPTION
1	VDD	Positive voltage supply terminal. The positive voltage (+1.5~+4.5V) has to be supplied. Please connect a bypass capacitor with GND terminal for excellent RF performance.
2	P1	RF input / output port. External capacitor is required to block the DC bias voltage of internal circuit.
3	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
4	P2	RF input / output port. External capacitor is required to block the DC bias voltage of internal circuit.
5	VCTL	Control signal input terminal. This terminal is set to High-Level (+1.35~+4.5V) or Low-Level (0~+0.45V). Please connect a bypass capacitor with GND terminal for excellent RF performance.
6	PC	RF input/output port. No DC blocking capacitor is required for this port because of internal capacitor.

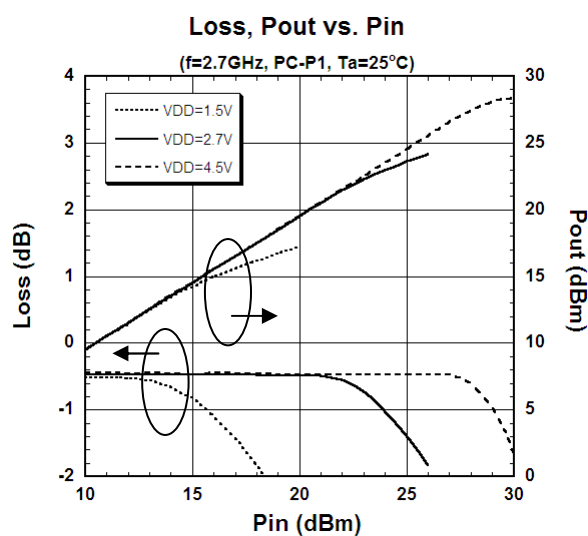
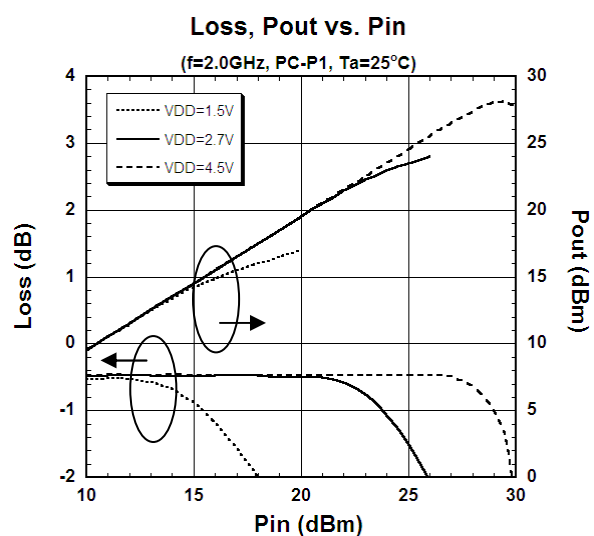
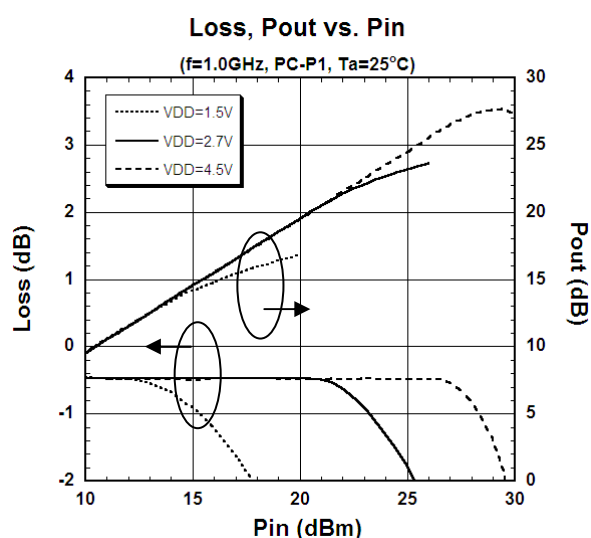
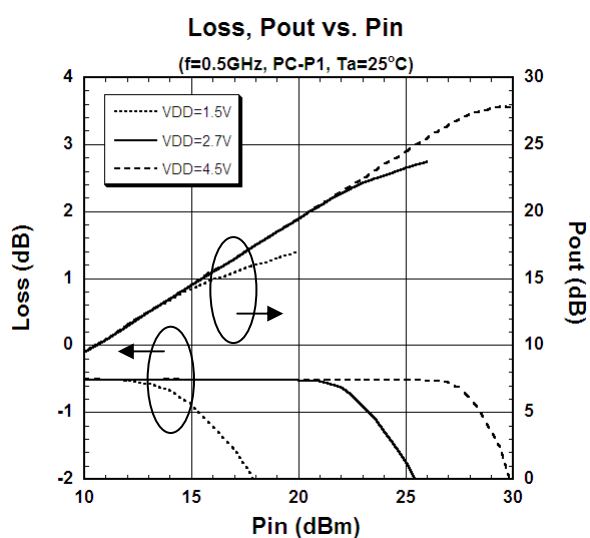
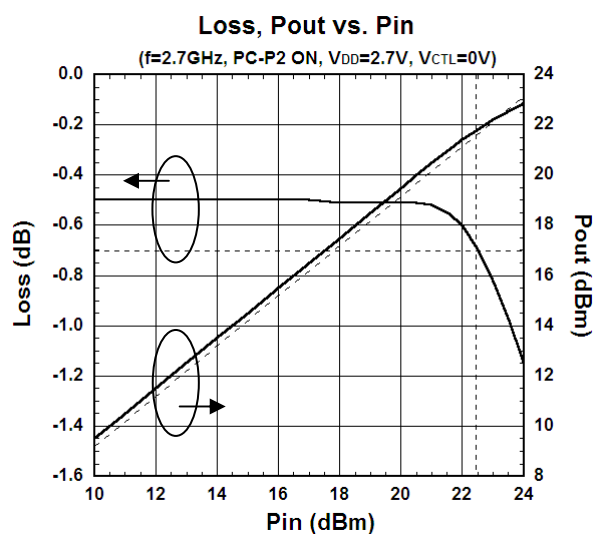
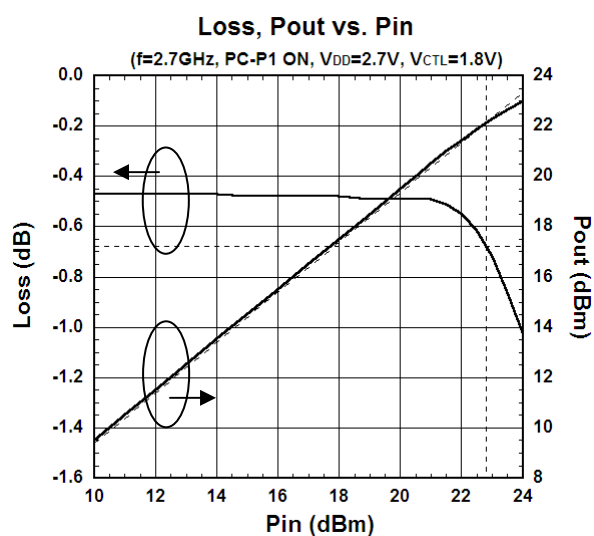
■ ELECTRICAL CHARACTERISTICS (With Application circuit)



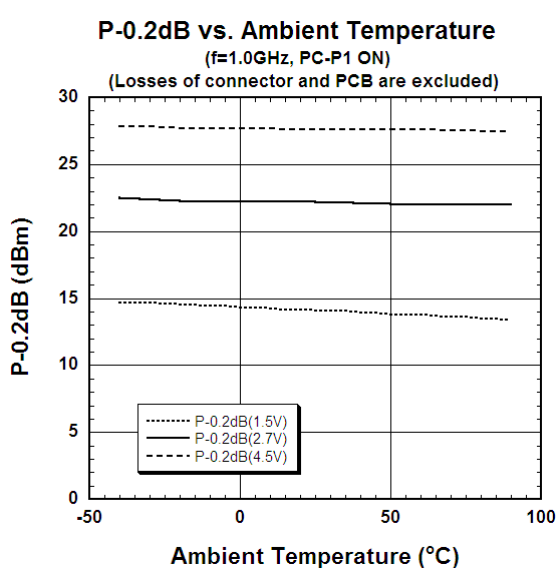
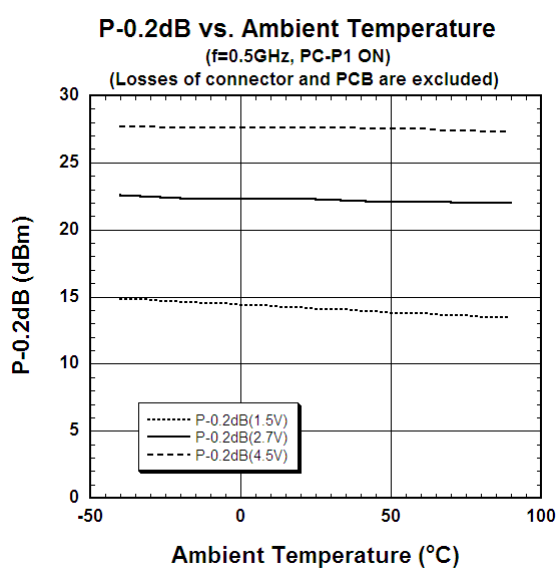
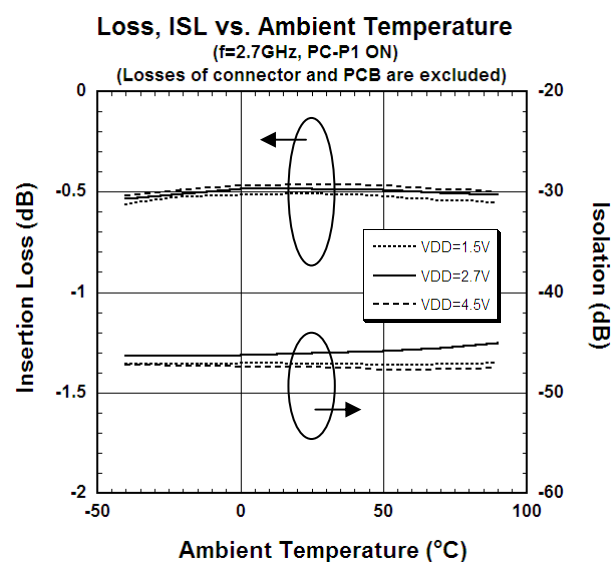
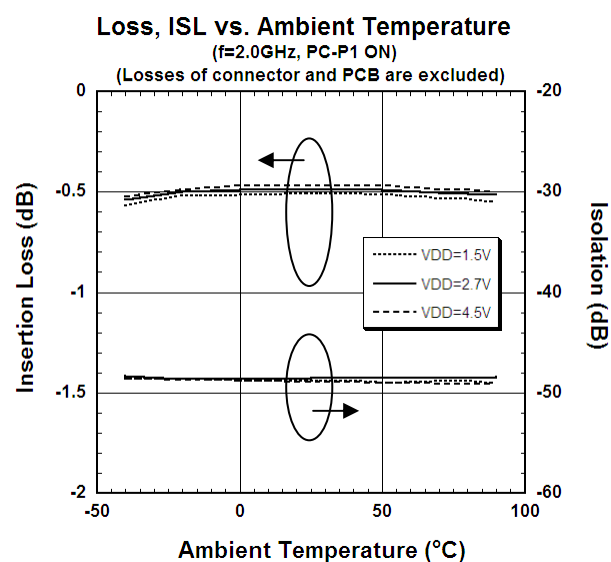
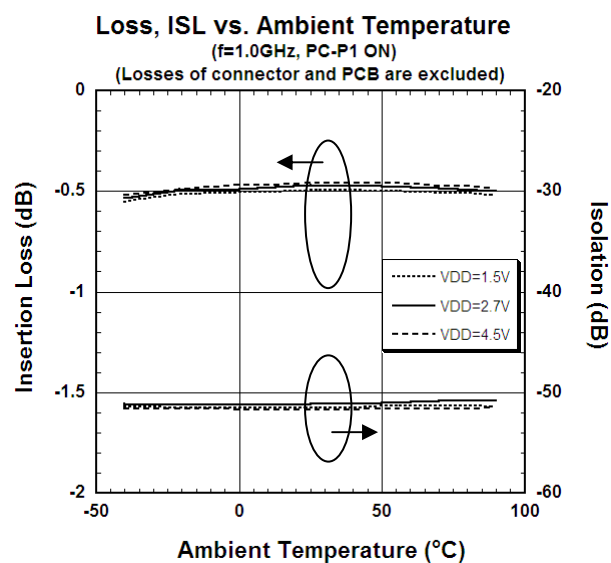
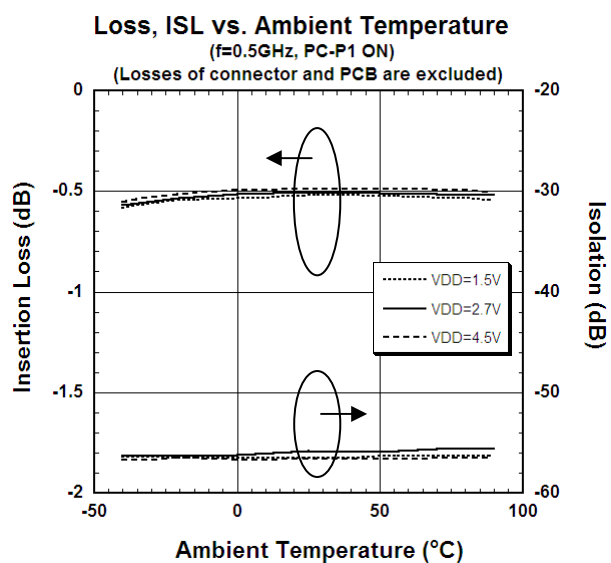
■ ELECTRICAL CHARACTERISTICS (With Application circuit)



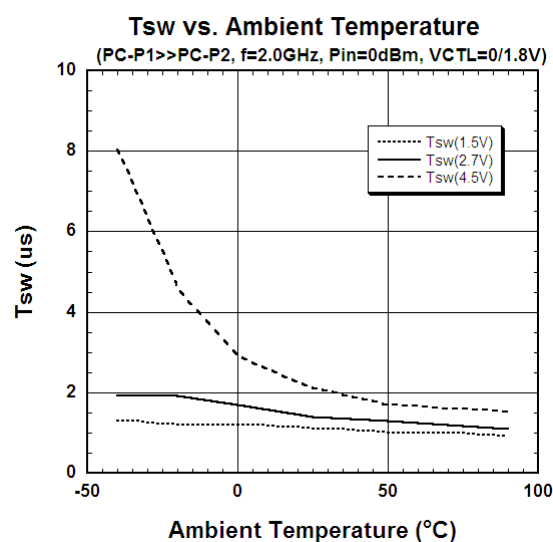
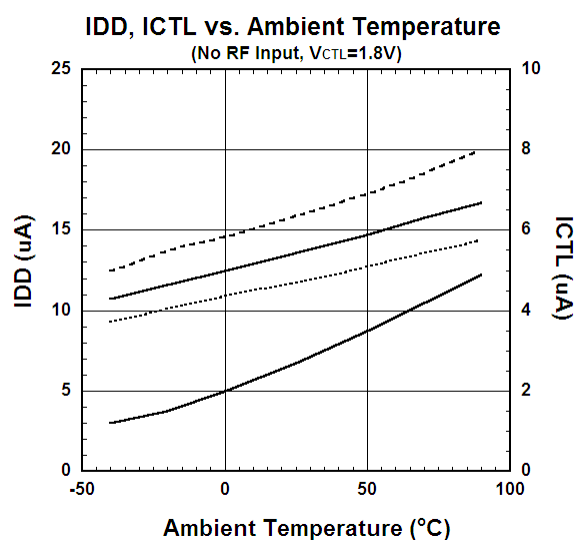
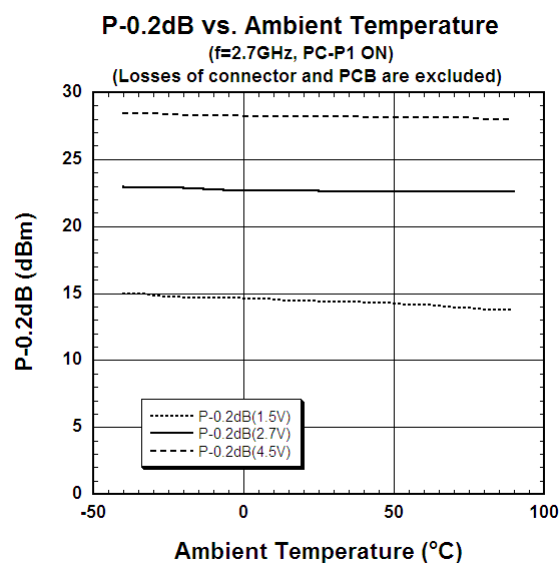
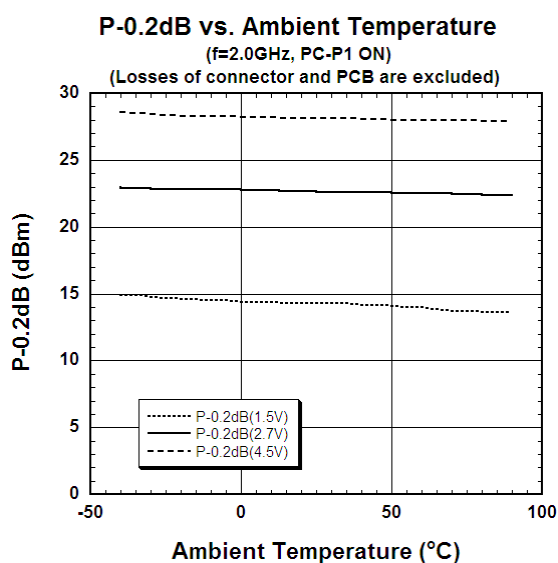
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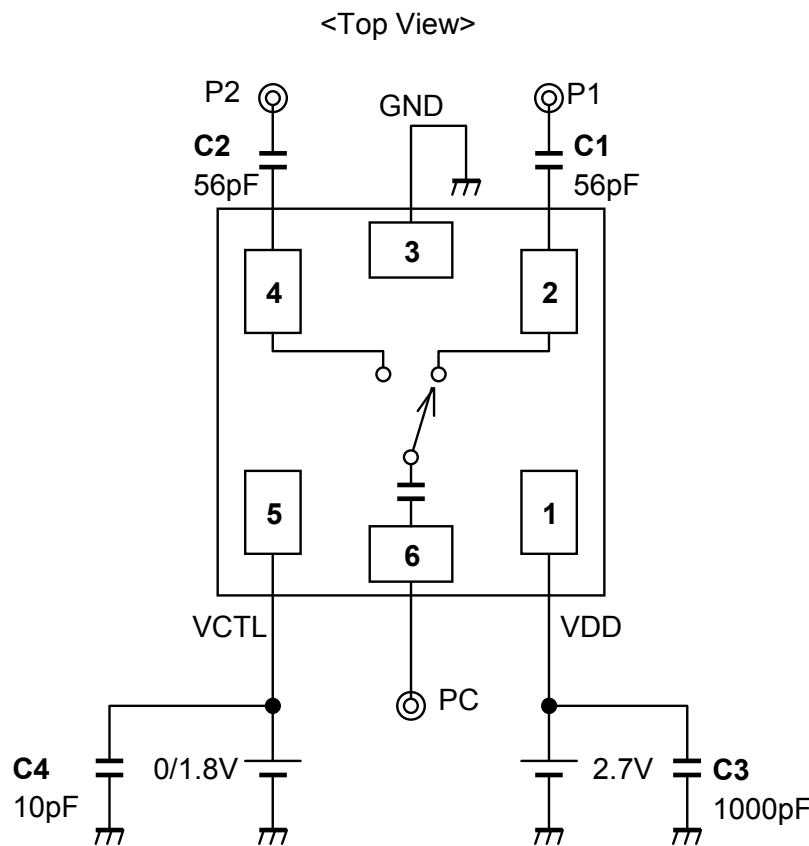
■ ELECTRICAL CHARACTERISTICS (With Application circuit)



■ ELECTRICAL CHARACTERISTICS (With Application circuit)



APPLICATION CIRCUIT



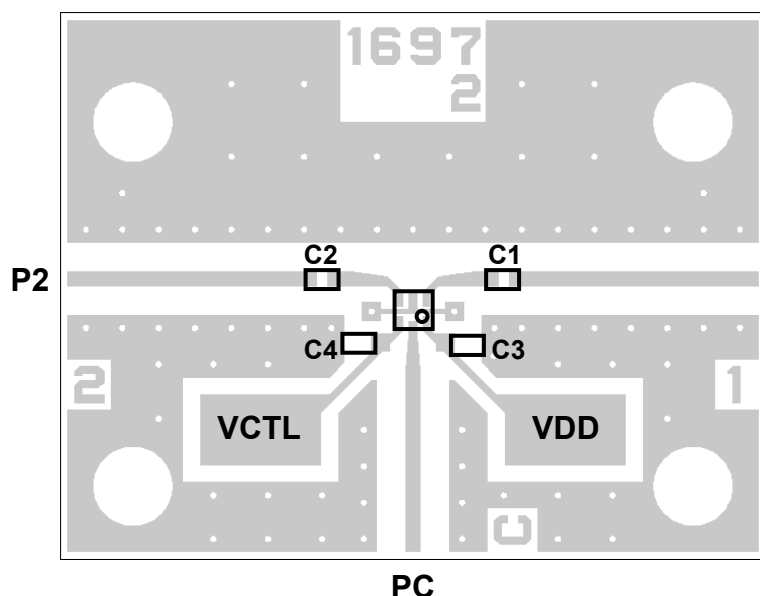
Note:
The DC blocking capacitor is not necessary at PC Port because of the integrated DC blocking capacitor.

PARTS LIST

Part ID	Value	Notes
C1~C2	56pF	MURATA (GRM15)
C3	1000pF	MURATA (GRM15)
C4	10pF	MURATA (GRM15)

■ APPLIED CIRCUIT BOARD EXAMPLES

(TOP VIEW)



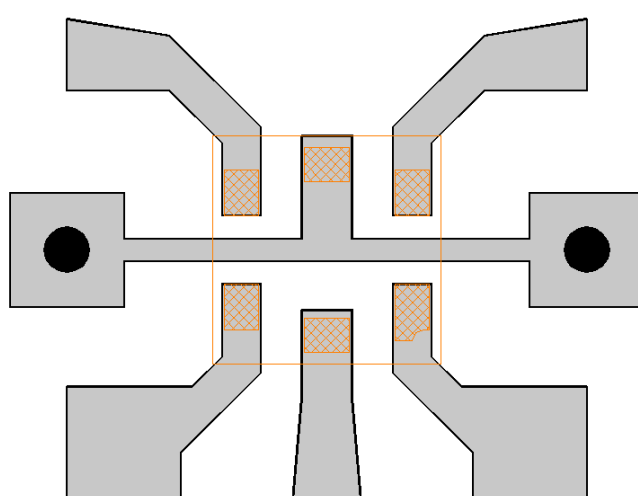
PCB: FR-4, t=0.2mm
 Capacitor Size: 1005 (1.0 x 0.5 mm)
 Strip Line Width: 0.4mm
 PCB Size: 19.4 x 15.0mm
 Through Hole Diameter: 0.2mm

P1 Losses of PCB, capacitors and connectors

Paths	Frequency (GHz)	Loss (dB)
PC-P1, PC-P2	0.5	0.12
	1.0	0.17
	2.0	0.30
	2.7	0.36

<PCB LAYOUT GUIDELINE>

(TOP VIEW)



-  PCB
-  PKG Terminal
-  PKG Outline
-  GND Via Hole
Diameter: $\phi = 0.2\text{mm}$

To achieve the isolation specified in the datasheet, it is needed that the ground plane located beneath the device as shown above figure. In this case, the minimum line and space width of PCB is 0.1mm.

PRECAUTIONS

- [1] The DC current at RF ports must be equal to zero, which can be achieved with DC blocking capacitors (C1, C2). (However, in case there is no possibility that DC current flows, the DC blocking capacitors are unnecessary, i.e. the RF signals are fed by SAW filters that block DC current by nature, etc.)
- [2] To reduce stripline influence on RF characteristics, please locate the bypass capacitor C3 and C4 close to VDD and VCTL terminal.
- [3] For good isolation, the GND terminals must be connected to the PCB ground plane of substrate, and the through-holes connecting the backside ground plane should be placed near by the pin connection.

RECOMMENDED FOOTPRINT PATTERN (DFN6-M1 PACKAGE REFERENCE)

PKG : 1.0mm x 1.0mm

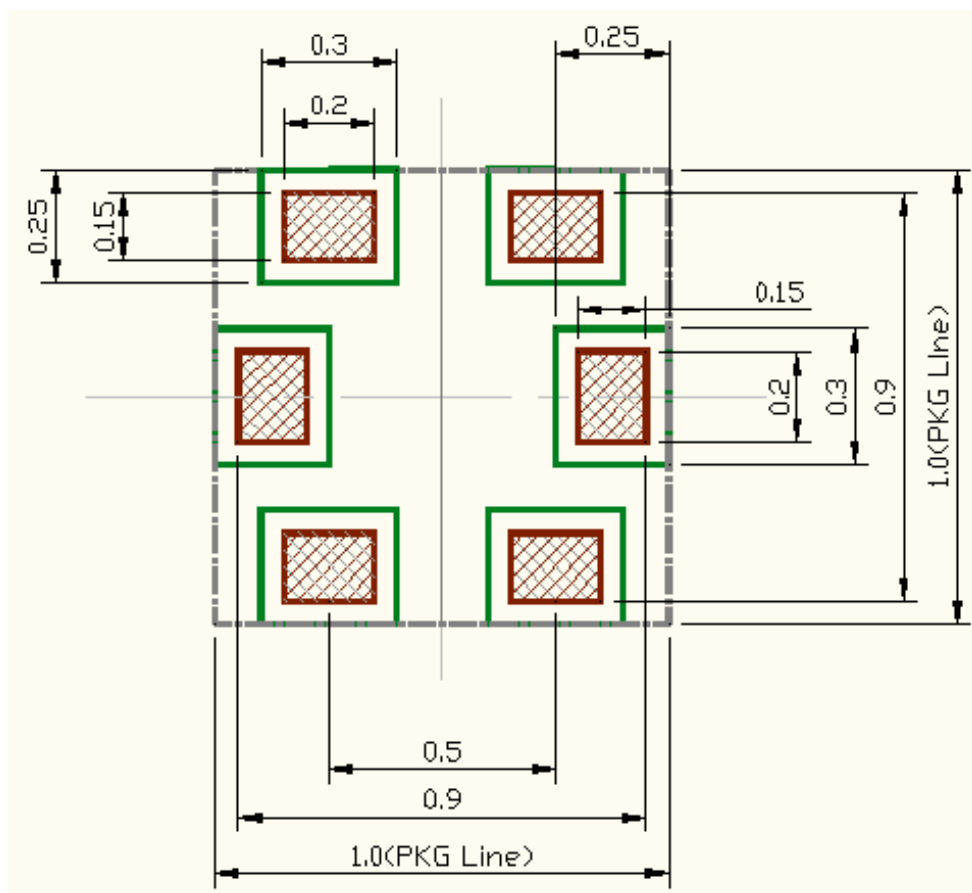
Pin pitch : 0.5mm

 : Land

 : Mask (Open area)

 : Resist(Open area)

*Metal mask thickness : 100 μ m



[illegible]

3

5



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- Do NOT eat or put into mouth

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.

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• Do NOT eat or put into mouth. • Do NOT dispose in fire or break up this product.	only given for information , without any guarantee as regards either mistakes or omissions
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• Do NOT chemically make gas or powder with this product. • To waste this product, please obey the relating law of your country.	The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.
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