150V V_{IN} and V_{OUT} Synchronous 4-Switch Buck-Boost Controller

FEATURES

- **4-Switch Current Mode Single Inductor Architecture Allows V_{IN} Above, Below or Equal to V_{OUT}**
- **Wide V_{IN} Range: 4.5V to 150V**
- **Wide Output Voltage Range: 1.2V ≤ V_{OUT} ≤ 150V**
- **Synchronous Rectification: Up to 99% Efficiency**
- **±1% 1.2V Voltage Reference**
- **Input or Output Average Current Limit**
- **Onboard LDO or External NMOS LDO for DRV_{CC}**
- **36V $EXTV_{CC}$ LDO Powers Drivers**
- **Programmable 6V to 10V DRV_{CC} Optimizes Efficiency**
- No Top FET Refresh Noise in Boost or Buck Mode
- V_{OUT} Disconnected from V_{IN} During Shutdown
- Phase-Lockable Fixed Frequency (50kHz to 600kHz)
- No Reverse Current During Start-Up
- Power Good Output Voltage Monitor
- 150V Rated RUN Pin with Accurate Turn-On Threshold
- Programmable Input Overvoltage Lockout
- Thermally Enhanced FE38 TSSOP Package Modified for High Voltage Operation

APPLICATIONS

- Industrial, Automotive, Medical, Military, Avionics

DESCRIPTION

The LTC®3779 is a high performance buck-boost switching regulator controller that operates from input voltages above, below or equal to the output voltage. The constant frequency current mode architecture allows a phase-lockable frequency of up to 600kHz, while an input/output constant-current loop provides support for battery charging.

With a wide 4.5V to 150V input and output range and seamless transfers between operating regions, the LTC3779 is ideal for automotive, telecom and battery-powered systems.

The LTC3779 features a precision 1.2V reference and power good output indicator. The MODE pin can select between pulse-skipping mode or forced continuous mode of operation. Pulse-skipping mode offers high efficiency at light load while forced continuous mode operates at a constant frequency for noise sensitive applications. The PLLIN pin allows the IC to be synchronized to an external clock. The SS pin ramps the output voltage during start-up. Current foldback limits MOSFET heat dissipation during short-circuit conditions.

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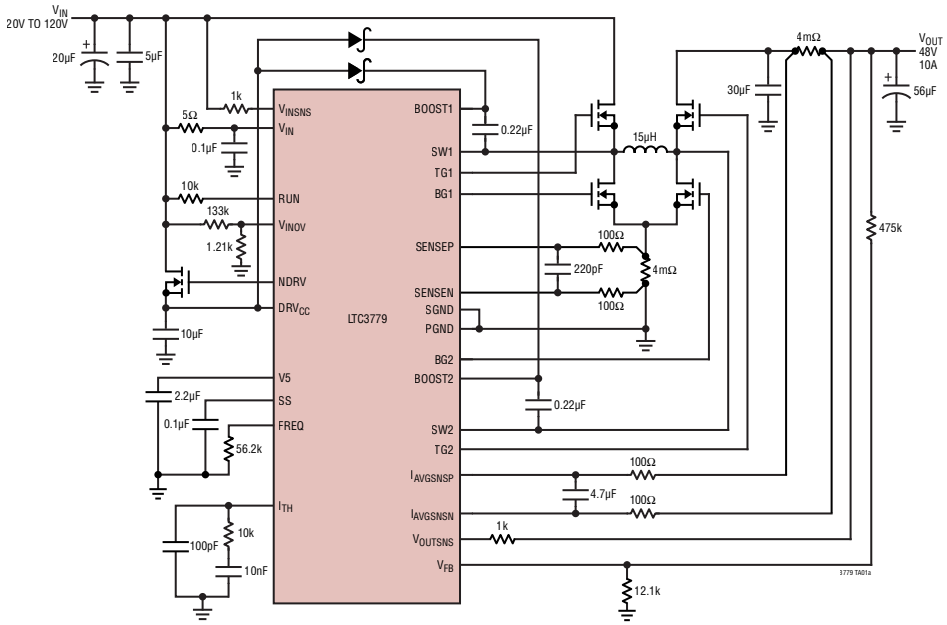
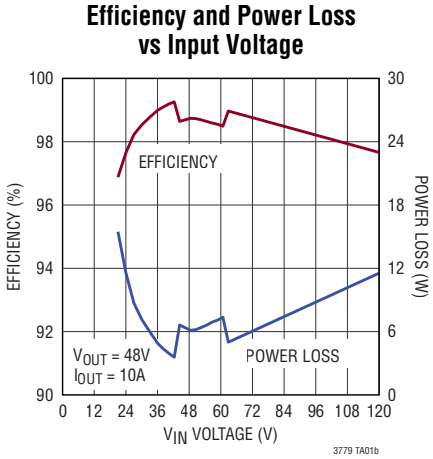
TYPICAL APPLICATION





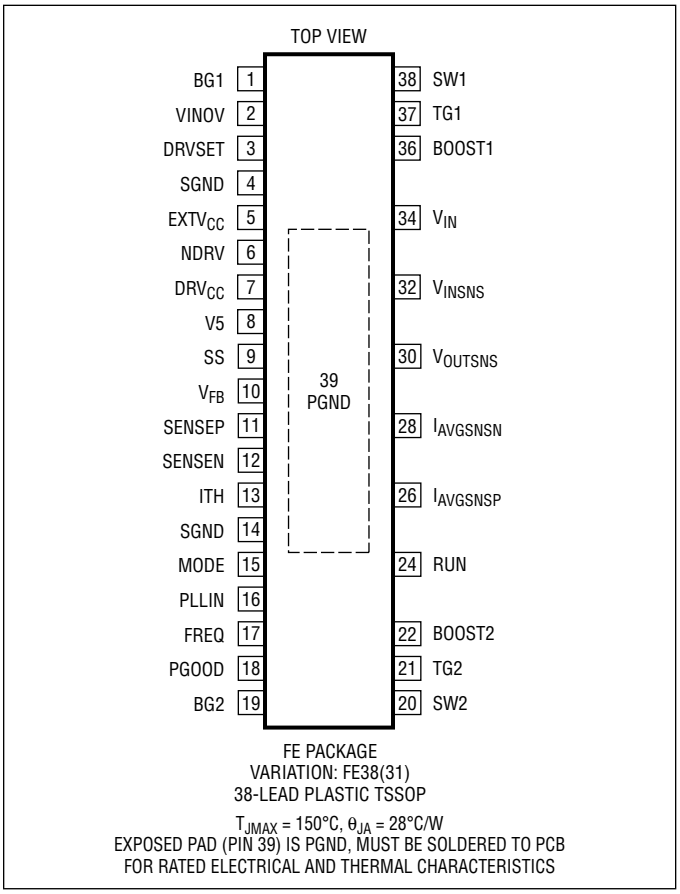
Rev A

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage (V_{IN}) ..... 150V to –0.3V
Topside Driver Voltage
BOOST1, BOOST2 ..... 161V to –0.3V
Switch Voltage SW1, SW2 ..... 150V to –5V
RUN ..... 150V to –0.3V
$I_{AVGSNSP}$, $I_{AVGSNSN}$ ..... 150V to –10V
V_{INSNS}, V_{OUTSNS} ..... 150V to –0.3V
$EXTV_{CC}$ Voltage ..... 36V to –0.3V
NDRV Voltage ..... (Note 9)
DRV_{CC} Voltage ..... 11V to –0.3V
BOOST1-SW1, BOOST2-SW2 ..... 11V to –0.3V
TG1-SW1, TG2-SW2, BG1, BG2 ..... (Note 8)
V5 Voltage ..... 6V to –0.3V
MODE, PLLIN, SS, PGOOD ..... V5 to –0.3V
ITH, FREQ, DRVSET ..... V5 to –0.3V
SENSEP, SENSEN, VINOV ..... V5 to –0.3V
V_{FB} Voltage ..... 2.7V to –0.3V
Operating Junction Temperature
Range (Notes 2, 3) ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
$EXTV_{CC}/DRV_{CC}$ Peak Current 100mA

PIN CONFIGURATION



FE PACKAGE
VARIATION: FE38(31)
38-LEAD PLASTIC TSSOP

T_{JMAX} = 150°C, θ_{JA} = 28°C/W
EXPOSED PAD (PIN 39) IS PGND, MUST BE SOLDERED TO PCB
FOR RATED ELECTRICAL AND THERMAL CHARACTERISTICS

ORDER INFORMATION

http://www.linear.com/product/LTC3779#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3779EFE#PBF	LTC3779EFE#TRPBF	LTC3779FE	38-Lead Plastic TSSOP	–40°C to 125°C
LTC3779IFE#PBF	LTC3779IFE#TRPBF	LTC3779FE	38-Lead Plastic TSSOP	–40°C to 125°C
LTC3779HFE#PBF	LTC3779HFE#TRPBF	LTC3779FE	38-Lead Plastic TSSOP	–40°C to 150°C

Consult ADI Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2), V_{IN} = 15V, V_{RUN} = 5V, V_{EXTVCC} = 0V, V_{DRVSET} = 0V, V_{VINOV} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Supply Operating Voltage Range	(Note 4)		4.5		150	V
V_{OUT}	Output Supply Operating Voltage Range			1.2		150	V
	Regulated Feedback Voltage	(Note 5); ITH Voltage = 1.4V	●	1.188	1.2	1.212	V
	Feedback Current	(Note 5)			–15	-50	nA
	Reference Voltage Line Regulation	(Note 5); V_{IN} = 7V to 100V			0.02	0.2	%
	Output Voltage Load Regulation	(Note 5); Measured in Servo Loop; ΔITH Voltage = 1.5V to 2V	●		0.01	0.2	%
	Transconductance Amplifier gm	(Note 5); ITH = 1.4V; Sink/Source 5μA			1.5		mmho
I_Q	Input DC Supply Current	(Note 6)			3.6	5.5	mA
	Shutdown	RUN = 0V			40	75	μA
	Undervoltage Lockout	V5 Ramping Up		4.1	4.35	4.6	V
		V5 Ramping Down		3.6	3.85	4.1	V
	RUN Pin ON Threshold	V_{RUN} Rising		1.1	1.2	1.3	V
	RUN Pin Hysteresis				100		mV
	RUN Pin Source Current	V_{RUN} < 1.2V			2.5		μA
	RUN Pin Hysteresis Current	V_{RUN} > 1.2V			6.5		μA
	V_{IN} Overvoltage Lockout Threshold (Rising)	V_{VINOV} Rising		1.18	1.28	1.38	V
	V_{IN} Overvoltage Hysteresis				50		mV
	SENSE Pins Current	V_{SENSEP} = V_{SENSEN} = 0				±2	μA
$I_{AVGSNSP}$ $I_{AVGSNSN}$	I_{AVGSNS} Pins Current	$V_{IAVGSNSP}$ = $V_{IAVGSNSN}$ = 10V				15	μA
	Soft-Start Charge Current	V_{SS} = 0V		4	5	6	μA
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold (Buck Region Valley Current Mode)	V_{FB} = 1V	●	70	90	110	mV
	Maximum Current Sense Threshold (Boost Region Peak Current Mode)	V_{FB} = 1V	●	120	140	160	mV
	Maximum Input / Output Average Current Sense Threshold	$V_{IAVGSNSP}$ = $V_{IAVGSNSN}$ = 10V, V_{FB} = 1V		47.5	50	52.5	mV
$DC_{(MAX, BOOST)}$	Maximum Duty Factor	% Switch C On			90		%
$DC_{ON(MIN, BOOST)}$	Minimum Duty Factor for Main Switch in Boost Operation	% Switch C On			9		%
$DC_{ON(MIN, BUCK)}$	Minimum Duty Factor for Main Switch in Buck Operation	% Switch B On			9		%
Gate Driver							
	TG Pull-Up On Resistance TG Pull-Down On Resistance	V_{DRVCC} = 9V			3.1 1.3		Ω
	BG Pull-Up On Resistance BG Pull-Down On Resistance	V_{DRVCC} = 9V			5.5 3		Ω
	TG Transition Time: Rise Time Fall Time	V_{DRVCC} = 9V (Note 7) C_{LOAD} = 3300pF			60		ns
	BG Transition Time: Rise Time Fall Time	V_{DRVCC} = 9V (Note 7) C_{LOAD} = 3300pF			60		ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2), V_{IN} = 15V, V_{RUN} = 5V, V_{EXTVCC} = 0V, V_{DRVSET} = 0V, V_{VINOV} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Top Gate Off to Bottom Gate On Delay Synchronous Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver, V_{DRVSET} = V5			60		ns
	Bottom Gate Off to Top Gate On Delay Top Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver, V_{DRVSET} = V5			60		ns
DRV_{CC} LDO Regulator							
V_{DRVCC}	DRV_{CC} Regulation Voltage from NDRV Regulator	NDRV Driving External NFET, V_{EXTVCC} = 0V 7V < V_{IN} < 150V, V_{DRVSET} = 0V 8V < V_{IN} < 150V, V_{DRVSET} = 1/4 V_{V5} 9V < V_{IN} < 150V, V_{DRVSET} = Float 10V < V_{IN} < 150V, V_{DRVSET} = 3/4 V_{V5} 11V < V_{IN} < 150V, V_{DRVSET} = V_{V5}		 5.8 6.8 7.8 8.75 9.65	 6.1 7.1 8.1 9.1 10	 6.4 7.4 8.4 9.45 10.35	 V V V V V
	DRV_{CC} Regulation Voltage from Internal V_{IN} LDO	V_{NDRV} = V_{DRVCC}, V_{EXTVCC} = 0V 7V < V_{IN} < 150V, V_{DRVSET} = 0V 8V < V_{IN} < 150V, V_{DRVSET} = 1/4 V_{V5} 9V < V_{IN} < 150V, V_{DRVSET} = Float 10V < V_{IN} < 150V, V_{DRVSET} = 3/4 V_{V5} 11V < V_{IN} < 150V, V_{DRVSET} = V_{V5}		 5.5 6.5 7.5 8.45 9.15	 5.8 6.8 7.8 8.8 9.5	 6.1 7.1 8.1 9.15 9.85	 V V V V V
	DRV_{CC} Load Regulation from V_{IN} LDO	I_{CC} = 0mA to 50mA, V_{EXTVCC} = 0V			0.5	2	%
V_{EXTVCC}	DRV_{CC} Regulation Voltage from Internal $EXTV_{CC}$ LDO	7V < V_{EXTVCC} < 30V, V_{DRVSET} = 0V 8V < V_{EXTVCC} < 30V, V_{DRVSET} = 1/4 V_{V5} 9V < V_{EXTVCC} < 30V, V_{DRVSET} = Float 10V < V_{EXTVCC} < 30V, V_{DRVSET} = 3/4 V_{V5} 11V < V_{EXTVCC} < 30V, V_{DRVSET} = V_{V5}		5.8 6.8 7.8 8.75 9.65	6.1 7.1 8.1 9.1 10	6.4 7.4 8.4 9.45 10.35	V V V V V
	DRV_{CC} Load Regulation from Internal $EXTV_{CC}$ LDO	I_{CC} = 0mA to 50mA, V_{EXTVCC} = 12V V_{DRVSET} = 0V			0.5	2	%
	$EXTV_{CC}$ LDO Switchover Voltage	$EXTV_{CC}$ Ramping Positive			DRV_{CC} – 0.5		V
	$EXTV_{CC}$ Hysteresis	% of DRV_{CC} Regulation Voltage			10		%
V5 Linear Regulator							
	V5 Regulation Voltage	6V < V_{DRVCC} < 10V		5.3	5.5	5.7	V
	V5 Load Regulation	I_{V5} = 0mA to 20mA, V_{DRVCC} = 10V			0.5	1	%
Oscillator and Phase-Locked Loop							
	Nominal Frequency	R_{FREQ} = 68.5kΩ		225	250	275	kHz
	Low Fixed Frequency	R_{FREQ} ≤ 20kΩ		30	40	50	kHz
	High Fixed Frequency	R_{FREQ} = 135kΩ		450	500	550	kHz
	PLLIN Input Threshold	V_{PLLIN} Rising V_{PLLIN} Falling		2		 1.2	V V
	PLLIN Input Resistance				200		kΩ
	Synchronizable Oscillator Frequency	PLLIN = External Clock	●	50		600	kHz
I_{FREQ}	Frequency Setting Current		●	18	20	22	µA
PGOOD Output							
	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.1	0.3	V
	PGOOD Leakage Current	V_{PGOOD} = 5.5V				±1	µA
	PGOOD Trip Level	V_{FB} with Respect to Set Regulated Voltage					
		V_{FB} Ramping Negative			–10		%
		V_{FB} Ramping Positive			10		%
	PGOOD delay	V_{PGOOD} High to Low			125		µs

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3779 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3779E is guaranteed to meet performance specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3779I is guaranteed over the full –40°C to 125°C operating junction temperature range. The LTC3779H is guaranteed over the full –40°C to 150°C operating junction temperature range. High junction temperature degrades operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA}),$$

where θ_{JA} = 28°C/W for the TSSOP package.

Note 3: This IC includes over temperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

Note 4: When biased from an auxiliary supply through the $EXTV_{CC}$ pin, the LTC3779 can operate from a V_{IN} voltage lower than 4.5V. Otherwise the minimum V_{IN} operational voltage is 4.5V after startup.

Note 5: The LTC3779 is tested in a feedback loop that servos V_{ITH} to a specified voltage and measures the resultant V_{FB}.

Note 6: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

Note 7: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

Note 8: Do not apply a voltage or current source to these pins. They must be connected to capacitive loads only, otherwise permanent damage may occur. These pins are rated for an absolute maximum voltage of –0.3V to 11V.

Note 9: Do not apply a voltage or current source to the NDRV pin, other than tying NDRV to DRV_{CC} when not used. If used it must be connected to capacitive loads only (see DRVCC Regulator in the Applications Information section), otherwise permanent damage may occur.

TYPICAL PERFORMANCE CHARACTERISTICS

Efficiency and Power Loss vs Load Current and Input Voltage Continuous Mode

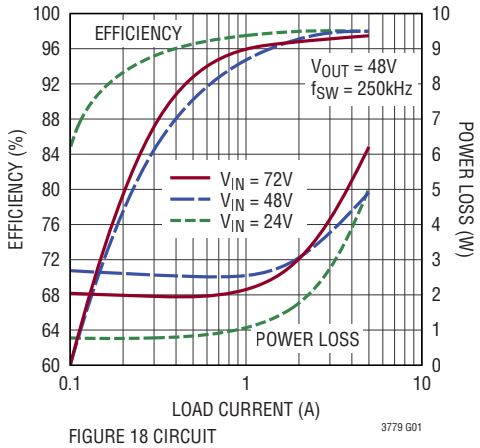
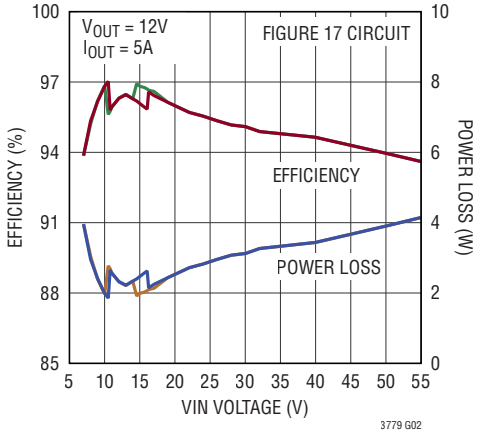
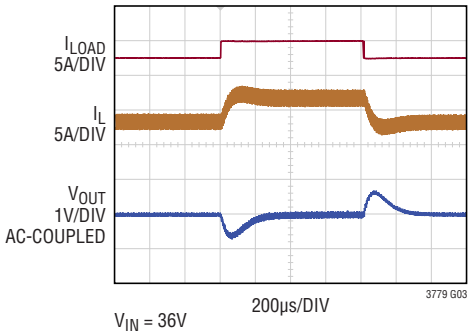


FIGURE 18 CIRCUIT

Efficiency and Power Loss vs Input Voltage

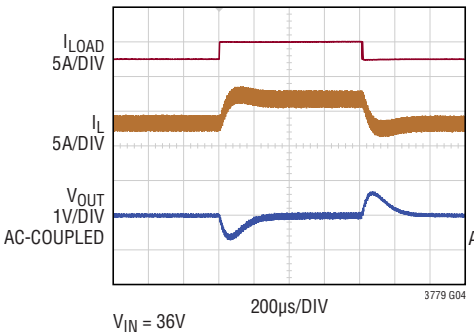


Load Step Boost Region Continuous Mode



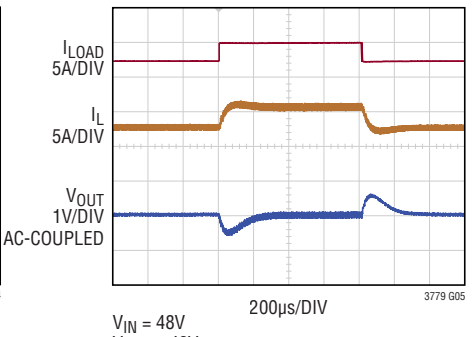
V_{IN} = 36V
V_{OUT} = 48V

Load Step Boost Region Pulse-Skipping Mode



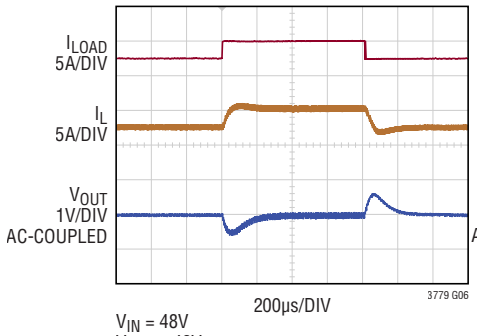
V_{IN} = 36V
V_{OUT} = 48V

Load Step Buck-Boost Region Continuous Mode



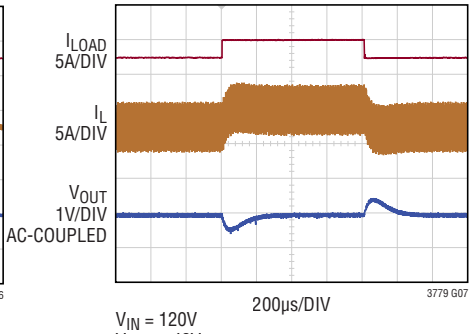
V_{IN} = 48V
V_{OUT} = 48V

Load Step Buck-Boost Region Pulse-Skipping Mode



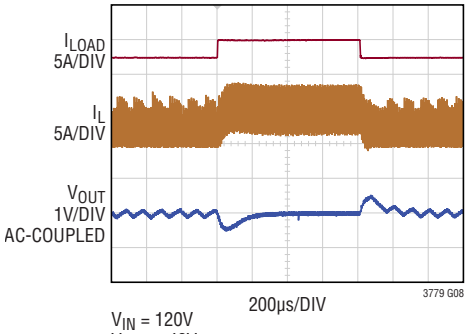
V_{IN} = 48V
V_{OUT} = 48V

Load Step Buck Region Continuous Mode



V_{IN} = 120V
V_{OUT} = 48V

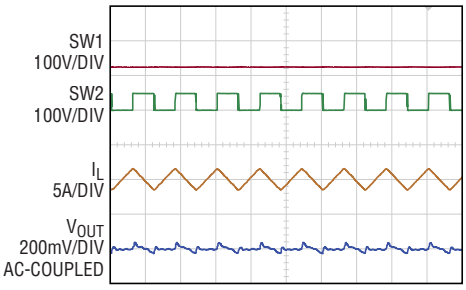
Load Step Buck Region Pulse-Skipping Mode



V_{IN} = 120V
V_{OUT} = 48V

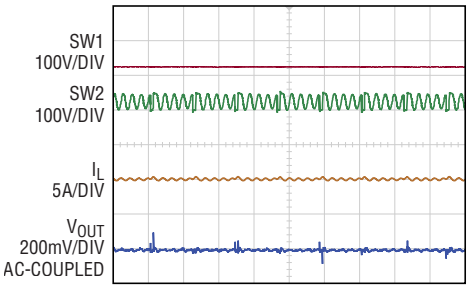
TYPICAL PERFORMANCE CHARACTERISTICS

Forced Continuous Mode Boost Region



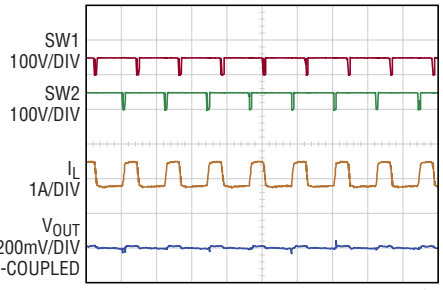
V_{IN} = 24V
V_{OUT} = 48V
I_{LOAD} = 0A

Pulse-Skipping Mode Boost Region



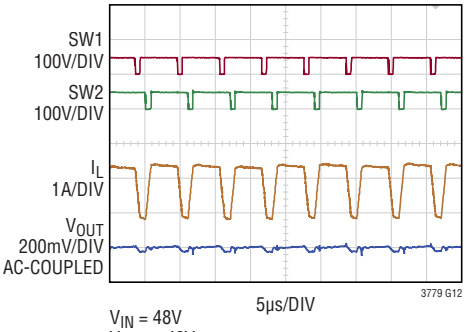
V_{IN} = 24V
V_{OUT} = 48V
I_{LOAD} = 0A

Forced Continuous Mode Buck-Boost Region



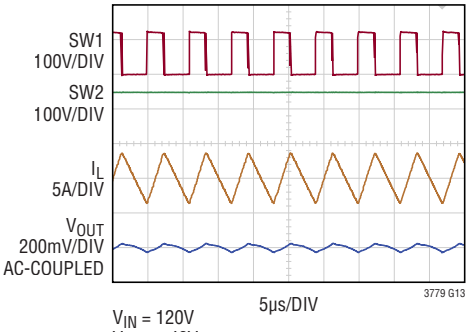
V_{IN} = 48V
V_{OUT} = 48V
I_{LOAD} = 0A

Pulse-Skipping Mode Buck-Boost Region



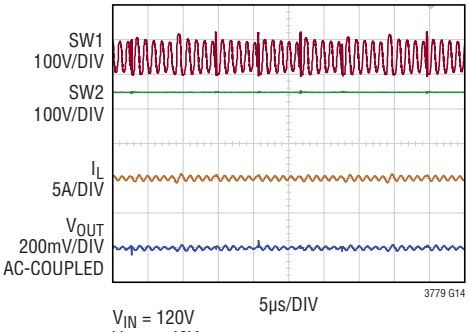
V_{IN} = 48V
V_{OUT} = 48V
I_{LOAD} = 0A

Forced Continuous Mode Buck Region



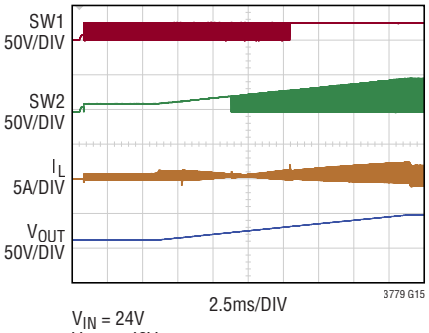
V_{IN} = 120V
V_{OUT} = 48V
I_{LOAD} = 0A

Pulse-Skipping Mode Buck Region



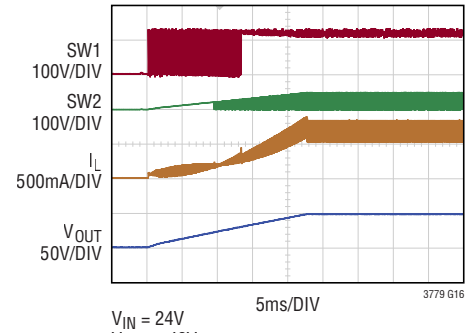
V_{IN} = 120V
V_{OUT} = 48V
I_{LOAD} = 0A

Start-Up from RUN Forced Continuous Mode Pre-Biased Output



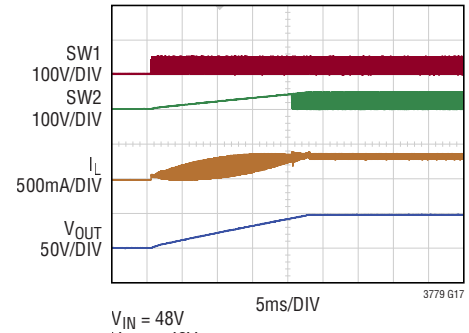
V_{IN} = 24V
V_{OUT} = 48V
V_{OUT} PRE-BIAS = 12V
200mA LOAD

Start-Up Forced Continuous Mode Boost Region



V_{IN} = 24V
V_{OUT} = 48V
15Ω RESISTIVE LOAD

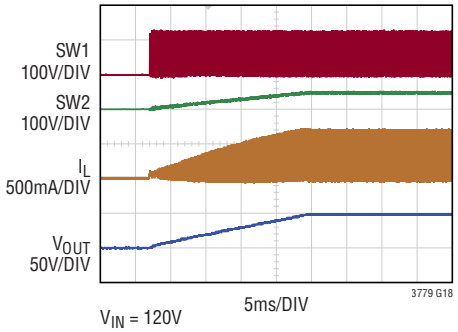
Start-Up Forced Continuous Mode Buck-Boost Region



V_{IN} = 48V
V_{OUT} = 48V
15Ω RESISTIVE LOAD

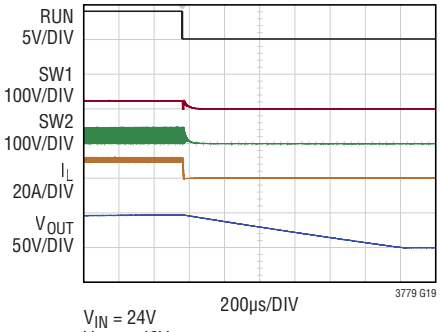
TYPICAL PERFORMANCE CHARACTERISTICS

Start-Up Forced Continuous Mode Buck Region



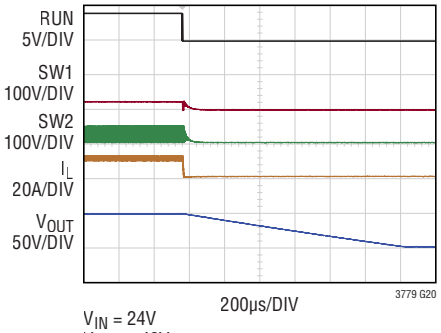
V_{IN} = 120V
V_{OUT} = 48V
15Ω RESISTIVE LOAD

Shutdown from RUN Forced Continuous Mode Boost Region



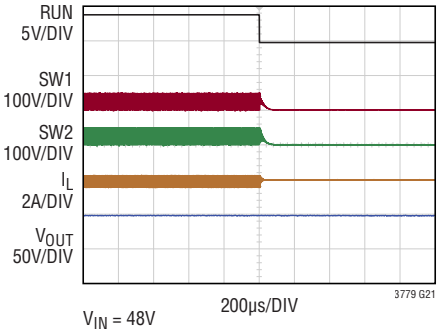
V_{IN} = 24V
V_{OUT} = 48V
5A LOAD

Shutdown from RUN Pulse-Skipping Mode Boost Region



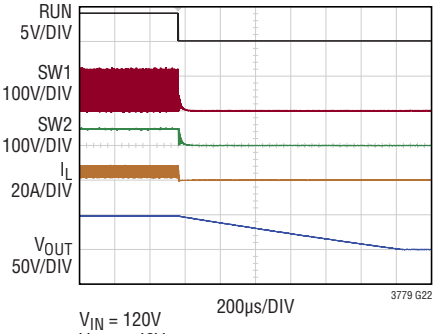
V_{IN} = 24V
V_{OUT} = 48V
5A LOAD

Shutdown from RUN Forced Continuous Mode Buck-Boost Region



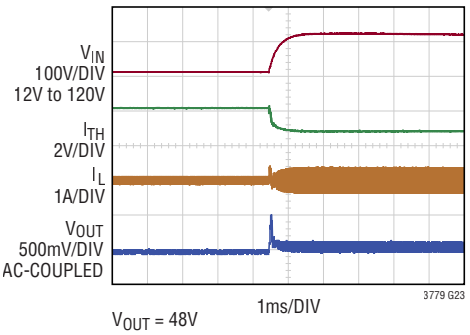
V_{IN} = 48V
V_{OUT} = 48V
NO LOAD

Shutdown from RUN Forced Continuous Mode Buck Region



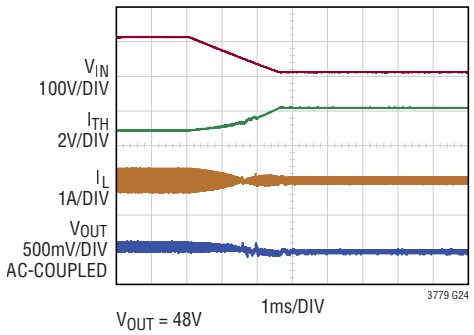
V_{IN} = 120V
V_{OUT} = 48V
I_{LOAD} = 5A

Line Transient Rising Edge



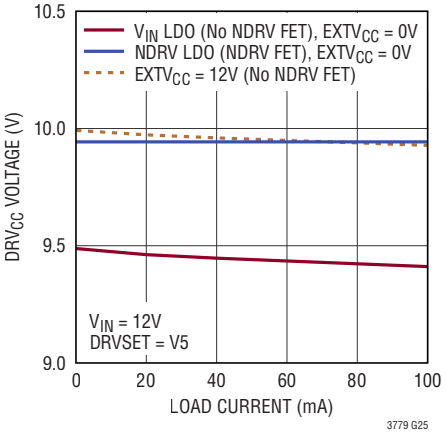
V_{OUT} = 48V

Line Transient Falling Edge

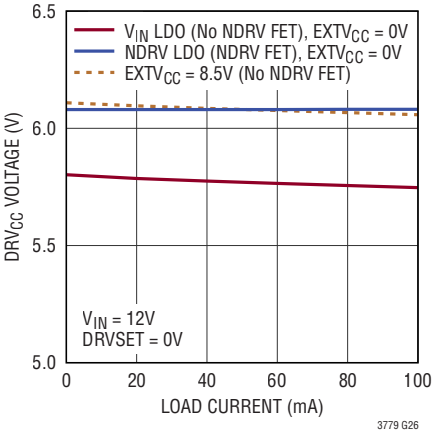


V_{OUT} = 48V

DRV_{CC} vs Load Current

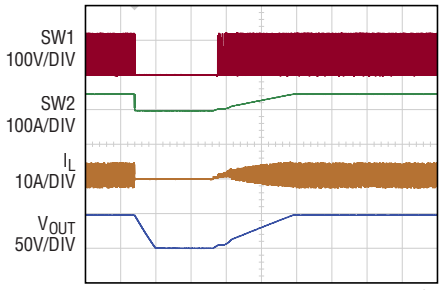


DRV_{CC} vs Load Current



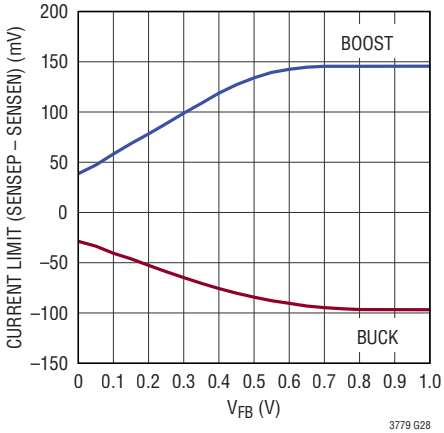
TYPICAL PERFORMANCE CHARACTERISTICS

VINOV Transient Forced Continuous Mode Buck Region

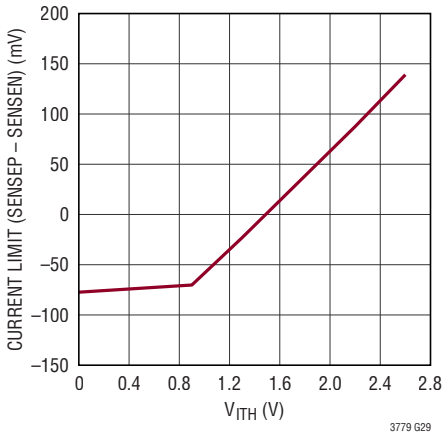


V_{IN} = 120V
V_{OUT} = 48V
50Ω RESISTIVE LOAD

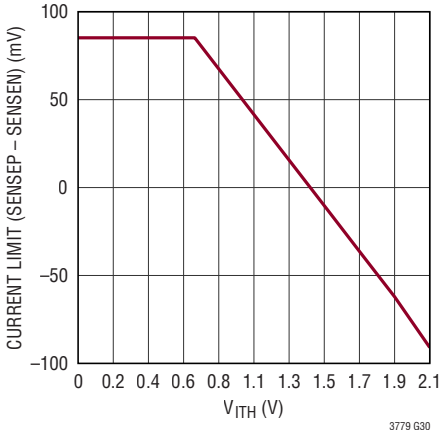
Current Foldback Limit



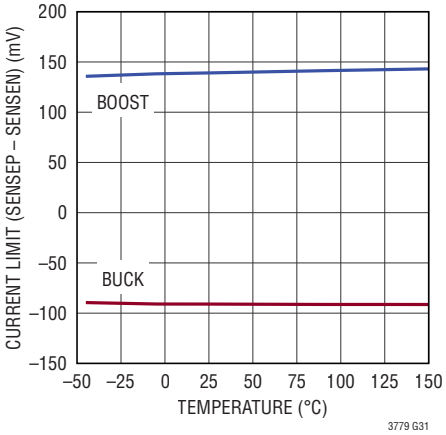
Peak Current Threshold vs V_{ITH} (Boost)



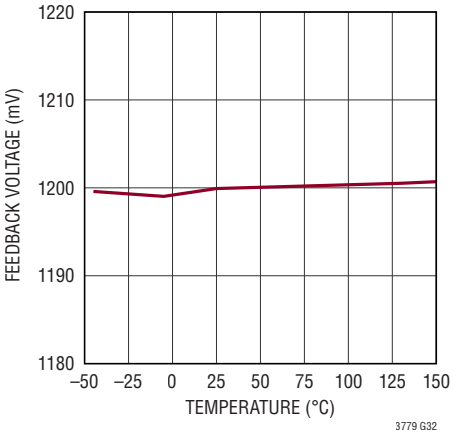
Valley Current Threshold vs V_{ITH} (Buck)



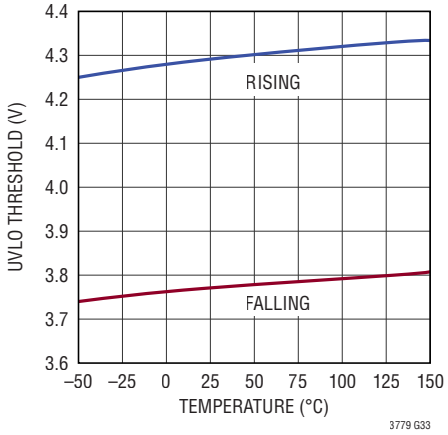
Maximum Current Limit vs Temperature



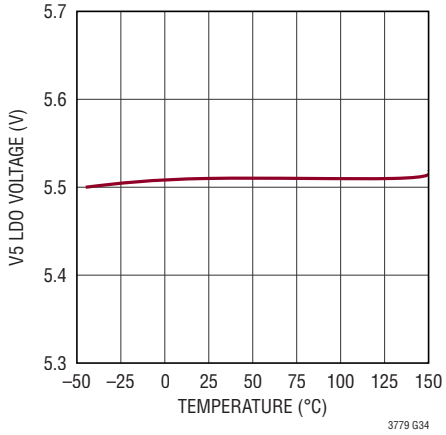
Regulated Feedback Voltage vs Temperature



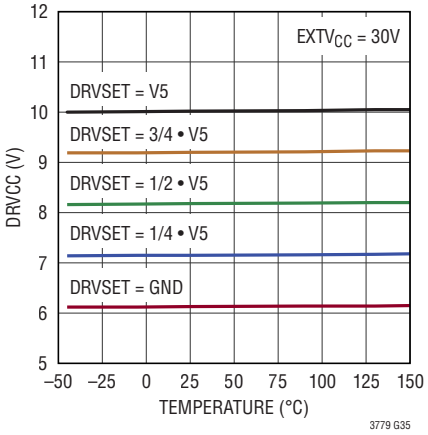
Undervoltage Lockout Threshold (V5) vs Temperature



V5 Low Dropout Regulation Voltage vs Temperature

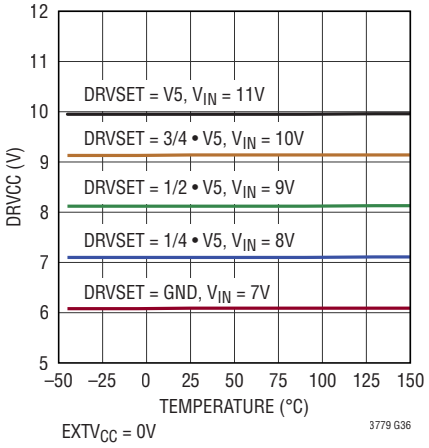


$EXTV_{CC}$ LDO vs Temperature



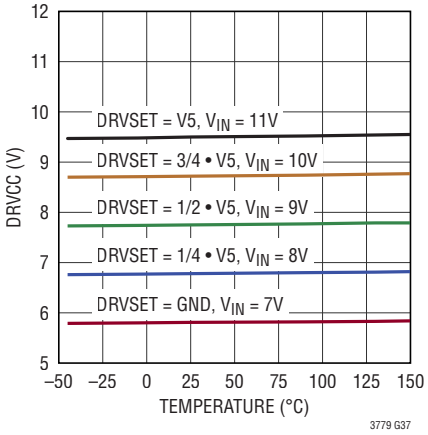
TYPICAL PERFORMANCE CHARACTERISTICS

NDRV LDO vs Temperature

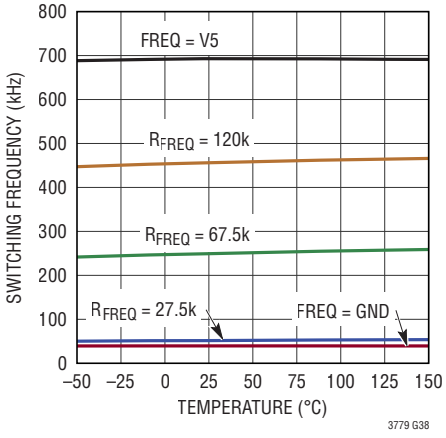


EXTVCC = 0V

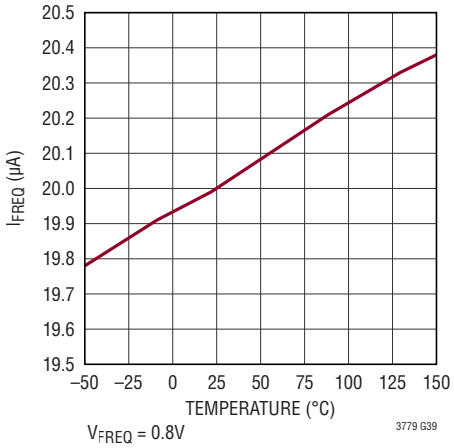
VIN LDO vs Temperature



Oscillator Frequency vs Temperature

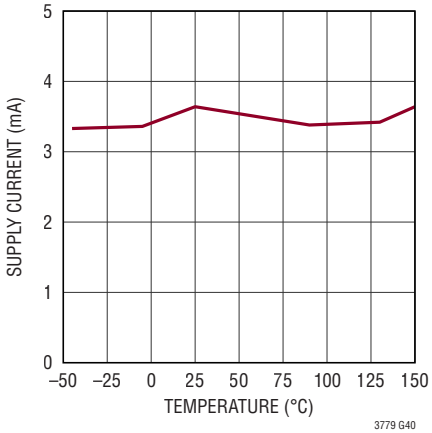


Frequency Setting Current vs Temperature

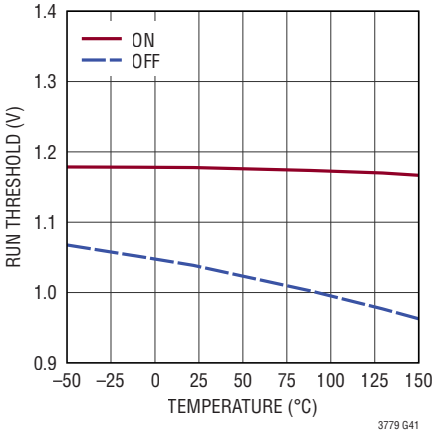


VFREQ = 0.8V

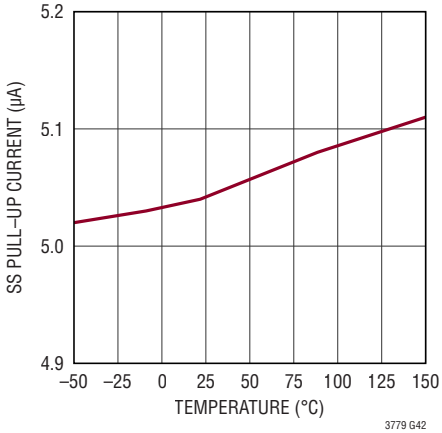
Input Supply Current vs Temperature



RUN Threshold vs Temperature



Soft-Start Pull-Up Current vs Temperature



PIN FUNCTIONS

BG1/BG2 (Pins 1 and 19): Bottom Gate Driver Outputs. This pin drives the gate(s) of the bottom N-Channel MOSFET between PGND to DRV_{CC}.

VINOV (Pin 2): Connect to the input supply through a resistor divider to set the over-voltage lockout level. A voltage on this pin above 1.28V disables all switching, and the top GATE pins are held low, the bottom GATE pins are held high, and V_{OUT} is disconnected from V_{IN}. DRV_{CC} and V5 regulation is maintained during an over-voltage event. Normal operation resumes when the voltage on this pin decreases below 1.23V. Exceeding the VINOV lockout threshold triggers a soft-start reset, resulting in a graceful recovery from an input supply transient. Tie this pin to ground if the overvoltage function is not used.

DRVSET (Pin 3): Sets the regulated output voltage of the DRV_{CC} linear regulator from 6V to 10V in 1V increments. Tying this pin to SGND sets DRV_{CC} to 6V, tying it to 1/4•V5 sets DRV_{CC} to 7V, while floating this pin sets DRV_{CC} to 8V, tying it to 3/4•V5 sets DRV_{CC} to 9V, and tying it to V5 sets DRV_{CC} to 10V.

SGND (Pins 4 and 14): Signal ground. All feedback and soft-start connections should return to SGND. For optimum load regulation, the SGND pin should be Kelvin connected to the PCB location between the negative terminals of the output capacitors.

$EXTV_{CC}$ (Pin 5): External Power Input to an Internal LDO Connected to DRV_{CC}. When the voltage on this pin is greater than the DRV_{CC} LDO setting minus 500mV, this LDO bypasses the internal LDO powered from V_{IN} or the external LDO connected to NDRV. Tie this pin to ground if the $EXTV_{CC}$ is not used.

NDRV (Pin 6): Drive Output for External Pass Device of the LDO Regulator connected to DRV_{CC}. Connect to the gate of an external NMOS pass device. To disable the external linear regulator, tie NDRV to DRV_{CC}. An internal charge pump can drive NDRV above V_{IN} for low dropout performance.

DRV_{CC} (Pin 7): Output of the Internal or External Low Dropout Regulator. The gate drivers are powered from this voltage source. The DRV_{CC} voltage is set by the DRVSET pin. A low ESR 4.7µF (X5R or better) ceramic bypass capacitor should be connected between DRV_{CC} and PGND, as close as possible to the IC. Do not use the DRV_{CC} pin for any other purpose.

V5 (Pin 8): Output of the Internal 5.5V Low Dropout Regulator. The control circuits are powered from this voltage. Bypass this pin to SGND with a minimum of 4.7µF low ESR tantalum or ceramic capacitor, as close as possible to the IC.

SS (Pin 9): Soft-Start Input. The voltage ramp rate at this pin sets the voltage ramp rate of the regulated voltage. This pin has a 5µA pull-up current. A capacitor to ground at this pin sets the ramp time to final regulated output voltage.

V_{FB} (Pin 10): Error Amplifier Input. The FB pin should be connected through a resistive divider network to V_{OUT} to set the output voltage.

SENSEP (Pin 11): The positive input to the differential current comparator. This pin is normally connected to a sense resistor at the source of the power MOSFET. The ITH pin voltage and controlled offsets between the SENSEP and SENSEN pins, in conjunction with R_{SENSE}, set the current trip threshold.

SENSEN (Pin 12): The negative input to the differential current sense comparator. This pin is normally connected to the ground side of the sense resistor.

ITH (Pin 13): Error Amplifier Output. The current comparator trip threshold increases with the ITH control voltage. The ITH pin is also used for compensating the control loop of the converter.

MODE (Pin 15): Mode Selection pin. Tying this pin to SGND or below 0.8V enables forced continuous mode. Tying it to V5 enables pulse-skipping mode.

PIN FUNCTIONS

PLLIN (Pin 16): External Synchronization Input to Phase Detector. For external sync, apply a clock signal to this pin and the internal PLL will synchronize the internal oscillator to the clock. The PLL compensation network is integrated into the IC. When synchronized to an external clock, the regulator can operate either in forced continuous or pulse-skipping mode. The mode of operation is controlled by the setting on the MODE pin.

FREQ (Pin 17): The frequency control pin for the internal VCO. Frequencies between 50kHz and 600kHz can be programmed by using a resistor between FREQ and SGND. The resistor and an internal 20µA source current create a voltage used by the internal oscillator to set the frequency.

PGOOD (Pin 18): Fault indicator Output. Open-drain output that pulls to ground when the voltage on the V_{FB} pin is not within ±10% of its set point.

SW1, SW2 (Pins 38 and 20): Switch Node Connections to the Inductors.

TG1, TG2 (Pin 37 and 21): High Current Gate Drives for Top N-Channel MOSFETs. These are the outputs of floating high side drivers with a voltage swing equal to DRV_{CC} superimposed on the switch node voltage SW.

BOOST1, BOOST2 (Pin 36 and 22): Boosted Floating Driver Supplies. The (+) terminal of the bootstrap capacitor connects to this pin. This pin swings from a diode drop below DRV_{CC} up to V_{IN} + DRV_{CC}.

RUN (Pin 24): Enable Control Input. A voltage above 1.2V turns on the IC. There is a 2.5µA pull-up current on this pin. Once the RUN pin rises above the 1.2V threshold the pull-up current increases to 6.5µA. Forcing this pin below 1.1V shuts down the controller. This pin can be tied to V_{IN} for always-on operation. Do not float this pin.

$I_{AVGSNSP}$ (Pin 26): The positive input to the Input / Output Average Current Sense Amplifier.

$I_{AVGSNSN}$ (Pin 28): The negative input to the Input / Output Average Current Sense Amplifier. Short $I_{AVGSNSP}$ and $I_{AVGSNSN}$ pins together, and tie them to V5, if this average current loop function is not used.

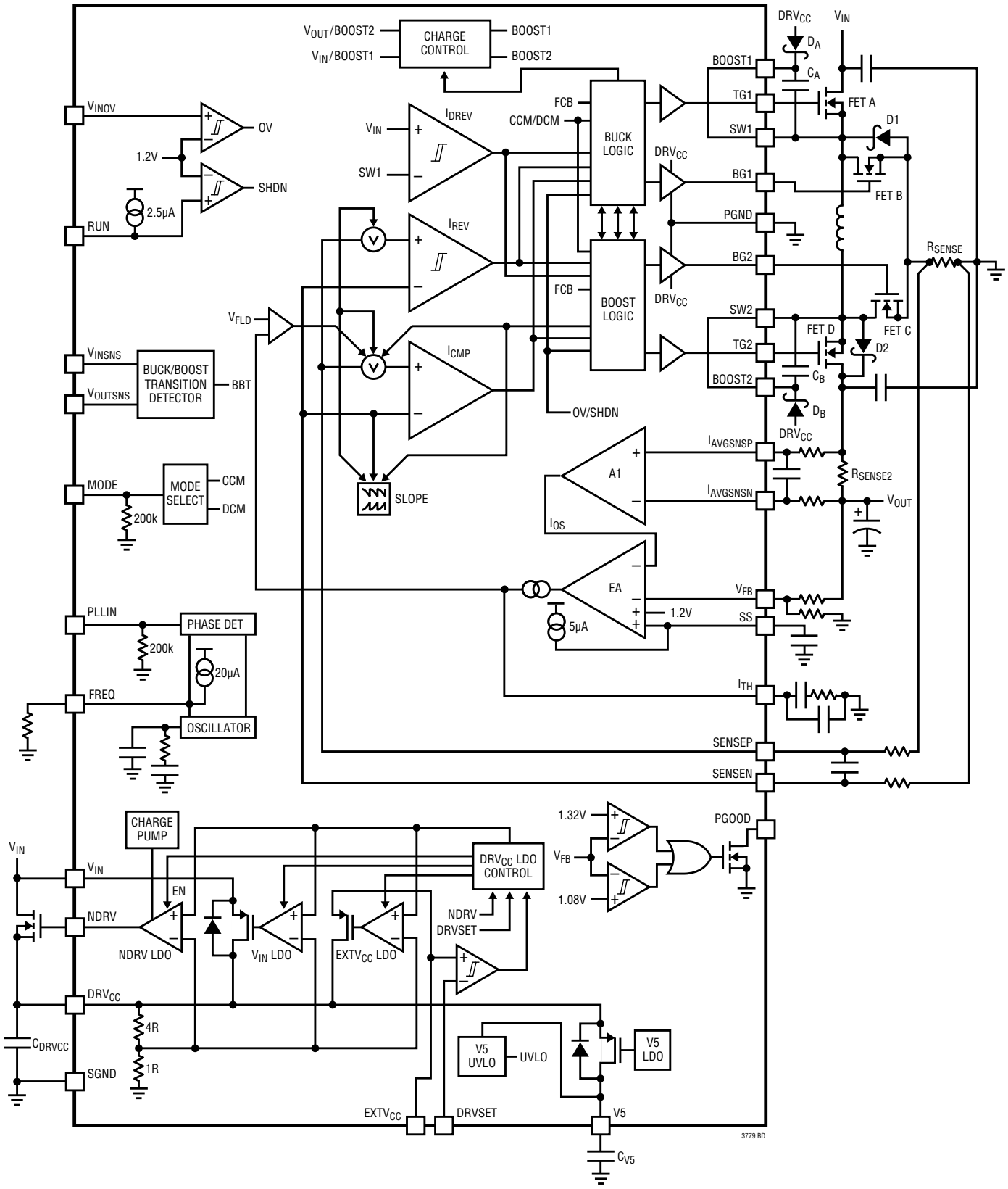
V_{OUTSNS} (Pin 30): V_{OUT} Sense Input to the Buck-Boost Transition comparator. Connect this pin to the drain of the top N-channel MOSFET on the output side through a 1kΩ resistor.

V_{INSNS} (Pin 32): V_{IN} Sense Input to the Buck-Boost Transition comparator. Connect this pin to the drain of the top N-channel MOSFET on the input side.

V_{IN} (Pin 34): Main Supply Pin. A bypass capacitor should be tied between this pin and the PGND pin.

PGND (Exposed Pad Pin 39): Driver Power Ground. Connects to the (–) terminal of C_{IN}, C_{OUT} and R_{SENSE}. The exposed pad must be soldered to PCB ground for electrical contact and rated thermal performance.

BLOCK DIAGRAM



OPERATION

MAIN CONTROL LOOP

The LTC3779 is a current mode controller that provides an output voltage above, equal to or below the input voltage. The ADI proprietary topology and control architecture employs a current-sensing resistor. The inductor current is controlled by the voltage on the I_{TH} pin, which is the output of the error amplifier EA. The V_{FB} pin receives the voltage feedback signal, which is compared to the internal reference voltage by the EA. If the input/output current regulation loop is implemented, the sensed inductor current is controlled by either the sensed feedback voltage or the input/output current.

DRV_{CC}/$EXTV_{CC}$/V5 Power

Power for the top and bottom MOSFET drivers is derived from the DRV_{CC} pin. The DRV_{CC} supply voltage can be programmed from 6V to 10V in 1V steps using the DRVSET pin. Two separate LDOs (low dropout linear regulators) can provide power from V_{IN} to DRV_{CC}. The internal V_{IN} LDO uses an internal P-channel pass device between the V_{IN} and DRV_{CC} pins. To prevent high on-chip power dissipation in high input voltage applications, the LTC3779 also includes an NDRV LDO that utilizes the NDRV pin to supply power to DRV_{CC} by driving the gate of an external N-channel MOSFET acting as a linear regulator with its source connected to DRV_{CC} and drain connected to V_{IN}. The NDRV LDO includes an internal charge pump that allows NDRV to be driven above V_{IN} for low dropout performance.

When the $EXTV_{CC}$ pin is tied to a voltage below its switchover voltage (DRV_{CC}–500mV), the V_{IN} and NDRV LDOs are enabled and one of them supplies power from V_{IN} to DRV_{CC}. The V_{IN} LDO has a slightly lower regulation point than the NDRV LDO. If the NDRV LDO is being used with an external N-channel MOSFET, the gate of the MOSFET tied to the NDRV pin is driven such that DRV_{CC} regulates above the V_{IN} LDO regulation point, causing all DRV_{CC} current to flow through the external N-channel MOSFET, and bypassing the internal V_{IN} LDO pass device. If the NDRV LDO is not being used, all DRV_{CC} current flows through the internal P-channel pass device between the V_{IN} and DRV_{CC} pins.

If $EXTV_{CC}$ is taken above its switchover voltage, the V_{IN} and NDRV LDOs are turned off and an $EXTV_{CC}$ LDO is turned on. Once enabled, the $EXTV_{CC}$ LDO supplies power from $EXTV_{CC}$ to DRV_{CC}. Using the $EXTV_{CC}$ pin allows the DRV_{CC} power to be derived from a high efficiency external source such as the LTC3779 switching regulator output.

Most of the internal circuitry is powered from the V5 rail that is generated by an internal linear regulator from DRV_{CC}. The V5 pin needs to be bypassed with a 1µF to 10µF external capacitor between V5 and SGND. This pin provides a 5.5V output that can supply up to 20mA of current. See the Applications Information section for more details.

Top MOSFET DRIVER and Internal Charge Path

Each of the two top MOSFET drivers is biased from its floating bootstrap capacitor, which is normally recharged by DRV_{CC} through an external diode when the top MOSFET is turned off and when SW goes low. When the LTC3779 operates exclusively in the buck or boost regions, one of the top MOSFETs is constantly on. An internal charge path, from V_{OUT} and BOOST2 to BOOST1 or from V_{IN} and BOOST1 to BOOST2, charges the bootstrap capacitor so that the top MOSFET can be kept on. However, if a high leakage external diode is used such that the internal charge path cannot provide sufficient charge to the external bootstrap capacitor, an internal UVLO comparator, which constantly monitors the drop across the capacitor, will sense the (BOOST – SW) voltage when it is below the boost capacitor refresh threshold. This will turn off its top MOSFET for about one-twelfth of the clock period every four cycles to allow the bootstrap capacitor to recharge. The boost capacitor refresh threshold varies with the DRVSET pin setting.

Shutdown and Start-Up

The LTC3779 can be shut down by pulling the RUN pin low. Pulling RUN below 1.1V shuts down the main control loop for the controller and most internal circuits, including the DRV_{CC} and V5 regulators. Releasing RUN allows an internal 2.5µA current to pull-up the pin and enable the controller. When RUN is above the accurate threshold of 1.2V, the internal LDO will power up DRV_{CC}. At the same

OPERATION

time, a 6.5µA pull-up current will kick in to provide more RUN pin hysteresis. The RUN pin may be externally pulled up or driven directly by logic. The RUN pin can tolerate up to 150V (absolute maximum), so it can be conveniently tied to V_{IN} in always-on applications where the controller is enabled continuously and never shut down. The RUN pin will have no internal pull-up current when externally driven to a voltage above 4V.

Soft-Start

The start-up of the controller's output voltage V_{OUT} is controlled by the voltage on the SS pin. When the voltage on the SS pin is less than the 1.2V internal reference, the LTC3779 regulates the V_{FB} voltage to the SS voltage instead of the 1.2V reference. This allows the SS pin to be used to program soft-start by connecting an external capacitor from the SS pin to SGND. An internal 5µA pull-up current charges this capacitor, creating a voltage ramp on the SS pin. As the SS voltage rises linearly from 0V to 1.2V (and beyond), the output voltage V_{OUT} rises smoothly from zero to its final value. When RUN is pulled low to disable the controller, or during an overvoltage event on the V_{IN} input supply or during an overtemperature shutdown event, or when V5 drops below its undervoltage lockout threshold of 3.85V, the SS pin is pulled low by an internal MOSFET. When in undervoltage lockout, the controller is disabled and the external MOSFETs are held off.

Certain applications can require the start-up of the converter into a non-zero load voltage, where residual charge is stored on the V_{OUT} capacitor at the onset of converter switching. In order to prevent the V_{OUT} from discharging under these conditions, the part will be forced into discontinuous mode of operation until the SS voltage crosses V_{FB} or 1.32V, whichever is lower.

Power Switch Control

Figure 1 shows a simplified diagram of how the four power switches are connected to the inductor, V_{IN}, V_{OUT} and GND. Figure 2 shows the regions of operation for the LTC3779 as a function of $V_{OUT} - V_{IN}$ or switch duty cycle, DC. The power switches are properly controlled so the transfer between regions is continuous. Hysteresis is added to prevent chattering when transitioning between regions.

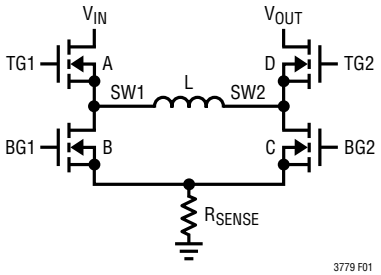


Figure 1. Simplified Diagram of the Output Switches

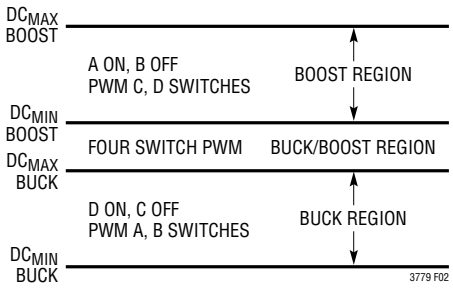


Figure 2. Operating Region vs Duty Cycle

Buck Region ($V_{IN} >> V_{OUT}$)

When V_{IN} is significantly higher than V_{OUT}, the part will run in the buck region. In this region switch C is always off. At the start of every cycle, synchronous switch B is turned on first. Inductor current is sensed when synchronous switch B is turned on. After the sensed inductor valley current falls below a reference voltage, which is proportional to V_{ITH}, synchronous switch B is turned off and switch A is turned on for the remainder of the cycle. Switches A and B will alternate, behaving like a typical synchronous buck regulator. The duty cycle of Switch A increases until the maximum duty cycle of the converter reaches $DC_{(MAX_BUCK)}$, given by:

$$DC_{(MAX,BUCK)} = \left(1 - \frac{1}{12}\right) \bullet 100\% = 91.67\%$$

OPERATION

Figure 3 shows the typical buck region waveforms. If V_{IN} approaches V_{OUT}, the buck-boost region is reached.

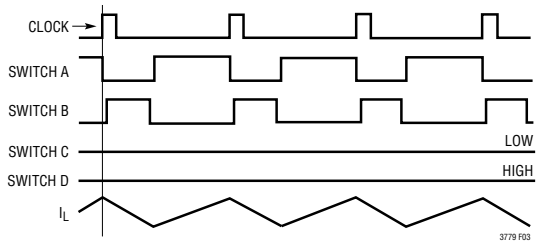
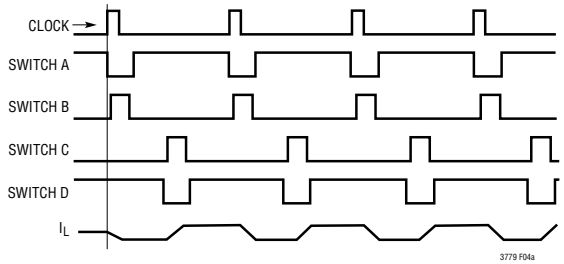


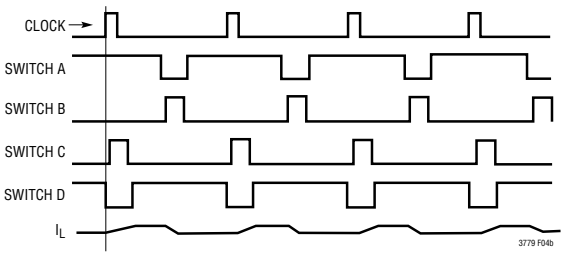
Figure 3. Buck Region (V_{IN} >> V_{OUT})

Buck-Boost Region (V_{IN} ≈ V_{OUT})

When V_{IN} is close to V_{OUT}, the controller enters the buck-boost region. Figure 4 shows the typical waveforms in this region. At the beginning of a clock cycle, if the controller starts with B and D on, the controller first operates as if in the buck region. When I_{CMP} trips, switch B is turned off, and switch A is turned on. At 120° clock phase, switch C is turned on. The LTC3779 starts to operate as a boost until I_{CMP} trips. Then, switch D is turned on for the remainder of the clock period. If the controller starts with switches A and C on, the controller first operates as a boost, until I_{CMP} trips and switch D is turned on. At 120°, switch B is turned on, making it operate as a buck. Then, I_{CMP} trips, turning switch B off and switch A on for the remainder of the clock period.



(4a) Buck-Boost Region (V_{IN} ≥ V_{OUT})



(4b) Buck-Boost Region (V_{IN} ≤ V_{OUT})

Figure 4. Buck-Boost Region

Boost Region (V_{IN} << V_{OUT})

Switch A is always on and synchronous switch B is always off in the boost region. In every cycle, switch C is turned on first. Inductor current is sensed when synchronous switch C is turned on. After the sensed inductor peak current exceeds what the reference voltage demands, which is proportional to V_{ITH}, switch C is turned off and synchronous switch D is turned on for the remainder of the cycle. Switches C and D will alternate, behaving like a typical synchronous boost regulator.

The duty cycle of switch C decreases until the minimum duty cycle of the converter reaches $DC_{(MIN,BOOST)}$, given by:

$$DC_{(MIN,BOOST)} = \left(\frac{1}{12}\right) \bullet 100\% = 8.33\%$$

Figure 5 shows typical boost region waveforms. If V_{IN} approaches V_{OUT}, the buck-boost region is reached.

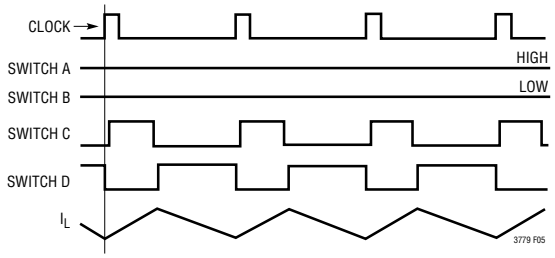


Figure 5. Boost Region (V_{IN} << V_{OUT})

Light Load Current Operation (MODE Pin)

The LTC3779 can be enabled to enter pulse-skipping mode or forced continuous conduction mode. To select forced continuous operation, tie the MODE pin to a DC voltage below 0.8V (e.g., SGND). To select pulse-skipping mode of operation, tie the MODE pin to V5.

Pulse-Skipping Mode: When the LTC3779 enters pulse-skipping or discontinuous mode, in the boost region, synchronous switch D is held off whenever reverse current through switch A is detected. At very light loads, the current comparator, I_{CMP}, may remain tripped for several cycles and force switch C to stay off for the same number of cycles (i.e., skipping pulses). In the buck region, the inductor current is not allowed to reverse.

OPERATION

Synchronous switch B is held off whenever reverse current on the inductor is detected. At very light loads, the current comparator, I_{CMP}, may remain untripped for several cycles, holding switch A off for the same number of cycles. Synchronous switch B also remains off for the skipped cycles. In the buck-boost region, the controller operates alternatively in boost and buck regions in one clock cycle, as in continuous operation. A small amount of reverse current is allowed, to minimize ripple. For the same reason, a narrow band of continuous buck and boost operation is allowed on the high and low line ends of the buck-boost region.

Forced Continuous Mode: The forced continuous mode allows the inductor current to reverse directions without any switches being forced "off" to prevent this from happening. At very light load currents the inductor current will swing positive and negative as the appropriate average current is delivered to the output. During soft-start, if the SS pin is lower than V_{FB}, the part will be forced into discontinuous mode to prevent pulling current from the output to the input. After SS voltage crosses V_{FB} or 1.32V, whichever is lower, forced continuous mode will be enabled.

Output Overvoltage

If the output voltage is higher than the value commanded by the V_{FB} resistor divider, the LTC3779 will respond according to the mode and region of operation. In continuous conduction mode, the LTC3779 will sink current into the input. If the input supply is capable of sinking current, the LTC3779 will allow up to about 80mV/ R_{SENSE} to be sunk into the input. In pulse-skipping mode and in the buck or boost regions, switching will stop and the output will be allowed to remain high. In pulse-skipping mode, and in the buck-boost region as well as the narrow band of continuous boost operation that adjoins it, current sunk into the input through switch A is limited to approximately 40mV/ $R_{DS(ON)}$ of switch A. If this level is reached, switching will stop and the output will rise. In pulse-skipping mode, and in the narrow continuous buck region that adjoins the buck/ boost region, current sunk into the input through R_{SENSE} is limited to approximately 40mV/R_{SENSE}.

Voltage Regulation Loop

The LTC3779 provides a constant-voltage regulation loop, for regulating the output voltage. A resistor divider between V_{OUT}, V_{FB} and GND senses the output voltage. As with traditional voltage regulators, when V_{FB} rises near or above the reference voltage of EA (1.2V typical, see Block Diagram), the ITH voltage is reduced to command the amount of current that keeps V_{OUT} regulated to the desired voltage.

Constant-Current Regulation ($I_{AVGSNSP}$ and $I_{AVGSNSN}$ Pins)

The LTC3779 provides a constant-current regulation loop for either input or output current. A sensing resistor close to the input or output capacitor will sense the input or output current. When the current exceeds the programmed current limit, the voltage on the ITH pin will be pulled down to maintain the desired maximum input or output current. The input current limit function prevents overloading the DC input source, while the output current limit provides a building block for battery charger or LED driver applications. It can also serve as an extra current limit protection for a constant-voltage regulation application. The input or output current limit function has an operating voltage range of GND to the absolute maximum V_{IN} or V_{OUT}, respectively.

Frequency Selection and Phase-Locked Loop (FREQ and PLLIN Pins)

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage. The switching frequency of the LTC3779's controllers can be selected using the FREQ pin. If the SYNC pin is not being driven by an external clock source, the FREQ pin can be used to program the controller's operating frequency from 50kHz to 600kHz.

Switching frequency is determined by the voltage on the FREQ pin. Since there is a precision 20µA current flowing out of the FREQ pin, the user can program the

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controller's switching frequency with a single resistor to SGND. Figure 9 in the Applications Information section shows the relationship between the FREQ pin resistor value and the switching frequency.

A phase-locked loop (PLL) is integrated on the LTC3779 to synchronize the internal oscillator to an external clock source driving the PLLIN pin. While LTC3779 is being synchronized to an external clock source, depending on the voltage of the MODE pin, it can be enabled to enter pulse-skipping mode or forced continuous conduction mode. The PLL filter network is integrated inside the LTC3779.

The PLL is capable of locking to any frequency within the range of 50kHz to 600kHz. The frequency setting resistor should always be present to set the controller's initial switching frequency before locking to the external clock.

Power Good (PGOOD) Pins

The PGOOD pin is connected to the open drain of an internal N-channel MOSFET. When V_{FB} is not within ±10% of the 1.2V reference voltage, the PGOOD pin is pulled low. The PGOOD pin is also pulled low when RUN is below 1.1V or when the LTC3779 is in the soft-start phase. There is an internal 125µs power good or bad mask when V_{FB} goes in or out of the ±10% window. The PGOOD pin is allowed to be pulled up by an external resistor to V5 or an external source of up to 6V.

Short-Circuit Protection, Current Limit and Current Limit Foldback

The maximum current threshold of the controller is limited by a voltage clamp on the ITH pin. In every boost cycle, the sensed maximum peak voltage is limited to 140mV. In every buck cycle, the sensed maximum valley voltage is limited to 90mV. In the buck-boost region, only peak sensed voltage is limited by the same threshold as in the boost region.

The LTC3779 includes current foldback to help limit load current when the output is shorted to ground. If the output falls below 50% of its nominal output level, then the maximum sense voltage is progressively lowered from its maximum value to one-third of the maximum value. Foldback current limiting is disabled during the soft-start. Under short-circuit conditions, the LTC3779 will limit the current by operating as a buck with very low duty cycles, and by skipping cycles. In this situation, synchronous switch B will dissipate most of the power (but less than in normal operation).

Thermal Shutdown

The LTC3779 has a temperature sensor integrated on the IC, to sense the die temperature near the gate driver circuits. When the die temperature exceeds 175°C, all switching actions stop, the top GATE pins are held low, and the bottom GATE pins are held high, and V_{OUT} is disconnected from V_{IN}. At the same time, the SS pin is pulled low by an internal MOSFET. When the temperature drops 10°C below the trip threshold, the part goes through a SS reset cycle and normal operation resumes.

Input Undervoltage and Overvoltage Lockout

The LTC3779 implements a protection feature that inhibits switching when the input voltage rises above a programmable operating range. By using a resistor divider from the input supply to ground, the RUN and VINOV pins serve as a precise input supply voltage monitor. Switching is disabled when either the RUN pin falls below 1.1V or the VINOV pin rises above 1.28V, which can be configured to limit switching to a specific range of input supply voltage.

When switching is disabled, the LTC3779 can safely sustain input voltages on the RUN pin up to the absolute maximum rating of 150V. Input supply undervoltage or overvoltage events trigger a soft-start reset, which results in a graceful recovery from an input supply transient.

APPLICATIONS INFORMATION

The Typical Application on the first page is a basic LTC3779 application circuit. External component selection is driven by the load requirement, and begins with the selection of R_{SENSE} and the inductor value. Next, the power MOSFETs are selected. Finally, C_{IN} and C_{OUT} are selected. This circuit can be configured for operation up to an input voltage of 150V.

Inductor Current Sensing and Slope Compensation

The LTC3779 operates using inductor current mode control. The LTC3779 measures the peak of the inductor current waveform in the boost region and the valley of the inductor current waveform in the buck region. The inductor current is sensed across the R_{SENSE} resistor with pins SENSEP and SENSEN. During any given cycle, the peak (boost region) or valley (buck region) of the inductor current is controlled by the ITH pin voltage.

Slope compensation provides stability in constant frequency architectures by preventing subharmonic oscillations at high duty cycles in boost operation and at low duty cycles in buck operation. This is accomplished internally by adding a compensating ramp to the inductor current signal at duty cycles in excess of 40% in the boost region, or subtracting a ramp from the inductor current signal at lower than 40% duty cycles in the buck region. Normally, this results in a reduction of maximum inductor peak current for duty cycles >40% in the boost region, or an increase of maximum inductor current for duty cycles <40% in the buck region. However, the LTC3779 uses a scheme that counteracts this compensating ramp, which allows the maximum inductor current to remain unaffected throughout all duty cycles.

R_{SENSE} Selection and Maximum Output Current

The R_{SENSE} resistance must be chosen properly to achieve the desired amount of output current. Too much resistance can limit the output current below the application requirements. Start by determining the maximum allowed R_{SENSE} resistance in the boost region, $R_{SENSE(MAX,BOOST)}$. Follow this by finding the maximum allowed R_{SENSE} resistance in the buck region, $R_{SENSE(MAX,BUCK)}$. The selected R_{SENSE} resistance must be smaller than both. Figure 6 shows how $I_{LOAD(MAX)} \bullet R_{SENSE}$ varies with input and output voltage.

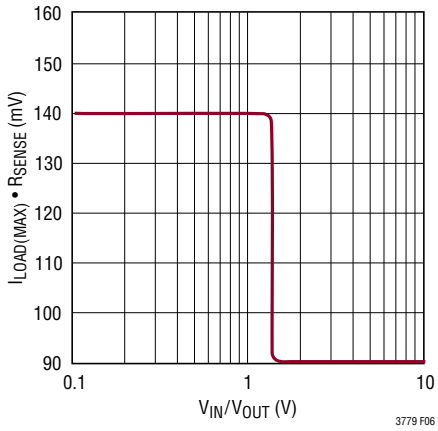

Figure 6. Load Current vs V_{IN}/V_{OUT}

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Boost Region: In the boost region, the maximum output current capability is the least when V_{IN} is at its minimum and V_{OUT} is at its maximum. Therefore R_{SENSE} must be chosen to meet the output current requirements under these conditions.

Start by finding the boost region duty cycle when V_{IN} is minimum and V_{OUT} is maximum using:

$$DC_{(MAX,C,BOOST)} \cong \left(1 - \frac{V_{IN(MIN)}}{V_{OUT(MAX)}}\right) \bullet 100\%$$

For example, an application with a V_{IN} range of 12V to 48V and V_{OUT} set to 36V will have:

$$DC_{(MAX,C,BOOST)} \cong \left(1 - \frac{12V}{36V}\right) \bullet 100\% = 67\%$$

Next, the inductor ripple current in the boost region must be determined. If the main inductor L is not known, the maximum ripple current $\Delta I_{L(MAX,BOOST)}$ can be estimated by choosing $\Delta I_{L(MAX,BOOST)}$ to be 30% to 50% of the maximum inductor current in the boost region as follows:

$$\Delta I_{L(MAX,BOOST)} \cong \frac{V_{OUT(MAX)} \bullet I_{OUT(MAX,BOOST)}}{V_{IN(MIN)} \bullet \left(\frac{100\%}{\%Ripple} - 0.5\right)} A$$

where:

$I_{OUT(MAX,BOOST)}$ is the maximum output load current required in the boost region

%Ripple is 30% to 50%

For example, using $V_{OUT(MAX)}$ = 36V, $V_{IN(MIN)}$ = 12V, $I_{OUT(MAX,BOOST)}$ = 2A and %Ripple = 40% we can estimate:

$$\Delta I_{L(MAX,BOOST)} \cong \frac{36V \bullet 2A}{12V \bullet \left(\frac{100\%}{40\%} - 0.5\right)} = 3A$$

Otherwise, if the inductor value is already known then $\Delta I_{L(MAX,BOOST)}$ can be more accurately calculated as follows:

$$\Delta I_{L(MAX,BOOST)} = \frac{\left(\frac{DC_{(MAX,C,BOOST)}}{100\%}\right) \bullet V_{IN(MIN)}}{f \bullet L} A$$

where:

$DC_{(MAX,C,BOOST)}$ is the maximum duty cycle percentage in the boost region as calculated previously.

f is the switching frequency

L is the inductance of the main inductor

After the maximum ripple current is known, the maximum allowed R_{SENSE} in the boost region can be calculated as follows:

$$R_{SENSE(MAX,BOOST)} = \frac{2 \bullet V_{RSENSE(MAX,BOOST,MAXDC)} \bullet V_{IN(MIN)}}{\left(2 \bullet I_{OUT(MAX,BOOST)} \bullet V_{OUT(MIN)}\right) + \left(\Delta I_{L(MAX,BOOST)} \bullet V_{IN(MIN)}\right)} \Omega$$

where $V_{RSENSE(MAX,BOOST,MAXDC)}$ is the maximum inductor current sense voltage as discussed in the previous section.

Using values from the previous examples:

$$R_{SENSE(MAX,BOOST)} = \frac{2 \bullet 140mV \bullet 12}{(2 \bullet 2A \bullet 36V) + (3A \bullet 12V)} = 18.66m\Omega$$

Buck Region: The duty cycle for buck operation can be calculated using:

$$DC_{(MAX,B,BUCK)} \cong \left(1 - \frac{V_{OUT(MIN)}}{V_{IN(MAX)}}\right) \bullet 100\%$$

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Before calculating the maximum R_{SENSE} resistance, however, the inductor ripple current must be determined. If the main inductor L is not known, the ripple current $\Delta I_{L(MIN,BUCK)}$ can be estimated by choosing $\Delta I_{L(MIN,BUCK)}$ to be 10% of the maximum inductor current in the buck region as follows:

$$\Delta I_{L(MIN,BUCK)} \cong \frac{I_{OUT(MAX,BUCK)}}{\left(\frac{100\%}{10\%} - 0.5\right)} A$$

where:

$I_{OUT(MAX,BUCK)}$ is the maximum output load current required in the buck region.

If the inductor value is already known then $\Delta I_{L(MIN,BUCK)}$ can be calculated as follows:

$$\Delta I_{L(MIN,BUCK)} = \frac{\left(\frac{DC_{(MIN,B,BUCK)}}{100\%}\right) \bullet V_{OUT(MIN)}}{f \bullet L} A$$

where:

$DC_{(MIN,B,BUCK)}$ is the minimum duty cycle percentage in the buck region as calculated previously.

f is the switching frequency

L is the inductance of the main inductor

After the inductor ripple current is known, the maximum allowed R_{SENSE} in the buck region can be calculated as follows:

$$R_{SENSE(MAX,BUCK)} = \frac{2 \bullet V_{RSENSE(MAX,BUCK,MINDC)}}{\left(2 \bullet I_{OUT(MAX,BUCK)}\right) - \Delta I_{L(MIN,BUCK)}} \Omega$$

Programming Input/Output Current Limit

As shown in Figure 7 and Figure 8, input/output current sense resistor R_{SENSE2} should be placed between the bulk capacitor for V_{IN} or V_{OUT} and the decoupling capacitor. A lowpass filter formed by R_F and C_F is recommended to reduce the switching noise and stabilize the current loop. The input/output current limit is set internally to 50mV. If

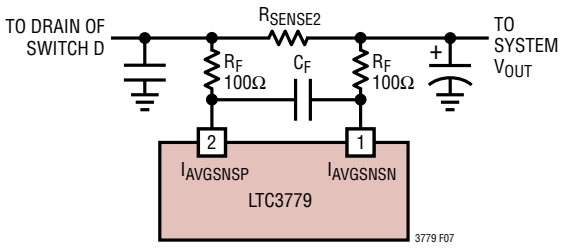

Figure 7. Programming Output Current Limit

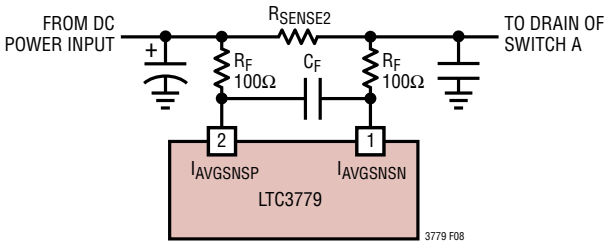

Figure 8. Programming Input Current Limit

input/output current limit is not desired, the $I_{AVGSNSP}$ and $I_{AVGSNSN}$ pins should be shorted together to V5.

With the typical 100Ω resistors shown here, the value of capacitor C_F should be 1µF to 4.7µF. The current loop's transfer function should approximate that of the voltage loop. Crossover frequency should be one-tenth the switching frequency, and gain should decrease by 20dB/decade. Similar current and voltage loop transfer functions will ensure overall system stability.

When the I_{AVGSNS} common mode voltage is above ~4V, the $I_{AVGSNSN}$ pin sources 10µA. The $I_{AVGSNSP}$ pin, however, sources 15µA, when a constant current is being regulated. The error introduced by this mismatch can be offset to a first order by scaling the $I_{AVGSNSP}$ and $I_{AVGSNSN}$ resistors accordingly. For example, if the $I_{AVGSNSP}$ branch has a 100Ω resistor, the 1.50mV across it can be replicated in the $I_{AVGSNSN}$ branch by using a 150Ω resistor.

When the I_{AVGSNS} common mode voltage falls below ~4V, the I_{AVGSNS} current decreases linearly; it reaches approximately –300µA at zero volts. The maximum current sinking can vary by 20% to 30% due to process

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variation. Ensure that I_{AVGSNS} common mode voltage never exceeds its absolute maximum of –10V below ground. Pay special attention to short-circuit conditions in high power applications.

Phase-Locked Loop and Frequency Synchronization

The LTC3779 has a phase-locked loop (PLL) comprised of an internal voltage-controlled oscillator (VCO) and a phase detector. This allows the turn-on of the bottom MOSFET of the controller to be locked to the rising edge of an external clock signal applied to the PLLIN pin. The phase detector is an edge sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector does not exhibit false locking to harmonics of the external clock.

The output of the phase detector is a pair of complementary current sources that charge or discharge the internal filter network. There is a precision 20µA of current flowing out of the FREQ pin. This allows a single resistor to SGND to set the switching frequency when no external clock is applied to the PLLIN pin. The internal switch between FREQ and the integrated PLL filter network is on, allowing the filter network to be pre-charged at the same voltage as the FREQ pin. The relationship between the voltage on the FREQ pin and operating frequency is shown in Figure 9 and specified in the Electrical Characteristics table. If an external clock is detected on the PLLIN pin, the internal switch previously mentioned will turn off and isolate the influence of the FREQ pin.

Note that the LTC3779 can only be synchronized to an external clock whose frequency is within range of the LTC3779's internal VCO. This is guaranteed to be between 50kHz and 600kHz. A simplified block diagram is shown in Figure 10.

If the external clock frequency is greater than the internal oscillator's frequency, f_{OSC}, then current is sourced continuously from the phase detector output, pulling up the filter network. When the external clock frequency is less than f_{OSC}, current is sunk continuously, pulling down the filter network. If the external and internal frequencies

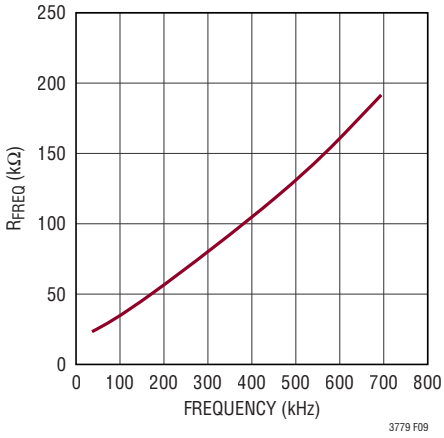

Figure 9. FREQ Pin Resistor Value vs Frequency

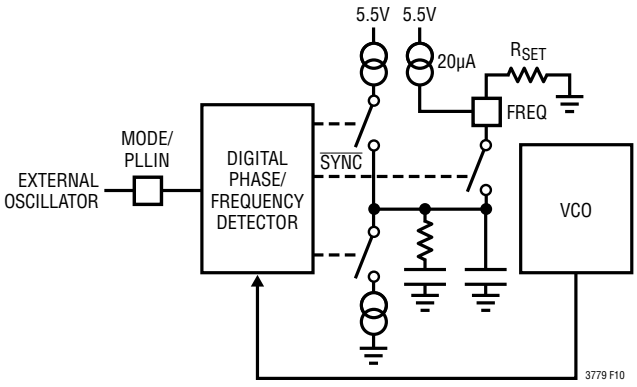

Figure 10. Phase-Locked Loop Block Diagram

are the same but exhibit a phase difference, the current sources turn on for the amount of time corresponding to the phase difference. The voltage on the filter network is adjusted until the phase and frequency of the internal and external oscillators are identical. At the stable operating point, the phase detector output is high impedance and the filter capacitor holds the voltage.

Typically, the external clock (on the PLLIN pin) input high threshold is 2V, while the input low threshold is 1.2V.

The operating frequency of the LTC3779 can be approximated using the following formula:

$$R_{FREQ} = 0.000115(f_{OSC})^2 + 0.174\ (f_{OSC}) + 18.5$$

where f_{OSC} is in kHz and R_{FREQ} is in kΩ.

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Inductor Selection

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. The inductor value has a direct effect on ripple current. The inductor current ripple ΔI_L is typically set to 20% to 40% of the maximum inductor current in the boost region at $V_{IN(MIN)}$. For a given ripple the inductance terms in continuous mode are as follows:

$$L_{BOOST} > \frac{V_{IN(MIN)}^2 \bullet \left(V_{OUT} - V_{IN(MIN)}\right) \bullet 100}{f \bullet I_{OUT(MAX)} \bullet \%Ripple \bullet V_{OUT}^2} H,$$

$$L_{BUCK} > \frac{V_{OUT} \bullet \left(V_{IN(MAX)} - V_{OUT}\right) \bullet 100}{f \bullet I_{OUT(MAX)} \bullet \%Ripple \bullet V_{IN(MAX)}} H$$

where:

f is operating frequency, Hz

% Ripple is allowable inductor current ripple

$V_{IN(MIN)}$ is minimum input voltage, V

$V_{IN(MAX)}$ is maximum input voltage, V

V_{OUT} is output voltage, V

$I_{OUT(MAX)}$ is maximum output load current, A

For high efficiency, choose an inductor with low core loss, such as ferrite. Also, the inductor should have low DC resistance to reduce the I^2R losses, and must be able to handle the peak inductor current without saturating. To minimize radiated noise, use a toroid, pot core or shielded bobbin inductor.

Inductor Core Selection

Once the inductance value is determined, the type of inductor must be selected. Core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates “hard,” which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

C_{IN} and C_{OUT} Selection

In the boost region, input current is continuous. In the buck region, input current is discontinuous. In the buck region, the selection of input capacitor C_{IN} is driven by the need to filter the input square wave current. Use a low ESR capacitor sized to handle the maximum RMS current. For buck operation, the input RMS current is given by:

$$I_{RMS} \approx I_{OUT(MAX)} \bullet \frac{V_{OUT}}{V_{IN}} \bullet \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT(MAX)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to derate the capacitor.

In the boost region, the discontinuous current shifts from the input to the output, so C_{OUT} must be capable of reducing the output voltage ripple. The effects of ESR (equivalent series resistance) and the bulk capacitance must be considered when choosing the right capacitor for a given output ripple voltage. The steady ripple due to charging and discharging the bulk capacitance is given by:

$$\Delta V_{RIPPLE(BOOST,CAP)} = \frac{I_{OUT(MAX)} \bullet \left(V_{OUT} - V_{IN(MIN)}\right)}{C_{OUT} \bullet V_{OUT} \bullet f} V$$

where C_{OUT} is the output filter capacitor.

The steady ripple due to the voltage drop across the ESR is given by:

$$\Delta V_{(BOOST,ESR)} = I_{OUT(MAX,BOOST)} \bullet ESR$$

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In buck mode, V_{OUT} ripple is given by:

$$\Delta V_{OUT} \le \Delta I_L \left(ESR + \frac{1}{8 \bullet f \bullet C_{OUT}} \right)$$

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Aluminum electrolytic and ceramic capacitors are available in surface mount packages. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient. Bulk capacitors are now available with low ESR and high ripple current ratings, such as OSCON and aluminum electrolytics with hybrid conductive polymers.

Power MOSFET Selection and Efficiency Considerations

The LTC3779 requires four external N-channel power MOSFETs, two for the top switches (switches A and D, shown in Figure 1) and two for the bottom switches (switches B and C, shown in Figure 1). Important parameters for the power MOSFETs are the breakdown voltage $V_{BR,DSS}$, threshold voltage $V_{GS,TH}$, on-resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS} and maximum current $I_{DS(MAX)}$.

The peak-to-peak drive levels are set by the DRV_{CC} voltage. This voltage can range from 6V to 10V depending on the DRVSET pin setting. Therefore, both logic-level and standard-level threshold MOSFETs can be used in most applications, depending on the programmed DRV_{CC} voltage. Pay close attention to the BV_{DSS} specification for the MOSFETs as well.

The LTC3779's ability to adjust the gate drive level between 6V to 10V allows an application circuit to be precisely optimized for efficiency. When adjusting the gate drive level, the final arbiter is the total input current for the regulator. If a change is made and the input current decreases, then the efficiency has improved. If there is no change in input current, then there is no change in efficiency.

In order to select the power MOSFETs, the power dissipated by the device must be known. For switch A, the maximum power dissipation happens in the boost region, when it remains on all the time. Its maximum power dissipation at maximum output current is given by:

$$P_{A,BOOST} = \left(\frac{V_{OUT}}{V_{IN}} \bullet I_{OUT(MAX)} \right)^2 \bullet \rho_\tau \bullet R_{DS(ON)}$$

where ρ_τ is a normalization factor (unity at 25°C) accounting for the significant variation in on-resistance with temperature, typically about 0.4%/°C, as shown in Figure 11. For a maximum junction temperature of 125°C, using a value ρ_τ = 1.5 is reasonable.

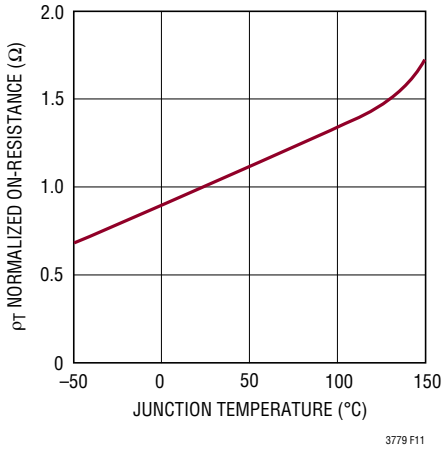

Figure 11. Normalized $R_{DS(ON)}$ vs Temperature

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Switch B operates in the buck region as the synchronous rectifier. Its power dissipation at maximum output current is given by:

$$P_{B,BUCK} = \frac{V_{IN} - V_{OUT}}{V_{IN}} \bullet I_{OUT(MAX)}^2 \bullet \rho_\tau \bullet R_{DS(ON)}$$

Switch C operates in the boost region as the control switch. Its power dissipation at maximum current is given by:

$$P_{C,BOOST} = \frac{(V_{OUT} - V_{IN})V_{OUT}}{V_{IN}^2} \bullet I_{OUT(MAX)}^2 \bullet \rho_\tau$$

$$\bullet R_{DS(ON)} + k \bullet V_{OUT}^3 \bullet \frac{I_{OUT(MAX)}}{V_{IN}} \bullet C_{RSS} \bullet f$$

where C_{RSS} is usually specified by the MOSFET manufacturers. The constant k, which accounts for the loss caused by reverse recovery current, is inversely proportional to the gate drive current and has an empirical value of 1.7.

For switch D, the maximum power dissipation happens in the boost region, when its duty cycle is higher than 50%. Its maximum power dissipation at maximum output current is given by:

$$P_{D,BOOST} = \frac{V_{IN}}{V_{OUT}} \bullet \left(\frac{V_{OUT}}{V_{IN}} \bullet I_{OUT(MAX)} \right)^2 \bullet \rho_\tau \bullet R_{DS(ON)}$$

For the same output voltage and current, switch A has the highest power dissipation and switch B has the lowest power dissipation unless a short occurs at the output.

From a known power dissipated in the power MOSFET, its junction temperature can be obtained using the following formula:

$$T_J = T_A + P \bullet R_{TH(JA)}$$

The $R_{TH(JA)}$ to be used in the equation normally includes the $R_{TH(JC)}$ for the device plus the thermal resistance from the case to the ambient temperature ($R_{TH(JC)}$). This value of T_J can then be compared to the original, assumed value used in the iterative calculation process.

Schottky Diode (D1, D2) Selection

The Schottky diodes, D1 and D2, shown in the Block Diagram, conduct during the dead time between the conduction of the power MOSFET switches. They are intended to prevent the body diode of synchronous switches B and D from turning on and storing charge during the dead time. In particular, D2 significantly reduces reverse recovery current between switch D turn-off and switch C turn-on, which improves converter efficiency and reduces switch C voltage stress. In order for the diode to be effective, the inductance between it and the synchronous switch must be as small as possible, mandating that these components be placed adjacently.

Setting Output Voltage

The LTC3779 output voltage is set by two external feedback resistive dividers carefully placed across the output, as shown in Figure 12. The regulated output voltage is determined by:

$$V_{OUT} = 1.2V \bullet (1 + R_B/R_A)$$

To improve the frequency response, a feed forward capacitor, C_{FF}, may be used. Great care should be taken to route the V_{FB} line away from noise sources, such as the inductor or the SW line.

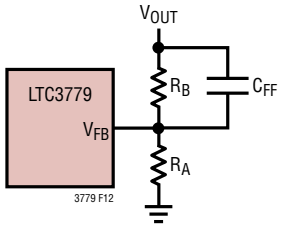

Figure 12. Setting Output Voltage

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RUN Pin and Overvoltage/Undervoltage Lockout

The LTC3779 is enabled using the RUN pin. It has a rising threshold of 1.2V with 100mV of hysteresis. Pulling the RUN pin below 1.1V shuts down the main control loop for the controller and most internal circuits, including the DRV_{CC} and V5 LDOs. In this state the LTC3779 draws only 40µA of quiescent current. Releasing the RUN pin allows an internal 2.5µA current to pull-up the pin and enable the controller. The RUN comparator itself has about 100mV of hysteresis. When the voltage on the RUN pin exceeds 1.2V, the current sourced into the RUN pin is switched from 2.5µA to 6.5µA current. The user can therefore program both the rising threshold and the amount of hysteresis using an external resistive divider.

The RUN pin is high impedance above 3V and must be externally pulled up/down or driven directly by logic, as shown in Figure 13. The RUN pin can tolerate up to 150V (absolute maximum), so it can be conveniently tied to V_{IN} in always-on applications where the controller is enabled continuously and never shut down.

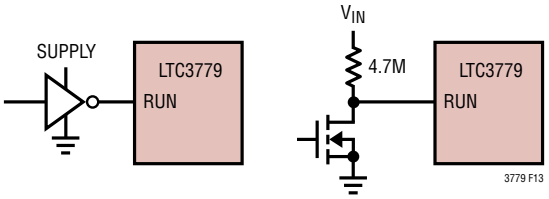

Figure 13. RUN Pin Interface to Logic

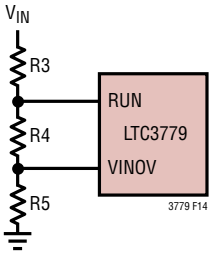

Figure 14. Adjustable UV and OV Lockout

The RUN and VINOV pins can alternatively be configured as undervoltage (UVLO) and overvoltage (OVLO) lockouts on the V_{IN} supply with a resistor divider from V_{IN} to ground. A simple resistor divider can be used as shown in Figure 14 to meet specific V_{IN} voltage requirements. One can program additional hysteresis for the RUN comparator by adjusting the values of the resistive divider.

The current that flows through the R3-R4-R5 divider will directly add to the shutdown and active current of the LTC3779, and care should be taken to minimize the impact of this current on the overall efficiency of the application circuit. Resistor values in the megohm range may be required to keep the impact on quiescent shutdown current low. To pick resistor values, the sum total of R3 + R4 + R5 (R_{TOTAL}) should be chosen first based on the allowable DC current that can be drawn from V_{IN}.

The individual values of R3, R4 and R5 can then be calculated from the following equations:

$$R5 = R_{TOTAL} \bullet \left(\frac{1.2V}{\text{Rising } V_{IN} \text{ OVLO Threshold}} \right)$$

$$R4 = R_{TOTAL} \bullet \left(\frac{1.2V}{\text{Rising } V_{IN} \text{ UVLO Threshold}} \right) - R5$$

$$R3 = R_{TOTAL} - R4 - R5$$

For applications that do not need a precise external OVLO, the VINOV pin should be tied directly to ground. The RUN pin in this type of application can be used as an external UVLO using the following equations with R5 = 0Ω.

$$V_{IN(ON)} = 1.2V\left(1 + \frac{R3}{R4}\right) - 2.5\mu \bullet R3$$

$$V_{IN(OFF)} = 1.1V\left(1 + \frac{R3}{R4}\right) - 6.5\mu \bullet R3$$

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Similarly, for applications that do not require a precise UVLO, the RUN pin can be tied to V_{IN}. In this configuration, the UVLO threshold is limited to the internal V_{IN} UVLO thresholds as shown in the Electrical Characteristics table. The resistor values for the OVLO can be computed using the previous equations with R3 = 0Ω.

Be aware that the VINOV pin cannot be allowed to exceed its absolute maximum rating of 6V. To keep the voltage on the VINOV pin from exceeding 6V, the following relation should be satisfied:

$$V_{IN(MAX)} \bullet \left(\frac{R5}{R3+R4+R5} \right) < 6V$$

Soft-Start

The start-up of V_{OUT} is controlled by the voltage on the SS pin. If its RUN pin voltage is below 1.1V the controller is in the shutdown state; its SS pin is actively pulled to ground in this shutdown state. If the RUN pin voltage is above 1.2V, the controller powers up. A soft-start current of 5µA then starts to charge the SS soft-start capacitor. Note that soft-start is achieved not by limiting the maximum output current of the controller but by controlling the output ramp voltage according to the ramp rate on the SS pin. When the voltage on the SS pin is less than the internal 1.2V reference, the LTC3779 regulates the V_{FB} pin voltage to the voltage on the SS pin instead of the internal reference. Current foldback is disabled during this phase. The soft-start range is defined to be the voltage range from 0V to 1.2V on the SS pin. The total soft-start time can be calculated as:

$$t_{SS} = C_{SS} \bullet \left(\frac{1.2V}{5\mu A} \right)$$

DRV_{CC} Regulator

The LTC3779 features three separate low dropout linear regulators (LDO) that can supply power at the DRVCC pin. The internal V_{IN} LDO uses an internal P-channel pass device between the V_{IN} and DRV_{CC} pins. The internal $EXTV_{CC}$ LDO uses an internal P-channel pass device between the $EXTV_{CC}$ and DRV_{CC} pins. The NDRV LDO utilizes the NDRV pin to drive the gate of an external N-channel MOSFET acting as a linear regulator with its drain connected to V_{IN}.

The NDRV LDO provides an alternative method to supply power to DRVCC from the input supply without dissipating the power inside the LTC3779 IC. It has an internal charge pump that allows NDRV to be driven above the V_{IN} supply, allowing for low dropout performance. The V_{IN} LDO has a slightly lower regulation point than the NDRV LDO, such that all DRV_{CC} current flows through the external N-channel MOSFET (and not through the internal P-channel pass device) once DRV_{CC} reaches regulation.

When laying out the PC board, care should be taken to route NDRV away from any switching nodes, especially SW, TG, and BOOST. Coupling to the NDRV node could cause its voltage to collapse and the NDRV LDO to lose regulation. If this occurs, the internal V_{IN} LDO would take over and maintain DRV_{CC} voltage at a slightly lower regulation point. However, internal heating of the IC would become a concern. High frequency noise on the drain of the external NFET could also couple into the NDRV node (through the gate-to-drain capacitance of the NDRV NFET) and adversely affect NDRV regulation. The following are methods that could mitigate this potential issue (refer to Figure 15).

1. Add local decoupling capacitors right next to the drain of the external NDRV NFET in the PCB layout.
2. Insert a resistor (~100Ω) in series with the gate of the NDRV NFET.
3. Insert a small capacitor (~1nF) between the gate and source of the NDRV NFET.

When testing the application circuit, be sure the NDRV voltage does not collapse over the entire input voltage and output current operating range of the buck-boost regulator. If the NDRV LDO is not being used, connect the NDRV pin to DRV_{CC} (Figure 15b).

The DRV_{CC} supply is regulated between 6V to 10V, depending on the DRVSET pin setting. The internal V_{IN} and $EXTV_{CC}$ LDOs can supply a peak current of at least 50mA. The DRV_{CC} pin must be bypassed to ground with a minimum of 4.7µF ceramic capacitor. Good bypassing is needed to supply the high transient currents required by

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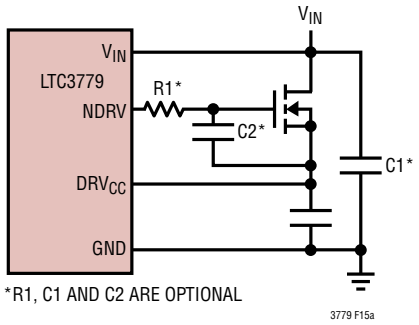

Figure 15a. Configuring the NDRV LDO

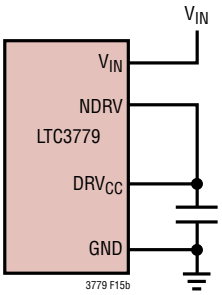

Figure 15b. Disabling the NDRV LDO

the MOSFET gate drivers. The DRVSET pin programs the DRV_{CC} supply voltage and selects the appropriate $EXTV_{CC}$ switchover threshold voltages as shown in the Electrical Characteristics table. The DRVSET pin has five logic level states. When DRVSET is either grounded, floated or tied to V5, the typical value for the DRV_{CC} voltage will be 6V, 8V and 10V respectively. Use the 10V setting with careful PCB layout. This is because any overshoot between BOOST and SW would exceed the absolute maximum voltage of 11V for the floating driver. Set DRVSET to one-fourth of V5 and three-fourths of V5 for 7V and 9V DRV_{CC} voltages. Please note that the DRVSET pin has an internal 200k pull-down to SGND and a 200k pull-up to V5. The $EXTV_{CC}$ turn on threshold is the selected DRV_{CC} regulation voltage minus 500mV. The turn off threshold is 500mV below the turn on threshold.

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC3779 to be exceeded. The DRV_{CC} current, which is dominated by the gate charge current, may be supplied by the V_{IN} LDO, NDRV LDO or the $EXTV_{CC}$ LDO. When the voltage on the $EXTV_{CC}$ pin is less than its switchover threshold (as determined by the DRVSET pin), the V_{IN} and NDRV LDOs are enabled. Power dissipation in this case is highest and is equal to $V_{IN} \bullet I_{DRVCC}$. If the NDRV LDO is not being used, this power is dissipated inside the IC. The gate charge current is dependent on operating frequency as discussed in the Efficiency Considerations section.

The junction temperature can be estimated by using the equations given in Note 2 of the Electrical Characteristics table. For example, if DRV_{CC} is set to 6V, the DRV_{CC} current is limited to less than 49mA from a 40V supply when not using the $EXTV_{CC}$ or NDRV LDO's at a 70°C ambient temperature:

$$T_J = 70°C + (49mA)(40V)(28°C/W) = 125°C$$

To prevent the maximum junction temperature from being exceeded, the V_{IN} supply current must be checked while operating in forced continuous mode (MODE = SGND) at maximum V_{IN}.

When the voltage applied to $EXTV_{CC}$ rises above its switchover threshold, the V_{IN} and NDRV LDOs are turned off and the $EXTV_{CC}$ LDO is enabled. The $EXTV_{CC}$ LDO remains on as long as the voltage applied to $EXTV_{CC}$ remains above the switchover threshold minus the comparator hysteresis. The $EXTV_{CC}$ LDO attempts to regulate the DRV_{CC} voltage to the voltage as programmed by the DRVSET pin, so while $EXTV_{CC}$ is less than this voltage, the LDO is in dropout and the DRV_{CC} voltage is approximately equal to $EXTV_{CC}$. When $EXTV_{CC}$ is greater than the programmed voltage, up to an absolute maximum of 36V, DRV_{CC} is regulated to the programmed voltage.

Using the $EXTV_{CC}$ LDO allows the MOSFET driver and control power to be derived from the LTC3779's switching regulator output ($5.7V \le V_{OUT} \le 36V$) during normal operation and from the V_{IN} or NDRV LDO when the output is out of regulation (e.g., start-up, short-circuit).

Significant efficiency and thermal gains can be realized by powering DRV_{CC} from the output, since the V_{IN} current resulting from the driver and control currents will be scaled by a factor of (Duty Cycle)/(Switcher Efficiency).

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For 5.5V to 36V regulator outputs, this means connecting the $EXTV_{CC}$ pin directly to V_{OUT}. Tying the $EXTV_{CC}$ pin to a 12V supply reduces the junction temperature in the previous example from 125°C to:

$$T_J = 70°C + 49mA \bullet (12V)(28°C/W) = 86°C$$

While using the $EXTV_{CC}$ LDO there is an V_{IN} under voltage detection circuit that disables the $EXTV_{CC}$ LDO if the V_{IN} voltage is less that the DRV_{CC} voltage that is set by the DRVSET pin.

For applications where the minimum V_{IN} voltage of LTC3779 needs to be less than 4.5V, the $EXTV_{CC}$ pin can be used to power the V_{IN} of LTC3779. The V_{IN} under voltage detection circuit is disabled when DRVSET is set to three-fourths of V5, for 9V DRV_{CC} voltage. Under this condition the DRV_{CC} voltage can be higher than the V_{IN} of LTC3779 and an external blocking diode should be connected from the V_{IN} pin of LTC3779 to the external V_{IN} supply, to avoid back feeding the V_{IN} supply.

The following list summarizes the four possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ grounded. This will cause DRV_{CC} to be powered from the internal V_{IN} or NDRV LDO resulting in an efficiency penalty of up to 10% at high input voltages.
2. $EXTV_{CC}$ connected directly to the regulator output. This is the normal connection for a 5.5V to 36V regulator and provides the highest efficiency.
3. $EXTV_{CC}$ connected to an external supply. If an external supply is available in the 5.5V to 36V range, it may be used to power $EXTV_{CC}$ providing it is compatible with the MOSFET gate drive requirements.
4. $EXTV_{CC}$ connected to the regulator output through an external Zener diode. If the output voltage is greater than 36V, a Zener diode can be used to drop the necessary voltage between V_{OUT} and $EXTV_{CC}$ such that $EXTV_{CC}$ remains below 36V (Figure 16). In this configuration, a bypass capacitor on $EXTV_{CC}$ of at least 0.1µF is recommended. An optional resistor between $EXTV_{CC}$ and GND can be inserted to ensure adequate bias current through the Zener diode.

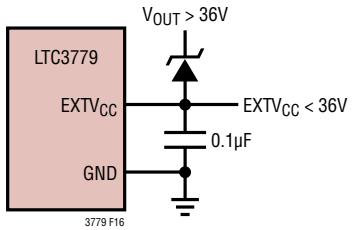

Figure 16. Using a Zener Diode Between V_{OUT} and $EXTV_{CC}$

V5 Regulator

An additional P-channel LDO supplies power at the V5 pin from the DRV_{CC} pin. Whereas DRV_{CC} powers the gate drivers, V5 powers much of the LTC3779's internal circuitry. The V5 LDO regulates the voltage at the V5 pin to 5.5V when DRV_{CC} is at least 6V. The LDO can supply a peak current of 20mA and must be bypassed to ground with a minimum of 4.7µF ceramic capacitor or low ESR electrolytic capacitor. No matter what type of bulk capacitor is used, an additional 0.1µF ceramic capacitor placed directly adjacent to the V5 and SGND pins is highly recommended. V5 is also used as a pull-up to bias other pins, such as MODE, DRVSET and SS.

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Pre-Biased Output Start-Up

There may be situations that require the power supply to start up with a pre-bias on the output capacitors. In this case, it is desirable to start up without discharging that output pre-bias. The LTC3779 can safely power up into a pre-biased output without discharging it.

If the voltage on the SS pin is lower than V_{FB}, to prevent pulling current from the output to the input, the LTC3779 forces the part into discontinuous mode of operation irrespective of the status of the MODE pin. If V_{FB} is >1.12V, or when the SS voltage crosses V_{FB} or 1.32V, whichever event happens first, then the MODE pin setting determines the mode of operation.

Topside MOSFET Driver Supply

In the Block Diagram, the external bootstrap capacitors C_A and C_B, connected to the BOOST1 and BOOST2 pins, supply the gate drive voltage for the topside MOSFET switches A and D. When the top switch A turns on, the switch node SW1 rises to V_{IN} and the BOOST1 pin rises to approximately V_{IN} + DRV_{CC}. When the bottom switch B turns on, the switch node SW1 is low and the boost capacitor C_A is charged through D_A from DRV_{CC}. When the top switch D turns on, the switch node SW2 rises to V_{OUT} and the BOOST2 pin rises to approximately V_{OUT} + DRV_{CC}. When the bottom switch C turns on, switch node SW2 is low and the boost capacitor C_B is charged through D_B from DRV_{CC}. The boost capacitors C_A and C_B need to store about 100 times the gate charge required by the top switches A and D. In most applications, a 0.1µF to 0.47µF, X5R or X7R dielectric capacitor is adequate.

Fault Conditions: Current Limit and Current Foldback

The maximum inductor current is inherently limited in a current mode controller by the maximum sense voltage. In the boost region, maximum sense voltage and the sense resistance determine the maximum allowed inductor peak current, which is:

$$I_{L(MAX,BOOST)} = \frac{140mV}{R_{SENSE}}$$

In the buck region, maximum sense voltage and the sense resistance determine the maximum allowed inductor valley current, which is:

$$I_{L(MAX,BUCK)} = \frac{90mV}{R_{SENSE}}$$

To further limit current in the event of a short circuit to ground, the LTC3779 includes foldback current limiting. If the output falls by more than 50%, then the maximum sense voltage is progressively lowered to about one-third of its full value.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\% \text{ Efficiency} = 100\% - (L1 + L2 + L3 + ...)$$

where L1, L2, etc. a e the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC3779 circuits: 1) IC V_{IN} current, 2) MOSFET driver current, 3) I^2R losses, 4) topside MOSFET transition losses.

1. The V_{IN} current is the DC supply current given in the Electrical Characteristics table. V_{IN} current typically results in a small (<0.1%) loss.
2. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from the driver supply to ground. The resulting dQ/dt is a current out of the driver supply that is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the topside and bottom side MOSFETs.

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3. I^2R losses are predicted from the DC resistances of the fuse (if used), MOSFET, inductor and current sense resistor. In continuous mode, the average output current flows through L and R_{SENSE}, but is chopped between the topside MOSFET and the synchronous MOSFET. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and R_{SENSE} to obtain I^2R losses. For example, if each $R_{DS(ON)}$ = 10mΩ, R_L = 10mΩ, R_{SENSE} = 5mΩ, then the total resistance is 25mΩ. This results in losses ranging from 0.6% to 2% as the output current increases from 3A to 15A for a 12V output.

   Efficiency varies as the inverse square of V_{OUT} for the same external components and output power level. The combined effects of increasingly lower output voltages and higher currents required by high performance digital systems is not doubling but quadrupling the importance of loss terms in the switching regulator system!

4. Transition losses apply only to the topside MOSFET(s), and become significant only when operating at high input voltages (typically 15V or greater). Transition losses can be estimated from:

   Transition Loss = $(1.7)\ V_{IN}^2 \bullet I_{O(MAX)} \bullet C_{RSS} \bullet f$

Other hidden losses such as copper trace and internal battery resistances can account for an additional 5% to 10% efficiency degradation in portable systems. It is very important to include these system level losses during the design phase. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and very low ESR at the switching frequency. A 25W supply will typically require a minimum of 20µF to 40µF of capacitance having a maximum of 20mΩ to 50mΩ of ESR. Other losses including Schottky conduction losses during dead time and inductor core losses generally account for less than 2% total additional loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to ΔI_{LOAD} • ESR, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. The availability of the ITH pin not only allows optimization of control loop behavior but also provides a DC-coupled and AC-filtered closed-loop response test point. The DC step, rise time and settling at this test point truly reflects the closed-loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin.

The ITH external components shown in the Typical Application circuit will provide an adequate starting point for most applications. The ITH series R_C-C_C filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1µs to 10µs will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop.

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Placing a power MOSFET directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the ITH pin signal which is in the feedback loop and is the filtered and compensated control loop response.

The gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. If R_C is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of C_{LOAD} to C_{OUT} is greater than 1:50, the switch rise time should be controlled so that the load rise time is limited to approximately 25 • C_{LOAD}. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC.

1. Are the signal and power grounds kept separate? The combined IC signal ground pin and the ground return of C_{DRVCC} must return to the combined C_{OUT} (–) terminals. The path formed by the top N-channel MOSFET, bottom N-channel MOSFET and the C_{IN} capacitor should have short leads and PC trace lengths. The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor by placing the capacitors next to each other.
2. Does the LTC3779 V_{FB} pin's resistive divider connect to the (+) terminal of C_{OUT}? The resistive divider must be connected between the (+) terminal of C_{OUT} and signal ground. The feedback resistor connections should not be along the high current input feeds from the input capacitor(s).
3. Are the SENSEN and SENSEP leads routed together with minimum PC trace spacing? The filter capacitor between $SENSE^+$ and $SENSE^-$ should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the SENSE resistor.
4. Is the DRV_{CC} and decoupling capacitor connected close to the IC, between the DRV_{CC} and the ground pin? This capacitor carries the MOSFET drivers' current peaks.
5. Keep the SW, TG, and BOOST nodes away from sensitive small-signal nodes. All of these nodes have very large and fast moving signals and therefore should be kept on the output side of the LTC3779 and occupy minimum PC trace area.
6. The path formed by switch A, switch B, D1 and the C_{IN} capacitor should have short leads and PC trace lengths. The path formed by switch C, switch D, D2 and the C_{OUT} capacitor also should have short leads and PC trace lengths.
7. Use a modified star ground technique: a low impedance, large copper area central grounding point on the same side of the PC board as the input and output capacitors with tie-ins for the bottom of the DRV_{CC} decoupling capacitor, the bottom of the voltage feedback resistive divider and the GND pin of the IC.

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Design Example

V_{IN} = 6V to 100V

V_{OUT} = 12V

$I_{OUT(MAX)}$ = 5A

f = 200kHz

Maximum ambient temperature = 60°C

Set the frequency at 200kHz by applying 1.11V on the FREQ pin (see Figure 9). The 20µA current flowing out of the FREQ pin will give 1.11V across a 55.6k resistor to GND. The inductance value is chosen first based on a 30% ripple current assumption. In the buck region, the ripple current is:

$$\Delta I_{L,BUCK} = \frac{V_{OUT}}{f \bullet L} \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

$$I_{RIPPLE,BUCK} = \frac{\Delta I_{L,BUCK} \bullet 100}{I_{OUT}} \%$$

The highest value of ripple current occurs at the maximum input voltage. In the boost region, the ripple current is:

$$\Delta I_{L,BOOST} = \frac{V_{IN}}{f \bullet L} \bullet \left(1 - \frac{V_{IN}}{V_{OUT}}\right)$$

$$I_{RIPPLE,BOOST} = \frac{\Delta I_{L,BOOST} \bullet 100}{I_{IN}} \%$$

The highest value of ripple current occurs at $V_{IN} = V_{OUT}/2$.

A 15µH inductor will produce 10% ripple in the boost region (V_{IN} = 6V) and 70% ripple in the buck region (V_{IN} = 100V).

The R_{SENSE} resistor value can be calculated by using the maximum current sense voltage specification with some accommodation for tolerances.

$$R_{SENSE} = \frac{2 \bullet 140mV \bullet V_{IN(MIN)}}{2 \bullet I_{OUT(MAX,BOOST)} \bullet V_{OUT} + \Delta I_{L,BOOST} \bullet V_{IN(MIN)}}$$

$$= 13.3m\Omega$$

Adding an additional 30% margin, choose R_{SENSE} to be 13.3mΩ/1.3 = 10mΩ.

Output voltage is 12V. Select R_A as 12.1k. R_B is:

$$R_B = \frac{V_{OUT} \bullet R_A}{1.2} - R_A$$

Select R_B as 110k. Both R_A and R_B should have a tolerance of no more than 1%.

Selecting MOSFET Switches

The MOSFETs are selected based on voltage rating and $R_{DS(ON)}$ value. It is important to ensure that the part is specified for operation with the available gate voltage amplitude. In this case, the amplitude is 10V and MOSFETs with an $R_{DS(ON)}$ value specified at V_{GS} = 4.5V can be used.

Select QA and QB. With 100V maximum input voltage MOSFETs with a rating of at least 150V are used. As we do not yet know the actual thermal resistance (circuit board design and airflow have a major impact) we assume that the MOSFET thermal resistance from junction to ambient is 50°C/W.

If we design for a maximum junction temperature, $T_{J(MAX)}$ = 125°C, the maximum $R_{DS(ON)}$ value can be calculated. First, calculate the maximum power dissipation:

$$P_{D(MAX)} = \left(\frac{T_{J(MAX)} - T_{A(MAX)}}{R_{(j-a)}}\right)$$

$$P_{D(MAX)} = \frac{(125 - 60)}{50} = 1.3W$$

APPLICATIONS INFORMATION

The maximum dissipation in QA occurs at minimum input voltage when the circuit operates in the boost region and QA is on continuously. The input current is then:

$$\frac{V_{OUT} \bullet I_{OUT(MAX)}}{V_{IN(MIN)}}, \text{ or } 10A$$

We calculate a maximum value for $R_{DS(ON)}$:

$$R_{DS(ON)}\,(125°C) < \frac{P_{D(MAX)}}{I_{IN(MAX)}^{2}}$$

$$R_{DS(ON)}\,(125°C) < \frac{1.3W}{(10A)^2} = 0.013\Omega$$

The Infineon BSC360N15NS3G has a typical $R_{DS(ON)}$ of 0.036Ω at V_{GS} = 10V. Two MOSFETs can be used in parallel to handle the power dissipation.

The maximum dissipation in QB occurs at maximum input voltage when the circuit is operating in the buck region. The dissipation is:

$$P_{B,BUCK} = \frac{V_{IN} - V_{OUT}}{V_{IN}} \bullet I_{OUT(MAX)}^{2} \bullet \rho_{\tau} \bullet R_{DS(ON)}$$

$$R_{DS(ON)}(125°C) < \frac{1.3W}{\left(\frac{100V - 12V}{100V}\right) \bullet (5A)^2} = 0.059\Omega$$

The Infineon BSC190N15NS3G with a typical $R_{DS(ON)}$ of 19mΩ can be used.

Select QC and QD. With 12V output voltage we need MOSFETs with 20V or higher rating.

The highest dissipation occurs at minimum input voltage when the inductor current is highest. For switch QC the dissipation is:

$$P_{C,BOOST} = \frac{(V_{OUT} - V_{IN})V_{OUT}}{V_{IN}^{2}} \bullet I_{OUT(MAX)}^{2} \bullet \rho_{\tau} \bullet R_{DS(ON)} + k \bullet V_{OUT}^{3} \bullet \frac{I_{OUT(MAX)}}{V_{IN}} \bullet C_{RSS} \bullet f$$

where C_{RSS} is usually specified by the MOSFET manufacturers. The constant k, which accounts for the loss caused by reverse recovery current, is inversely proportional to the gate drive current and has an empirical value of 1.7.

The dissipation in switch QD is:

$$P_{D,BOOST} = \frac{V_{IN}}{V_{OUT}} \bullet \left(\frac{V_{OUT}}{V_{IN}} \bullet I_{OUT(MAX)}\right)^{2} \bullet \rho_{\tau} \bullet R_{DS(ON)}$$

BSC050NE2LS is a possible choice for QC and QD. The calculated power loss at 6V input voltage is then 0.392W for QC and 0.375W for QD.

C_{IN} is chosen to filter the square current in the buck region. In this mode, the maximum input current peak is:

$$I_{IN,PEAK(MAX,BUCK)} = 5A \bullet \left(1 + \frac{70\%}{2 \bullet 100\%}\right) = 6.75A$$

A low ESR (10mΩ) capacitor is selected. Input voltage ripple is 67.5mV (assuming ESR dominates the ripple).

C_{OUT} is chosen to filter the square current in the boost region. In this mode, the maximum output current peak is:

$$I_{OUT,PEAK(MAX,BOOST)} = \frac{12}{6} \bullet 5 \bullet \left(1 + \frac{10\%}{2 \bullet 100\%}\right) = 10.5A$$

A low ESR (5mΩ) capacitor is suggested. This capacitor will limit output voltage ripple to 53mV (assuming ESR dominates the ripple).

APPLICATIONS INFORMATION

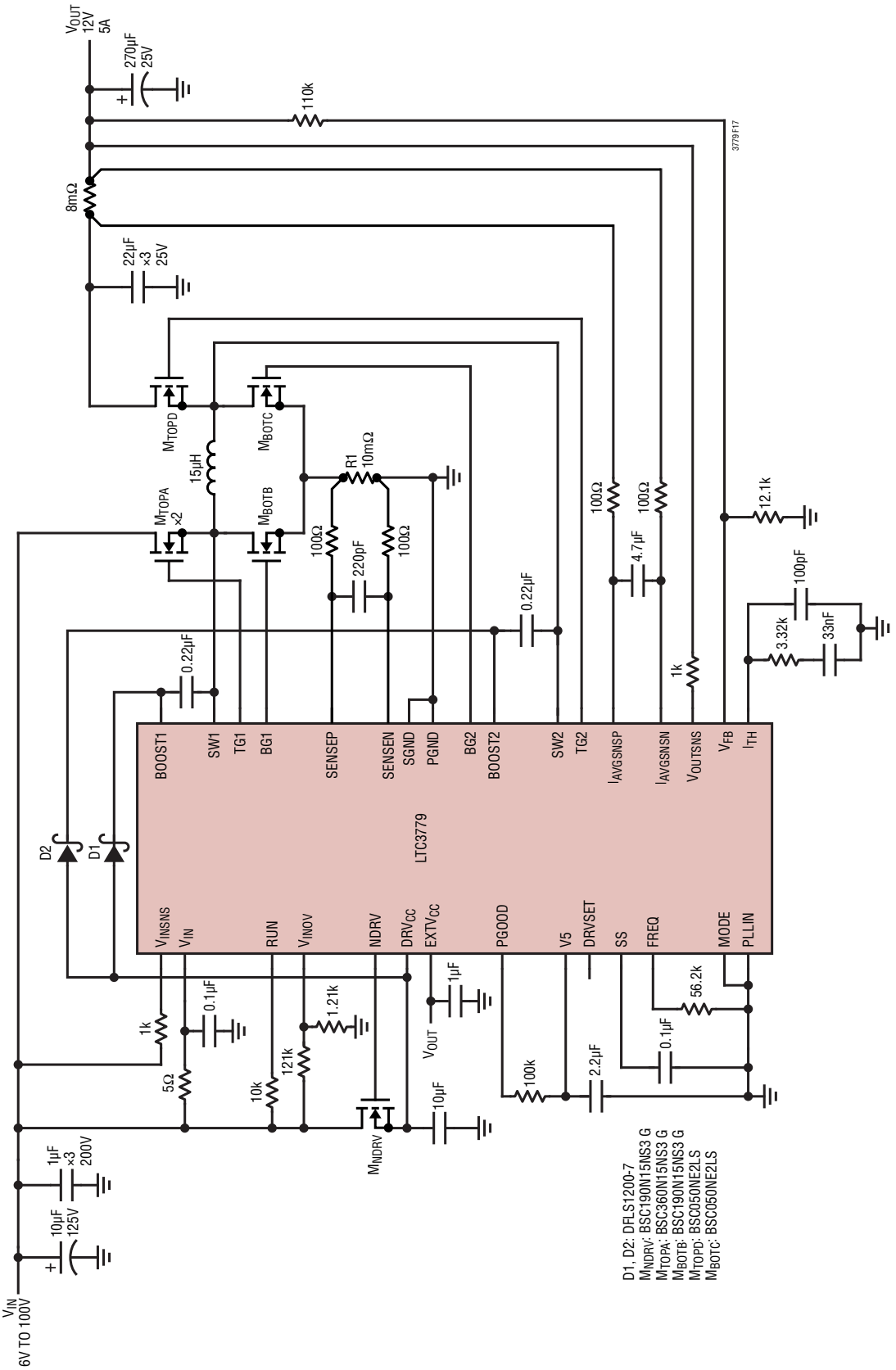
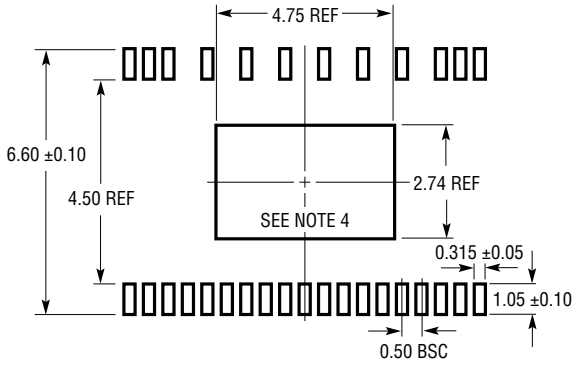


Figure 17. 97% Efficient 12V/5A Output Buck-Boost Converter

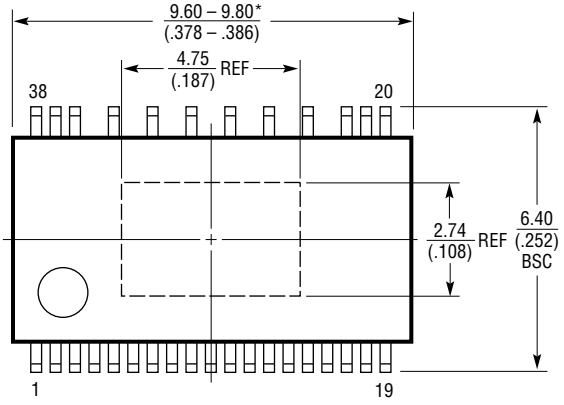
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3779#packaging for the most recent package drawings.

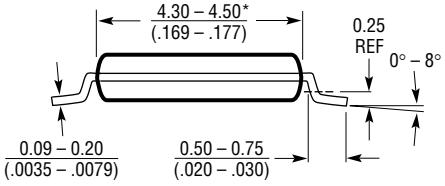
FE Package
Package Variation: FE38 (31)
38-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1865 Rev B)
Exposed Pad Variation AB

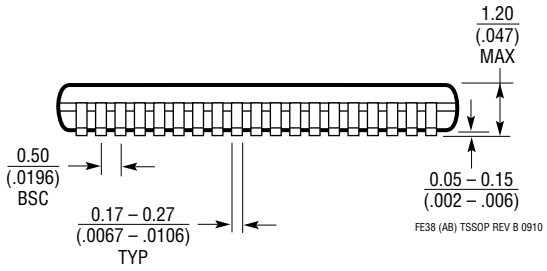


RECOMMENDED SOLDER PAD LAYOUT



PIN NUMBERS 23, 25, 27, 29, 31, 33 AND 35 ARE REMOVED





NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	04/18	Added I_Q limits	2
		Added graph, Efficiency and Power Loss vs Load Current and Input Voltage Continuous Mode	6
		Corrected pinouts, SW1, SW2, TG1, TG2, BOOST1, BOOST2	12

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TYPICAL APPLICATION

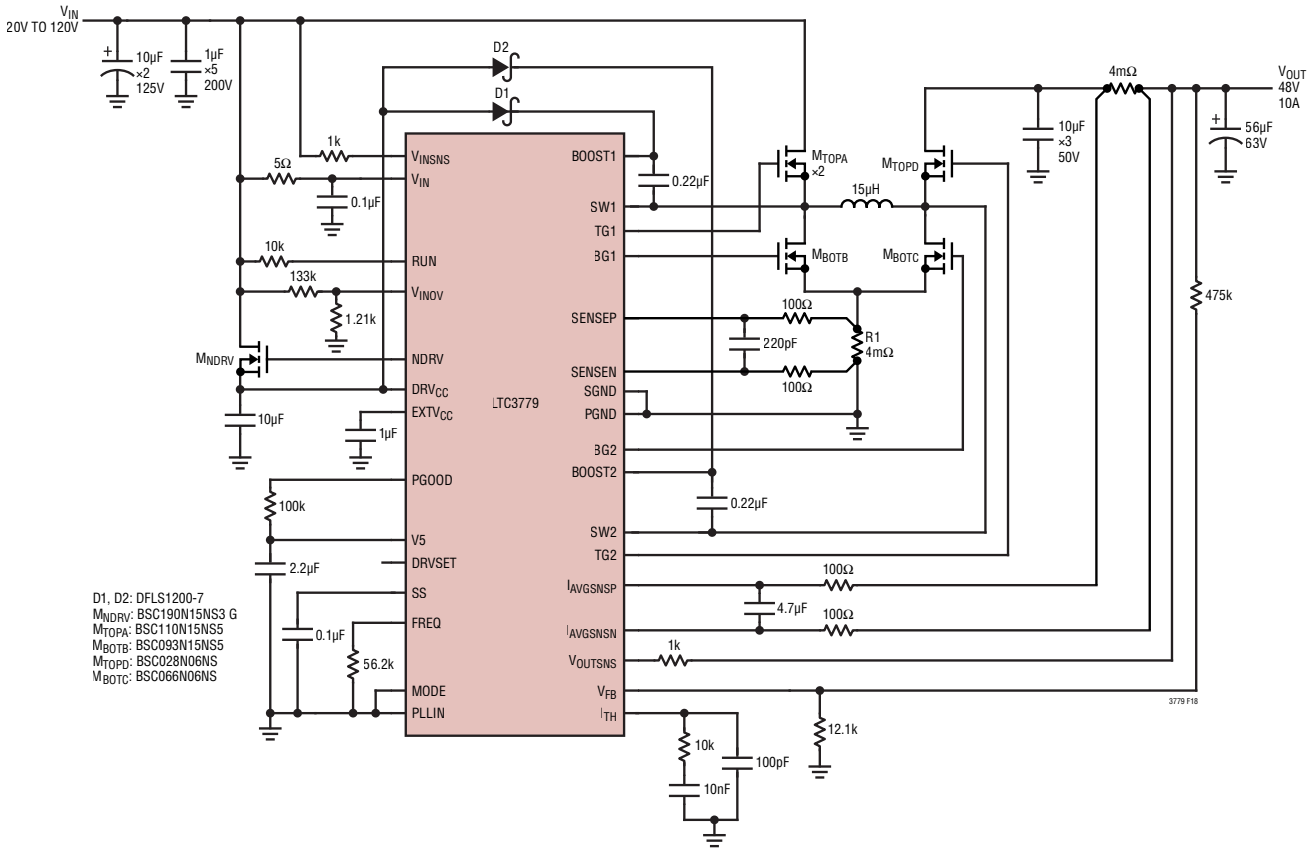

Figure 18. 99% Efficient 480W, 48V Output Buck-Boost Converter

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT®8705A	80V V_{IN} and V_{OUT} Synchronous 4-Switch Buck-Boost DC/DC Controller	2.8V ≤ V_{IN} ≤ 80V, Input and Output Current Monitor, 5mm × 7mm QFN-38 and TSSOP-38
LTC7813	60V Low I_Q Synchronous Boost+Buck Controller Low EMI and Low Input/Output Ripple	4.5V (Down to 2.2V After Start-Up) ≤ V_{IN} ≤ 60V, Boost V_{OUT} Up to 60V, 0.8V ≤ Buck V_{OUT} ≤ 60V, I_Q = 29µA, 5mm × 5mm QFN-32
LTC3899	60V, Triple Output, Buck/Buck/Boost Synchronous Controller with 29µA Burst Mode I_Q	4.5V (Down to 2.2V After Start-Up) ≤ V_{IN} ≤ 60V, V_{OUT} Up to 60V, Buck V_{OUT} Range: 0.8V to 60V, Boost V_{OUT} Up to 60V
LTM®8056	58V Buck-Boost µModule Regulator, Adjustable Input and Output Current Limiting	5V ≤ V_{IN} ≤ 58V, 1.2V ≤ V_{OUT} ≤ 48V 15mm × 15mm × 4.92mm BGA Package
LTC3895	150V Low I_Q, Synchronous Step-Down DC/DC Controller with 100% Duty Cycle	4V ≤ V_{IN} ≤ 140V, 150V Absolute Maximum, PLL Fixed Frequency 50kHz to 900kHz, 0.8V ≤ V_{OUT} ≤ 60V, Adjustable 5V to 10V Gate Drive, I_Q = 40µA
LTC3639	150V High Efficiency 100mA Synchronous Step-Down Regulator	Integrated Power MOSFETs, 4V≤ V_{IN} ≤ 150V, 0.8V ≤ V_{OUT} ≤ V_{IN}, I_Q = 12µA, MSOP-16(12)
LTC3638	140V High Efficiency 250mA Step-Down Regulator	Integrated Power MOSFETs, 4V≤ V_{IN} ≤ 140V, 0.8V ≤ V_{OUT} ≤ V_{IN}, I_Q = 12µA, MSOP-16(12)
LTC7138	140V High Efficiency 400mA Step-Down Regulator	Integrated Power MOSFETs, 4V≤ V_{IN} ≤ 140V, 0.8V ≤ V_{OUT} ≤ V_{IN}, I_Q = 12µA, MSOP-16(12)
LTC7103	105V, 2.3A Low EMI Synchronous Step-Down Regulator	4.4V ≤ V_{IN} ≤ 105V, 1V ≤ V_{OUT} ≤ V_{IN}, I_Q = 2µA Fixed Frequency 200kHz to 2MHz, 5mm × 6mm QFN

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